Optical regeneration based on noise generated in bistable devices: going from 2R to 3R

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ABSTRACT

In this paper we propose to employ an instability that occurs in bistable devices as a control signal at the reception stage to generate the clock signal. One of the adopted configurations is composed of two semiconductor optical amplifiers arranged in a cascaded structure. This configuration has an output equivalent to that obtained from Self-Electrooptic Effect Devices (SEEDs), and it can implement the main Boolean functions of two binary inputs. These outputs, obtained from the addition of two binary signals, show a short spike in the transition from "1" to "2" in the internal processing. A similar result is obtained for a simple semiconductor amplifier with bistable behavior. The paper will show how these structures may help recover clock signals in any optical transmission system.

Keywords: Optical bistability, optical computing, optical logic cells, clock signal, clock recovery

1. INTRODUCTION

In any transmission system there is signal degradation as a consequence of attenuation and time distortion. Likewise, noise and interference sources are present that degrade the Bit Error Rate –BER- of the digital communication system. In optical communications the worst noise source for a long-haul system is the amplified spontaneous emission – ASE-. This source of interference and noise significantly affects the BER as the noise is present in the transmission of a bit 1 and of a bit 0. The BER value of a given communication system is related to the Signal-to-Noise ratio at the front end of the receptor. The SNR can be evaluated by way of an eye pattern, which allows an estimation of the noise, the timing jitter and the dispersion in a bit 1 and bit 0. In this work we will use the eye pattern representation as a tool to evaluate the best configuration for our proposed technique to use noise as a clock signal detector.

Optical network architectures for long-haul transmission need signal regeneration; also in present optical networks are new architectures with optical switching matrices. Signal degradation can arise during fiber transmission as well as in switching nodes. All-optical 3R (Re-amplification, Re-shaping, Re-timing) signal regeneration is needed to avoid the accumulation of noise, crosstalk and non-linear distortion and to ensure a good signal quality for transmission over any path in the all-optical network. Currently the most widespread regenerators are optoelectronic. The new technologies provide the opportunity to replace required optical detection and electronic regeneration with all-optical processing. Many structures, mainly based on nonlinear phenomena, have been proposed for 2R- (Re-amplification- Re shaping) configurations.

Clock recovery is the most critical stage in regeneration. The device we choose must offer flexibility to the optical network, and cannot depend either on wavelength or on the bit rate of the transmitted signal. Some basic ideas are given in (1). Most devices used in 2R or 3R structures are semiconductor devices plus an interferometer, e.g. the MZI/SOA configuration. In this paper we present a new technique for clock recovery, also based on semiconductor amplifiers, that makes use of nonlinear bistability. There is an unavoidable feature of bistable action: the presence of an output intensity spike brought about by the fact that the phase must always pass through a resonance during switch-up (and switch-down). From a practical point of view this mainly affects timing since there is an associated time delay before a steady-state output is achieved. These studies have been carried out for Fabry-Perot and Distributed Feedback (DFB) structures. A reference exploring the potential of optical bistability in DFB amplifiers both theoretically and experimentally can be found in (2).

With the help of these spikes we make possible reading the current frequency from the data signal. First, it is required to process the signal with a clock reference signal and, later on, the signal obtained from the spikes is post-

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processed, thus providing the information about phase and frequency. All processing devices are Semiconductor Laser Amplifiers (SLA) with a bistable behavior. As we are dealing with digital signals, all the functions are Boolean functions. We used an optical computing device designed by us and reported previously (3): the Optical Programmable Logic Cell (OPLC). The OPLC is based on the Self-Electrooptic-Effect-Device (SEED) behavior and on the well-know On-Off device. The on-off device known as Optical Logic Element (OLE) can be obtained from a bistable device, passive or active. The OPLC has been demonstrated with bistable active devices an SLA (4).

Clock recovery requires being able to read information from data signals. This basic idea, being able to obtain information from data signals, is also applied in packet switching. In order to take advantage of packet switching in the optical domain, it is required to read the address carried in the direction bytes. Some ideas on how to do this, also with the OPLC, have been reported previously (5).

2. BIT NOISE FROM AN OPTICAL LOGIC GATE

In an eye pattern there is enough information about the performance of data transmission or, as in this case, of data processing. The eye pattern is defined as the synchronized superposition of all possible realizations of the signal of interest. The width of the eye opening defines the time interval over which the timing error can vary and the height of the eye opening, at a specific sampling time, defines the noise margin of the system or device. In the case of M-ary systems, the eye pattern contains (M-1) eyes openings stacked up vertically one on top of the other, where M is the number of discrete amplitude levels used to construct the transmitted signal.

In order to obtain a clear eye pattern, a random input signal has to be used. A high bandwidth is necessary to take into account the greatest number of longitudinal modes of the laser cavities, mainly in the case of the Fabry-Perot structures. A deeper study of and possibilities that the eye pattern can offer to evaluate a logic gate based on SLAs have been reported in (6).

2.1. Bistability in an SLA.

The Optical Bistability in Semiconductor Laser Amplifiers under external light injection has been the object of extensive research.. It has been studied for different types of SLA structures, such as SLA-FP, SLA-DFB and, of course, the most practical structure due to its fabrication characteristics, VCSLA (7). The physical phenomenon that causes the optical bistability in laser amplifiers is the dispersive nonlinearity, characterized by the existence of a resonator in a medium whose refractive index depends on the incident optical power. An increment in the injected optical power makes its resonant frequency move toward longer wavelengths as a result of the variation of the refractive index. This means that the injection of an optical signal detuned to the long wavelength side of the resonant frequency mode of the laser will cause a positive wavelength shift of the resonant emission frequency of the laser as a consequence of the variation of the refractive index of the active medium. Once a threshold is exceeded the optical bistability can be observed. For a more detailed explanation of the optical bistability in laser amplifiers see (8).

In previous works, we studied the optical bistability phenomenon in Fabry-Perot and DFB structures with the VPI_ComponentMaker™ software tool (6). Figure 1 shows two bistable loops, both corresponding to transmission mode and anticlockwise hysteresis cycles..We have used the most common wavelength in long-haul systems, 1550nm.

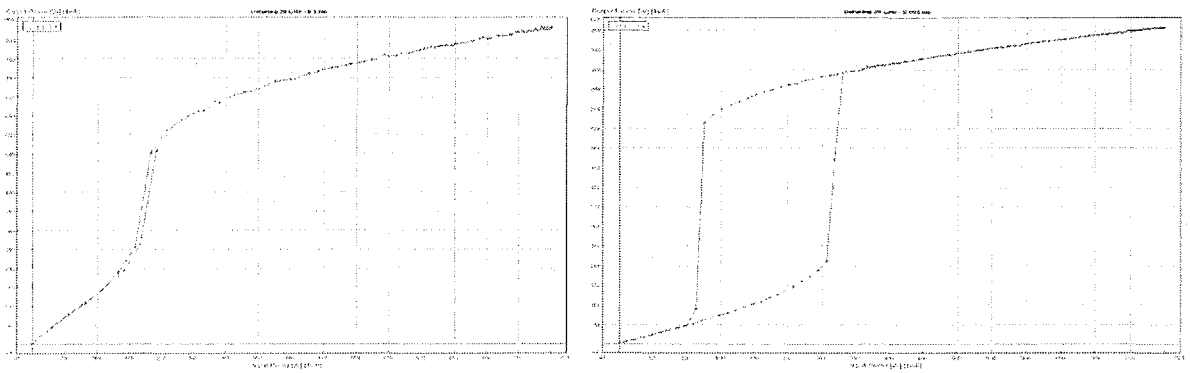

Fig. 1. Optical bistability in an FP-SLA at 1500nm, with an initial detuning of 20GHz for linewidths a) 0.015nm and b)0.005nm

The two bistable loops shown in figure 1 correspond to the same initial detuning of 20GHz, being the spectral width of the injected signal 0.015nm in one case and 0.005nm in the other. It is obvious that the internal parameters of a device that govern the optical bistability transfer function are inexorably determined during fabrication. However, this transfer function can be modified by the variation of the optical input signal, since the optical bistability depends on the optical power and the wavelength of the injected external signal. Also, the bias current applied to the bistable SLA device will affect the final bistability function, which means there are at least three parameters to control the desired performance. All these dependence parameters can be applied to the use of the SLA as a sensor element (9) and more specific applications related to the control of the logic functions (10).

2.2. SLA as an optical logic cell and bit noise.

Figure 2 shows the block diagram of the Q-device along with its logic table for different control signal levels. The input and output data are binary, the cw-control signal is a 3-level signal and the internal processing is a multilevel process. Figure 3 shows the schematic model simulated by the VPI_ComponentMaker™ software tool for the Q-device. The input signals, whether data or control, all come from one laser source, which allows coherence processing and phase control of the signals before they impinge upon the bistable device. The details of the transition that affects the noise present on the eye pattern more significantly are also represented.

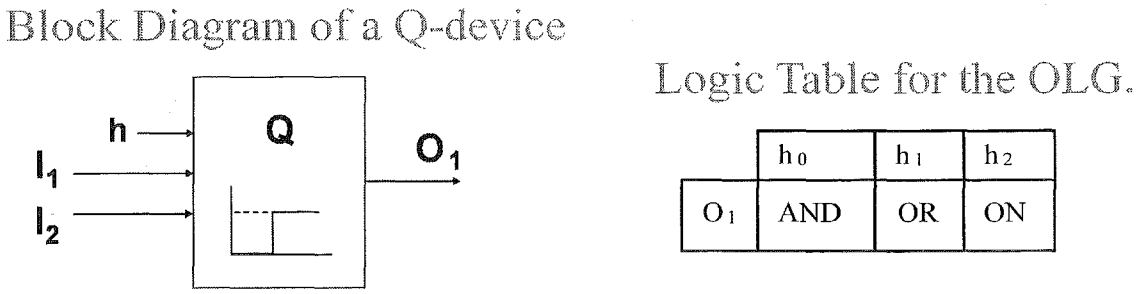

Fig. 2. Block diagram and logic table of the Q device of the OPLC. Three inputs: two data signals and one cw-control signal; one output.

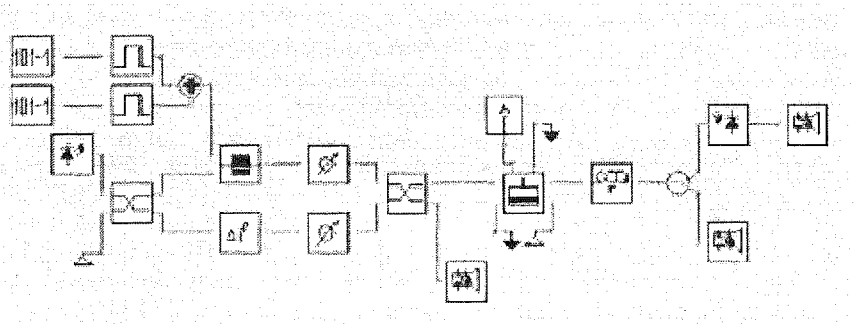

Fig. 3. Schematic model of the Q device simulated with the VPI_ComponentMaker™ software tool.

In order to find out how much noise the logic gate introduces in a bit we analyze a scheme modeled making use of the VPI_ComponentMaker™ software tool. The amplifier is biased below the threshold current. The eye pattern has been obtained under specific conditions of the laser diode and the optical signal used for the data. Any change of these parameters would produce different results.

We have simulated the logic response for any combination of the input signals for a given bistable loop in either an FP-SLA or a DFB-SLA structure. In all cases the wavelength chosen for the injected signal had a detuning of 20GHz and the hysteresis cycle was anticlockwise. The second and third transmission windows, 1300nm and 1500nm, have been compared, finding out that the optical power for the former case had to be almost one order of magnitude smaller than for the latter (10). In this work we have only considered the 1500nm window as this is the wavelength used for long-haul transmission, where clock recovery is more interesting, even though we acknowledge that signals at 1300nm would be less power-consuming.

In figure 4 we present a summary of the conditions under which the different logic functions are achieved. A bit power of 36 μW is used for a bit 1, which is also the power level of the control signal for the OR function to be implemented, whereas the AND logic function requires a null control signal (h_0). It can be seen that for the AND function a delay time is introduced, for which reason the bistable devices are not very quick. The spike, which is the effect we are interest in, is more significant when the power level starts at a higher value of the switching-on power.

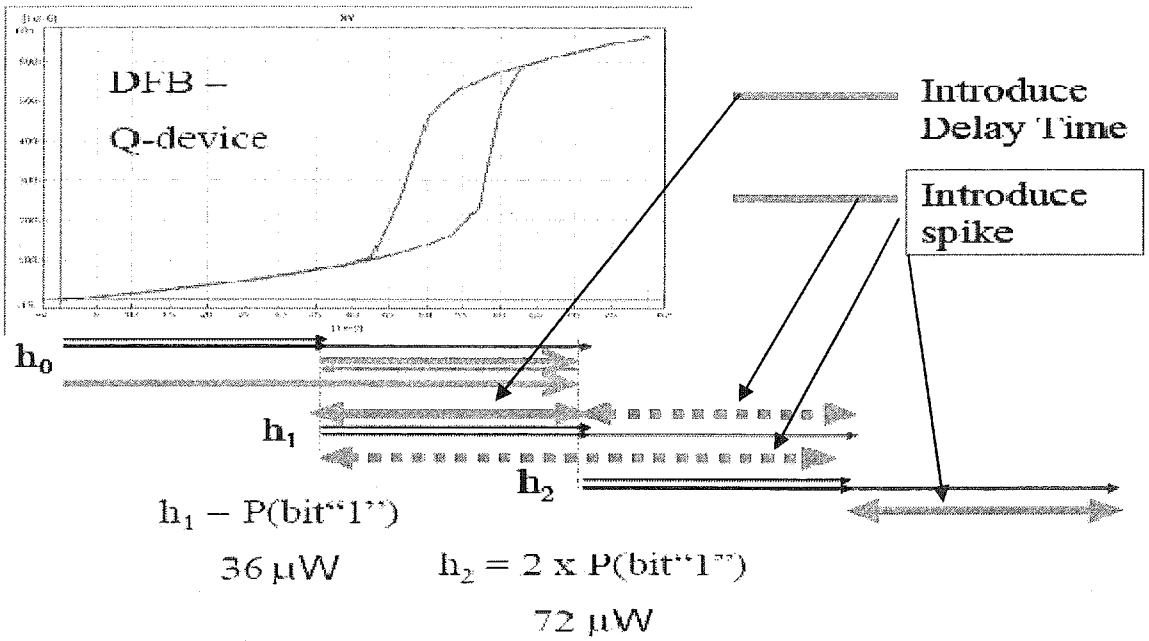

Fig. 4. Summary of the internal multilevel signal process and transition were spikes are present. Solid lines represent the transitions where the effect is more significant.

Based on figure 4, the most significant spike occurs when the control signal is at least twice as high as the bit power, which causes the output of the system to be an ON logic function. In this case, we can see in figure 5 that transitions from 0 to a double bit 1 generate high spikes. These spikes will be used to synchronize the data bit stream with the signal from the clock generator. Also, as can be observed, there is a significant downward spike when the input signal goes from 2 (double bit 1) to 0. This will also be used for the clock generator as we will see in next section.

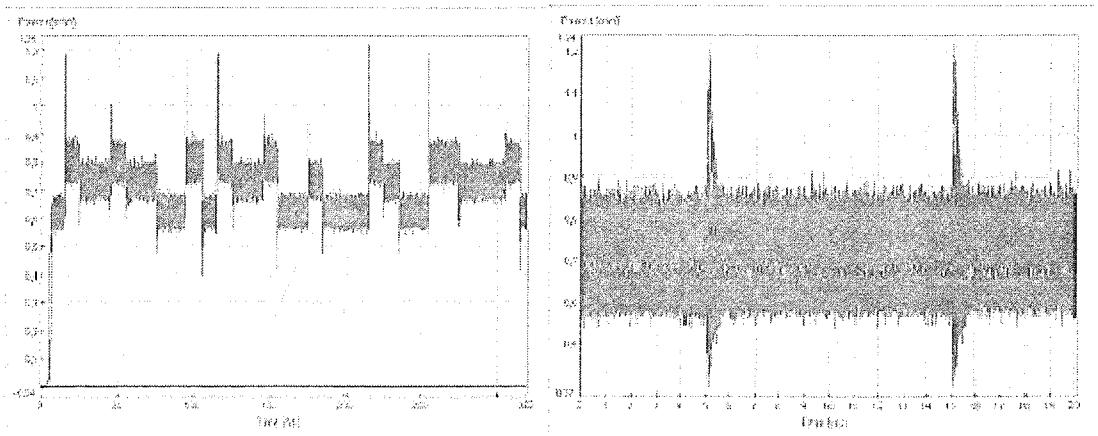

Fig. 5. Output of the Q-device with $h=h_2$, which corresponds to an ON function (left-hand side graph). Eye diagram that shows the spikes; these are due to transitions from a bit 0 in both data signals to a simultaneous bit 1 in both input data signals (right-hand side graph).

3. OPTICAL CLOCK RECOVERY

In order to recover the clock signal of the data bit stream we split the signal and make a part of it go into the block proposed by us and represented in figure 6. As can be seen, five components are used, all of which are implemented by OPLCs, since this cell can execute any of the Boolean functions required. The clock generator is also implemented with an OPLC, but, as this component needs a special configuration of inputs, it will be described in the next section.

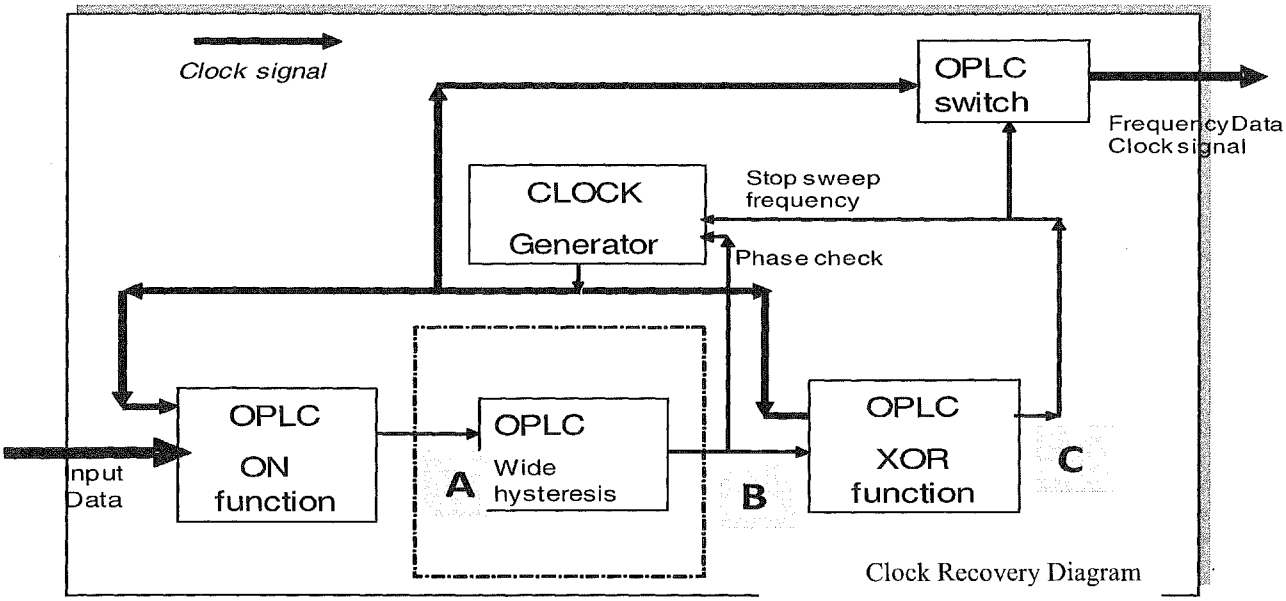

Fig. 6. Clock recovery block diagram. The OPLC is the basic block. At point A (input of block OPLC-wide hysteresis) there is an ON signal with spikes when the reference clock signal and a data bit time-up occur simultaneously and a lower value of the ON signal when the reference clock signal and the data time-down coincide. At point B a signal similar to the clock signal is obtained with an input data stream 0101010. At C, a bit 1 is produced when the clock signal and the data signal are equal. This last 1 tells the clock generator that the frequency has been recovered. The frequency of the data clock signal can thus be used for retiming.

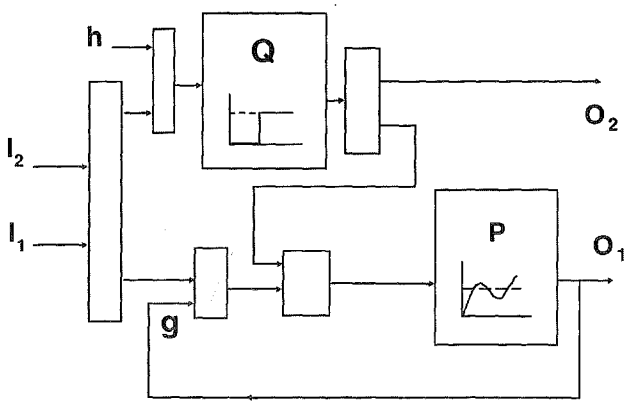

Fig. 7. Block diagram of the internal OPLC. Shown are the two internal devices (Q-device and P-device) and optical couplers to optically add the input and control signals.

In figure 6, the first block (the OPLC executing the ON function) yields the very same result already represented in figure 5. The resulting signal goes into the second block (OPLC –wide hysteresis-), which uses the same transfer function depicted in figure 1 only with a wider hysteresis cycle, and biases the device in the middle of the hysteresis loop. The high spike sets the output (point B) to a bit 1, and it remains there until a downward spike appears. This downward spike can be seen in figure 5 and corresponds to the instant when the clock signal and the data time-down from 1 to 0 happen at the same time. Following this behavior, if the input data signal is 01010101, at point B we will have this same sequence of bits when the frequency of the clock signal matches the frequency of the data.

The first time a bit 1 appears, the clock generator is told that the initial phase of the clock signal is right.

This process has been indicated in figure 6 with the label "phase check". When output B is 010101 with the same frequency as the data, and the clock signal also has the same frequency, the XOR function generates a 0 at point C. This informs the clock generator that the frequency sweep must stop. The clock generator starts from a high frequency and has the possibility if tuning the frequency continuously, this will be reported on next section.. By the way, when the value is 0 on point C the clock signal is ready to be used for re-shaping and re-timing. The way to send the clock signal detected is represented with the block: OPLC switch

As was pointed out before, a single cell (the OPLC) has been employed for the clock recovery. The basic scheme of this cell is displayed in figure 7. It is composed of two devices (P and Q) with nonlinear behaviour. The outputs of each of them correspond to the two final outputs (O_1 and O_2) of the cell. There are four inputs to the circuit: two input data signals, I_1 and I_2, and two control signals, g and h. The arrangement of these four inputs inside the circuit is also shown in figure 7. Although we have carried out a practical implementation of the processing element based on an optoelectronic configuration, a computer simulation has been adopted in the present work. In a laboratory implementation, the lines in figure 7 would represent optical multimode fibers. By using conventional optical couplers the optical input signals are added and the resulting signals that impinge on the individual devices are multilevel signals. The characteristic transfer functions of nonlinear devices P and Q are also shown in figure 7. Device Q is a thresholding or switching device, and device P is a multistate device, being the response of this nonlinear optical device the one represented in figure 2. This response is similar to the behaviour of a SEED device and it may be implemented by two semiconductor optical amplifiers, arranged in cascade, with a feedback from the second to the first one. Some details of this situation have been reported by us (4).

Because the cell works with optical signals, it allows an internal multilevel processing. In this way, input and output data signals are binary but the control is performed by multilevel signals. Table 1 lists the different programming combinations available from our Optical Programmable Logic Cell, OPLC. At least in one of the outputs, the eight Boolean functions - AND, OR, XOR, ON and the negative NAND, NOR, XNOR and OFF - can be obtained.

TABLE I.- Output functions of the optical-programmable logic circuit.

Q – Control Signal ---------- P - Control Signal	Q-Output: AND 0-0.4 ---------- P - Output	Q-Output: OR 0.5-0.9 ---------- P - Output	Q-Output: ON 1.0-2.0 ---------- P - Output
0-0.4	XOR	XOR	NAND
0.5	NAND	NOR	NOR
0.6-0.9	ON	XNOR	XNOR
1.0	XNOR	XNOR	AND
1.1-1.4	XNOR	ON	OR
1.5	AND	OR	OR
1.6-2.0	OR	OR	ON
2.0-2.5	ON	ON	ON

In figure 6 only the data inputs to the OPLC were represented. In some blocks the two data inputs are used, it is the case where the logic function is identify On the other cases, the desired performance can be obtained through several functions.

As figure 6 also shows, we only use one output in all cases . Looking at table I, we can recognize the value of the control signals required to execute the logic functions at each output. All the functions can be realized with a Q-device except for the XOR function, which needs a P device.

The control signal is supposed to be applied in all the cases with the values required to execute the logic function..

The only different block is the one that detects the spikes. We say it is different because we do not execute a logic function with it; we want it to behave like a flip-flop. However, it has been labeled as an OPLC because the only different requirement in this case is that the Q device must have a wide hysteresis cycle.

The clock generator is implemented with an OPLC. A cw signal at the input and a feedback of one of the outputs to one of the control signal inputs is enough to make the OPLC generate a periodic signal, as we will see in the next section.

4. CLOCK SIGNAL GENERATOR

The method we use to obtain periodic outputs from an OPLC is –as may be seen in figure 8 – to introduce a feedback between an output gate of the OPLC and one of the possible inputs. In our present case, we have taken the output from the P device. This feedback introduces a time delay. This time delay determines the frequency of the oscillation. Moreover, it is necessary an input signal. In the case represented in figure 8, this signal is a continuous signal obtained from a step function. It is important to recall that the oscillation frequency is a function of the introduced time delay. This time delay has been designed in such a way that the signal needs to set up its configuration, determines the delay and, as a consequence, the frequency. This configuration works as a VCO (Voltage Controller Oscillator). The voltage, in our present situation is given by a ramp that allows the tuning. When the frequency oscillator matches the frequency of the data the value at point C in figure 6, the voltage ramp will be asked to stop tuning.

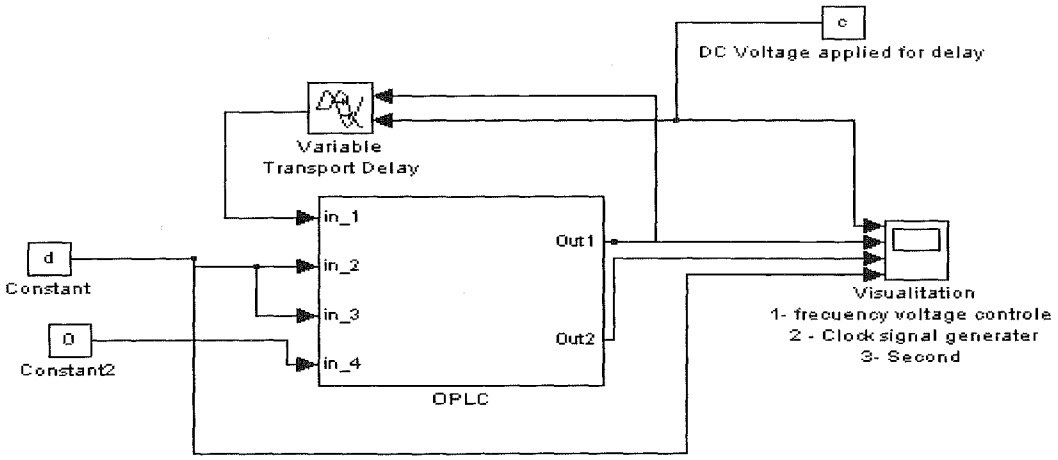

Fig. 8. Basic configuration of the clock signal generator based on an OPLC.

The implemented system, as it was computer simulated, appears in figure 8, where the main blocks are represented. In figure 9 the results obtained for three different values of DC voltage with a specific value of input "d" (a constant in figure 8) can be seen.

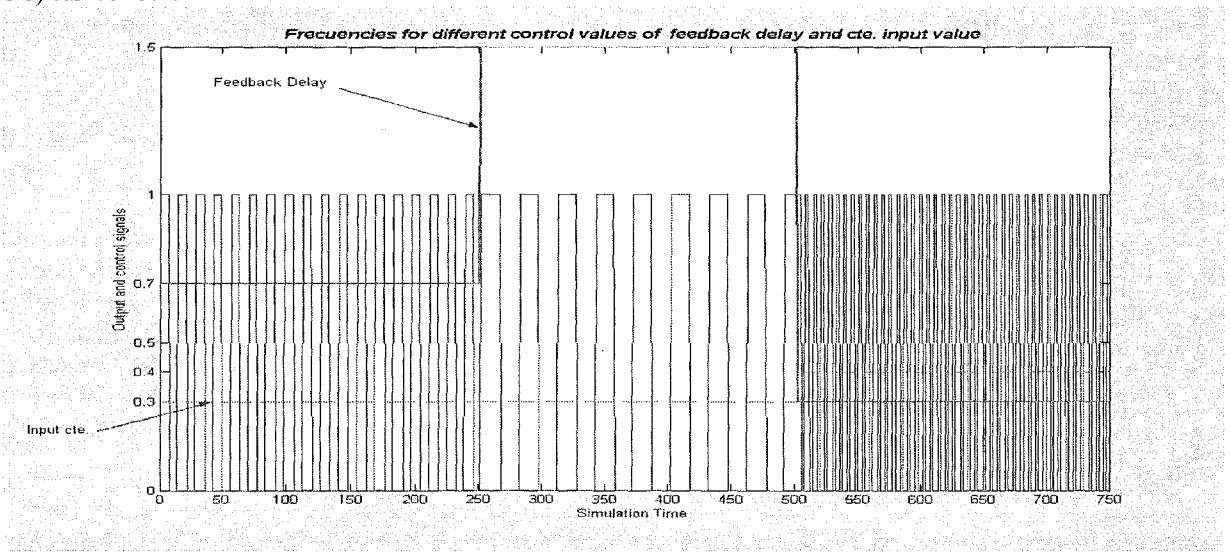

Fig. 9. Periodic solutions obtained for three different feedback times.

5. CONCLUSION

We have reported new ideas for designing a clock recovery system based on just one type of device: a semiconductor laser amplifier biased near threshold. Under this bias condition the SLA has a nonlinear gain, and a bistable behavior can be obtained with different anticlockwise hysteresis cycles. With an SLA a Q-device is implemented; with two SLA, where the reflected signal of the first SLA is applied as an input to the second SLA, the transmission output of the second SLA corresponds to the output of the P-device.

Q and P devices configure the OPLC-optical programmable logic cell-, basic element in the block diagram presented in figure 6. The devices have been demonstrated separately, as has the functional block simulation.

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REFERENCES

1. *3R Regeneration for All-Optical Networks.* **Sartorius, B.** 2001. ITCOM. págs. 333-337.
2. *Effecto of chirped gratings on reflective optical bistability in DFB semiconductor laser amplifier.* **Maywar, Drew N. y Agrawal, Govind P.** 12, December de 1998, IEEE Journal of Quantum Electronics, Vol. 34, págs. 2364-2370.
3. *Digital chaotic output from an optically processing element.* **González-Marcos, Ana y Martín-Pereda, José A.** 2, s.l. : Society of Photo-Optical Instrumentation Engineers, February de 1996, Optical Engineering, Vol. 35, págs. 525-533.
4. *An All-Optical Progrmmable Logic Gate with 1550nm Semiconductor Laser Amplifiers.* **Hurtado-villavieja, A. y González-Marcos, A.** 2004. EOS Topical Meeting Optics in Computing . Vols. OIC-2004. ISBN 3-00-013069-1.
5. *Photonics Switching Arquitectures with Logic Cells.* **González-Marcos, Ana P. y Martín-Pereda, José A.** [ed.] Benjamin B. Dingel, y otros. s.l. : Procedings of the SPIE, 2003. Optical Transmission Systems and Equipment for WDM Networking II. Vol. 5247, págs. 569-579.
6. *Bit noise with an optical logic gate with laser diode.* **Gonzalez-Marcos, Ana P., Martín-Pereda, Jose A. y Hurtado, A.** [ed.] Peter Heszler. Gran Canaria : Proceddings of the SPIE, 2004. Fluctuations and Noise in Photonics and Quantm Optics II. Vol. 5468, págs. 56-65.
7. *All-Optical Vertical-Cavity logic Gate.* **Hurtado, A., González-Marcos, A. y Martín-Pereda, J.A.** Saint-Petesburg : s.n., 2004. International Topical Meeting. Optoinformatics. ISBN: 5-7577-0157-7.
8. **Kawaguchi, H.** *Bistabilities and Nonlinearities in Laser Diodes.* s.l. : Artech House, 1994.
9. *Laser diode bistability as sensor of ooptical signal parameters.* **Gonzalez-Marcos, Ana P., Martin-Pereda, Jose A. y Hurtado, A.** [ed.] John C. Armitage, Roger A. Lessard y George A. Lampropoulus. s.l. : Proceedings of SPIE, 2004. Photonics North2004: Photonic Applications in Telecommunications, Sensors, Software, and Lasers. Vol. 5579, págs. 152-159.
10. *Linewidth influence in photonics technologies.* **Gonzalez-Marcos, A. P., Vivero, T. y Martin-Pereda, J. A.** [ed.] A. Serpengüzel, G. Badenes y C. Righini. 2007. Photonic Materials, Devices, and Applications. Vol. 6593.