Analysis of irregular behaviour on an optical computing logic cell

A. González-Marcos*, J.A. Martín-Pereda

E.T.S.I. Telecomunicación, Universidad Politécnica de Madrid, Ciudad Universitaria, 28040-Madrid, Spain

Abstract

A new methodology to study irregular behaviours in logic cells is reported. It is based on two types of diagrams, namely phase and working diagrams. Sets of four bits are grouped and represented by their hexadecimal equivalent. Some hexadecimal numbers correspond to certain logic functions. The influence of the internal and external tolerances, namely those appearing in the employed devices and in the working signals, may be analysed with this method. Its importance in the case of logic structures with chaotic behaviours is studied.

Keywords: Logic cells; Chaotic behaviour; Digital chaos; Working diagram; Phase diagram; Optical computing

1. Introduction

As it is well known, most of the digital optical computing architectures nowadays are based on optical devices with some non-linear properties. Although there are two main philosophies, namely guided and free-space configurations, both are based on similar concepts. Optical input signals are processed inside the adopted structure to give rise to a particular output. This output is a function of the initial data. Two are the more important types of employed devices to perform these functions. The first one are devices with "on–off" switching characteristics. They offer a "zero" output up to a certain level of the input signal and "one" for higher level values. The second type corresponds to devices with more complex behaviours. Although output signals remain "0"s and "1"s as before, they are obtained for different values of the input signals, with a pattern depending on the adopted device. One of the more employed, corresponding to this type of behaviour, is the self-electrooptic effect device (SEED). Its properties are well documented in the literature [1].

The two above-mentioned devices have been the basis to implement different optical computing systems. In most of the cases, they configure a main structure, called in some cases as unit cell or unit block. Larger systems are constructed from this structure. The more common configuration of these units is a black box with a pair of input ports and a single output gate. The fourth input is sometime added to allow a control signal. The output signal is the result of a logic function between the two input signals. We reported an extension of these structures in the form of an optically programmable logic cell [2]. Our cell was able to offer two outputs from two input signals being these outputs the result of different logic functions performed inside. Two other input gates were added for control signals.

The main objective in almost anyone of the previously reported architectures was to obtain as many logic functions as possible and to apply them to optical computing architectures. Flexibility, a good yield and an easy way to handle and maintain them were the main targets. Several have been the published papers concerning this type of applications. Many of them were published between 1990 and 1995 – see, for instance, the volume indicated in [9]. The last years have seen an important number of news works most of them related with computer arithmetic for optical computing. Li et al. have reported [3] parallel optical negabinary signed-digit computing, with algorithm and optical implementation. Electron-trapping devices [4] have been some of the employed technologies. Qian et al. proposed a new two-step digit-set-restricted modified signed-digit addition-subtraction algorithm [5]. Finally, Zhang and Karm [6] have presented a programmable addition module based on binary logic gates.

Moreover, as it has been shown, these structures exhibit some other type of behaviours. As a matter of fact, under

* Corresponding author. Tel.: +34-913-36-73-04; fax: 34-913-36-73-19.

E-mail address: agonmar@tfo.upm.es (A. González-Marcos).

certain conditions they offer the possibility to present an irregular output than, in some cases, becomes chaotic. These types of signals are potentially good candidates to be employed in secure systems if both, emitter and receiver are synchronised [7]. It is because that a deep knowledge of the internal behaviour of these structures is needed. If it is important to know their working conditions when they are employed in computational structures, these conditions are even more important if they are employed in communications systems. This is because there is no way to recover the transmitted information when synchronisation is lost. It is not just to lose a bit, as it can be in data processing. It is the whole communication that is lost.

Two are the main needs derived from the above considerations. The first one is the certainty to obtain a particular logic function at the unit cell, when needed. The second one is the ability to maintain an irregular behaviour, with identical chaos characteristics, at two synchronised chaos generators. In both cases, these needs can be just achieved when a proper knowledge of the working conditions of the employed devices and circuits is available.

The analysis of chaotic structures has been the object of a large number of papers in the last years. Most of them are related to the behaviours derived from the implementation of some set of partial differential equations at a particular system. In many cases, this system was an electronic set-up with a particular set of controlling equations. These equations have been analysed previously from a mathematical point of view. Chua's circuits are one of the most well-known studied case [8]. In any of them, due to the characteristics of the initial conditions, signals were analogue. This fact allows the use of standard mathematical analysis techniques.

But the above situation is no longer valid when the system and the output have a digital character. The type of analysis previously employed in analogue systems may not be directly applied here. For instance, a straightforward method to study chaos, the phase diagram, cannot be applied in these situations. Because just two possible outputs, a "1" and a "0", are obtained, the phase diagram of this system should be composed by four points only. This type of diagram should give no information about its properties. If this is the case for a simple situation, as the phase diagram, other employed methods in analogue chaos would give similar problems. This is the reason why other techniques need to be implemented when one is dealing with digital signals.

We have reported a digital chaotic system in several places [9–12]. Its properties have been analysed by numerical techniques and some conclusions have been obtained. But a particular aspect of this system has not been studied yet. It is related to the fractal-like properties that appear when its digital behaviour is represented in a working diagram. Because it has not been possible, by now, to determinate a set of equations that give indication about its way of working, a peculiar logic diagram was presented. It offers the possibility to know what type of logic function is performed depending on the type of applied control signal and the level of signals. The important point of this working diagram is that offers a fractal-like structure depending on its properties on the precision adopted in the computer simulation. Moreover, because the boundary contour between the different logic operations performed by the cell has that fractal-like structure, its behaviour will be related with the jumps between regions.

Several are the influences of the above considerations. If the optical logic cell operates under strict logic conditions the fractal properties of the boundary between regions will affect to the precision of the performed logic function. This is the case when it works, for example, as a part of an optical computer. If it is working under a chaotic regime, the chaotic output properties will have some relation with the above-mentioned fractal structure. The main objective of this paper is to study some of the possible indicated relations between the different working regions in a diagram and the chaotic regime.

The paper will be divided into three main parts. The first one will be just a short summary of the main properties of the optical logical cell to be studied. Although most of them have been reported previously, it is necessary to review some of them because they will be necessary for our study. The second one will present the dynamical properties derived from some changes in the parameters of the cell and its simulation. Finally, the third one will deal with a new form to study non-linear behaviours in digital optical structures. This last part is an extension of previous studies carried out by us in this field and presents a new methodology to be applied in similar situations. In this paper we will report just the main aspects concerning a particular region of our logic cell working diagram.

2. Optical computing logic cell

The use of a dynamically programmable logic cell results in an efficient implementation of complex digital circuits. This is a well-known fact in electronics where it has been one of the main battle-horses almost since the beginning of computer architecture [13]. Although several equivalent configurations have been reported also in photonics, its use is not so widespread. The one presented here was reported previously by us [15], the design and the used devices being the main difference with the previous ones. Input and output signals are optical and the devices, optical non-linear devices with digital characteristics.

Fig. 1a shows a block representation of our basic cell. Its two outputs, O_1 and O_2, are logic functions of two independent signals, I_1 and I_2, applied to the cell. The type of functions performed by the cell at a particular time is determined by the values of two controlling signals, g and h.

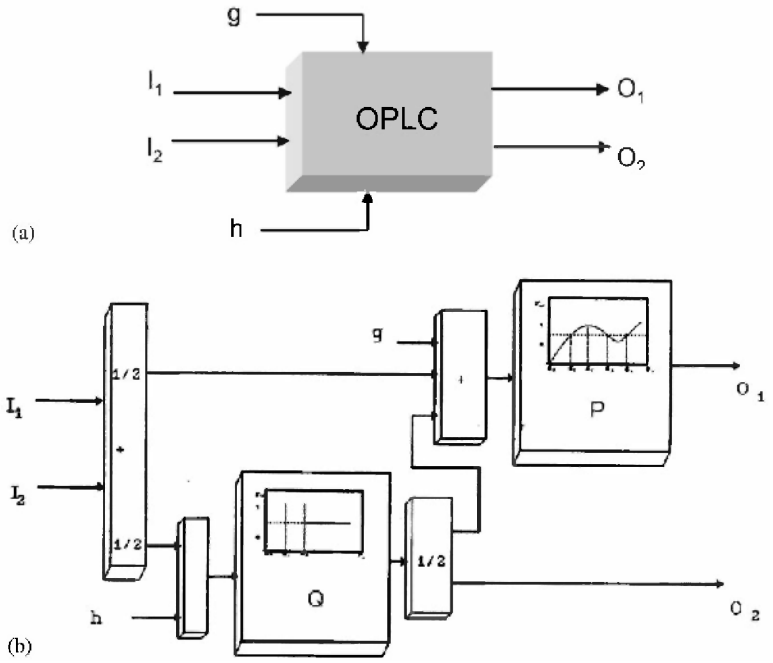

Fig. 1. (a) Block representation; (b) internal representation of the OPLC.

Table 1
Programmable logic functions of the OPLC

Control signal P-device O_1	Output signals O_2	O_1	O_2	O_1	O_2	
g_0	XOR		XOR		NAND	
g_1	NAND		NOR		NOR	
g_2	XNOR	AND	XNOR	OR	AND	ON
g_3	AND		OR		OR	
g_4	OR		OR		ON	
Control signal → Q-device	h_0		h_1		h_2	

Because the cell works with optical signals, it allows an internal multilevel processing. In this way, input and output data signals are binary but the control is performed by multilevel signals. Table 1 lists the different programming combinations available from our optical programmable logic cell (OPLC). At least in one of the outputs, the eight Boolean functions – AND, OR, XOR, ON and the negative NAND, NOR, XNOR and OFF – can be obtained.

Fig. 1b shows the real internal configuration of the OPLC with its two basic non-linear optical devices. The main characteristics of these non-linear devices are also shown. Device Q corresponds to a thresholding or switching device. Device P response is similar to that achieved by a self-electro-optic-effect-device (SEED) [14]. Further details, ample than what is presented here as well as its physical implementation, can be found in [15].

The study reported here was performed by computer simulation of the OPLC, with the Simulink™ application from Matlab™. It has been considered an ideal response of the non-linear devices. This fact concerns to the output level but not to the possible hysteresis. The hysteresis appears in any real behaviour of a non-linear device and it should be the origin of non-controlling responses when the signal level is out of the tolerance range.

For an easier understanding of the work presented here, and because the versatility of our OPLC is mainly due to the P device, we will concentrate our attention here on its behaviour. Device Q allows the possibility to obtain a second output gate with some particular logic function of the input data. This is important when the cell is employed in optical computing. But if it is employed as chaos generator, as it is our present interest, the main influence comes from the P device. From another point of view, this case may be associated with a particular situation. It corresponds to a control signal, g, equal to zero and to a value of the decision level for the thresholding device, Q, so high that the addition of the two input signals never reaches that value. In this way, the output of Q-device is equal to "0" and hence does not affect the input of P-device.

The main aspect concerning its possible application in optical computing is related to the diagram shown in Fig. 2. It shows the representation of P-device output when an OFF function is obtained at Q-device output O_2. Input data level is fixed. The x-axis corresponds to the equidistant value d_1 (as it can be seen in Fig. 3b) and y-axis is the level of the control signal applied to the P-device, all of them being normalized to input data level

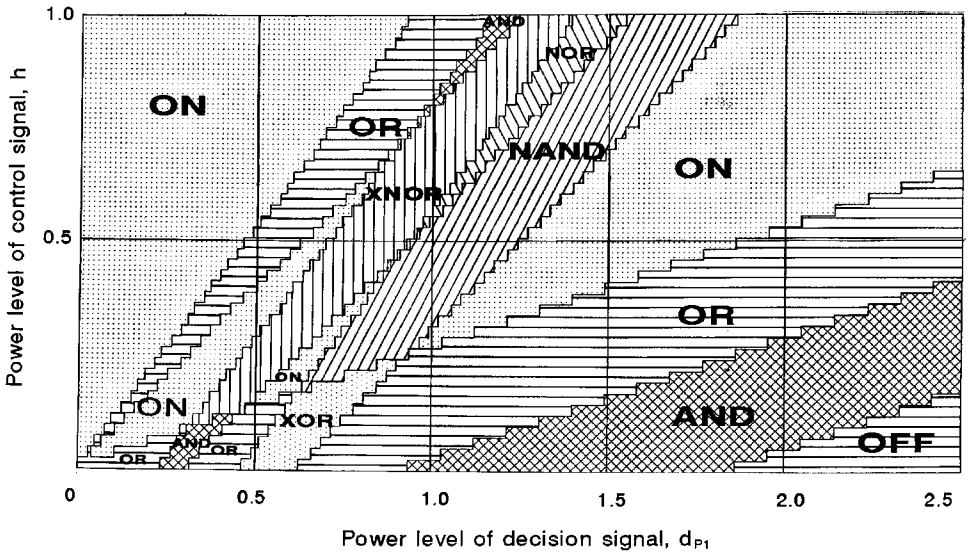

Fig. 2. OPLC working diagram for output O_1 (output O_2=OFF).

"1". The geometric pattern of this figure shows different areas corresponding to the different Boolean logic function, the OPLC is able to perform. As it can be seen, the boundaries are step-like. If we try to measure the total area for a particular logical function the task is not straightforward. This is because there is no clear mathematical function defining the cell behaviour. This is due to the discrete character of the functions involved in the process. Moreover, it is difficult too because there always exists a certain hysteresis in any real device depending on the type and characteristics of its fabrication. So we can say that this geometric figure is similar to the problem of coast length evaluation that gives us a different length depending on the scale employed to measure it and hence it has a fractal-like structure. Similar diagrams may be obtained for other logic functions at output O_2.

Another important parameter to be fixed on the performed simulation is the width value of the existing hysteresis cycles. Fig. 3a shows how we modelled the device P. As it can be seen, it is based on three step functions related according to the rules indicated on that figure. In any case, there is a certain tolerance in the definition of the transition from the lower to the higher state. This tolerance, that it may be called "internal tolerance", has as a consequence the presence of the indicated hysteresis cycles. Moreover, there is another "external tolerance" related to the previous one. Its influence on the final result appears in the example of Fig. 3b. It is related to the real position of the control value with respect to the decision level. The same input signals may give different results depending on where the control signal with respect to the decision level is located. In the example a function NAND performed in one case and an OR in the other one are shown. These tolerances are of a great importance when our logic cell is applied in optical computing. But, as it will be shown later, they strongly affect any dynamical behaviour. This is the case when a chaotic signal is needed: according to the decision levels, both internal and external, chaos may or may not be obtained although similar conditions are present.

It is clear that the precision adopted at the model has a direct relation with the real situation. When a hardware set-up is present, any device has a certain tolerance in its nominal value. This tolerance is equivalent to the previous one.

3. Dynamical behaviour of the logic cell

In order to analyse dynamically our programmable logic cell, we have extended the above-mentioned method. It is based on a certain representation of the working characteristics of the structure. We call it, the "working diagram" of the cell. This diagram represents the input/output characteristic on a 3D representation. The z-axis gives the Boolean function generated at the output, corresponding to a particular pair of values for control and input signals. The Boolean function is characterised by an hexadecimal value. The reason for choosing this representation will be clarified latter. In this case, we understand as input signal the situation when two equal bits, with value "1", arrive at both input data gates. Moreover, in order to obtain this diagram, the two input data signals must maintain a relation between their frequencies. In this case, the period of an input signal have to be double than the period of the other one. In this way, the internal input signal to P-device is the one represented in Fig. 4. Then, every four bits of the output signal correspond to a Boolean function truth table. We convert these four bits to its hexadecimal value and obtain the corresponding point at the working diagram. Fig. 4 shows also the corresponding hexadecimal value for each Boolean function.

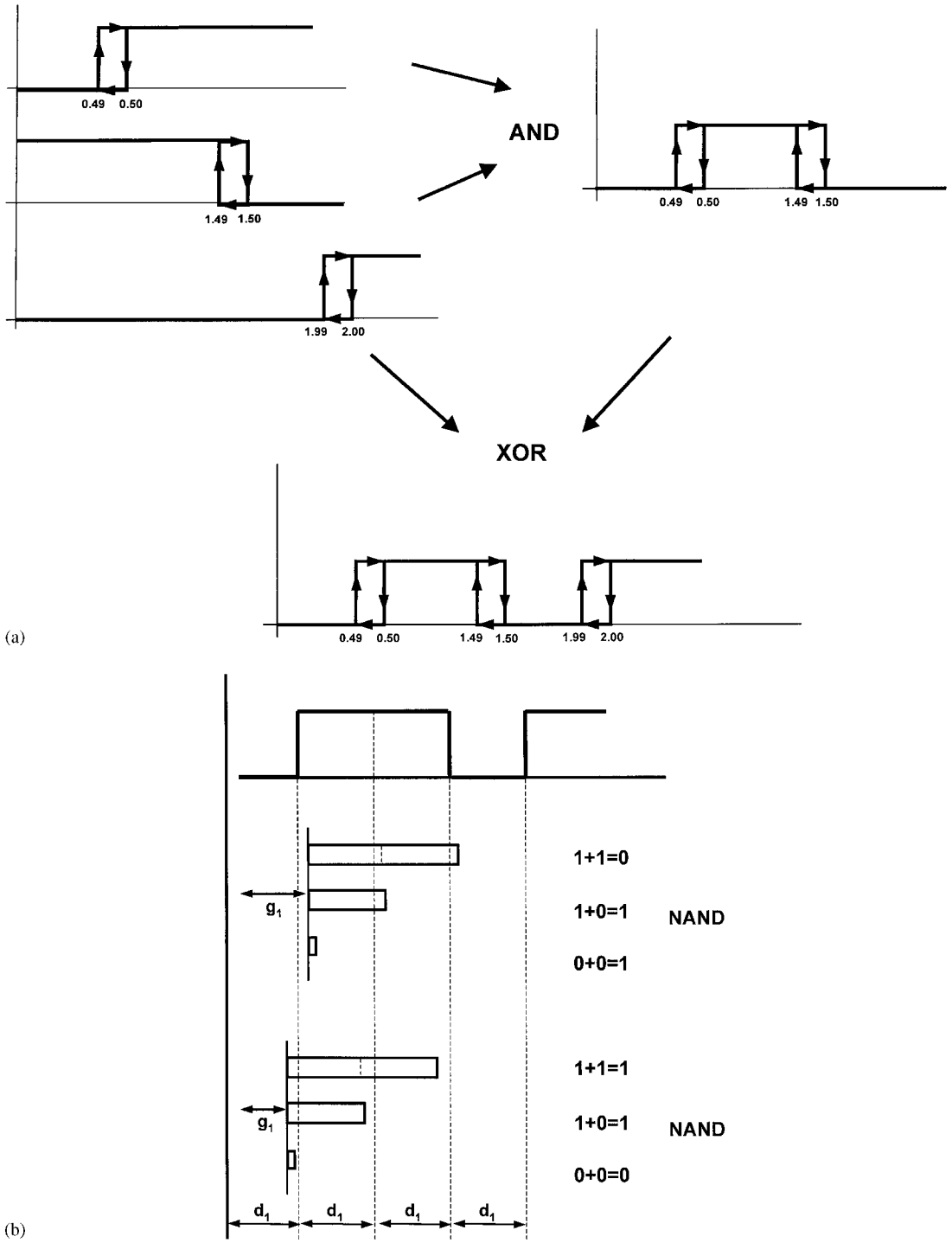

Fig. 3. (a) Influence of internal tolerance on P device characteristics; (b) influence of external tolerance on the obtained logic function.

Fig. 5a is an example of the input/output characteristics for the P-device behaviour on a particular situation. Fig. 5b shows the top view as a 2D diagram. This will be the type of diagrams we will adopt because they are much easier to handle than the previous 3D diagram. Moreover, it has the same information and it is easier to visualise. The case represented here corresponds to an equidistant position between the decision levels on P device, as shown in Fig. 3a. This situation is slightly different from the one reported by us in previous papers. The working diagram in previous works showed the variation with d_1, the equidistant value, normalised to a bit "1", as it is shown in Fig. 2. The representation here corresponds to the behaviour for different values of the input data, for a bit

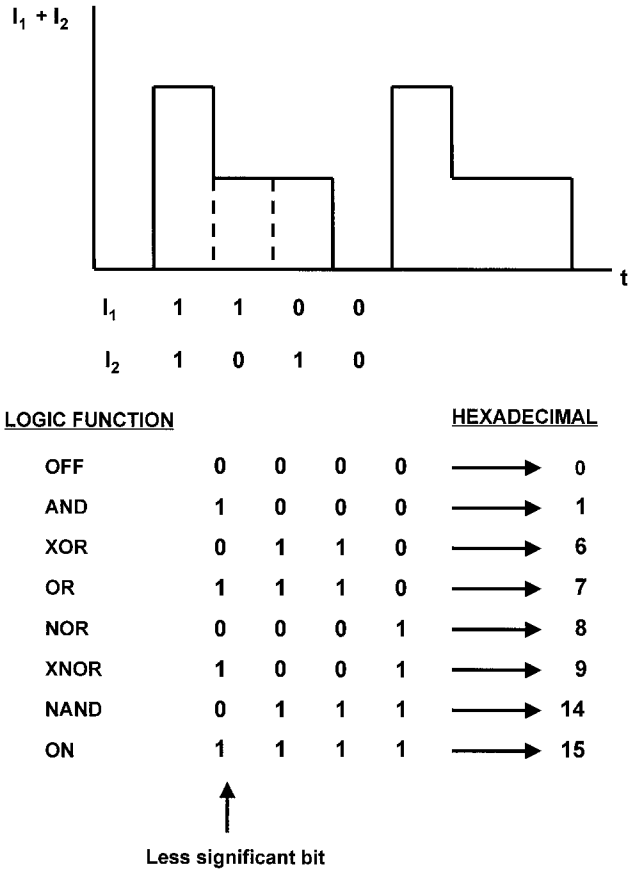

Fig. 4. Internal input signal to P device. Hexadecimal representation of Boolean functions.

"1", and for $d_1 = 0.5$. As it can be expected the representation when the input value of a bit "1" is over 2, the P-device characteristic is obtained as we change the control level. Further studies of OPLC will be reported with its behaviour dependence on the distance between the decision level.

4. Analysis of non-linear behaviour

The situation to be analysed here corresponds to the particular case when a chaotic output is obtained. As it has been shown in the literature, the dynamics of non-linear systems depend strongly on the type of delay that is added to it. This problem was first analysed for optical bistable devices, mainly for the case of hybrid systems, when a finite feedback delay comparable to or greater than the combined time constants of all system components is added. The mathematical analysis was made by difference–differential equations because the behaviour was analogue. Ikeda was the first to apply this type of analysis to a ring cavity system with a non-linear medium [16]. He concluded that new types of instabilities should be found in such system yielding periodic and chaotic solutions. The main result obtained is that the non-linear solution depends on the ratio between external time delay and internal time response. When this ratio (external time over internal time) is much larger than one, a highly non-linear dynamics is achieved. This means that when external time is larger than one order of magnitude than the internal time the situation originates, under certain conditions, a chaotic solution. Furthermore, Okada and Takizawa [17] investigated the effect of a delayed feedback in a hybrid electrooptic system with the restriction that the delay is less than or comparable to the response time of such a system. Neyer and Voges [18], finally, studied the pure effect of the feedback delay on the behaviour of an electrooptic system, neglecting all time constants of the system components.

In order to study the non-linear behaviour we have applied an external delay of 200 time units. The chaotic output has also a dependence on input data period. We have to study this dependence but it is not the objective of this work to analyse it. Here we have to take a relation where the period for one input data is 20 samples time and 33 for the other, and with a pulse width of 10 and 16 samples times, respectively. In this configuration, the input signal to device P shows a form like the one shown in Fig. 6. It corresponds to the addition of two trains of pulses coming from generators f_1 and f_2.

The general diagram of the model simulated appears in Fig. 6. We have studied the dependence, with the amplitude of a bit "1", of input and output digital signals. The output digital signal is feedback with a certain delay and acts as a control signal for device P on the OPLC. Levels for input data and feedback signal are manually changed on the model of Fig. 7. The position where the levels are modified is choosen for a better understanding of the block representation. For example, the output can be modified before the delay without changes on results.

The final result is analysed with a phase diagram as indicated. Simulation time was over 300,000 time units. This phase diagram is similar to other phase diagrams reported by us in previous papers. It represents the situation at the system at time t_{i+1} as a function of the state at time t_i. Because just two states are possible, namely "0" and "1", we have taken four bits sets and represented their hexadecimal value. More details can be seen in Ref. [9].

We have studied, with this method, the region around an input data signal level of value 1 and the region around feedback signal level of value 0.5. Results are shown in Table 2. As it can be seen, there is a strong influence on the precision value adopted. We have indicated with "*yes*" values that give rise to chaotic behaviour and with "*no*" where there is a periodic solution. There is a fractal-like structure similar to the one appearing in Fig. 2.

Figs. 8a–c show the results for a feedback signal fixed to 0.501 and three values of input data, namely 0.99, 0.9999 and 1.0001. They are representatives of Table 2. Fig. 8a shows a time evolution that after a certain interval returns to the initial value and starts again the same

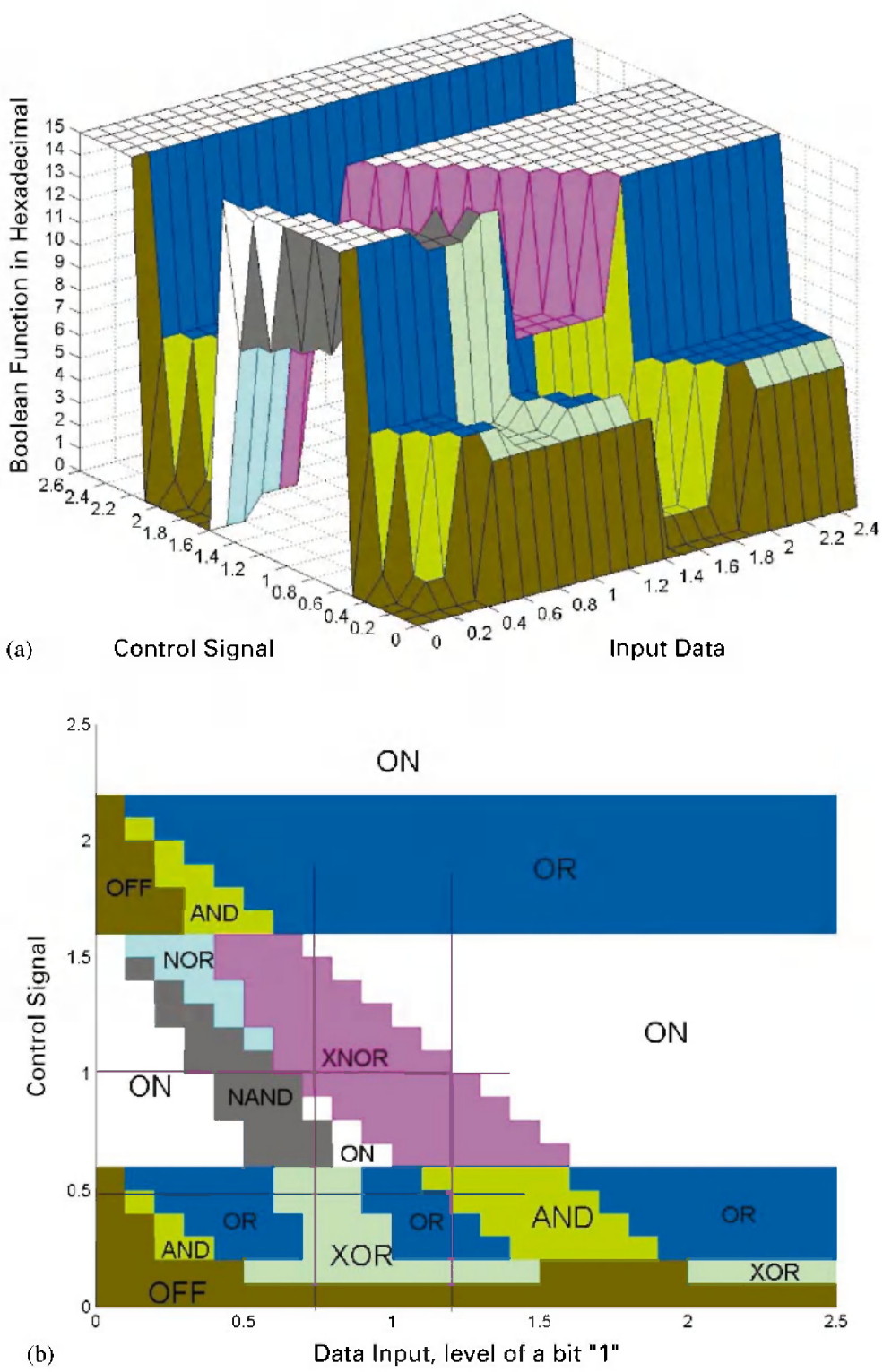

Fig. 5. Working diagram of P device. (a) 3D; (b) 2D.

cycle. Hence, it has a definite period. This time evolution, which does not change after some simulation time, does not give information about period length. It gives information about the time that takes the system to respond with a periodic output. Fig. 8a is representative of the borderline of Table 2 where there is no chaos behaviour for input data values over 1.

The second one, analysed by the same methods employed by us previously in other papers, offers a chaotic behaviour.

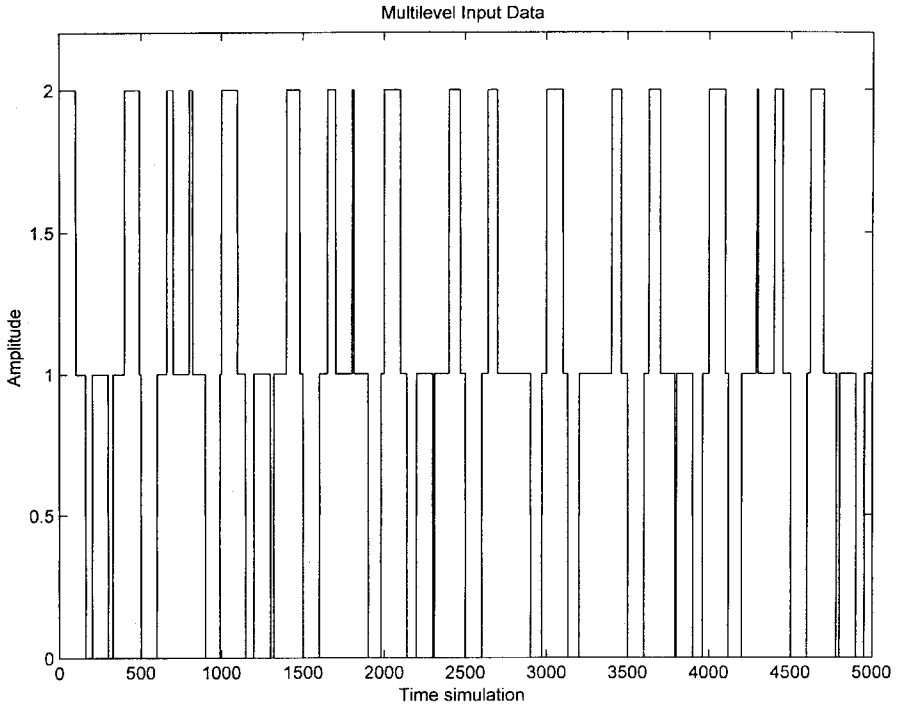

Fig. 6. Real input data signal to P device in Fig. 7.

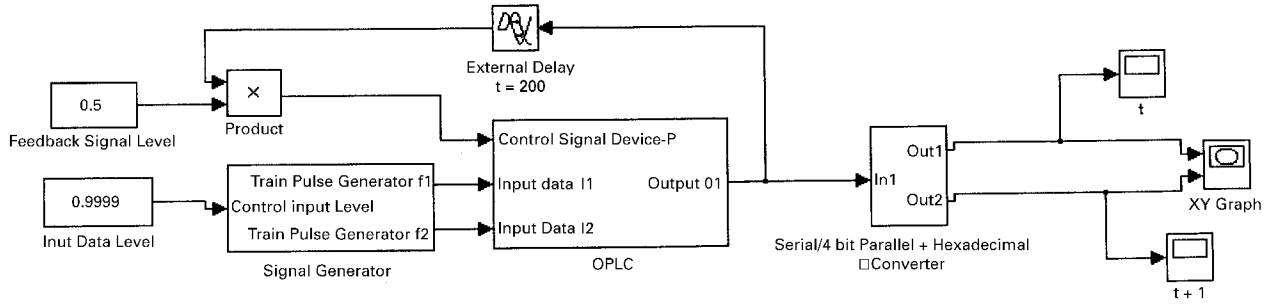

Fig. 7. Simulink^{TM} model for phase diagram generator.

Table 2
Signal levels for chaos generation in the studied interval

		Feedback signal level										
		0.61	0.6	0.5999	0.599	0.59	0.51	0.501	0.5001	0.5	0.4999	0.4
Input data signal level	1.0001	No	No	No	No	No	No	No[a]	No	No	No	No
	1	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No
	0.9999	Yes	Yes	Yes	Yes	Yes	Yes	Yes[a]	Yes	No	No	No
	0.999	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	No
	0.99	Yes	Yes	Yes	Yes	Yes	Yes	No[a]	No	No	No	No
	0.98	Yes	Yes	Yes	Yes	Yes	No	No	No	No	No	No
	0.9	Yes	Yes	Yes	No	No	No	No	No	No	No	No

[a]Results represented in Fig. 8.

Finally, the third one, that it is not chaotic, has a time evolution to a periodic output shorter than the case in Fig. 8a but with a larger fix period. There are other cases as when the input data level is 0.9 (further from the chaos behaviour) that after a simulation time the output is fixed to a value of "1" which is represented on the phase diagram as a point on ($15H$, $15H$).

As a consequence of this result we observe that the non-linear behaviour dependence is not only due to the frequency and delay relation. We have presented only the

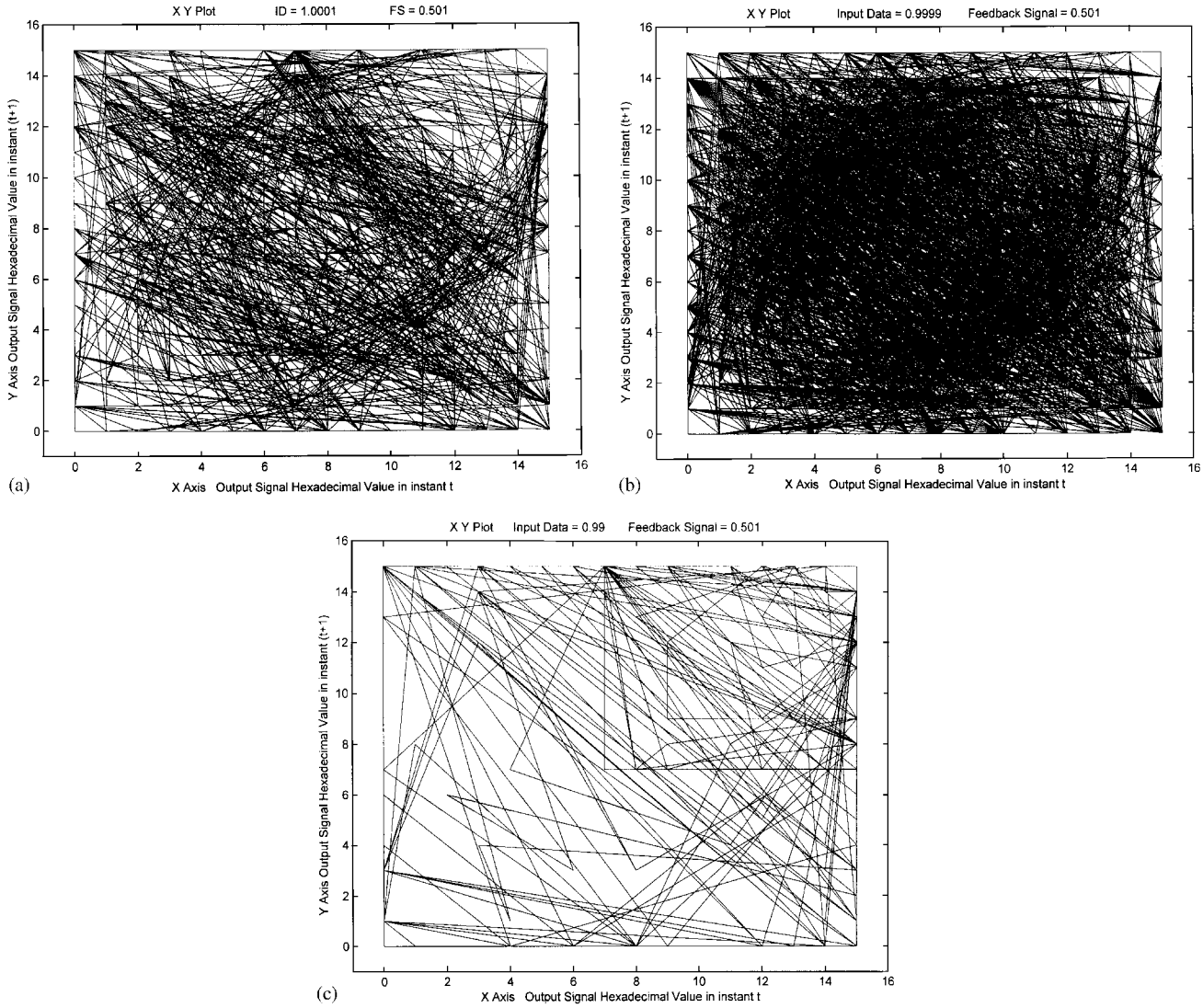

Fig. 8. Phase diagrams for feedback signal level 0.501 and input data signal level: (a) 10001; (b) 0.9999; (c) 0.9900.

results of modifying the value of a bit "1", but the same kind of results has been obtained modifying the value of a bit "0", that in a real design has also a tolerance value.

Also if we look at the working diagram of Fig. 5b we see that around point $(1, 0.5)$ we are almost on the borderline between logic function regions. This can be better appreciated for working diagram with different precision level or scale. Further study will show the dependence of fractal structure of Table 2 and the corresponding diagram. Some ideas related to this aspect are reported in [19].

5. Conclusions

As it is well known, the study of chaotic digital signals is not possible with the same techniques employed in chaotic analogue signals. A different approach is needed and this paper offers a new way to do it. A particular situation has been analysed among the many problems appearing in any optical digital systems. It is the one related to the influence of the precision levels both in components and in signals. Its importance is not just because it may have some incidence on a particular result. It may give rise to very different dynamical behaviours with respect to the previously envisaged. This effect is of particular importance when logic structures are applied in chaotic situations. Signals may have a very long period and in some aspects be like chaotic. The difference with a real chaotic signal is, in some cases, the result of just a small variation in the precision level of some of the involved signals. It is because that a new method to study this situation has been reported in this paper. The main difference with other techniques is the use of a working diagram where some of the main parameters are represented. Logic functions – working diagram – as well as the train

of pulses – phase diagram, have been represented in hexadecimal form. This solution allows us the possibility to represent quantities with higher values than "0" and "1" as are present in binary circumstances. Phase diagrams and 3D representation are now possible. In this way, a first study of how this method can be applied to a particular situation has been reported. It concerns the influence of the adopted precision in input data and feedback signal levels on the onset of chaotic behaviour. The obtained results give us the possibility to establish the validity of our method.

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A. González-Marcos got her Ph.D. from ETS. Ingenieros de Telecomunicacion, U.P.M. (Madrid Politechnical University), in 1993. She was working previously for some private companies in CAD-CAE topics. After her Doctoral Thesis, she was an Assistant Professor at the Alcalá de Henares University and Associate Professor at the Alfonso X University, both in Madrid. She is presently a Professor, from 1996, at the ETS. Ingenieros de Telecomunicacion, U.P.M. Her present interests are Optical Computing, the applications of Chaos Theory to Optical Communications and the modelling of the mammalian retina. She has published several papers on the above topics in technical journals.

J.A. Martín-Pereda got his Ph.D. from ETS. Ingenieros de Telecomunicación in 1971. He is a full Professor at the Madrid Politechnical University from 1975 and a member of several Technical Programme Conferences, mainly in Optical Communications (ECOC, OFC, IOOC) since 1985. Member of the ESPRIT Advisory Board between 1990 and 1993. Member of the Royal Spanish Academy of Engineering since 1995. Senior Member of IEEE and a Member of OSA and SPIE. He has published more than 100 papers in journals and books and has got several academic and technical prizes. His present interest is on the application of Chaos Theory to Optical Communications and Biological Systems.