All-Optical Logic Gates with 1550nm Fabry-Perot and Distributed Feedback Semiconductor Laser Amplifiers

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Abstract

The optical bistability occurring in laser diode amplifiers is used to design an all-optical logic gate capable to provide the whole set of logic functions. The structure of the reported logic gate is based on two connected 1550nm Laser Amplifiers (Fabry-Perot and Distributed Feedback Laser Amplifiers).

1. Introduction

OPTICAL bistability in semiconductor laser amplifiers has attracted attention for use in optical communications and optical computing because of inherent advantages, including optical gain, large fanout, low input power requirements for operation etc. (see for example[1]). The optical bistability appearing in semiconductor laser amplifiers has been used for the development of optical logic gates [2], flip-flop devices [3], optical signal regeneration [4] etc. Under external optical injection, due to the nonlinear dependence of the refractive index of active region's medium and the saturation of gain, a semiconductor laser amplifier exhibits optical bistability. This phenomenon has been studied in Fabry-Perot Semiconductor Laser Amplifiers (FPSLAs) as well as in Distributed Feedback Semiconductor Laser Amplifiers (DFBSLAs) (see for example[1]). The optical bistability has been studied when the amplifier is operated either in transmission or in reflection. When the laser is operated in transmission, its transfer function shows an anticlockwise bistable loop, while in the reflection case, depending on the bias current, the bistable loop changes to a clockwise shape for low enough values of this parameter[5]. These different bistable behaviors occurring either in reflection and transmission have been used to model an all-optical logic gate capable to provide the whole set of logic functions. The structure of the logic gate is based on a two-coupled 1550nm Laser Amplifier configuration and has been modeled with FPSLAs and with DFBSLAs.

2. Schematic of the Logic Gate

Fig. 1. represents a block diagram of the basic structure of the logic gate. Three optical input signals enter into the logic gate. P_{1A} and P_{1B} are two optical data digital input signals while g is an optical control signal. The combination of these signals enter altogether into the logic gate whose Output/Input power relationship is drawn inside the rectangle representing the logic gate. Finally, at the output of the logic gate an optical output signal O_1 is generated and its value is directly a logic function obtained from the two digital data optical signals.

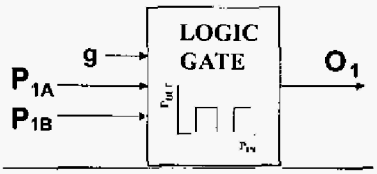

Fig. 1. Block- diagram of the all-optical logic gate.

The '1' bit optical power level of the data signals may have only two distinct power values: P_1 and $2{\cdot}P_1$. The control signal will have one between five different optical power levels: $g_0{=}0{\cdot}P_1$, $g_1{=}1{\cdot}P_1$, $g_2{=}2{\cdot}P_1$, $g_3{=}3{\cdot}P_1$ and $g_4{=}4{\cdot}P_1$. The working mechanism of the logic gate can be explained from fig. 2. The transfer function of the logic gate has only two output states, '1' and '0', depending on the input power and is characterized by three transition points between output states, two changes from '0' to '1' and only one transition from '1' to '0'. Depending on the particular value of the optical control signal g, and the amplitude of the '1' bit of the data digital optical signals a different logic function will be attained at the output of the logic gate. As seen in fig. 2., the whole set of logic functions: OR, AND, XOR, NOR, NAND and XNOR could be obtained at the output of the logic gate.

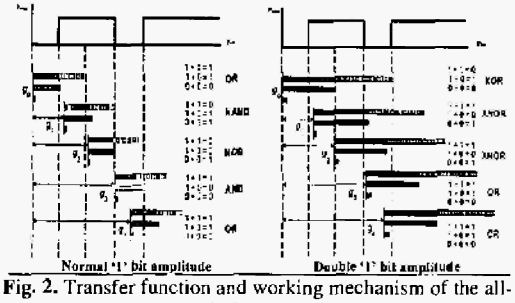

Fig. 2. Transfer function and working mechanism of the all-optical logic gate.

3. All-Optical Logic Gates with SLAs

The basic structure of the all-optical logic gate consists on two-coupled 1550nm Laser Amplifiers and has been modelled using the VPI_ComponentMaker™ software tool. The first laser amplifier is operated in reflection and performs the bulk of the signal processing, while the second laser amplifier, working in transmission, acts as a power threshold detector. A block diagram of this structure appears in Fig. 3. The logic gate has been modelled with FPSLAs and with DFBSLAs. In Table 1 are listed all the parameters used for the simulation of the semiconductor laser amplifiers that compound the configuration of the logic gate.

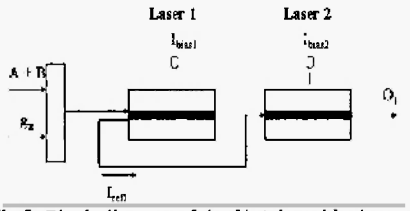

Fig.3. Block-diagram of the SLA based logic gate.

3.1. FPSLA Logic Gate

The individual transfer functions of the two-coupled FPSLAs appear in figs. 4(a) and 4(b) while the final transfer function of the logic gate is represented in Fig. 4(c). To analyze the output/input power relations of figs. 4(a-c) an external optical sinusoidal signal of 1Mhz is injected into the lasers in each case. This optical sinusoidal signal is the result of the external modulation of the output of a CW laser at the wavelength of 1552.52nm, with an electrical sinusoidal signal.

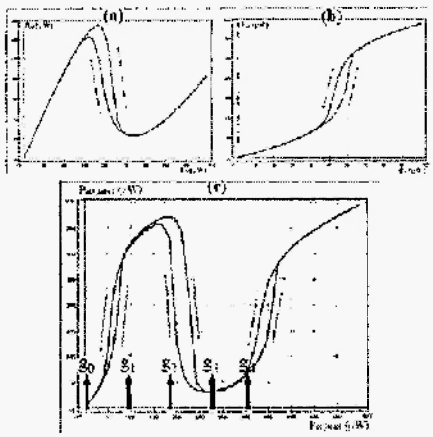

Fig. 3. Transfer functions of the: (a) first FPSLA, (b) second FPSLA, (c) two-coupled FPSLAs.

Working in reflection an FPSLA may exhibit three different forms of optical bistability: anticlockwise, X-shaped and clockwise bistability[5]. The shape of the appearing bistable loop in the output/input power relation changes from an anticlockwise to a clockwise bistable loop as the bias current applied to the FPSLA is decreased. The same evolution also appears as it is increased the frequency detuning existing between the resonant cavity wavelength of the FPSLA and the wavelength of the external signal. As it can be seen in Table 1, the first FPSLA of the logic gate works in reflection and it is polarized with a low bias current (Ibias=0.8·Ith) and a relatively high frequency detuning with the wavelength of the external signal (30Ghz). Under these conditions, the obtained output/input power relation for the first FPSLA, represented in fig. 4(a), is characterized by a clockwise bistable loop with switching between states for an input power of 240μW. In the opposite side the second FPSLA works in transmission and for this mode of operation the appearing optical bistability is always characterized by an anticlockwise bistable loop[5]. As it is observed in fig. 4(b), the output/input power characteristic, of the second FPSLA, switches from a low to a high output state for an input power of 65μW with an associated anticlockwise bistable loop. Under these conditions the second laser amplifier acts as a threshold detector of the power coming out from the first FPSLA. Finally, in fig. 4(c) it is shown the transfer function of the two-coupled FPSLAs that conform the logic gate. This output/input power relation has only two output states and three switching points between output states at 80, 250 and 420μW. This two-FPSLA based structure could perform the functionality of the logic gate if a proper choice of the power levels of the optical input signals is considered. As indicated in fig. 4(c) the final power values chosen are: P_1=90μW, g_0=0·P_1=0μW, g_1=1·P_1=90μW, g_2=2·P_1=180μW, g_3=3·P_1=270μW, g_4=4·P_1=360μW

3.2. DFBSLA Logic Gate

The structure of the logic gate has been modeled also with two connected DFBSLAs whose main parameters are included in Table 1. The individual transfer functions of the laser amplifiers are represented in figs. 5(a) and 5(b). In Fig. 5(c) appears the output/input power relation of the two-DFBSLA connected structure. Once again, to analyze these transfer functions a 1Mhz optical sinusoidal signal at the wavelength of 1552.52nm has been injected into the laser amplifiers.

As in the FPSLA logic gate, the transfer function of the first DFBSLA (working in reflection) is characterized by a clockwise bistable loop while the second one (working in transmission) has a transfer function that switches from a low to a high output state for an input power of 35μW with an associated anticlockwise bistable loop. The resulting transfer function of the two-coupled DFBSLA structure, shown in fig. 5(c), exhibits only two different output states and three switching points at 45, 200 and 330μW. By a

proper choice of the power levels of the input signals, the two DFBSLA coupled structure could also perform the functionality of the logic gate. As indicated in fig. F(c) the final power values are in this case: P_1=70μW, g_0=0·P_1=0μW, g_1=1·P_1=70μW, g_2=2·P_1=140μW, g_3=3·P_1=210μW, g_4=4·P_1=280μW.

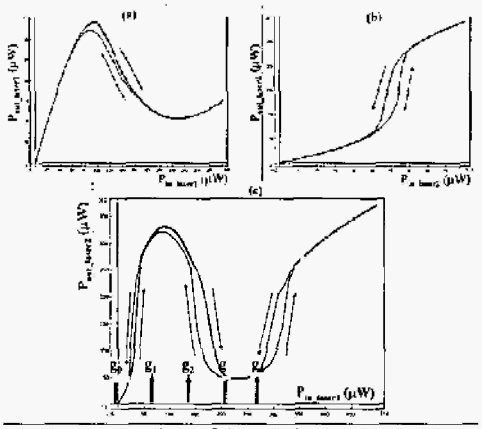

Fig. 5. Transfer functions of the: (a) first DFBSLA, (b) second DFBSLA, (c) two-coupled DFBSLAs.

4. Results

The simulation setup of fig. 6 has been used to study the possible application of the FPSLA and the DFBSLA based structures for the modelling of the proposed all-optical logic gate. A unique CW laser has been used. The output signal of the CW laser is divided in two branches using a 3dB coupler. The lower branch of the coupler output configures the optical control signal *g*. The different levels of the control signal are obtained by controlling an optical attenuator placed in this lower branch. A 90° optical phase shifter is used to correct the laser signal phase shift produced by the coupler. The upper branch of the first optical coupler is used to generate the data digital optical input signals. Two Pseudo Random Bit Sources (PRBS) of 100Mbps are coded electrically with two rectangular electrical signal generators. The two electrical digital signals generated, are added electrically. A Mach-Zender optical modulator is included in the setup to convert that multilevel electrical signal to the optical domain. An optical attenuator is placed after the modulator to adjust the optical power level to the desired '1' bit optical power levels. Finally, by the use of a 3dB optical passive coupler, both signals (the control signal *g*, and the data digital optical signals) are combined and injected into the two-connected semiconductor laser amplifiers, either FPSLAs and DFBSLAs.

Figs. 7(a-f) show the results obtained at the output of the two-FPSLAs and the two-DFBSLAs configurations. In both cases when applying a normal '1' bit amplitude and the control signal g_1 the logic function NAND is attained at the output of the logic gate. In the second case, for the double '1' bit amplitude and the control signal g_3 is applied an OR logic function will be obtained. For the five different control signals, the two possible '1' bit amplitudes the resulting logic functions are exactly the same to that described in section 2 for both kinds of laser amplifiers. Complete results and further analysis is left for future publication.

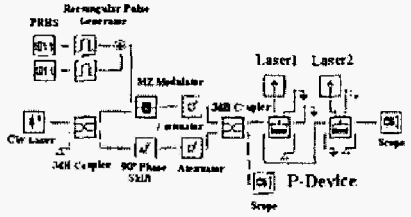

Fig. 6. Simulation setup.

For both laser amplifiers, FPSLAs and DFBSLAs, the whole set of logic functions, including the OR, AND, XOR, NOR, NAND and XNOR, can be executed with power requirements below 100μW for the input data digital signals and below 400μW for the control signals. No time respond study has been done, but it is known that the speed of the logic gate will be limited by the speed of the optical bistability in SLAs, which is in fact governed by the carrier recombination time [6].

5. Conclusions

An all-optical logic gate is reported in this work. The logic gate is composed by two connected Semiconductor Laser Amplifiers and its working mechanism is based in the dispersive optical bistability occurring in this kind of devices. Two different SLAs have been modeled, the first one with Fabry Perot resonant cavity and the second with Distribuited FeedBack configutration.. Both logic gates have the same functionality, and are capable to provide the whole set of logic functions, OR, AND, NOR, NAND, XOR and XNOR, directly in the optical domain at the wavelength of 1.55μm and with low input power requirements for the optical signals involved in the processing. The use of DFBSLAs instead of FPSLAs, due to its single mode operation, results on a lower noise level in the output signal and lower input requirement for switching. The structure of the logic gate proposed in this work can be modeled also with Vertical-Cavity Semiconductor Optical Amplifiers (VCSOAs). These present optical bistability under external optical injection[7], and are expected to have lower input power requirements for operation, being easily integrated in 2-D arrays for parallel processing. The final objective is to evaluate which SLA configuration, of the structure proposed in this work, has the best performance to be used at the Optically Programmable Logic Cell (OPLC) previously reported by the authors[8] in an optical computing architecture.

TABLE I
Laser Parameter for the Fabry-Perot and DFB Laser Amplifiers used along the study.

FP1	FP2	Laser Parameter	DFB1	DFB2
350	400	*Cavity Length (μm)*	300	300
0.3	0.3	*Left/Right Facet Reflectivity*	-	-
0.5	0.5	*Confinement Factor*	0.3	0.3
$2.2\cdot10^{-16}$	$2.2\cdot10^{-16}$	*Linear Material Gain Coeff. (cm^2)*	$3\cdot10^{-16}$	$3\cdot10^{-16}$
6.9	6.9	*Linewidth Enhancement Factor*	5	5
$1\cdot10^{8}$	$1\cdot10^{8}$	*Linear Recombination Coeff. (1/s)*	$1\cdot10^{8}$	$1\cdot10^{8}$
$2\cdot10^{-16}$	$2\cdot10^{-16}$	*Bimolecular Recomb. Coeff. (m^3/s)*	$2\cdot10^{-16}$	$2\cdot10^{-16}$
$8.25\cdot10^{-41}$	$8.25\cdot10^{-41}$	*Auger Recombination Coeff. (m^6/s)*	$8\cdot10^{-41}$	$8\cdot10^{-41}$
10^{24}	10^{24}	*Transparency Carrier Density ($1/m^3$)*	$1.5\cdot10^{24}$	$1.5\cdot10^{24}$
5000	5000	*Fixed Internal Loss (1/m)*	1500	1500
-	-	*Index Grating Coupling Coeff. (1/m)*	10000	10000
$0.8\cdot I_{th}$	$0.88\cdot I_{th}$	*Bias current*	$0.856\cdot I_{th}$	$0.932\cdot I_{th}$
30	15	*Frequency detuning (Ghz)*	10	11

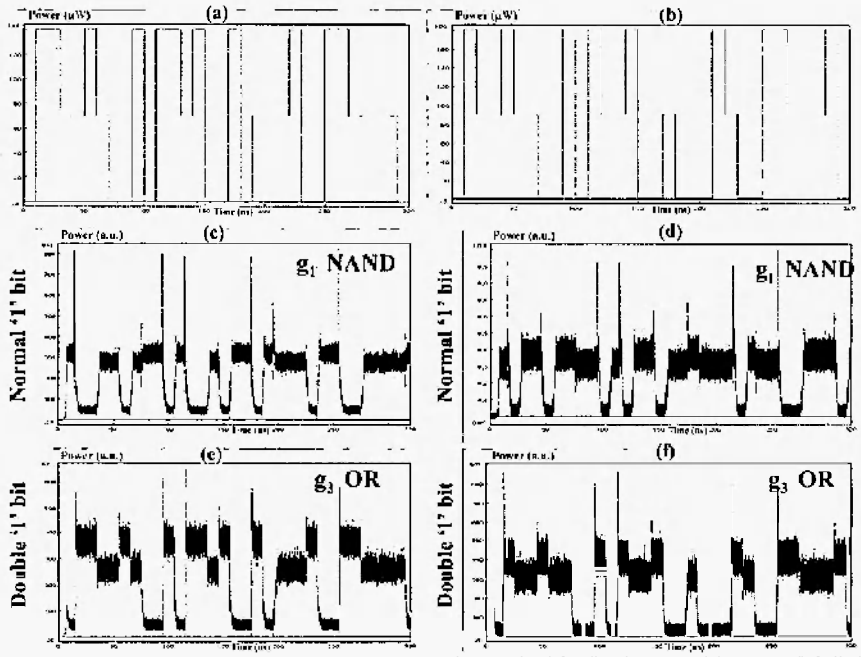

Fig. 6. Input signal (a) FPSLA, (b) DFBSLA; Control signal g1 and normal '1' bit for the (c) FPSLA and (d) DFBSLA logic gate (NAND logic function); Control signal g3 and double '1' bit for the (e) FPSLA and (f) DFBSLA logic gate. OR logic function.

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