

# Loss Model for a High Frequency and Low Load dc-dc Synchronous Buck Converter

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**ABSTRACT** — *This work presents a behavioral-analytical hybrid loss model for a buck converter. The model has been designed for a wide operating frequency range up to 4MHz and a low power range (below 20W). It is focused on the switching losses obtained in the power MOSFETs. Main advantages of the model are the fast calculation time and a good accuracy. It has been validated by simulation and experimentally with one GaN power transistor and two Si MOSFETs. Results show good agreement between measurements and the model.*

## I. INTRODUCTION

One of the most useful tools in the design and optimization of a converter is a power losses model. It can be used to select the best architecture for a set of specifications or to choose the best devices at the topology level to optimize the efficiency of the converter. In the literature, several types of model can be identified:

- Analytical model [1,2,3,4,5]
- Behavioral model [6,7]
- Physics model [8,9]

A physics based model has the advantages of a high level of detail, but the disadvantages of a long time of computation, even with a high performance computer. The behavioral model is balanced in terms of accuracy and computation time, but can have accuracy problems if the static and dynamic nonlinear effects are not considered. Finally, the analytical model relies on equations that take into account the non-idealities of the converter, and provides a faster simulation. Despite being a faster method compared to the other ones, its accuracy is the weakest point.

In this work a hybrid implementation between a behavioral and an analytical loss model is presented. It combines the advantages of both of them to manage good accuracy in the efficiency estimation for a low power range and high frequency buck converter, where switching losses are dominant. Main advantages are: firstly a good accuracy, even for low load operating conditions and for a wide frequency range (up to 4MHz). Also the model can be easily applied to any MOSFET whose main datasheet parameters are known. Additionally, due to the behavioral characteristic of the model, the calculation of the main waveforms of the switching transition is done, allowing a validation using any of the time domain simulators available in the market. For this work, it has been used PSpice to

compare the obtained waveforms in the switching transitions with the simulations.

Despite it has not been designed for a particular application, due to the high switching frequency and low power range, one of the most suitable one is the design and optimization of the envelope amplifier to supply the high efficiency radiofrequency power amplifier for EER technique. This application demands a high efficiency power supply that works in a wide range of frequencies, and with a highly variable load. The power and switching frequency requirements can fit applications as the radiofrequency power amplifier for microsatellites or for medium bandwidth communication services as satellite telephony or trunked radio systems.

## II. DESIGN OF THE BUCK LOSS MODEL

The presented model is based on a simplified synchronous buck converter and has been mainly focused on the MOSFETs losses (power losses in magnetic components and capacitors haven't been modeled in this work). Figure 1 shows the schematic circuit of the synchronous buck converter. Due to the high frequency operation, the parasitic inductances of the MOSFET ( $L_d$ ,  $L_s$ ,  $L_g$ ) and also the parasitic inductance of the PCB,  $L_{pcb}$ , are considered.

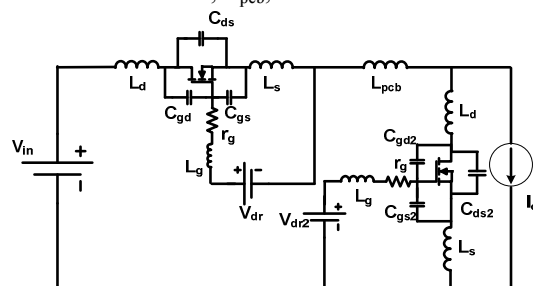


Figure 1. Schematic circuit of the modeled synchronous buck converter

Main assumptions of the model are the load behavior as a current source and the soft-switching of the low side MOSFET. The inductor used in experiments has been designed to obtain an output DC current in all the operating range to decouple the core losses and the wire AC losses from the converter losses.

Analytical expressions to model the nonlinear parasitic capacitances and the forward transconductance have been considered. The parasitic capacitances are obtained using the equation (1) to fit the datasheet

curves, where  $C_p$  ( $C_{ds}$ ,  $C_{gs}$  or  $C_{gd}$ ) depends on the  $V_{ds}$  and on three constant parameters:

$$C_p = (V_{ds}(t) + k_1)^{k_2} \cdot k_3 \quad (1)$$

The equation model of the transconductance is based on the same equation type. The three constant parameters are calculated to fit accurately the datasheet curves. Where this equation has not fitted properly the capacitance curve a piecewise-polynomial function has been used. This method for modeling the capacitances is important because allows the use of the model for different types of power transistors, as GaN, with a different shape for the parasitic capacitances compared to Si MOSFETs.

Additionally, the following parameters are considered for the model:  $V_{dr}$  and  $V_{dr2}$  (drivers input voltages),  $V_d$  (body diode forward voltage),  $Q_g$ ,  $Q_{rr}$ ,  $V_{th}$ , dead times between control signals,  $R_g$  and inductor  $R_{dc}$ . All these parameters have been also obtained from the datasheet. However, measurements of parasitic capacitances, transconductance at different  $V_{gs}$  voltages,  $R_{DSon}$  have been done to increase the accuracy of the analytical expressions and to check the accuracy of the datasheet parameters.

As it can be deduced from Figure 1, it is very complex to obtain the equation that describes the converter in a closed form, especially when it is necessary to model non linear capacitors and variable transconductance. These parameters have strong influence on the efficiency estimation as it will be shown in the final paper and if they are modeled with constant values it can lead to huge error in the estimation. Therefore, a different approach has been used:

- Obtention of the equivalent circuit for each period of the transition.
- Calculation of the differential equations of the state variables for each period.
- Iterative process of the numerical calculation of the state variables evolution with a fixed time step (1ps).
- At the end of the transition all the losses are calculated from the energy losses obtained during the transition. After the last period of a switching transition, the energy stored in the parasitic components is discharged and therefore, taken into account as part of the losses.

The proposed model is based on two main transition periods (high side turn-on and high side turn-off) that are modeled independently. Starting from the steady state conditions at the beginning of the transitions, the main waveforms and the losses can be obtained. The main intervals are based on [5], but the implementation of the equations, the converter model, the parameters that are considered and the analytical curves obtained has been done under a different approach. Each switching transition is divided into several sub-periods,

so each one corresponds to a different equivalent circuit whose differential equations are calculated.

*1.-High side MOSFET turn-on:*

1.1-( $V_{gs} \leq V_{th}$ ): The turn on interval starts with the high side MOSFET off and with the driver voltage  $V_{dr}$  applied, so  $V_{gs}$  starts to increase. The behavior of the transistor is an open circuit for this interval, which lasts until  $V_{gs}$  reaches the threshold voltage of the MOSFET. The differential equations of the state variables in this period are the following:

$$\frac{di_d}{dt} = \frac{V_{in} + V_d - V_{ds}(t) + L_s \cdot \left( \frac{V_{gs}(t) + R_g \cdot i_g(t) - V_{dr}}{L_g + L_s} \right)}{(L_d + L_{pcb} + L_d + L_s + \frac{L_g \cdot L_s}{L_g + L_s})} \quad (2)$$

$$\frac{di_s}{dt} = \frac{(V_{dr} - R_g \cdot i_g(t) - V_{gs}(t)) \cdot (L_d + L_{pcb} + L_d + L_s) + L_g \cdot (V_{in} + V_d - V_{ds}(t))}{L_s \cdot L_g + (L_d + L_{pcb} + L_s + L_d) \cdot (L_s + L_g)} \quad (3)$$

$$\frac{dV_{ds}}{dt} = \frac{\frac{i_d(t) + i_g(t)}{C_{gs}} + \frac{i_d(t)}{C_{gd}}}{1 + \frac{C_{ds}}{C_{gd}} + \frac{C_{ds}}{C_{gs}}} \quad (4)$$

$$\frac{dV_{gs}}{dt} = \frac{\frac{i_d(t) + i_g(t)}{C_{ds}} - \frac{i_d(t)}{C_{ds} + C_{gd}}}{\frac{C_{gs}}{C_{ds}} + \frac{C_{gd}}{C_{ds} + C_{gd}}} \quad (5)$$

The equations for the other state variables of the simplified buck converter ( $i_g$  and  $V_{gd}$ ) are obtained from (2) to (5). These values are added to the state variables value of the previous period in an iterative process.

1.2- ( $V_{ds}(t) > R_{DSon} \cdot I_o$ ) & ( $I_d \leq I_o$ ): The second stage starts when  $V_{gs} > V_{th}$  and lasts until  $i_d$  or  $V_{ds}$  reach their final values. As a simplification, it is used  $I_o$  instead  $I_o - (\Delta I_o / 2)$  due to the design of the inductor so the current has only DC component. For this interval, the transistor is modeled by a current source whose value is the transconductance analytical equation calculated from the datasheet.

Equations (2) and (3) are valid for this sub-interval. However, the equations for the voltages change:

$$\frac{dV_{ds}}{dt} = \frac{\frac{i_d(t) - i_{source} + i_g(t)}{C_{gs}} + \frac{i_d(t) - i_{source}}{C_{gd}}}{1 + \frac{C_{ds}}{C_{gd}} + \frac{C_{ds}}{C_{gs}}} \quad (6)$$

$$\frac{dV_{gs}}{dt} = \frac{\frac{i_d(t) - i_{source} + i_g(t)}{C_{ds}} - \frac{i_d(t) - i_{source}}{C_{ds} + C_{gd}}}{\frac{C_{gs}}{C_{ds}} + \frac{C_{gd}}{C_{ds} + C_{gd}}} \quad (7)$$

1.3- If ( $V_{ds} \leq R_{DSon} \cdot I_o$ ) & while ( $I_d < I_o$ ): In this third period, the transistor is modeled by the on resistance of the datasheet. If the current is faster than the drain-source voltage, the model skips this period and the analysis goes to the final period.

In this sub-period, only the voltages equations are modified, substituting  $i_{source}$  from (6) and (7) for  $V_{ds}(t)/r_{on}$ .

1.4- In the final part of this transition it is considered, for the parasitic inductances and the capacitances, the discharge of the remaining energy until the steady state is reached, and in this process the losses are produced by ringing. It is assumed that, in the range of operation, the parasitic components are discharged and the steady state is reached both in  $t_{on}$  and  $t_{off}$  intervals.

1.5- A final calculation of the losses is done so when the second transition ends all the data are available. Losses in this period are in:

- Driver
- Body diode conduction
- Reverse recovery
- Dead time
- Ringing loss due to the energy stored in the parasitic components of the high side MOSFET.
- Switching losses

Additionally, the conduction losses are added. An advantage of the implementation method for calculating the losses is that for  $C_{oss}$  discharge (in case the voltage is slower than the current), at the end of the transient, it can be updated the value of the capacitance each step as the  $V_{ds}$  is decreasing, which has a high impact in the value of this partial losses.

2.-High side turn-off: Initially, the  $V_{dr}$  of the high side MOSFET is turned to zero and the  $V_{gs}(t)$  starts to decrease. During this transient, the low side MOSFET is considered to behave as an open circuit. Parasitic inductances are considered the same for both MOSFETs.

2.1- ( $i_d \leq i_{source} = f(V_{gs})$ ): The HS side transistor is modeled by the on resistance. The differential equations of the state variables in this interval are the following:

$$\frac{di_d}{dt} = \frac{A(t)+B(t)}{C} \quad (8)$$

$$A(t) = V_{in} - V_{ds}(t) - V_{ds2}(t) \quad (9)$$

$$B(t) = \left( \frac{V_{gs}(t)+R_g \cdot i_g(t)+V_{gs2}(t)+R_{g2} \cdot i_{g2}(t)}{L_g+L_s} \right) \cdot L_s \quad (10)$$

$$C = 2 \cdot L_d + L_{pcb} + 2 \cdot L_s \cdot \frac{L_g}{L_g+L_s} \quad (11)$$

$$\frac{di_s}{dt} = - \frac{(V_{gs}(t)+R_g \cdot i_g(t) - \left[ \frac{di_d}{dt} \right] \cdot L_g)}{L_s+L_g} \quad (12)$$

$$\frac{di_{s2}}{dt} = - \frac{(V_{gs2}(t)+R_{g2} \cdot i_{g2}(t) - \left[ \frac{di_d}{dt} \right] \cdot L_g)}{L_s+L_g} \quad (13)$$

$$\frac{dV_{ds}}{dt} = \frac{i_d(t) \cdot \frac{V_{ds}(t)}{r_{on}} + i_g(t) \cdot \left( i_d(t) \cdot \frac{V_{ds}(t)}{r_{on}} \right)}{C_{gs} + \frac{C_{ds}}{1 + \frac{C_{ds}}{C_{gd} + C_{gs}}}} \quad (14)$$

$$\frac{dV_{gs}}{dt} = \frac{(i_d(t) \cdot \frac{V_{ds}(t)}{r_{on}} + i_g(t)) \cdot C_{gd} + (i_g(t) \cdot C_{ds})}{C_{gs} \cdot C_{ds} + C_{gd} \cdot C_{gs} + C_{gd} \cdot C_{ds}} \quad (15)$$

$$\frac{dV_{ds2}}{dt} = \frac{\left( \frac{-I_o + i_d(t) + i_{g2}(t)}{C_{gs}} + \frac{-I_o + i_d(t)}{C_{gd2}} \right)}{1 + \frac{C_{ds2}}{C_{gd2}} + \frac{C_{ds2}}{C_{gs}}} \quad (16)$$

$$\frac{dV_{gs2}}{dt} = \frac{(-I_o + i_d(t) + i_{g2}(t)) \cdot C_{gd2} + (i_{g2}(t) \cdot C_{ds2})}{C_{gs} \cdot C_{ds2} + C_{gd2} \cdot C_{gs} + C_{gd2} \cdot C_{ds2}} \quad (17)$$

2.2- ( $V_{gs} > V_{th}$ ) and ( $V_{dsLS} > -V_d$ ): The high side MOSFET behaves as a current source. The  $V_{dsLS}$  voltage continues decreasing.

For this subinterval, the same current formulas are applied. The equations for the voltages of the high side MOSFET change by modifying (14) and (15) substituting the term  $V_{ds}(t)/r_{on}$  for  $i_{source}$ .

2.3- ( $V_{gs} < V_{th}$ ) and while ( $V_{dsLS} > -V_d$ ) & (transition time < dead time): The gate-source voltage has decreased below the threshold voltage but there is still a  $V_{ds}$  voltage in low side. The high side MOSFET behaves as an open circuit.

The equations of the currents do not change and in the equations of the voltages of the high side MOSFET, the term  $i_{source}$  is eliminated.

2.4- ( $i_d > 0$ ) & (transition time < dead time): There is low side body diode conduction and the equations are recalculated again until one of the two conditions applies.

2.5- Finally, as in the previous transition, the ringing losses that correspond to the parasitic capacitances and inductances are obtained.

3.-Final calculations: Once all the losses are calculated, the efficiency is obtained and the desired waveforms are shown. The MOSFET voltages including the package (and the associated parasitic inductances) can be also obtained, which is useful to compare the obtained waveforms with the measurements.

### III. MODEL IMPLEMENTATION AND VALIDATION

The model has been implemented as a function in MATLAB and has the following input data: input and output voltages and output current, switching frequency,

dead times and all the parameters described in section II. With this loss model, as the equations are valid for any MOSFET that is used, the process to adapt it for a particular device is simplified as only the analytical equations have to be recalculated. The presented model allows, as said above, the calculation of the main waveforms of the converter. It can be used for a first theoretical validation, comparing the calculated waveforms to the simulation results obtained with a time domain simulator. Figure 2 shows the main waveforms of current and voltage of a high-side turn on transition and in Figure 3 it is shown the good correspondence on the first 2ns of the high side MOSFET turn-on between PSpice and the proposed model.

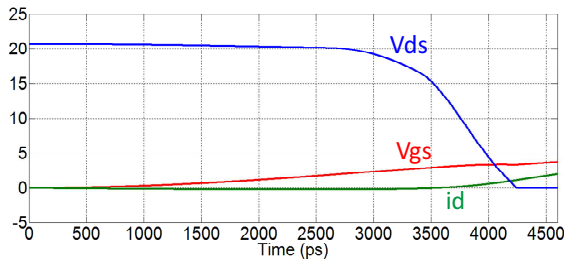


Figure 2. Waveforms of  $V_{ds}$ ,  $V_{gs}$  and  $i_d$  obtained with the proposed model for a high side turn-on transition

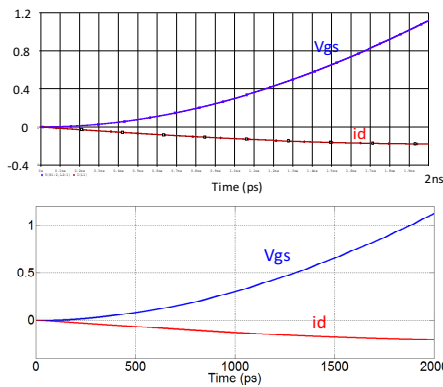


Figure 3. Waveforms of  $V_{gs}$  and  $i_d$  at the beginning of the high side turn-on transition (first 2ns). PSpice simulation (up) and proposed model (down)

#### IV. EXPERIMENTAL RESULTS

An experimental validation of the model has been done using three different MOSFETs. Two Si devices, IRFR3707Z and BSZ058N03, and one GaN device: EPC1015. Measurements have been done with the following specifications: Frequency from 500kHz to 4MHz, input voltages of 20V and 15V and an output voltage of 10V and 7.5V respectively and an output power range from 2.5W to 18W.

The dead times, drivers input voltages and currents together with input and output voltages and currents have been measured on the prototype. The parasitic inductances have been estimated from the simulation model that the fabricant supplies. For the driving stage,

ISO722 and EL7158 have been used. The magnetic component has been designed, to avoid having output current ripple.

On Figures 4 to 9 the results of the comparison can be seen. It can be appreciated that there is a good correspondence between measurements and the model for all the tests done. The highest efficiency differences are 3% at 18W and 6% at low load. But considering that a 6% of error is obtained at around 6W, the error in the power losses is very small (0.36W).

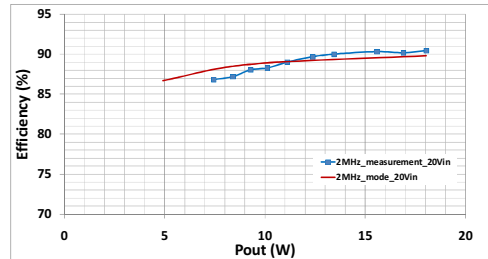


Figure 4. Measured and model efficiencies for IRFR3707Z at 2MHz for 20V  $V_{in}$  and 10V  $V_{out}$

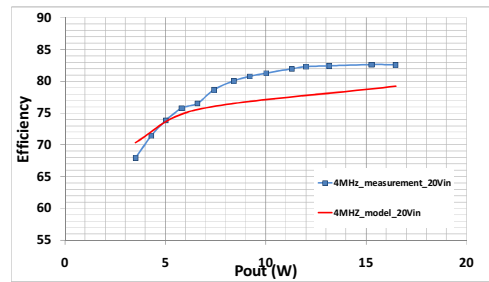


Figure 5. Measured and model efficiencies for IRFR3707Z at 4MHz for 20V  $V_{in}$  and 10V  $V_{out}$

Although good results have been obtained, the model does not include temperature dependencies, or variation of the transconductance curve with the  $V_{ds}$  voltage, which will be implemented in a optimization process of the model and may explain the small deviations between the model and the measurements, making the model more robust for different operating conditions.

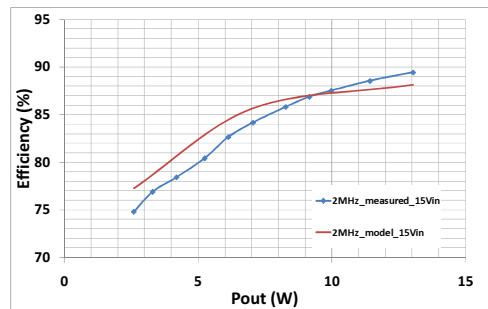


Figure 6. Measured and model efficiencies for BSZ058N03 at 2MHz for 15V  $V_{in}$  and 7.5V  $V_{out}$

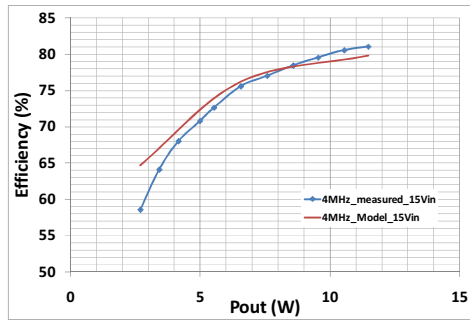


Figure 7. Measured and model efficiencies for BSZ058N03 at 4MHz for 15V  $V_{in}$  and 7.5V  $V_{out}$

Additional future work is an extension of the switching frequency over 4MHz and the consideration of the magnetic losses in the model. The calculation time is not higher than 10 seconds, because the power losses and waveforms are calculated only for one switching cycle.

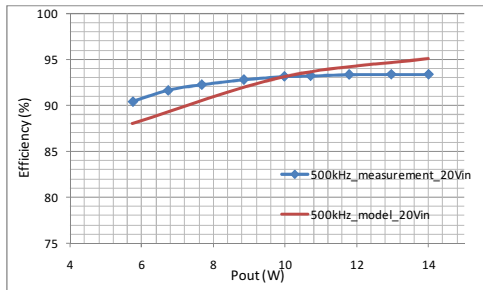


Figure 8. Measured and model efficiencies for GaN EPC1015 at 500kHz; 20V  $V_{in}$  & 10V  $V_{out}$

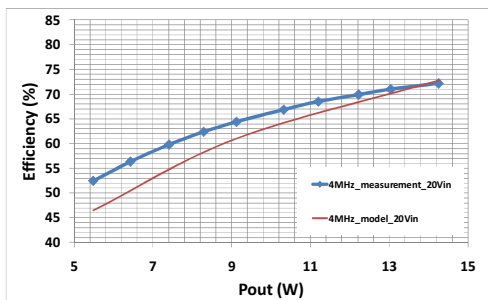


Figure 9. Measured and model efficiencies for GaN EPC1015 at 4MHz; 20V  $V_{in}$  & 10V  $V_{out}$

## V. CONCLUSION

In this work it is presented a hybrid behavioral-analytical model of a buck converter for high frequency range operation up to 4MHz and low power (3W to 18W and  $i_{outmax}=2.5A$ ). The model calculates the power losses of the converter in the switching transitions using only the datasheet main parameters. The computation time of the model is small and also main waveforms of the prototype are provided, using only the datasheet parameters. The model behavior has been validated by simulation comparing it with PSpice.

The model has been validated experimentally with three different devices, one GaN power transistor and two Si MOSFETs, obtaining a good accuracy even at high frequency and low load (maximum error of 6% at  $P_{out}=6W$  at high frequency and a 3% at  $P_{out}=18W$ ).

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