Implementation of intelligent data acquisition system for ITER fast controllers using RIO devices

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Outline

- Motivation and objective.
- ITER Fast Controllers:
  - HW elements.
  - SW elements.
- Methodology.
- Conclusions.

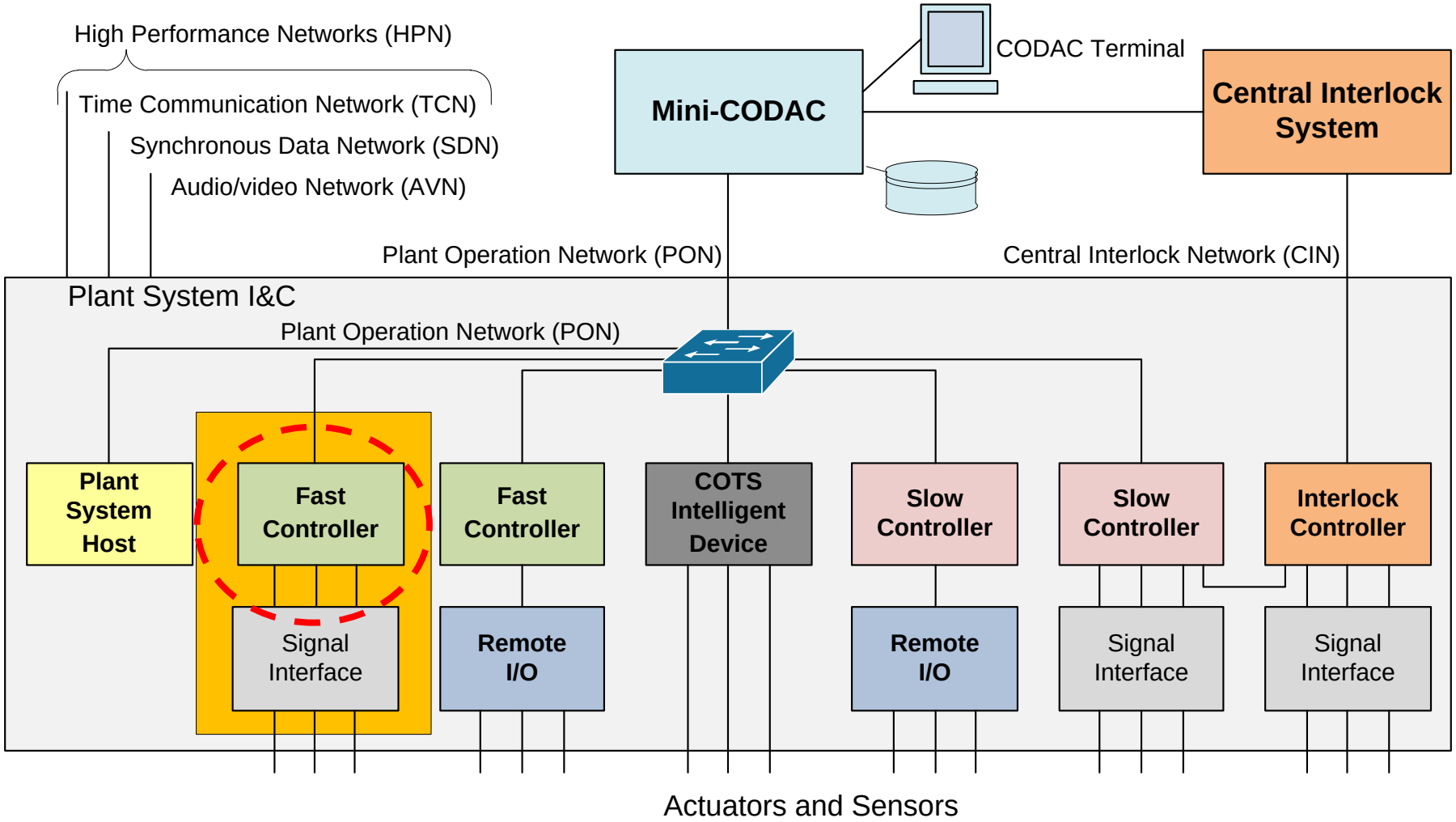
Motivation and Objective

- Implement "data analysis" as close as possible to the Data Acquisition Hardware-> Intelligent DAQ
- Traditional approach-> To Use host CPU to implement data analysis.
- New approaches-> To use FPGA in the DAQ device
  - Advantages:
    - DAQ functionalities are defined by the user.
    - Data analysis is implemented in the FPGA, therefore DAQ provide features of the signals acquired.
    - Simple control loops can be implemented in the FPGA Hardware. Therefore, we have deterministic applications.
  - Disadvantages:
    - No floating point available but you can use "fixed point" algorithms.
    - You need to program the FPGA with their specific tools. This is difficult in general!!!

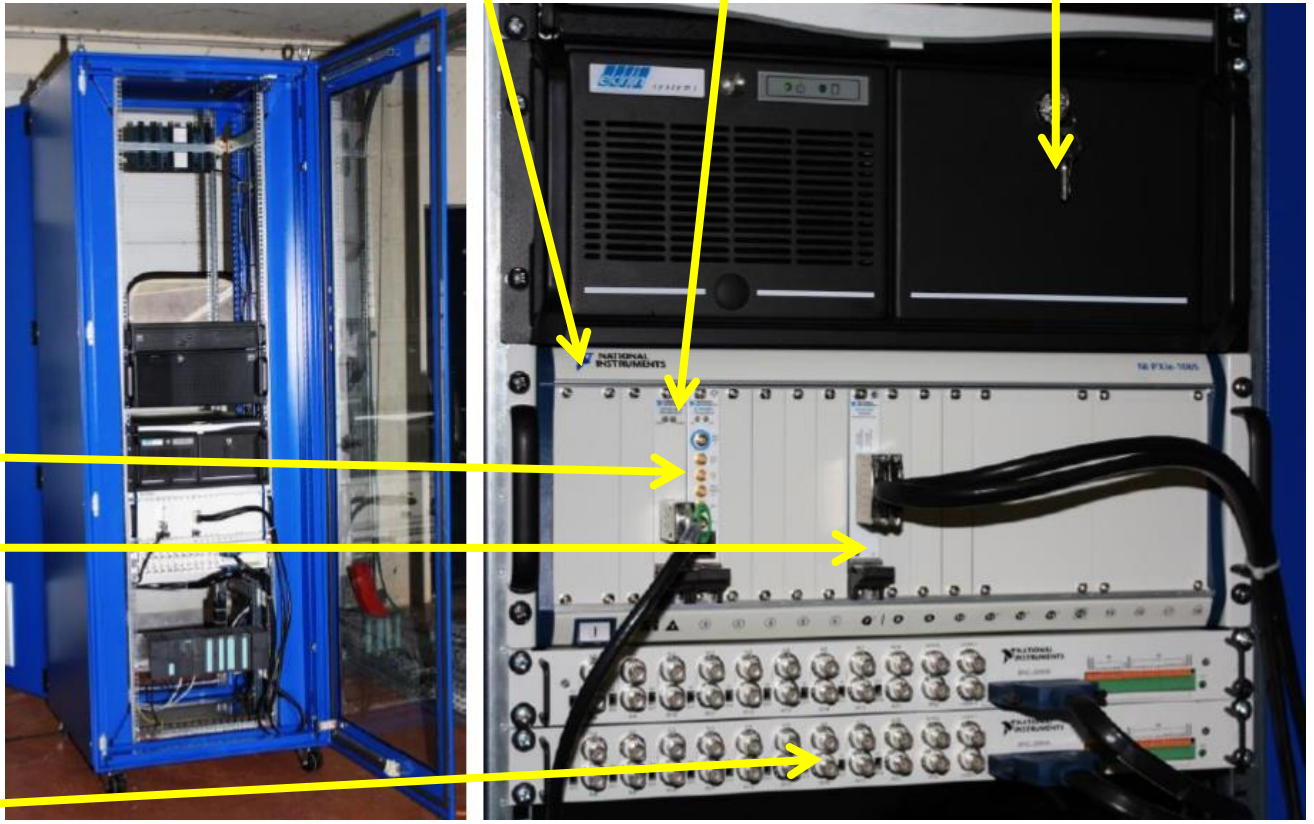
Some interesting points to discuss!!!

- Data analysis applications are infinite and the implementation possibilities too.
  - We need some kind of standardization methods. We have developed a methodology based in the use of reconfigurable input/output (RIO) devices .
- There are a lot of hardware platforms available to implement these applications.
  - We have selected PCIe based solutions in PXIe form factor.
- There are a lot software environment to integrate the solutions.
  - We have selected EPICs to provide compliant solutions to ITER CODAC.

Plant System Instrumentation and Control model defined by ITER-CODAC



Fast controller cubicle



Fast Controller Hardware Elements

PICMG 1.3
Industrial Computer

Ethernet PON

PCIe

PXIe
chassis

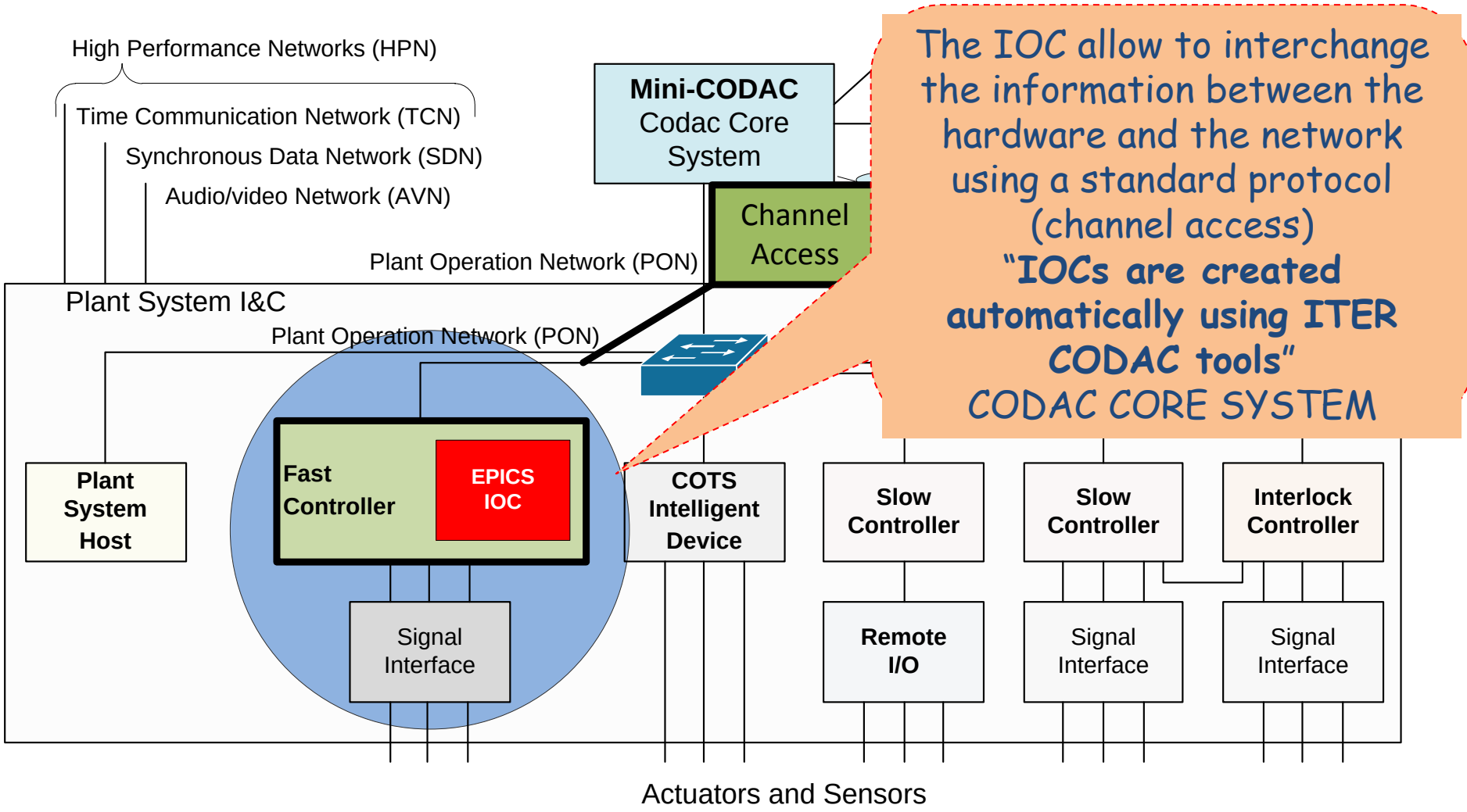
PXI6259
Multifunction DAQ

NI-PXI6682-1588

TCN

RIO
FPGA based DAQ- device

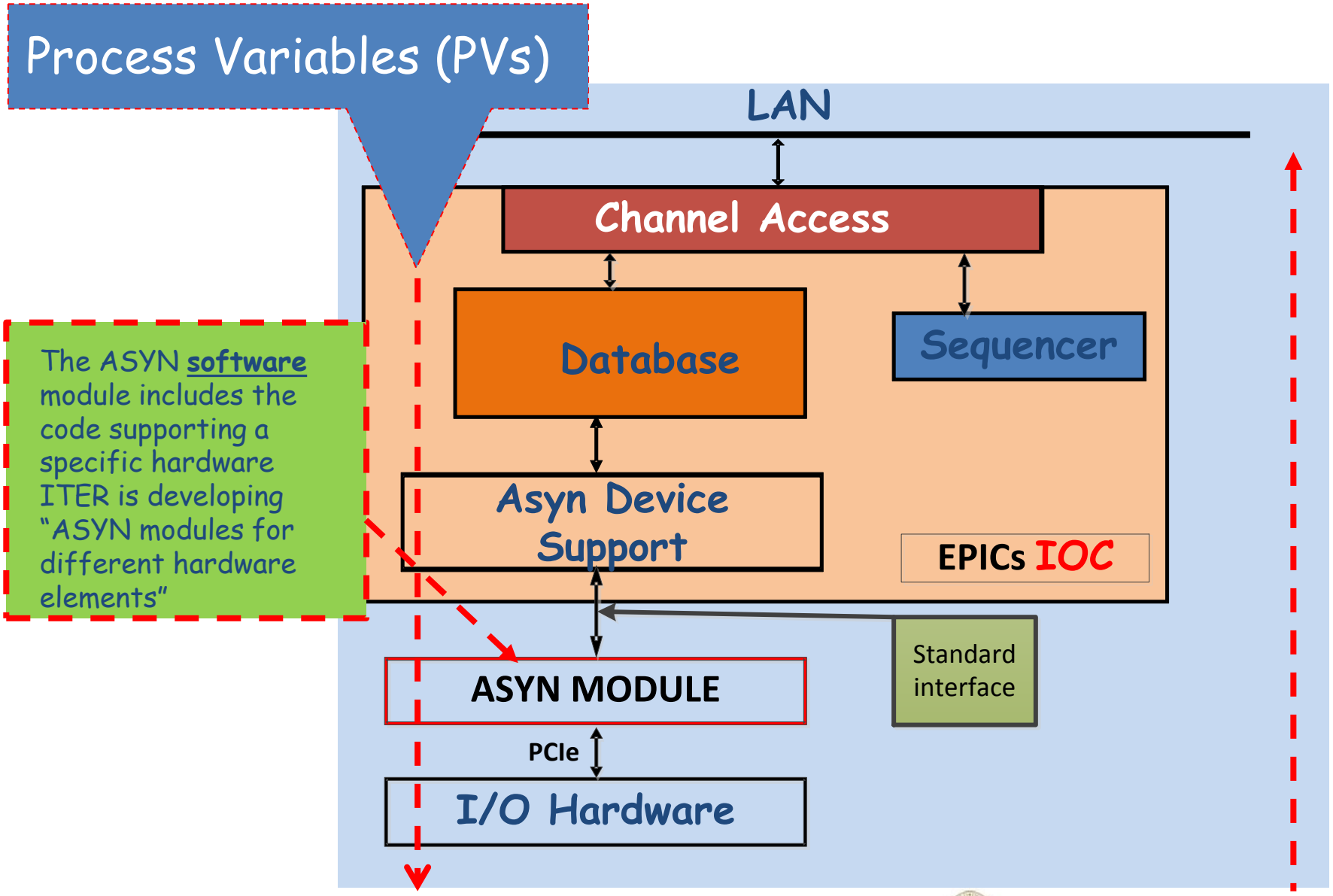
EPICS software architecture



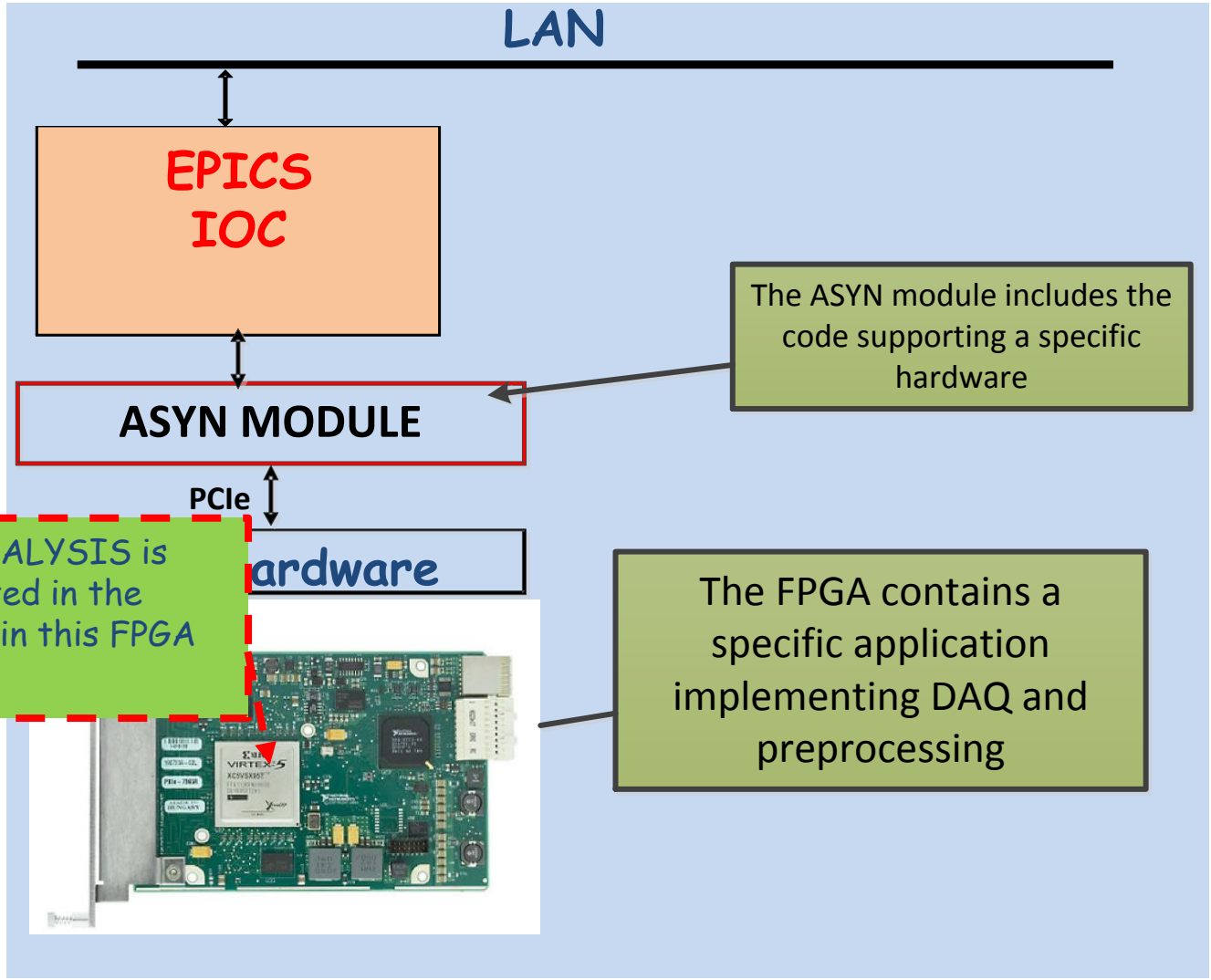
The IOC allow to interchange the information between the hardware and the network using a standard protocol (channel access)

"IOCs are created automatically using ITER CODAC tools"

CODAC CORE SYSTEM


Process Variables (PVs)
LAN
Channel Access
Database
Sequencer
Asyn Device Support
EPICs IOC
The ASYN software module includes the code supporting a specific hardware ITER is developing "ASYN modules for different hardware elements"
Standard interface
ASYN MODULE
PCIe
I/O Hardware

Intelligent DAQ devices



What are the contributions of this work?

- **Implementation of the NIRIO EPICS device support to connect the FPGA resources with ITER CODAC CORE SYSTEM applications.**
  - The implementation of a device support following ASYN methodology in EPICS is not easy. If we are going to implemented multiple solutions in the FPGA, for instance
    - data analysis
    - data processing
    - spectral estimation.
    - data reduction
    - Compression
    - pattern recognition
    - Filtering
    - image processing, etc

    we cannot implement specific device support for each application. We need a <<standard>> device support.
  - **We have created a set of rules to standardize this and we have built this general purpose "device support" for RIO devices.**
  - **The rules must be taken into account in the implementation of the FPGA code.**

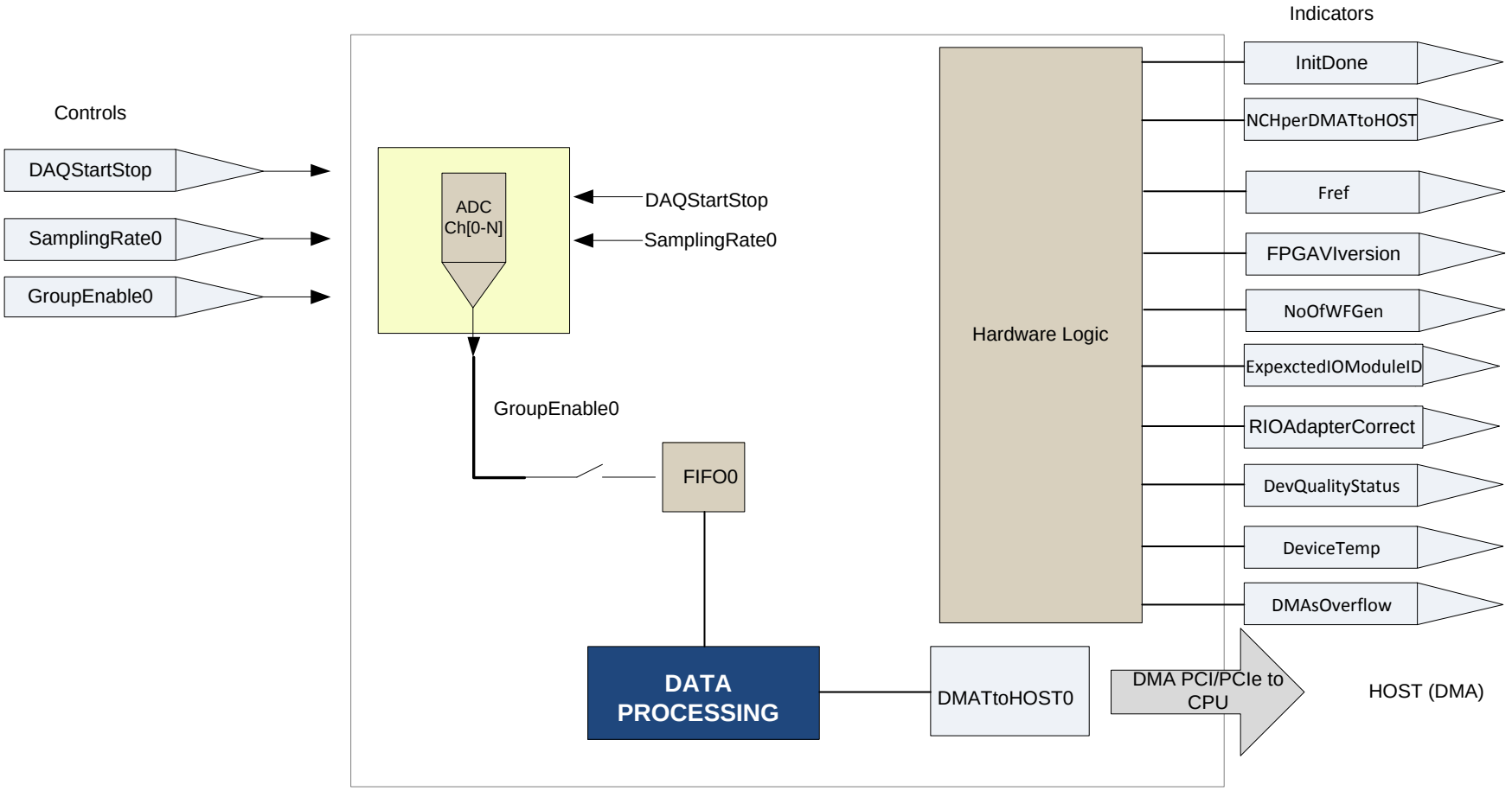
What is the contribution of this work?

- Implementation of the FPGA code supporting data acquisition and preprocessing for your specific application
  - We have simplified the process using LabVIEW for FPGA
    - We have created LabVIEW code patterns for
      - Continuous data acquisition + processing single sample oriented
      - Continuous data acquisition + processing waveform (block) oriented
      - Single event data acquisition + processing
      - Images data acquisition using camera-link interface.
      - Customized triggers
      - IEEE 1588 time-stamping for samples and blocks (using the PXI-6682)
      - Waveform (pattern) generation (periodic signals)
      - Digital input-output.

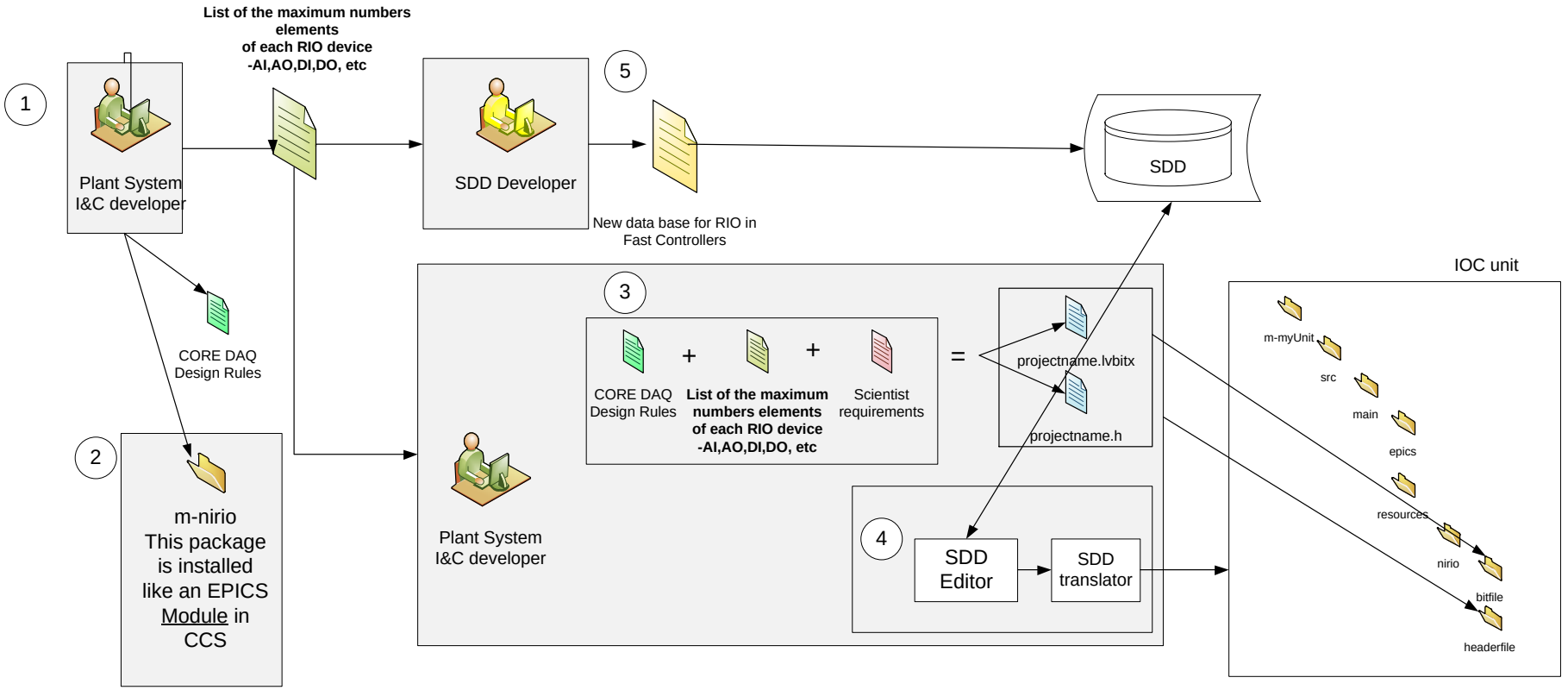
What is the contribution of this work?

- Implement the interface for EPICS to integrate your solution in ITER CODAC CORE SYSTEM.
  - NIRIO EPICS ASYN Device Support implemented
  - The device support searches for the resources available in the FPGA design
  - The device support automatically connects FPGA resources and EPICS records.

FPGA code implementation using "coreDAQ" pattern (block oriented)



Development cycle using CODAC CORE SYSTEM



Steps for implementing "intelligent data acquisition applications

- Select one RIO device and an adapter module
- Develop the FPGA code using LabVIEW for FPGA
  - Test the application!!
  - The output is a bitfile for programming the FPGA
- Download of resource files to the Fast Controller Host
- Create and IOC following ITER Codac Core System Application Manual

Some results obtained

- Continuous data acquisition moving the data to EPICS:
  - Up to 6MS/s using 2 analog input channel (16 bits) in PXI (PCI) modules (24 MB/s)
  - Up to 2MS/s using 32 analog input channel (16 bits) in PXIe (PCIe) modules (≈200MB/s)
- Single triggered data acquisition
  - Up to 100MS/s using 2 channels.
- Data Analysis and Pattern Recognition
  - Real Time Plasma Disruptions Detection in JET Implemented With the ITMS Platform Using FPGA Based IDAQ (IEEE TNS Volume: 58 Issue:4 pp: 1576 - 1581)

Conclusions

- The methodology for integrating data analysis applications in RIO devices has been developed.
- The methodology solves the integration of these applications in ITER fast controllers using EPICS and CODAC CORE SYSTEM tools.
- The FPGA processing capabilities are limited (if we compare them with CPUs or GPUs) therefore new methods like "peer to peer comunications" among FPGAs should be explored

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