Envelope Amplifier Based on Switching Capacitors for High-Efficiency RF Amplifiers

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***Abstract*—Modern transmitters usually have to amplify and transmit signals with simultaneous envelope and phase modulation. Due to this property of the transmitted signal, linear power amplifiers (class A, B, or AB) are usually used as a solution for the power amplifier stage. These amplifiers have high linearity, but suffer from low efficiency when the transmitted signal has high peak-to-average power ratio. The Kahn envelope elimination and restoration technique is used to enhance the efficiency of RF transmitters, by combining highly efficient, nonlinear RF amplifier (class E) with a highly efficient envelope amplifier in order to obtain a linear and highly efficient RF amplifier. This paper presents a solution for the envelope amplifier based on a multilevel converter in series with a linear regulator. The multilevel converter is implemented by employing voltage dividers based on switching capacitors. The implemented envelope amplifier can reproduce any signal with a maximum spectral component of 2 MHz and give instantaneous maximum power of 50 W. The efficiency measurements show that when the signals with low average value are transmitted, the implemented prototypes have up to 20% higher efficiency than linear regulators used as a conventional solution.**

***Index Terms*—Envelope amplifier, envelope estimation and restoration (EER), Kahn's technique, multilevel converter, switching capacitors.**

I. Introduction

In modern radio communications, it is necessary to transmit as much data as possible for the given bandwidth. The best signal modulations are those that perform simultaneous phase and amplitude modulation, and therefore the linearity of the power amplifiers used in these systems is essential. Due to this demand, linear power amplifiers, such as class A or class B, are employed, but, unfortunately, they suffer from extremely poor efficiency when the transmitted signal has low values. For example, ideal class A and class B amplifiers have average efficiency of only 5% and 28%, respectively, when signals with Rayleigh's envelope distribution are transmitted [1]. One of the techniques that are used to enhance the efficiency of the power amplifiers is Kahn's technique. Kahn's envelope elimination and restoration (EER) technique proposes using a dc–dc converter (envelope amplifier) to modulate the voltage supply of a highly efficient but nonlinear power amplifier (class E or class D) [2], (see Fig. 1). This idea is based on the fact that any narrow band signal can be presented as simultaneous amplitude (envelope) and phase modulation

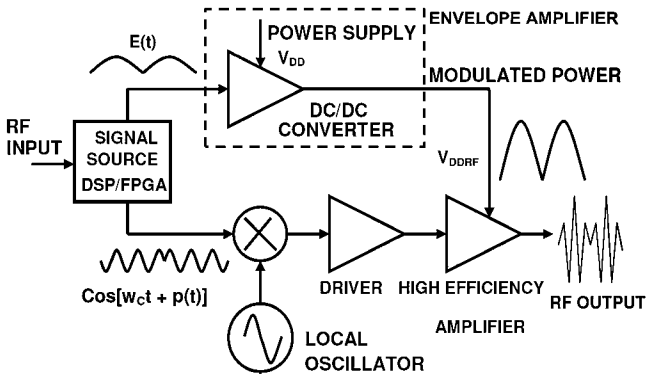

Fig. 1. Block scheme of Kahn-technique transmitter.

$$V_{\mathrm{RF}}(t) = I(t)\cos(2\pi ft) - Q(t)\sin(2\pi ft) = A(t)\cos(2\pi ft + \theta(t)) \quad (1)$$

$$\theta(t) = \operatorname{arctg}\left(\frac{Q(t)}{I(t)}\right) \qquad A(t) = \sqrt{I(t)^2 + Q(t)^2} \quad (2)$$

where f is the carrier frequency, and $Q(t)$ and $I(t)$ are the modulated signals.

Several solutions for the envelope amplifier can be found, such as a simple buck converter (class S modulator) in [3]–[5], multiphase buck converter in [6], three-level converter in [7] or linear-assisted switching amplifier in [8]–[10]. These solutions do not exceed the bandwidth of a few hundred kHz and the output power ranges from mW up to several tens of watts. Their use for applications that require bandwidth in the MHz range is however limited. For example, a buck converter with 1 MHz bandwidth should operate at a switching frequency of at least 5 MHz. In [11] a conventional buck converter with a switching frequency of 130 MHz was used as the solution for the envelope amplifier. The obtained bandwidth was 15 MHz. The fact that this solution was integrated on the silicon chip, together with the PA, facilitated the usage of high switching frequency due to reduced parasitic inductances that are the cause for high switching losses at such high switching frequencies. However, the average output power was just 1 W, while the peak power

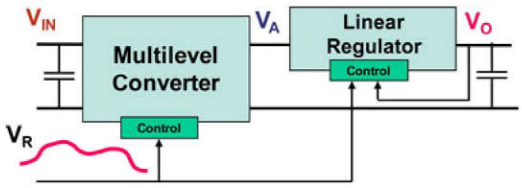

Fig. 2. Simplified schematic of the proposed envelope amplifier.

was 2.2 W. In [12], a solution based on multiple input buck converter is presented and it enables an easier design of the output filter due to pulse width modulation with various voltage levels.

The envelope amplifier should have high linearity, fast dynamic response, high efficiency, and small interference with the spectrum of the output signal. Regarding all these restrictions, a solution that is based on an open-loop multilevel converter in series with a high slew rate linear regulator is presented in Fig. 2 [13]. In this paper, two possible architectures of the multilevel converter are proposed and experimental results obtained with the multilevel converter based on stacked voltage cells are presented.

In this paper, the multilevel converter is based on the second proposed architecture, i.e., on independent voltage sources and analog multiplexer. The independent voltage sources are implemented by voltage dividers based on switching capacitors. Converters that employ switching capacitors offer high efficiency and do not need any bulky magnetic component; thus, their size is significantly smaller compared to classical converters, besides the feasibility of integration [14]. The implemented envelope amplifier can reproduce a sine wave or any other reference of 2 MHz, and give the maximum power of 50 W. Commercial (or academic) solutions to obtain this bandwidth for the envelope amplifier normally need high switching frequency. Unfortunately, this means low efficiency for the envelope amplifier, especially when the output signal has low voltage levels.

II. Proposed Solution

The multilevel converter has to supply the linear regulator and provide discrete voltage levels that are as close as possible to the output voltage of the envelope amplifier. If this is fulfilled, the power losses on the linear regulator will be minimal, because they are directly proportional to the difference of its input and output voltage. However, in order to guarantee correct operation of the linear regulator, the output voltage of the multilevel converter always has to be higher than the output voltage of the linear regulator. Time diagrams of the multilevel converter and linear regulator voltage are shown in Fig. 3.

The linear regulator can be designed to have very high bandwidth, and it should filter all the noise that could come from the multilevel converter. Therefore, the multilevel converter does not need any filter at its output and the design of the complicated filter as in the case of switched converters is avoided.

The multilevel converter presented in [13] is based on independent voltage cells that are put in series and turned ON and OFF depending on the level of the sent reference. The multi-

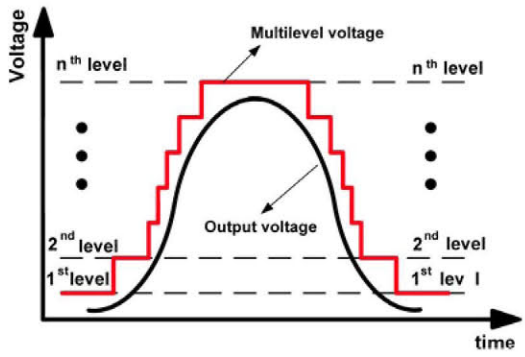

Fig. 3. Time diagrams of the proposed envelope amplifier.

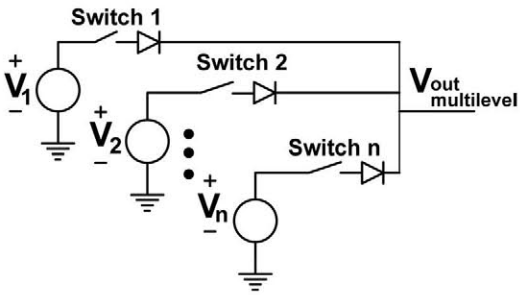

Fig. 4. Multilevel converter realized with independent supplies and analog multiplexer.

level solution in this paper was introduced in [13] and is based on the independent voltage sources that supply the linear regulator through an analog multiplexer. The selection of the active voltage source will depend on the level of the envelope reference. A simplified schematic of the multilevel converter is presented in Fig. 4.

The efficiency of the linear regulator depends on the number of the voltage levels that are applied and their distribution. In [13], it is shown that optimizing voltage levels leads to significant increase of efficiency versus the solution with equidistant voltage levels. Due to the tradeoff between the complexity of the layout, PCB parasitic and possible system efficiency, three voltage levels are selected as an efficient and feasible solution. The optimal distribution for three voltage levels when a signal with high peak-to-average power ratio (PAPR) is transmitted is approximately: V_{MAX}, $\frac{3}{4}\,V_{\mathrm{MAX}}$, $\frac{1}{2}\,V_{\mathrm{MAX}}$, where V_{MAX} is the maximum level of the output signal's envelope.

Due to convenient voltage distribution, these three voltage levels can be produced by two voltage dividers that are based on switching capacitors. The input terminals of the first voltage divider should be connected to V_{MAX} and ground and the voltage at its output would be $\frac{1}{2}\,V_{\mathrm{MAX}}$. The input terminals of the second voltage divider should be connected to V_{MAX} and $\frac{1}{2}\,V_{\mathrm{MAX}}$. Its output voltage would be $\frac{1}{4}\,V_{\mathrm{MAX}}$ referring it to the output of the first voltage divider, i.e., $\frac{3}{4}\,V_{\mathrm{MAX}}$ referring it to the ground of the system. Both voltage dividers are implemented in the same way, using the same topology presented in [14] and shown in Fig. 5.

The multilevel solutions that are based on flying capacitors normally need a capacitor voltage balancing algorithm in order to guarantee equal voltages on the capacitors or, in the

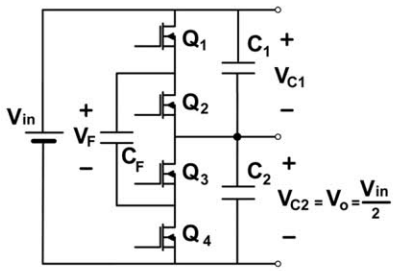

Fig. 5. Voltage divider based on switching capacitors.

TABLE I
VOLTAGE ACROSS THE FLYING CAPACITOR DEPENDING ON THE POSSIBLE SWITCHING STATES OF THE VOLTAGE DIVIDER

Switching State	Q_1	Q_2	Q_3	Q_4	V_F
S_1	1	0	1	0	V_{C1}
S_2	0	1	0	1	V_{C2}

case when these voltages are not the same, it is needed to use modulation techniques that are aware of this [16], [17]. Normally, these converters are used as solutions for inverters, where the output voltage is a sine wave. In the case that the signal to be synthesized is a random signal defined by its probability distribution [15], the time that the signal spends in certain level interval cannot be distinguished exactly, as in the case of a sine wave. These time intervals are easy to determine for deterministic signals, but, two nondeterministic signals with same probability density can have different time behavior and it is difficult to estimate the time intervals the signal spends at each level. This is very important because in most of the solutions based on flying capacitors these capacitors are approximately equally charged and discharged during one period of a sine wave, and, in that way, the voltage levels that are used are roughly equal. In the case of a nondeterministic signal, this equilibrium cannot be easily guaranteed.

Nevertheless, the voltage divider proposed in [14] does not need any special voltage balancing. The voltage balancing is inherently present in its way of functioning. There are only two switching states (Table I) and the role of the flying capacitor is to equilibrate voltages V_{C1} and V_{C2}, by connecting the same voltage during one switching cycle first to C_1 and then to C_2. Both switching states are alternately applied and when V_{C1} and V_{C2} are equilibrated (after several switching cycles), the output voltage and the voltage across the flying capacitor are equal to one half of the input voltage.

Fig. 6 shows the simplified block schematic of the proposed solution for the independent voltage sources.

Solutions based on switching capacitors offer high efficiency at very wide load profiles and low switching frequencies. Additionally, this topology does not use any inductive element and, therefore, are convenient for integration. This is a significant improvement over the proposed solution with the multilevel solution in [13], where it was necessary to implement a flyback converter with three outputs, and where the used transformer was a very bulky and less-efficient component. The possible problems in this solution are increased switching noise due to lack of filtering and complex designs that are used for closed

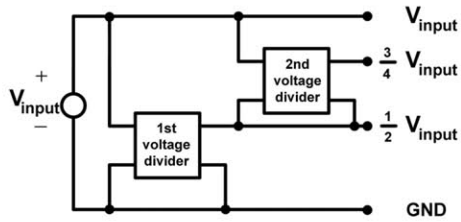

Fig. 6. Block schematic of the proposed solution for the independent voltage sources.

loop solutions. In the proposed solutions, the voltage dividers do not need to have precise control of its output voltages, because the linear regulator that is put in series will perform the fine regulation; therefore, the voltage dividers can work in open loop, while the linear regulator should filter all the noise within its bandwidth that may come from the voltage dividers and analog multiplexer.

The only part of the system that uses high switching frequency is the analog multiplexer. If the reference is a 2 MHz sine wave, the MOSFET's switching frequency inside the multiplexer will be 2 MHz as well. Therefore, it can be said that even in cases in which the reference is a high-frequency signal, the maximum switching frequency in the system is relatively low. The simplified schematic of the system is shown in Fig. 7.

III. MODELING POWER LOSSES

In order to estimate the efficiency of the proposed solution, it is necessary to model all the power losses in the system. The power losses in the proposed envelope amplifier can be divided into three groups.

1) The power losses in the voltage dividers.
2) The power losses in the voltage multiplexer.
3) The power losses in the linear regulator.

A. Power Losses in the Voltage Divider

The mechanism of power losses in the first stage can be divided into three different mechanisms:

1) The switching losses, due to the switching transitions of the used MOSFETs;
2) The conduction losses, due to finite MOSFET resistance ($R_{\rm on}$) and finite series resistance of the used capacitors (ESR);
3) The losses due to charge transition from differently charged capacitors (when the flying capacitor is connected with capacitors C_1 and C_2.

The power losses due to the second mechanism depend only on the selected capacitors and MOSFETs, while the switching losses depend on the MOSFET selection and on the switching frequency of the voltage divider. The last power loss mechanism depends solely on the voltage difference between the flying capacitor and capacitors C_1 and C_2 just before they are connected.

In order to obtain low-voltage ripple, it is desirable that the capacitors C_1, C_2, and C_F have high values because it guarantees that the load current is not able to discharge too much the capacitors C_1 and C_2. At the same time, it guarantees small

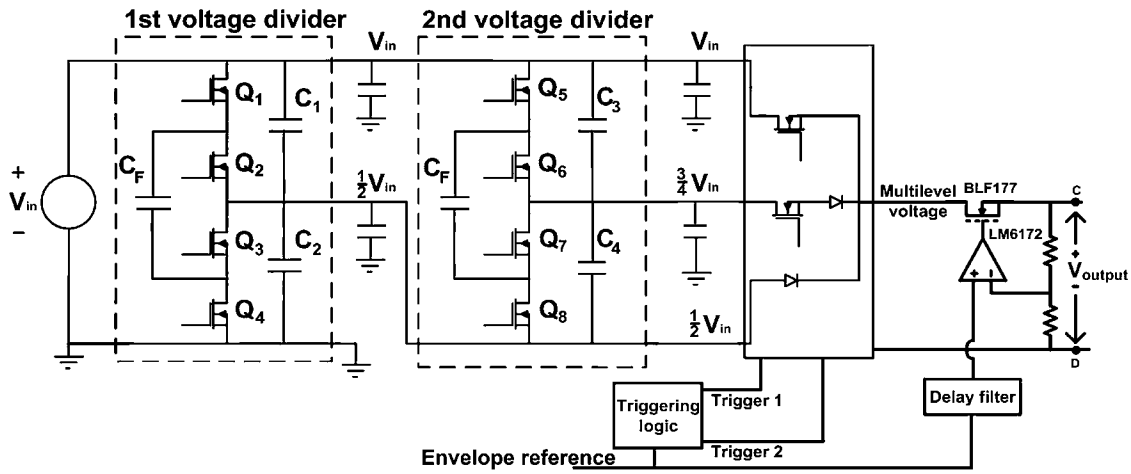

Fig. 7. Simplified schematic of the implemented envelope amplifier.

voltage difference between the flying capacitor and capacitors C_1 and C_2 just before they are connected and, therefore smaller power losses. Small output ripple that is needed to minimize the losses produced by the third mechanism can be obtained if the switching frequency is increased, then the charge and discharge time of capacitors C_1 and C_2 is small. However, as previously mentioned, the power losses produced by the second mechanism increase with the switching frequency.

The first loss mechanism is due to parasitic MOSFET capacitors that have to be charged and discharged. Due to the parasitic capacitor between gate and source of the MOSFET, the energy is lost each time the voltage of the gate is changed. The power losses due to the parasitic gate–source capacitor can be calculated as

$$P_{\text{gate}} = V_{\text{CC}} \Delta Q_{\text{gate}} \tag{3}$$

where V_{CC} is the driver supply voltage and ΔQ_{gate} is the charge that is supplied to the MOSFET in order to turn it on. V_{CC} can be determined from the information about the system, while the ΔQ_{gate} can be estimated from the datasheet.

Additionally, each MOSFET has a parasitic capacitance C_{oss} that is composed of C_{gd} (the parasitic capacitance between the gate and the drain) and C_{ds} (the parasitic capacitance between the drain and the source). Each time the MOSFET is turned on this capacitance is discharged through the MOSFET, and when the MOSFET is turned OFF, the capacitance is charged from the input power supply through the low impedance. Therefore, there are losses whether this capacitance is charged or discharged, and in both cases the losses are the same and equal to the energy that is stored in the parasitic capacitor. The power of these losses can be estimated as

$$P_{\text{oss}} = C_{\text{oss}} V_{\text{oss}}^2 f_{\text{sw}} \tag{4}$$

where C_{oss} is the value of the parasitic capacitance, V_{oss} is the voltage between the MOSFET's drain and source when it is turned OFF and f_{sw} is the switching frequency of the converter.

In order to model the power losses due to the last two mechanisms, the analysis shown in [18] can be applied. It is demonstrated that each converter based on switching capacitors can be presented as a voltage supply with finite output resistance, where the output resistance is

$$R_{\text{out}} = \frac{1}{C_F f_{\text{sw}}} \tag{5}$$

where C_F is the value of the flying capacitor and f_{sw} is the switching frequency of the converter. Therefore, the power losses due to this equivalent output resistance of the voltage divider can be written as

$$P_{\text{cap}} = \frac{1}{T_{\text{envelope}}} \int_0^{T_{\text{envelope}}} R_{\text{out}} i_{\text{divider}}^2 dt \tag{6}$$

where T_{envelope} is the time duration of the envelope and i_{divider} the current that is supplied by the voltage divider. Having in mind that the envelope is a random signal and that depending on the value of the generated envelope the load current comes from different voltage dividers, the previous equation can be rewritten using the information about the envelope distribution (due to the linear regulator it is assumed that the load current is equal to the current that comes from the voltage divider

$$P_{\text{cap}} = \int_{V_1}^{V_2} \frac{R_{\text{out}}}{R_{\text{load}}^2} v_{\text{out}}^2 p(v_{\text{out}}) dv_{\text{out}}. \tag{7}$$

where V_1 and V_2 are the voltage for which one voltage divider supplies the current to the load, R_{load} is the load's resistance and $p(v_{\text{out}})$ is the density of the probability of the transmitted envelope [15]. In the case of the voltage dividers that are used in this paper, the voltages V_1 and V_2 are 0 V and $\frac{1}{2}\ V_{\text{MAX}}$ for the first and $\frac{1}{2}\ V_{\text{MAX}}$ and $\frac{3}{4}\ V_{\text{MAX}}$ for the second divider.

B. Power Losses in the Analog Multiplexer

In the analog multiplexer there are three mechanisms that produce energy losses.

1) The losses due to the MOSFET resistance and voltage drop on the diode;
2) The losses in the gate of MOSFET due to parasitic capacitance between gate and source;
3) The losses due to charges and discharges of MOSFET's and diode's parasitic capacitors.

Fig. 8. Simple RC network that is used to present each branch of the implemented analog multiplexer.

The first loss mechanism in this part of the envelope amplifier can be described with the following equation

$$E_{\text{mux}} = \sum_{i=1}^{N} \int_t (R_{\text{on}} i^2_{\text{branch\_}i} + V_D i_{\text{branch\_}i}) dt \tag{8}$$

where N is the total number of multiplexor's outputs, R_{on} is the MOSFETs resistance when it conducts current, V_D is the voltage drop on the diode and $i_{\text{branch\_}i}$ is the current through each output of the multiplexor. Similar to the conduction power losses in the voltage divider, the conduction losses in the analog multiplexer can be rewritten using the statistical properties of the transmitted signal. Each branch of the analog multiplexer conducts only when the envelope is in a certain range. Therefore, the conduction power losses will be proportional to the probability to find the envelope inside that range (for example, for the second voltage divider this range is between $\frac{1}{2}\ V_{\text{MAX}}$ and $\frac{3}{4}\ V_{\text{MAX}}$). The conduction power losses in the analog multiplexer can be calculated as

$$P_{\text{mux}} = \sum_{i=1}^{N} \int_{V_{i1}}^{V_{i2}} \left(\frac{R_{\text{out}}}{R^2_{\text{load}}} v^2_{\text{out}} + \frac{V_D}{R_{\text{load}}} v_{\text{out}} \right) p(v_{\text{out}}) dv_{\text{out}}. \tag{9}$$

The power losses due to the second mechanism can be described with (3) and it will not be further discussed.

In order to estimate the power losses due to the third mechanism it is necessary to know that each change of the voltage on the output of the multilevel converter will produce losses in all the switches, not just in the one that is turned ON/OFF. The reason for this is that the analog multiplexer can be viewed as an RC network, see Fig. 8. For example, if we have a simple RC network and the voltage of point B is changed from V_2 to V_3, while the voltage of point A is constant, V_1, the power losses due to the resistance are

$$P_{\text{RC\_losses}} = C(V_1 - V_3)(V_2 - V_3) - \frac{1}{2} C[(V_1 - V_3)^2 - (V_1 - V_2)^2]. \tag{10}$$

Therefore, in order to estimate the power losses of the analog multiplexer it is necessary to observe each transition separately and calculate the losses for each one. In the case of the implemented analog multiplexer four transitions should be analyzed (from 12 to 18 V, from 18 to 24 V, from 24 to 18 V, and from 18 to 12 V).

The power losses due to the diode's reverse recovery has not been taken into account, because the quantity of the charge that is needed to take the diode carriers depends on the temperature, applied reverse voltage, and reverse current slope and it is difficult to estimate it correctly. Additionally, theses losses contribute such a small portion to the complete power losses of the envelope amplifier that are mainly due to the linear regulator.

C. Power Losses in the Linear Regulator

Power losses in the linear regulator are due the voltage drop on the transistor that is used as the pass element. Therefore, the instantaneous power losses are modeled easily as

$$p_{\text{lin\_regulator\_losses}} - i_{\text{envelope}}(v_{\text{multilevel}}(v_{\text{envelope}}) - v_{\text{envelope}}) \tag{11}$$

while the total power losses are obtained by integration similarly such as in (6) and (7)

$$P_{\text{lin\_regulator\_losses}} = \int_0^{V_{\max}} (v_{\text{multilevel}}(v_{\text{envelope}}) - v_{\text{envelope}}) \times \frac{1}{R_{\text{load}}} v_{\text{envelope}} p(v_{\text{envelope}}) dv_{\text{envelope}}. \tag{12}$$

Where $v_{\text{multilevel}}(v_{\text{envelope}})$ is the function that describes how the linear regulator is supplied by the multilevel converter and in the case of the system that is presented in this paper it is

$$v_{\text{multilevel}} \begin{cases} \frac{1}{2}V_{\max}, & v_{\text{envelope}} \in \left[0, \frac{1}{2}V_{\max}\right) \\ \frac{3}{4}V_{\max}, & v_{\text{envelope}} \in \left[\frac{1}{2}V_{\max}, \frac{3}{4}V_{\max}\right) \\ V_{\max}, & v_{\text{envelope}} \in \left[\frac{3}{4}V_{\max}, V_{\max}\right). \end{cases} \tag{13}$$

By using the simplified loss models proposed here it is possible to estimate the efficiency of the proposed envelope amplifier for any envelope. It is only necessary to know the envelope's time pattern in order to do so.

The results of the efficiency estimation for different sine waves are presented in Section V where they are compared with the actual measurements.

IV. System Design

In order to prove the concept, a prototype of envelope amplifier has been made. The specifications of the envelope amplifier prototype are as follows:

1) Input voltage: 24 V
2) Output voltage can be changed from 0 to 22 V
3) Maximum output power of the prototype: 50 W
4) Maximum frequency of the reference signal: 2 MHz

As previously mentioned, the voltage dividers will operate in an open loop, and, in order to guarantee stable voltages at their outputs, at each output there are two ceramic capacitors in parallel (each one of 22 μF). It has been previously explained that one part of the power losses in the voltage dividers is inversely proportional to the value of the "flying" capacitor and switching frequency. Therefore, for low power losses, it is necessary to apply low switching frequency and use a flying capacitor as big as possible (in this design there are five 22 μF ceramic capacitors in parallel). The switching frequency for both dividers is 50 kHz.

As explained in [14], the drivers are supplied by half of the voltage divider's input voltage. The input terminals of one driver are connected between the ground and the output terminal of the

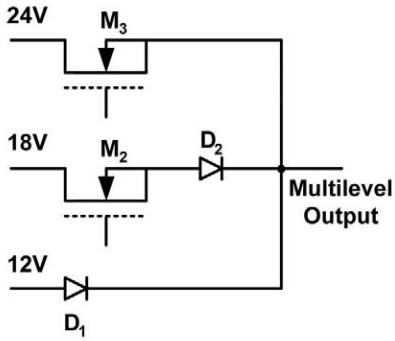

Fig. 9. Implemented analog multiplexer.

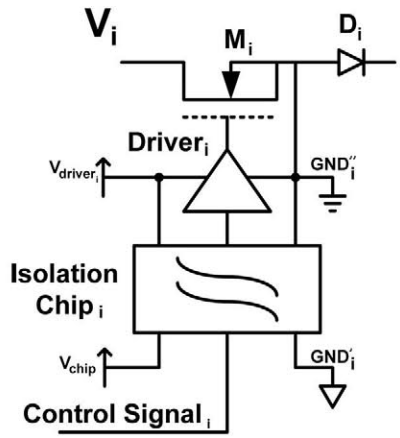

Fig. 10. Simplified schematic of the circuit used to drive the floating MOSFETs in the implemented analog multiplexer.

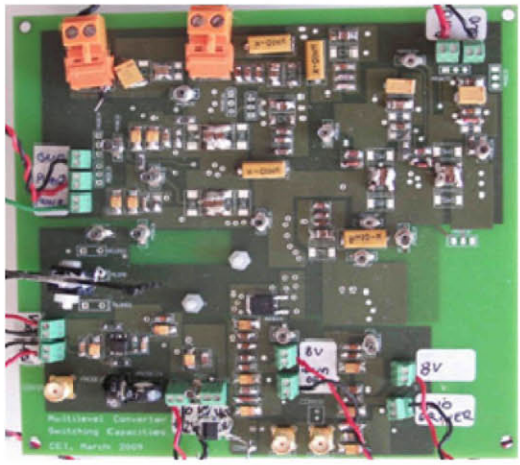

Fig. 11. Photograph of the implemented envelope amplifier.

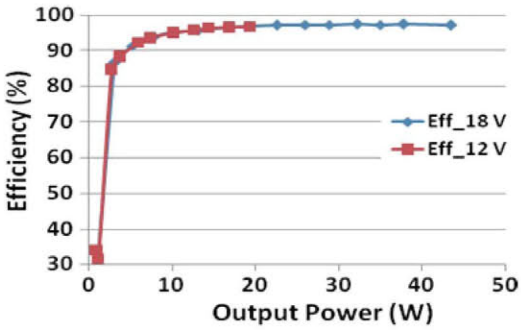

Fig. 12. Measured efficiency of the implemented multilevel converter.

voltage divider, while the input terminals of the second driver are connected between the input and output voltage. Having this in mind, in the first voltage divider the used driver has to be able to withstand $\frac{1}{2}\ V_{\mathrm{MAX}}$ as its supply voltage and in the second divider the maximum voltage supply is $\frac{1}{4}\ V_{\mathrm{MAX}}$. In the first voltage divider the used drivers are IR2181 and in the second, LM27222. The MOSFETs are the same in both voltage dividers, and they are Si4864. The analog multiplexer is implemented using MOSFETs and diodes as shown in Fig. 9.

The diodes are necessary in order to prevent the current flow between the voltage sources due to body diodes of the MOSFETs. As can be seen, the MOSFETs from the analog multiplexer have "floating" sources, and it is necessary to use additional power sources and isolation chips in order to control them because the control signals are referred to the ground of the input voltage, as in Fig. 10. The isolation chips are ISO721 and the drivers are EL7156.

The linear regulator that is used as the last stage of the envelope amplifier should have high bandwidth and the components are selected in order to accomplish this request. The MOSFET that is used as a pass element for the linear regulator (BLF 177) is from the HF/VHF power MOS family of transistors. The operational amplifier is LM6172, and it is selected because of its high bandwidth. It is very important to have a good layout between the output capacitors of the multilevel converter and the input side of the linear amplifier. Reducing any stray inductance and capacitance can reduce over voltage and high-frequency noise due to significant dv/dt and di/dt of the power switches.

The triggering logic is implemented in a FPGA that is used as a source of the digital signal reference. The digitalized signal reference is connected to a D/A converter and from there to the linear regulator. The same reference signal is sent to the triggering logic and to the linear regulator, but it is of the most importance that the reference to the linear regulator be synchronized with the output voltage of the multilevel converter. Only when these two voltages are synchronized, the system's output voltage will always be lower than the output voltage of the multilevel converter. Therefore, a digital delay filter is implemented in the FPGA as well, in order to compensate the delays in the system and synchronize the multilevel output voltage with linear regulator's reference. The load of the system is of a 10 Ω resistance.

Fig. 11 shows a photograph of the implemented envelope amplifier.

V. Experimental Results

Once the voltage dividers have been implemented, the efficiency of 12 and 18 V outputs was measured. The result of the measurement is shown in Fig. 12. It can be seen that the efficiency of both voltage dividers is higher than 95% in a very wide range of output power.

TABLE II
MEASURED EFFICIENCY OF THE IMPLEMENTED ENVELOPE AMPLIFIER FOR DIFFERENT SINE WAVES COMPARED WITH THE THEORETICAL EFFICIENCY OF AN IDEAL LINEAR REGULATOR SUPPLIED BY 23 V

Vsin(V)	Sine wave frequency (MHz)	Output Power (W)	Measured efficiency of the envelope amplifier based on switching capacitors	Estimated efficiency of the envelope amplifier based on switching capacitors	Measured efficiency of the envelope amplifier based on the independent voltage cells	Theoretical efficiency of an ideal linear regulator supplied by 23V
0-9	*0.5*	*2.7*	*47.5%*	*50,5%*	*40.4%*	*29.3%*
5-14	*0.5*	*8.9*	*61.5%*	*63,5%*	*57.6%*	*45.9%*
0-22.5	*0.5*	*17.3*	*75.2%*	*77,7%*	*69.8%*	*73.4%*
0-9	*2*	*2.8*	*48.2%*	*50,5%*	*40.8%*	*29.3%*
5-14	*2*	*8.9*	*59.0%*	*63,2%*	*55.1%*	*45.9%*
0-22.5	*2*	*17.1*	*70.9%*	*77.3%*	*68.8%*	*73.4%*

In order to characterize the envelope amplifier, it has been tested with different sine waves. In Table II, the efficiency of the implemented envelope amplifier is shown as a function of the frequency of the reproduced sine wave and its dc offset and amplitude. In the same table, the measured efficiency is compared with the efficiency of an ideal linear regulator and with the efficiency of the envelope amplifier that is implemented with independent voltage cells [13].

The implemented multilevel solution has better efficiency than the solution with only linear regulators, when signals with small average value are transmitted, and that is mostly the case when the EER technique is applied. For the tested sine waves, the efficiency of the envelope amplifier does not depend on when sine waves with small amplitudes and small average values are reproduced. The measured efficiency in this case is constant and around 48%, approximately 40% better efficiency than in the case of the ideal linear regulator. The reason for such a high efficiency is that only the 12 V level is active, and there are no switching losses, only conduction losses, regardless of the frequency of the sine wave. The implemented envelope amplifier has better efficiency than linear regulator even when the sine waves with medium average (sine wave with $V_{p\text{-}p}$ from 5 to 14 V) values are reproduced. The measured efficiency of the implemented envelope amplifier is around 59% and the prototype has 60% less power losses than the ideal linear regulator.

The difference between the estimated and measured efficiencies is not huge. The main reason for the difference lies in the fact that the model is very much simplified and does not account for any parasitic inductance on the PCB that has a strong influence on the switching losses, especially at high frequencies [19]. Nevertheless, it is shown that it is correct enough to make rough judgment on the overall efficiency.

Comparing the proposed solution with the envelope amplifier that is based on independent voltage cells [13], it can be easily seen that it has higher efficiency (few percents) regardless of the frequency and the type of the sine wave. The main reason for this is a very high efficiency of the first stage that supplies the multilevel converter. In the case when the envelope is a sine wave with the maximal amplitude (output power of 17 W), this means power savings between 1 and 1.6 W

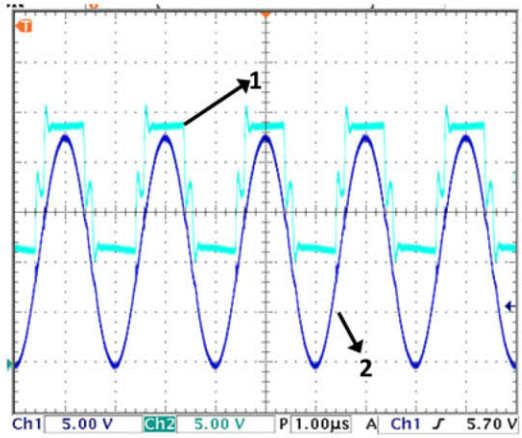

Fig. 13. Multilevel output voltage (label 1) and envelope amplifier's output voltage (label 2) in the case of a 500 kHz sine wave.

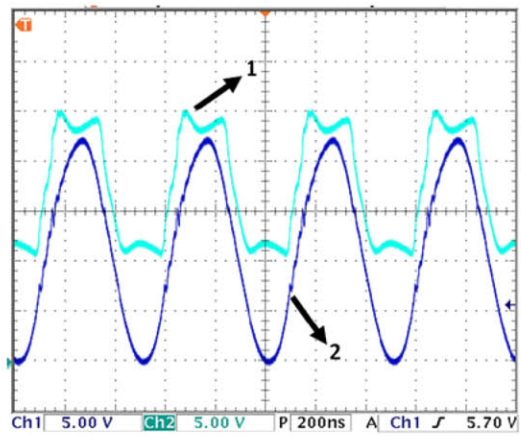

Fig. 14. Multilevel output voltage (label 1) and envelope amplifier's output voltage (label 2) in the case of a 2 MHz sine wave.

Figs. 13 and 14 show the multilevel and system's output voltage for a sine wave reference of 500 and 2 MHz, respectively.

The linearity and the bandwidth of the envelope amplifier are crucial in order to obtain high linearity of the power amplifier based on the EER technique; therefore, these measurements have been performed as well. The linearity measurements are

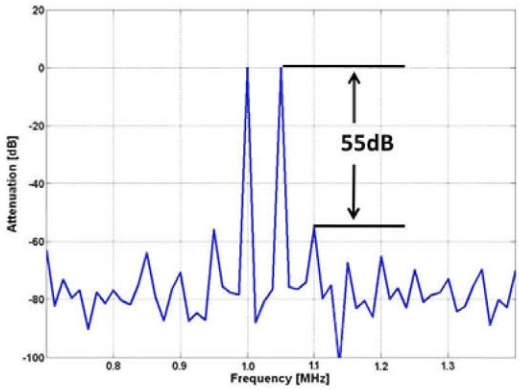

Fig. 15. Attenuation of the intermodulation harmonics for a reference signal composed of two tones, 1 and 1.05 MHz sine waves. The measurement is processed in MATLAB.

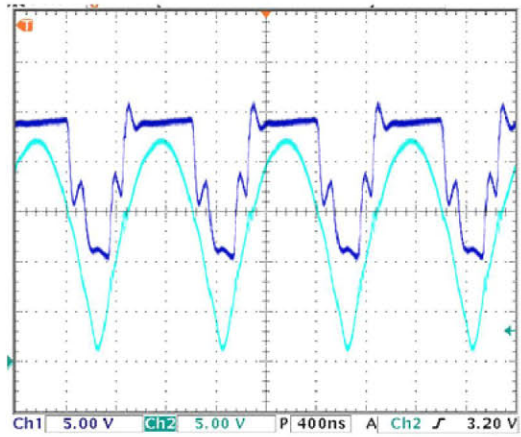

Fig. 16. Waveform of multilevel's output voltage and linear regulator's output voltage when a rectified 500 kHz sine wave is used as the reference.

conducted by two tone tests, where two sine waves of the same amplitude are used as a reference signal and at the output of the envelope amplifier the ratio between the reproduced amplitudes and the intermodulation harmonics that are produced by the envelope amplifier is observed. Fig. 15 shows the spectral content at the output of the implemented envelope amplifier in the case when a two-tone signal composed of 1 and 1.05 MHz is used. It can be observed that the attenuation of the intremodulation components is higher than 50 dB, which means high linearity of the envelope amplifier.

In [1], it has been explained that the bandwidth of the envelope amplifier has to be, at least, twice the bandwidth of the RF signal. The reproduced envelope should not have any attenuation up to 2 MHz and it has been shown that the proposed envelope amplifier can reproduce 2 MHz sine wave of the maximum amplitude. However, this does not mean that the implemented envelope amplifier cannot reproduce higher harmonics. The higher harmonics that are very important for high linearity of Kahn's transmitter usually are of much smaller amplitudes than the maximum amplitude that can be reproduced by the envelope amplifier. Based on the analysis presented in [1], a test with rectified sine wave has been conducted. If the reference signal is a rectified sine wave of frequency f, its spectrum is infinite and consists of tones that are placed at frequencies $2f$, $4f$, $6f$... A rectified 500 kHz sine wave of maximum amplitude has been used as the reference and the response of the envelope amplifier has been measured, see Fig. 16. The spectrum of the output signal is compared with the spectrum of the reference signal, see Fig. 17. It can be seen that the proposed envelope amplifier admits even harmonics higher than 2 MHz (practically all the harmonics are up to 6 MHz).

Once the high linearity and wide bandwidth of the envelope amplifier was confirmed, the tests with RF envelopes were conducted. The envelope reference was the envelope of a 64QAM RF signal. The RF signal was generated in the such a way that its $I(t)$ and $Q(t)$ component (1) had Gaussian distribution and, in that way, the envelope had high PAPR Rayleigh's distribution. The ratio between the envelope's maximum and average value was 8.6 dB and its probability distribution is shown in Fig. 18.

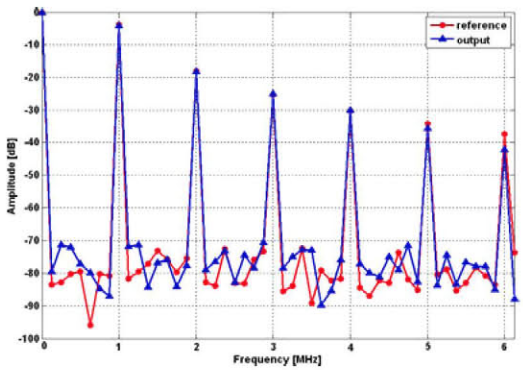

Fig. 17. Spectrum of the reference and output signal when a rectified 500 kHz sine wave is used as the reference. All the values are scaled to the dc value of the signal.

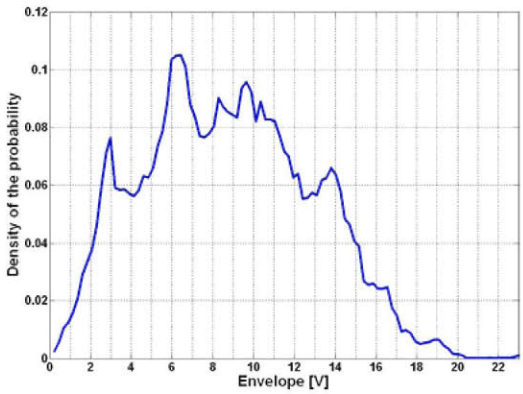

Fig. 18. Density of the probability of the envelope signal for the tested 64QAM pattern.

The measured efficiency of the envelope amplifier based on the switching capacitors was 65%. For the same envelope reference, the prototype based on independent voltage cells had an efficiency of 59%. In the terms of the power losses this means, approximately, 20% less power losses comparing these two solutions. The same linear regulator with constant voltage supply had an efficiency of just 45%. Therefore, the measurements clearly show that in the case of a high PAPR RF signal the

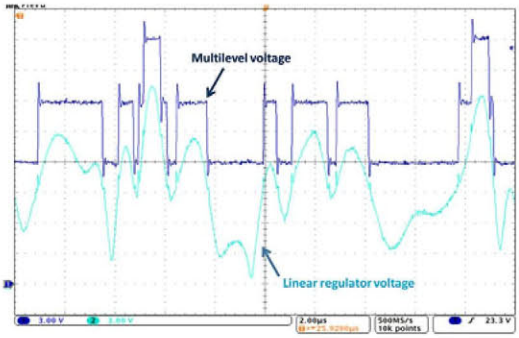

Fig. 19. Waveforms of the multilevel converter and linear regulator during the tests with the 64QAM signal.

proposed multilevel converter boosts the efficiency of the linear regulator by 20% (in terms of power losses the improvement is around 55%). Fig. 19 shows the waveforms of the multilevel converter and the linear regulator during the tests with 64QAM signal.

VI. Conclusion

In this paper, a solution for envelope amplifier for EER technique is presented. The solution consists of a multilevel converter in series with a linear regulator. The proposed multilevel converter is implemented by voltage dividers based on switching capacitors. The designed envelope amplifier can provide up to 50 W of instantaneous power and reproduce a sine wave up to 2 MHz. The switching frequency of voltage dividers is low (50 kHz) compared with the bandwidth of the envelope amplifier. Therefore, the proposed solution uses lower switching frequency than a conventional dc–dc converter for the same given bandwidth.

The multilevel voltage levels are selected in order to maximize the efficiency of the linear regulator for the signals with high PAPR. The efficiency of the envelope amplifier has been measured for different sine waves and its efficiency is up to 40% higher than in the case of an ideal linear regulator when sine waves have low average value (which is usually the case in the RF systems).

A simplified model of power losses has been proposed and explained in detail. The model has been validated by comparing estimated and actual measurements.

The proposed envelope amplifier is compared with the envelope amplifier based on the independent voltage cells. The proposed envelope amplifier has higher efficiency (few percents) mostly due to the higher efficiency of the first stage that supplies the multilevel converter. This slight advantage can be seen as power savings between 1 and 1.6 W when the envelope is a sine wave of maximal amplitude (output power around 17 W).

The linearity of the prototype is measured as well and the attenuation of the intermodulation products is higher than 50 dB. The implemented prototype has no magnetic component and, therefore, it is suitable for integration.

The implemented envelope amplifier was tested with the envelope of a high PAPR 64QAM signal and the measured efficiency was 65%. The same envelope reference was used with the envelope amplifier based on independent voltage cells and the power losses were 21% higher than in the case of the switching capacitor based prototype. The proposed multilevel converter for the same 64QAM signal boosted the efficiency of the linear regulator by 20% (around 55% in terms of power losses).

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