Wireless Optical Communications for Intra-Spacecraft Networks Based on OCDMA with Random Optical Codes

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INTRODUCTION

In recent years, spacial agencies have shown a growing interest in optical wireless as an alternative to wired and radio-frequency communications [1, 2]. The use of these techniques for intra-spacecraft communications reduces the effect of take-off acceleration and vibrations on the systems by avoiding the need for rugged connectors and provides a significant mass reduction. Diffuse transmission also eases the design process as terminals can be placed almost anywhere without a tight planification to ensure the proper system behaviour. Previous studies [3, 4] have compared the performance of radio-frequency and infrared optical communications. In an intra-satellite environment optical techniques help reduce EMI related problems, and their main disadvantages - multipath dispersion and the need for line-of-sight - can be neglected due to the reduced cavity size. Channel studies [5] demonstrate that the effect of the channel can be neglected in small environments if data bandwidth is lower than some hundreds of MHz.

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At the same time, Spread-Spectrum techniques are good candidates for data transmission in closed environments [6], allowing independent and simultaneous channel access for each network node. When applied to optical communications, they can help power savings by using low-duty cycle modulations, low-power electronics as emitters can be designed with a switching driver, and high-gain saturating amplifiers for the receviers, along with low-power programmable logic devices for most of the signal processing. As part of the Direct-Sequence Spread-Spectrum (DS-SS) techniques, wireless OCDMA communications offer low bit error rates for low-speed traffic in medium-sized systems. Optical code families based on prime numbers [7] have been widely used for OCDMA systems. They provide good auto- and cross-correlation properties but require long codewords when the number of nodes in the network is large. reducing the maximum data rate achievable. Recently, a new family of optical codes, named Random Optical Codes, was proposed [8]. These codes do not impose tight restrictions on the codeword design and selection while providing a BER for large numbers of users similar to those of the prime-based families with shorter codes.

Herein, a telecommand/telemetry network consisting of 25 autonomous terminals is described in which each terminal implements 256 16-bit registers to allow operation of different sensors and actuators. All terminals are capable of communicating with a central node – simulating the On-Board Computer (OBC) – through a full-duplex asynchronous optical wireless channel. Random Optical Codes have been used for OCDMA access, providing

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experimental results to validate previous simulations of the code families' behaviour.

This is organized as follows: The *Code Description* section presents the main aspects of ROC and its generation process, taking the network dimensions as an example. The *System Implementation* section describes the physical implementation of the system used for the tests. A detailed characterization of the terminals implemented is included, as well as power consumption and an estimated lifetime for the batteries. In the *Experimental Results* section, the tests performed and their results are discussed.

CODE DESCRIPTION

As presented in [8], Random Optical Codes are defined by two main parameters: Length L and weight w. The construction consists of selecting w random chip positions within the code length L, which will be the marked positions of the code. When a bit "1" is to be transmitted the spreading code is sent instead, while no impulses are sent for a bit "0." This method of generation does not rely on particular properties of the auto- and cross-correlation functions, making the cardinality of the family; i.e., number of different available codewords- larger than for traditional codes while maintaining a low error probability due to Multiple-Access Interference (MAI).





The generation process of ROC is extremely fast and simple, and although it may appear codes constructed in this way won't have good behaviour, previous simulations run [9] have shown they offer good performance. Also, its large cardinality allow some codes to be discarded if the system's performance falls below a desired level.

The probability of error due to MAI is calculated in [10], where an analytical formula is derived. Graphical representation of contour levels of this formula can be used for finding the optimum values of w and L for a desired error probability and number of simultaneous users, N + 1.

In our target application, 25 terminals will be communicating with the central node, so a total of 50 codewords are needed to ensure both upward and downward links can be active simultaneously. For a target error probability of $P_e = 10^{-7}$ and N + 1 = 50 simultaneous users, the contour levels for the optimum P_e (see Figure 1) show a minimum length of L = 900 is required [11].

Then we can find the optimum weight w for the code by looking on the contour levels shown in Figure 2. For the aforementioned design parameters (N + 1 = 50, L = 900) the weight of the codes should be w = 20 to optimize the performance, resulting in a signal to be transmitted with a duty cycle as low as 2%.

Reducing the code's weight w or increasing its length L more channels could be accommodated in the system, keeping the desired error probability. As a comparison, a prime code of L = 2809 and w = 53 would be needed to support the same 50 users with the given error probability, forcing the system to operate at higher frequencies. Thus, ROC allows faster transmission rates along with a simpler design process and improved flexibility.



Fig. 2. Optimum Weight w Calculation

SYSTEM IMPLEMENTATION

A test system has been implemented to perform the tests and measure the behaviour of ROC in a real environment.

System's Design

The terminals have been designed according to the following considerations:

- The network is intended for telecommand / telemetry and will offer a communication channel between the central node (OBC) and 25 remote terminals simulating sensors and actuators.
- The data rate is 1 kb/s well-suited for this network.
- Terminals should be self-powered, and therefore the transmission method must be energy-conservative.

• The main node starts all transactions by sending request commands to specific terminals. Then the terminals send the response asynchronously. Several answers can be emitted at the same time, so the central node should be able to identify each one.

The code selection, as presented in the Code Description section, shows that an error probability of 10^{-7} can be achieved using ROC with length L = 900 chips and weight w = 20 for N + 1 = 50 simultaneous users. Therefore to maintain the desired data rate the system's chip period must be 1.1 µs. The channel response has been calculated for a 5 m³ cavity obtaining no multipath contribution for delays larger than 25 ns. Thus, the channel effect over the communications can be neglected for the conditions given.

Terminals have been implemented using a modular structure. A logic module consisting of a nonvolatile FPGA controls both the communication process and the terminal's operation. This module is easily replaceable to allow upgrades if new functionalities are required and a different logic device (like a microcontroller) is to be used to control the terminals. A separate communication module consists of both a receiver and four transmitter chains, three using wide-angle (60°) diffusive LEDs and the other with a narrow-angle (15°) LEDs.

Table 1. Data Package



As the data acquisition module was beyond the objective of this system it has been replaced by a user interface for demonstration purposes. Each terminal implements 256 16-bit registers to simulate interfacing different sensors/actuators attached. These registers are individually addressable and can be accessed from the central node via simple READ/WRITE commands.

Data Package

The basic data package is comprised of 40 bits and organized as shown in Table 1. An initial sync header consisting of four "1" bits (i.e., the channel's codeword) is sent to ensure the receiver is properly synchronized during the transmission. Then a command is sent indicating actions to be taken on the terminal's side. For accessing data registers, the address is sent along with 16-bit data to be written into memory when applicable. Finally, an 8-bit Cyclic Redundancy Code (CRC) is calculated as an XOR of the previous packet contents. Transmission errors can be detected, although no forward error correction has been implemented.

Four commands have been defined for the network demonstrator, defined as follows. WRITE and READ commands allow remote update and inspection of terminal's internal registers. ACK packets are a general purpose response, which include the value stored in the last selected register. SYNC packets are sent by the main node to check the network status, as they are acknowledged from the terminal's side.

Main Node

The main node, which performs communication tasks for the OBC, has been implemented by a National Instruments'™ CompactRIO. This equipment integrates a microprocessor running a real-time OS (Unix VME) with an FPGA backplane, offering a fast interface with external signals. The main part of the software has been developed for the FPGA, including three main blocks:

• Clock Management:

Generates clocks at chip and bit frequencies and provides internal signals to identify the bit starting position (delay).

• Transmitter:

Communicates with the microprocessor's software which generates the data packets, through a memory-mapped FIFO to send the chip-period pulses to the optical emitter.

• Receiver:

Based on chip detection, uses a code length (900) shift register with the sampled incoming signal and checks for data bits from any of the 25 codes used for uplink. It also keeps one 40-bit shift register for data packets from each terminal, validates the incoming data, and sends those valid packets to the real-time computer using a memory-mapped FIFO.

The microprocessor's software generates the data packets for transmission and prepares the CDMA stream using the downlink codes. The transmitter performs an OR operation between all 25 streams before sending them, allowing multiple terminals to be addressed at the same time. On the other hand, the reception process retrieves the incoming data packets and hands them to the user application for inspection and debugging.

Table 2. Power Consumption

| Current [µA] |
|--------------|
| 8 |
| 30 |
| 14 |
| 7,500 |
| 5,000 |
| |



Fig. 3. Terminal Circuit

Terminals

Terminals have been implemented as a custom circuit board using commercial-off-the-shelf (COTS). The logical module is based on a nonvolatile FPGA operating at chip frequency. The OCDMA decoder is based on a shift register which stores the detected signal's samples and check for pulses at the appropriate positions. Both transmitter and receiver modules are programmed as two finite-state machines that control the data packets sent and received, perform CRC calculation and packet validation, as well as take proper actions and prepare response messages.

The data adquisition was beyond this demonstrator objective as it was intended for the communication system. Therefore, each terminal is prepared to simulate both sensor and actuator features by implementing a register memory. For demonstration purposes, the terminal board includes a rotary switch, a 4-digit display and 16 on-off switches. The rotary switch selects one register, whose value is shown in the display and can be altered by means of the 16-bit switches.

Terminals are powered using standard coin cell lithium batteries, at a nominal supply tension of 3V (although tested down to 2.6V). Power consumption details are shown in Table 2, although some optimization techniques could expand the batteries' lifetime. Each terminal has 4 unpluggable LED chains for optical transmission, working at 100 μ A each when on. Assuming one packet is sent every 10 seconds being half its bits "1," the average current for the emitter is 14.08 μ A with all LEDs connected. As for the rest of the circuit, power savings techniques could be implemented to reduce power consumption. As most of the power needs belong to the receiver circuit, a wake-up mechanism that allows turning part of the receiver off would drastically improve the batteries' load. Additionally, unused parts of the FPGA could be disabled to minimize the power consumption.

EXPERIMENTAL RESULTS

Terminals have been characterized prior to system validation tests performed. First, as the transmitter uses both low-angle and wide-angle LEDs, the emission pattern has been measured (see Figure 4). Maximum link distance has been measured to guarantee signal levels comply with 3.3V LVCMOS standard, as well as a maximum pulse widening of 10% due to the amplification process. A 2 meter distance was obtained in perfect alignment between transmitter and receiver.



Fig. 4. Emission Pattern

The receiver's sensitivity can be calculated from these results. Two photodiodes with an active area of 7 mm² each are used for detecting the optical signal, and as all emitter chains contribute in the radiation axis the total optical power is 423 mW/sr, according to manufacturer's data. Therefore the received power results in 1.5 μ W (-28 dBm). With this value, signal-to-noise ratio in normal operation conditions is above 40 dB. Thus, errors will not be caused by noise but due to multiple access interference and limited to the theoretically calculated value of 10^{-7} .

On-the-table tests have been performed to assess the behaviour of the system on a simulated environment. A custom test application was developed to control the OBC and operate over the terminal's registers, allowing quick validation of the transmission and interpretation process. Storing each terminal's sent and received bits was not feasible, so error rate calculations are based on erroneous data frames detected on the OBC side. One frame error is computed when an answer is missing from a terminal node (assuming the sent packet had errors on reception and was discarded) and when the received packet contains wrong data.



Fig. 5. Electrical Test Set-up

Electrical Tests

Electrical tests have been performed by connecting all 25 terminals to the main node through an OR gate to merge the data signals. To ensure the maximum workload, all terminals were addressed simultaneously from the main node (except for each particular chip's delay) with WRITE commands and generated an ACK response.

A visual inspection has been done of system behaviour, as the terminal's display was updated with the new data coming from the main node (downlink test), which also received the data selected on the 16-bit switch (uplink test).



Fig. 6. System Test Set-up

System's Optical Tests

Optical tests have been performed on an open environment, randomly deploying all 25 nodes on a 1.5 \times 1 μ



Fig. 7. Data Decoding

table with main node's interfaces placed 0.75 m above on one side. Under these conditions individual reception and data processing has been tested, as well as the overall system's behaviour and erroneous frames received.

As the system is designed for diffuse communication, operation in an open environment means part of the emitted optical power is lost and line-of-sight between both ends is required. In a closed environment, light is reflected at the walls, raising the optical power at the receiver and improving the system's signal-to-noise ratio.

Similar tests to those previously conducted were performed, ensuring the correct behaviour of each individual node – especially regarding clock regeneration. The system was tested by visual inspection and monitoring intermediate signals from the terminals, validating its performance under given conditions.

In Figure 7, data reception and decoding is presented. Upper signal shows the input pulses from the optical receiver. The lower signal shows the output of the decoder stage, which recovers bit values and builds the data packet to be processed by the terminal's logical module.

CONCLUSIONS AND APPLICATIONS

An optical wireless sensor network has been implemented, offering communication capabilities without affecting existing systems. The same techniques could be used for higher rate applications, providing independent channels for every user while avoiding EM interference. Applications such as in-cabin passenger connectivity or sensor monitoring could take advantage of this technology to increase flexibility and reduce harness.

A test system has been designed and implemented to validate the behaviour of different code families in an OCDMA environment for space applications. Specifically the ROC family has been tested, validating the results from the previous simulations and assessing its good properties for these kinds of applications: large cardinality, low error probability, low power modulation, and simple generation.

The experimental results show ROC is an appropriate family for systems with a large number of users. Due to the extraordinary simplicity of the generation process, an Adaptative Code-Hopping CDMA could be implemented, allowing users to be included in the system at any time while maximizing the throughput. The possibility of dynamically assigning codewords depending on the workload shall be studied to maximize the throughput and optimize the bandwith utilization.

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