Ultra Low Power FPGA-Based Architecture for Wake-up Radio in Wireless Sensor Networks

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Abstract—**In this paper the capabilities of ultra low power FPGAs to implement Wake-up Radios (WuR) for ultra low energy Wireless Sensor Networks (WSNs) are analyzed. The main goal is to evaluate the utilization of very low power configurable devices to take advantage of their speed, flexibility and low power consumption instead of the more common approaches based on ASICs or microcontrollers. In this context, energy efficiency is a key aspect, considering that usually the instant power consumption is considered a figure of merit, more than the total energy consumed by the application.**

Keywords-Wireless Sensor Networs, Wake-up radio; low power FPGA, energy efficiency, addressing capabilities, On-demand communicaitons.

I. INTRODUCTION

The number of applications for wireless sensor networks is growing continuously. In many of these applications the power consumption is critical and ultra low energy WSNs [1] are necessary. The main target of these WSNs is to get the longest lifetime possible. The applications based on this kind of WSNs use very low duty cycle (~1%) and low data rates (< 1 bit per second average); these two requirements are needed because the most power hungry element of a node is the communication stage. Therefore, as much as the number and length of messages in the networks is reduced, higher lifetime and energy saving are achieved. Furthermore, most of the power can be wasted listening unnecessarily to the communication channel, waiting for remote data. For this reason a lot of work has been done in order to improve the efficiency of communications, data dissemination and synchronization, among others [2].

In order to get more energy efficient communication protocols many communications schemes have been developed. For WSNs applications the most important improvements concerning energy efficiency have been achieved improving the usage of the communication channel.

The control of the communication channel availability is done by means of the medium access control (MAC) protocol. The most important MAC protocols for WSN can be divided into two main groups, Time Domain Medium Access (TDMA) and Contention-based Medium Access protocols (CMA).

The TDMA protocols, LMAC [3], TRAMA [4], PEDAMACS [5], etc., divide the channel time available into slots and nodes are only allowed to send messages in their own slot. Although it is known that the TDMA protocols are theoretically the most energy efficient they present important drawbacks that make TDMA protocols hard to use in real WSNs deployments. The most important of these drawbacks is related to the scalability, because the topology of the network is generally dynamic in WSNs (new nodes are introduced, nodes can change their position, nodes become unavailable) it is necessary to change the slots assignment. Making a trustable slot assignment policy needs a very accurate synchronization among the nodes.

Contention-based MAC protocols (B-MAC [6], S-MAC [7] and T-MAC [8] among others) carry out the medium access control by performing carrier sense in the senders combined with periodical listen/sleep scheme in the receivers. This group of protocols is the most spread in WSNs. They are quite robust and permit dynamic topology of the network. With properly duty-cycle policies it is possible to achieve good results for energy savings, but in ultra low duty-cycle applications a tradeoff between latency and energy spending should be accomplished. In these cases, the two main drawbacks are the need for long preambles and the high latency in multi hop data communication.

To avoid the synchronization problems of the TDMA protocols and the periodic listening of the Contention-based MAC protocols, on-Demand schemes can be used. The basic idea of these schemes in WSNs applications is to be able to switch off (or stand by) main components of the node: processing units, sensors and data communications hardware; the hardware is only activated (or wake-up) to accomplish a determined task if it has been demanded externally.

Focusing on the communication control, the communication stage is switched on only if an event that requires communications occurs, i.e., a neighbor node wants to communicate with a remote gateway node; otherwise the radio remains switched off. Usually, an ultra low power radio that remains always active while the rest of the hardware remains in low power mode is used to wake-up the node. This auxiliary radio, known as Wake-up Radio (WuR), is used for non-intense data communications; only simple data, like the address or simple commands, are enclosed. This kind of communication is completely asynchronous and un-slotted, avoiding the synchronization problem of the TDMA based protocol and the periodic listening of contention based schemes.

In this paper, the capabilities of ultra low power FPGA to implement Wake-up Radios for WSN are presented as follows; in section II the applications of on demand communications on Wireless Sensor Networks are presented. The possibilities for designing a Wake-up radio for a wireless sensor node are

presented in section III. In section IV, a new architecture for WSN nodes with WuR based on ultra low power FPGAs is presented. In Section V it is presented the first design for the proposed architecture, finally the conclusions and a comparison of the power estimation with different architectures in the literature are given in Section VI.

II. WAKE UP RADIOS

Wake-up Radios are the basic circuits for the on-demand communications scheme. The WuR handle the sending and receiving of wake-up messages that switch on the main processing unit or the main radio of the required node.

The basic requirements for wake-up radio based wireless sensor networks are proposed in [9]:

- Low power: Power consumption should be a low percentage of the power consumption of the node in standby without WuR.
- High sensitivity: A node should not loose wake-up calls.
- Resistance to interference: False wake-ups should be avoided.
- Fast wake-up: The latency of the network should be at least the same as the periodic listening schemes based networks.

Low power consumption is mandatory for the WuR receiver. Indeed, there are wake-up schemes that use a single receiver and share the main radio front end for high data traffic operation and for the wake-up functionality. The power consumption of the WuR receivers is ideally zero Watts, all the necessary energy is harvested from the wake-up message. But this is quite complex in real applications for WSNs: in order to get a fast response, a lot of power might be emitted by the node, otherwise whether the WuR response is too slow, or the nodes have to be close to each other (a few centimeters). This makes WuR harvester hard to use in real application nowadays.

Since zero Watts power receiver is not suitable for real WSNs applications, ultra low power receivers should be used. The power consumption has to be an order of magnitude below the power consumption of the node without the WuR.

Achieving an ultra low power receiver implies the use of a simple modulation scheme that simplifies the demodulation on the receiver side. This usually impacts on the throughput of the WuR channels. However, the size of the wake-up message should not be greater than a few bytes and a high throughput is not necessary.

Regarding sensitivity and resistance to interference, a tradeoff between hardware complexity and quality of the communications must be set. For better performance, bigger antennas, more complex modulation and demodulation schemes, and higher power consumption should be considered. The modulation has to be simple in order to get an easy demodulation. The most typical modulation techniques used by WuR based systems are: OOK (On-Off Keying) or 2ASK (2 levels Amplitude Shift Keying) [10]. Assuming that the antenna is on the size of the node, the minimum accepted sensitivity will be set by the maximum distance reachable without losing wake-up calls. Usually 5 meters is the minimum accepted distance. In order to avoid false wake-ups, addressing techniques can be used on the wake-up message.

Obtaining the fastest wake-up depends not only on the emitter but also on the processing speed of the message. This depends on the complexity of the message, the hardware availability and the performance of the algorithm that decodes the wake-up messages. Message decoding is faster if dedicated hardware is available than if the message is decoded in the processor, which should be awaken before decoding the data. The use of microcontrollers introduces a non-negligible latency in the process because of wake-up time and increases the power consumption, because the time employed by the microcontrollers in the decoding task must be taken into account.

A. Related Work

During the last years, different works in the literature have focused on the implementation of wake-up techniques for wireless sensor networks The design of ultra low power receivers based on integrated circuits, passive receivers, efficient communication protocols and even wake-up circuits based on acoustic or infrared signals are some examples of the active topics on this field. In [11] some examples of different solutions and works can be found.

The work presented in this paper is focused on a complete radio system for the wake-up channel, with the aim of avoiding false wake-ups caused by sharing the channel with the data communications radio which is one of the main problems of the systems with only one receiver. Since the goal is to implement a real WuR system, the works based on designing ASICs are out of the scope of the present work, while the works based on components of the shelf (CotS) are deeply analyzed. The related work is presented below.

In [12], Langedoen et al. propose a wake-up radio for the BT-Node platform, working at 868 MHz. Its main characteristics are: shared channel between WuR and main radio; addressing capabilities based on dedicated hardware and a low power microcontroller (PIC12F683). A BT-Node [13] is used including a CotS based receiver. In this implementation, the PIC is used to perform A/D conversion in order to discriminate between '0' and '1' and message decoding. A WuR prototype working at a distance of 2 m with high resistance to interferences, but with very high power consumption, mainly due to the PIC used to decode the wake-up messages signal is achieved.

In [14], Ansari et al. present a circuit board that can be used as an external peripheral for the Telos-B [15] platform. The implemented solution uses a separate channel for the WuR with addressing capabilities using the main processing unit of the node. The WuR is based on a Texas Instruments low power radio and an RF amplifier in the emitter side. For the implementation of the receiver, a three-stage low power consumption based on a CotS receiver is designed. The first stage is an ad-hoc antenna and a matching network. The second stage is a voltage multiplier to amplify the signal that also acts as envelope detector. Finally, a digital comparator to get the digital values of the RF signal and as over-voltage protection is used. The main drawback of this proposal is the use of the microcontroller unit in the address decoding process. This introduces extra latency and extra power consumption, due to the time needed to wake-up the microcontroller and the execution of the task. Since no other identification mechanism is included in their solution, the microcontroller needs to wake-

up every time a wake-up call arrives to the node, even if the node is not the desired destination.

After analyzing the work in the literature, a new architecture for WuR is proposed in this paper. In this WuR, dedicated hardware with an ultra low power FPGA is proposed in order to overcome the problems presented in the aforementioned works. The FPGA will contain the hardware involved in message decoding, and resources control capabilities. This allows accomplishing the task in a faster time and in a more energy efficient way than in the traditional microcontrollers used in WSN.

III. Implementing Wake-up Radio transceivers

As it has been presented before, the hardware of the WuR device should be designed and chosen carefully, in order to achieve the requirements about power consumption, range and sensitivity. Three different ways to get a functional WuR transceiver can be followed:

1) Using a full external transceiver in order to carry out the modulation/demodulation process and filtering. This can be done in two ways

   a) With a specific design based on discrete components, optimizing the design in power consumption. There are some examples in the state of the art, but the results are mainly based on simulations.

   b) Using a commercial transceiver. Nowadays, most of the low power transceivers are designed to work connected directly to a microcontroller, based on standard buses, mainly SPI. This is an inconvenience when working with an FPGA because extra hardware is required which means more power consumption and more dedicated input/outputs; in order to get better processing speed a direct connection can be better. Some products are available in the market with direct interconnection interface but with a power consumption of ~ 2 mA in reception, one order of magnitude over the target.

2) Using a commercial emitter and a full custom receiver. For complete wake-up radios this is the most used solution in the literature. This approach gets the lowest power consumption, because the transceivers and receivers available on the market have power consumption of mW, too much for a wake-up radio system.
   There are two kinds of receivers: ASIC-based designs which results are mainly based on simulations, and discrete components based, usually with real implementations but with lower performance.

3) Implement the modulator inside the FPGA. In this solution, the main problems are the restrictions of using an ultra low power FPGA and the power consumption required. To implement a modulator inside the FPGA high frequency generators are necessary and this will increase dramatically the power consumption of the hardware.

The design of an ASIC is the most power efficient solution but it has two very important drawbacks, the production price is nowadays prohibitive taking into account the market of WSNs, other very important drawback is the lack of flexibility of this solution, that is very important for WSN applications, something that works in one application is not valid for other, i.e. communication frequency, node densities, etc. On the other side once a design has been proved to be a good solution, it can be placed in one time programmable FPGAs which reduces its power consumption around a 50% compared with the same design in a regular FPGA.

Comparing microcontrollers and FPGA depends on many factors, application, configuration of the FPGA, etc. But in [16], it was demonstrated that for high performance computing the use of hardware implementations are much more efficient than the software implementations running in microprocessors used in WSN.

The use of the FPGA in WuR is not intended for high performance computing but anyway the characteristics of this devices can improve the energy efficiency of the task of encode and decode the messages over a traditional micro architecture, combined with the faster wake-up of the FPGA (1 µs versus 6 µs of a Texas Instruments MSP430) it can be thought that the ultra low power FPGA can accomplish good performance in this kind of applications.

IV. Proposed Architecture

In Figure 1 the proposed architecture is shown. The main elements are:

- Main radio. It is used for data communications. The most typical protocols for WSN applications are Zigbee or IEEE 802.15.4.
- Microcontroller. It is used for data acquisition, processing tasks and send and receive data messages through the main radio. Microcontrollers used in WSN are resource constrained and have usually several low power modes.
- Low power FPGA. The FPGA is used to process the wake-up radio messages and to control the hardware of the node depending on the content; it also drives the data sent through the wake-up emitter.
- Wake-up radio used for the wake-up messages, composed by an ultra low power receiver and an independent emitter that remains inactive when the node sleeps. The control of the sent/received data is done directly by the FPGA that generates/processes the wake-up messages.

Both the wake-up radio and the low power FPGA blocks are described deeply in the following subsections.

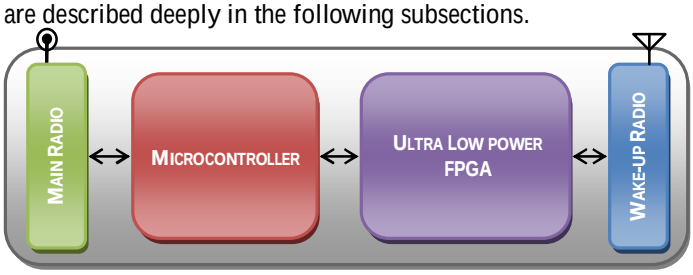

Figure 1 Proposed architecture

A. *Wake-up radio*

1) *Emitter.*

In the emitter a commercial chip is used. The main characteristics for a suitable emitter are:

- Ultra low power consumption while sleeping.
- Simple modulation (preferred OOK or ASK), in order to simplify the implementation of the demodulator.
- Capability to work in an ISM band (preferred 868 or 915 MHz).
- Direct access to the data transmission line, in order to save area avoiding the implementation of additional hardware blocks in the FPGA (i.e. a SPI controller).

2) *Receiver.*

In contrast with the general purpose receiver (in main radio in Figure 1), the WuR receiver for a WSN should be focused on minimizing the active power consumption over the energy efficiency of the communications as much as possible [17].

The receiver should protect the rest of the node against false wake-ups caused by noise in the channel but also has to be sensitive enough to detect the wake-up calls in a desired range in order to avoid retransmission for the calling nodes. A generic receiver structure is shown in Figure 2.

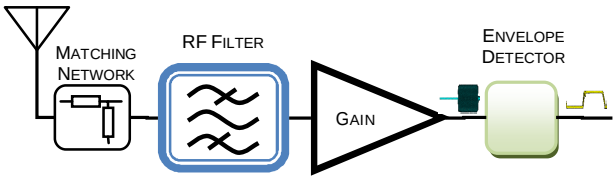

Figure 2 Generic Envelope Detector Receiver

B. *Low power FPGA.*

The desired devices should have low power consumption on active mode but also should be able to manage low power modes and fast wake-up time in order to process the wake-up calls.

In order to reduce the power consumption in the FPGA, different schemes can be applied. The main schemes are Clock gating and power down the FPGA.

The clock gating scheme is used to reduce the dynamic power consumption by disabling the clock of a specific block when it is not used while the static power consumption remains unchanged. This scheme has a very short wake-up time, but the non-negligible static power consumption will dramatically impact the lifetime of the node.

The power down scheme consists in powering down the FPGA while the node remains inactive and switching on the FPGA only when a wake-up call is received or when it is required by the main processor. This option reduces much more the power consumption but it also increments drastically the wake-up time which impacts directly in the latency of the network. Some devices have special low power modes that combine the best of both ultra low power consumption and fast wake-up methods.

Taking into account these factors, SRAM-based FPGAs are discarded in favor of the flash-based FPGAs. The main reason is that the static consumption is lower to in flash-based FPGAs than in SRAM-based devices. Moreover, these devices retain their configuration when the power is removed and do not need external memory for configuration [18].

The low power consuming FPGA family chosen is the Actel Igloo. Nowadays this family is the lowest power consuming in the market. Igloo FPGAs [19] have 6 different power modes, the most relevant for this work is the denominated *Flash*Freeze* (FF) Mode. FF mode is an ultra-low static power mode to reduce power consumption while preserving the state of the registers, memory banks and I/O states without switching off any power supplies, inputs, or input clocks. The FF mode needs 1 µs to switch from active state to freeze state, and vice versa. The FF mode enables the hardware to complete important tasks before allowing the device to enter in FF mode, such as transitioning into a safe state or completing the processing of a critical event.

The following section analyzes the interface of the FPGA with the elements of the architecture, paying special interest to the interface with the Wake-up Radio.

V. INTEGRATING WAKE UR RADIOS FUNCTIONALITIES IN MULTIHOP NETWORKS

One of the most complex tasks is to get a functional WSN that is able to combine the general purpose communication (main radio) and the WuR. Many factors must be taken into account in order to integrate a WuR device with a wireless sensor network, i.e., the structure of the network, routing protocols, scalability mechanisms, etc.

The ideal scenario is where the main radio carries all the tasks related to network management but shares the data (network address, routing tables, etc) with the WuR device. In this way the WuR will work as an "envelope" of the main communications infrastructure; if the share of the resources is not possible, the WuR device has to ask for the necessary data to the main processing unit and has to store it inside the FPGA.

In Figure 3, an example of the integration of WuR capabilities in a WSN is shown. In this example a remote node wants to communicate with a sink node as in a regular data gathering application. All the wakeup radios have stored the path to the sink node and their own address. In this way when a node receives a message it can send the message to the next node on the path. The wakeup mechanism works as follows.

In Figure 3a, node "A" wakes-up to communicate with the node "Sink". Once "A" is ready, it sends the wakeup message (W!) to the next node in the path (Fig 3b). When "A" receives the wakeup message (Fig 3c), "A" sends the data message to the next node in the route whereas the wakeup message is travelling to "Sink" two hops ahead (Fig 3d). In this way the latency of the wake-up process can be reduced and if the wakeup messages are short enough long hop distances can be reached.

In the next section, the implementation of the processing architecture of the WuR is presented.

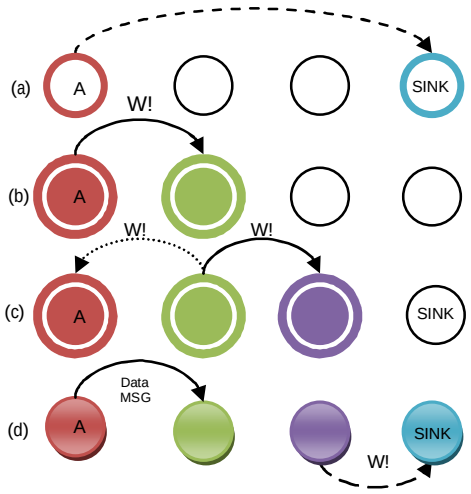

Figure 3 WSN with WuR: remote nodes communication

VI. WuR Implementation

1) *Emitter*

For the emitter a commercial chip will be used, the TX6001 [20], from RF Monolithics. Its main features are:

- 0.7 μA in sleep mode.
- 12 mA when transmitting.
- OOK and ASK modulation supported.
- 868.35 MHz carrier frequency.
- 2.7 to 3.5 Volts, power supply voltage.
- Direct connection to the *TX* port.
- 20 kbits per second in OOK transmission

The chosen transmitter has the minimum requirements for a wake-up emitter; low power consumption, one of the typical modulation for WuRs, low voltage power supply and transmission in an ISM band. If after the real test, the distance achieved is not long enough an RF amplifier could be included between the antenna and the transmitter, but this will impact negatively on the power consumption of the WuR.

2) *Receiver.*

In the receiver side there are several implementations found in the state of the art. The one presented in [14] has the best performance in power consumption using discrete components and it is used as a starting point in the receiver side; at this moment this solution is chosen to implement the receiver.

The structure of the receiver is based on 3 stages. The first stage, antenna, impedance matching and RF filter for the transmission frequency. The second stage is composed by a voltage multiplier that works as an amplifier and an envelope detector. The last stage is a digitizer stage based on an ultra low power comparator to perform an analog to digital conversion, and also to limit the input voltage in the FPGA as it is shown in Figure 4.

The reported power consumption of the implemented receiver (Figure 4) is 1.2 μW. This receiver contains the functionalities of a generic envelope detector as shown Figure 2. In this scheme the voltage multiplier and the digitizer act as the envelope detector and gain stages.

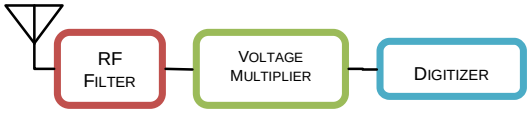

Figure 4 Receiver structure

3) *Ultra Low Power FPGA.*

The processing unit implemented in the FPGA is based on 5 functional blocks:

- Management of messages unit (MoM), it manages the activity of the processing unit and activates the switch to enable the emitter or the receiver.
- Data decoder, a Manchester decoder [10] is implemented. The utilization of this technique simplifies the message structure and avoids synchronization problems with the cost of an increment in the time needed for transmiting each bit.
- Data encoder, it is used in the transmission to convert the digital data into the Manchester coding; it receives the information through the MoM unit.
- Data processor, it acts as interface between the MoM unit and the decoder, it detects the type of the message and also evaluates the address of the incoming messages.
- Addressing data, this block stores the address of the node and the address of the corresponding hop in a route and receives the information from the microcontroller.

In order to get the lower power consumption in the FPGA the *Flash* Freeze* mode is used. In this operation mode, the FPGA is activated when a wake-up message arrives. Once it is active it captures and decodes the message; then it takes the necessary actions (wake-up the node, send a wakeup message, or discard the message) and when the task is complete it goes back to the *Flash*Freeze* mode. Using this scheme the most important decision is how to defrost the FPGA, different ways to wake-up the FPGA can be embraced.

The simplest approach is to use the first bit of the message; this scheme is based on very simple blocks, allowing the use of smaller devices that need fewer resources, i.e. without clock management block. This permits to reduce the power consumption in different modes of the FPGA (*Flash*Freeze* and running), but with the same speed and defined functionalities.

Figure 5 shows the basic blocks inside the FPGA. The estimated power consumption with the smallest usable FPGA, the Igloo AGL10 (10.000 equivalent gates) is: P_{active}= 0.093 mW, P_{iddle}= 8 μW, and an average power of $P_{average}$= 20 μW (15% active, 85% idle).

VII. Conclusions

In this paper, the usage of low power FGPAs to implement a complete Wake-up Radio for Wireless Sensor Networks has been evaluated.

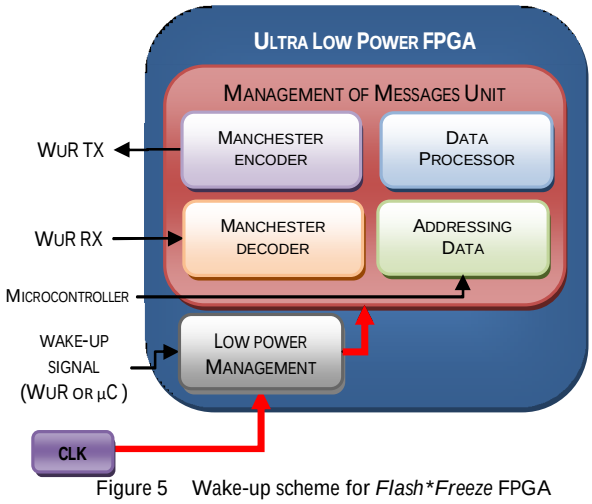

Figure 5 Wake-up scheme for *Flash*Freeze* FPGA

The theoretical results obtained for power consumption and system speed are interesting and motivate the real implementation of the presented architecture in order to measure the actual performance of the system.

As shown in Table 1, the proposed solution has power consumption in the range of the based on CotS implementations, which is very competitive taking into account the capabilities introduced with the usage of an ultra low power FPGA. The power consumption of the presented architecture can be reduced if low power design techniques for FPGAs are applied, (activating only some regions in the FPGA depending on the tasks, minimizing I/O signals, etc). The use of these kind of WuR combined with a deployment planner can lead to new ways for identification of the nodes or for routing the information in a more energy efficient way, all this path will be explored in future works.

TABLE I. WUR PLATFORMS BASED ON COTS

Institution	Based on CotS	Year	WSN platform	WuR Channel	Addressing	Nodes Distance (m)	Power WuR Receiver	Power Node Standby
Delft University of Technology [12]	Yes	2009	BT-Node	Shared	Yes, dedicated HW	3	801 µW	171 µW
RWTH Aachen University [13]	Yes	2009	TelosB	Dedicated	Yes, node µc	3	1.2 + 65 µW	120 µW
CEI-UPM	Yes	2011		Dedicated	Yes,dedicated HW	--	1,2 + 93 µW	--

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