

# Fabrication of sub-100 nm IDT SAW devices on insulating, semiconducting and conductive substrates

G.F. Iriarte\*, J.G. Rodriguez-Madrid, F. Calle

*Instituto de Sistemas Optoelectrónicos y Microtecnología, Universidad Politécnica de Madrid, ETSI Telecomunicación, Ciudad Universitaria s/n, 28040 Madrid, Spain*

## A B S T R A C T

This work describes the electron-beam (e-beam) lithography process developed to manufacture nano interdigital transducers (IDTs) to be used in high frequency (GHz) surface acoustic wave (SAW) applications. The combination of electron-beam (e-beam) lithography and lift-off process is shown to be effective in fabricating well-defined IDT finger patterns with a line width below 100 nm with a good yield. Working with insulating piezoelectric substrates brings about e-beam deflection. It is also shown how a very thin organic anti-static layer works well in avoiding this charge accumulation during e-beam lithography on the resist layer. However, the use of this anti-static layer is not required with the insulating piezoelectric layer laying on a semiconducting substrate such as highly doped silicon. The effect of the e-beam dose on a number of different layers (of insulating, insulating on semiconducting, semiconducting, and conductive natures) is provided. Among other advantages, the use of reduced e-beam doses increases the manufacturing time.

The principal aim of this work is to explain the interrelation among e-beam dose, substrate nature and IDT structure. An extensive study of the e-beam lithography of long IDT-fingers is provided, in a wide variety of electrode widths, electrode numbers and electrode pitches. It is worthy to highlight that this work shows the influence of the e-beam dose on five substrates of different conductive nature.

### Keywords:

E-beam lithography  
Insulating layers  
Charge accumulation  
Anti-static layer

## 1. Introduction

Surface acoustic wave (SAW) devices are now essential components in mobile communication and radar systems, among other applications. To achieve higher frequency demands the development of reliable lithography techniques, able to produce interdigital transducers (IDT) of several hundred periods with a reduced wavelength.

Smith (1974) explains thoroughly how to develop SAW devices by different lithography techniques as photolithography, electron lithography and X-ray lithography, comparing advantages and disadvantages of each technique. At that time, photolithography was the most convenient and economical technique, but scanning-electron-beam lithography was already suggested to be the future solution for complex high-resolution patterns. Yamanouchi et al. (1988) produced 10 GHz SAW devices based on  $\text{LiNbO}_3$  with 85 nm wide e-beam lithography IDT-fingers. Contrary to thin films, this substrate cannot be integrated in the CMOS technology.

The piezoelectric properties of the III-nitride semiconductors have attracted much attention in the last decade for the fabrication of high frequency acoustic wave devices, by means of

electron beam lithography and lift-off process. Due to the poor electrical conductivity and low chemical reactivity of these materials (in particular AlN), Palacios et al. (2002) tested several resist/metal multilayers, both by experiments and simulations, the most successful being the resist/metal/semiconductor and the resist/metal/resist/semiconductor schemes. Hatekeyama et al. (2004) achieved IDT-fingers of 180 nm wide; reduced size designs of 100 nm wide showed a poor production yield. Recently, SAW devices at 5 GHz have been fabricated on AlN/Si and GaN/Si structures by Neculoiu et al. (2009) and Müller et al. (2010), respectively. These high frequency devices in general show high losses likely due to the design of the test structures or impedance mismatch.

In addition to the lithography, the use of materials (layers and/or substrates) with high stiffness coefficients and low density also increases the device frequency. The most typical example is the AlN/diamond combination, used by Iriarte (2009) to fabricate SAW devices at 1 GHz with photolithographic IDT. E-beam devices operating at 5 GHz were developed by Kirsh et al. (2006). Assouar et al. (2007) also used the AlN/diamond structure to achieve SAW devices at 8 GHz with good temperature stability.

In summary, compared to the conventional optical lithography, e-beam lithography is most useful and practical for laboratory work, offering a better line resolution and a cost effective solution for iteration design-test structure. However, e-beam lithography

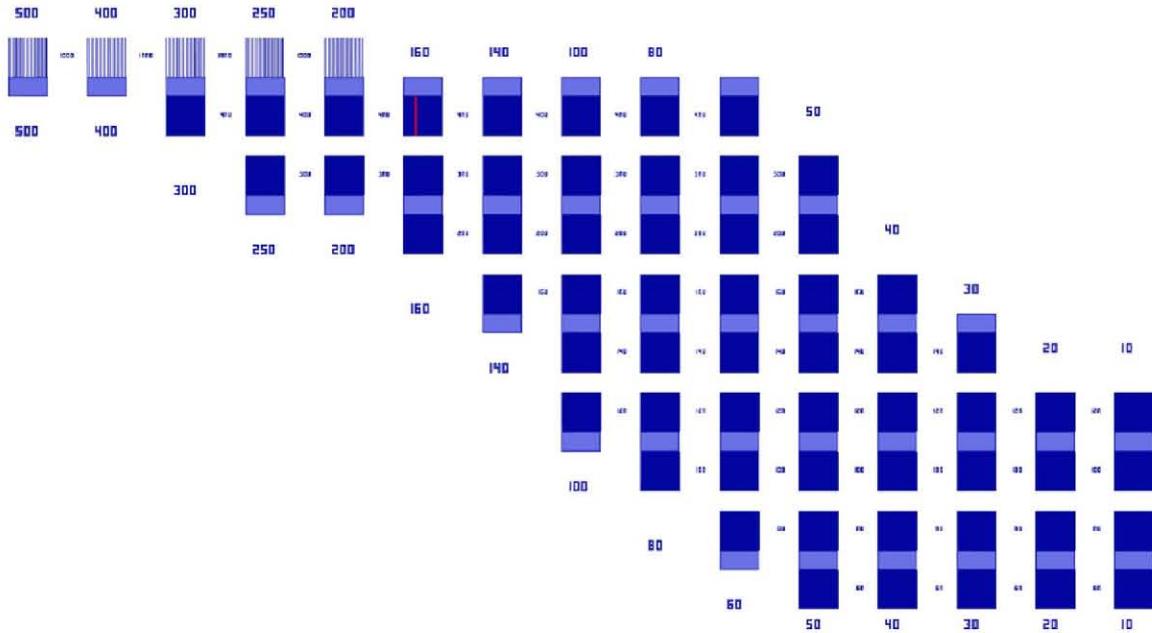


Fig. 1. Matrix of IDTs used in this work.

poses some disadvantages from the technical side, and charge accumulation and dose effects must be carefully considered. In this work, we have applied e-beam lithography and lift-off techniques for the fabrication of IDTs on five substrate types of different conductivity. Through this process, it is shown that well-defined IDT finger patterns with line widths below 100 nm can be fabricated at a good yield in conductive or semiconducting layers, but also on thin insulating layers deposited on conductive or semiconducting substrates. It is also shown that the use of a very thin organic antistatic layer is effective in minimizing the charge up issue for e-beam exposure on insulating substrates. As a result of this procedure, a SAW device with narrow electrode lines has been fabricated on AlN/diamond which operates at frequencies higher than 10 GHz.

## 2. Experimental procedure

The effect of the e-beam dose has been studied on five substrates of different character as regard the exposing e-beam. The substrates studied are the following ones:

- Platinum (Pt): conducting layer
- Silicon (Si): semiconducting layer
- AlN on Si: piezoelectric on semiconducting layer
- AlN on Al<sub>2</sub>O<sub>3</sub>: piezoelectric on insulating layer
- Al<sub>2</sub>O<sub>3</sub> (alumina): insulating layer

The e-beam dose time has been varied in the range of 0,40–0,70  $\mu$ s in 0,05  $\mu$ s steps. The field size used is of 600  $\mu$ m  $\times$  600  $\mu$ m; the amount of dots per field is 60.000. Dose time (Dt) in this work refers to the time the e-beam spends on each of these dots.

Table 1  
E-beam lithography conditions.

Resist	ZEP520-12
Resist thickness	150 nm
Acc. voltage	50 kV
Beam current	500 pA
Resist sens.	220 $\mu$ C/cm <sup>2</sup>
Field size	600 $\mu$ m $\times$ 600 $\mu$ m

In order to properly study the achievable resolution on each substrate, a matrix of IDTs has been used. Within this matrix, the line width goes from 300 nm down to 10 nm in steps of 20 nm, whereas the finger pitch is varied from 500 nm down to 10 nm in 20 nm steps. The length of the electrodes is 20  $\mu$ m. Fig. 1 shows its whole appearance.

The resist ZEP520 (diluted 1:2) was spun at 5000 rpm during 1 min, which resulted in a resist thickness of approximately 150 nm. After the e-beam lithography step, a thin Cr/Al layer (5 nm/20 nm) was evaporated on each sample. Chrome (Cr) was used to enhance the adhesion of the Al layer to the underlying substrate. After evaporation, the samples were introduced on a 1-methyl-2-pyrrolidone bath at 85  $^{\circ}$ C for 2 h to lift-off the resist and the metal on top of it. The lines remaining on the substrate were analyzed on the SEM, both after resist development as well as after the lift-off.

Both the exposure and imaging analysis after the resist development were performed by means of an e-beam lithography system based on a field-emission type filament (CRESTEC CABL-9500C). The system has a 50 keV column and resolves a minimum line width of 10 nm with a minimum beam diameter of 2 nm. The lowest AC

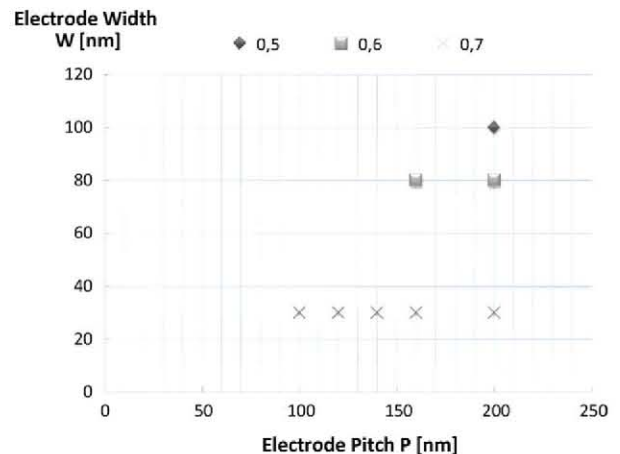


Fig. 2. Minimum dose times ( $\mu$ s) suggested for e-beam lithography of different IDTs on Pt substrates.

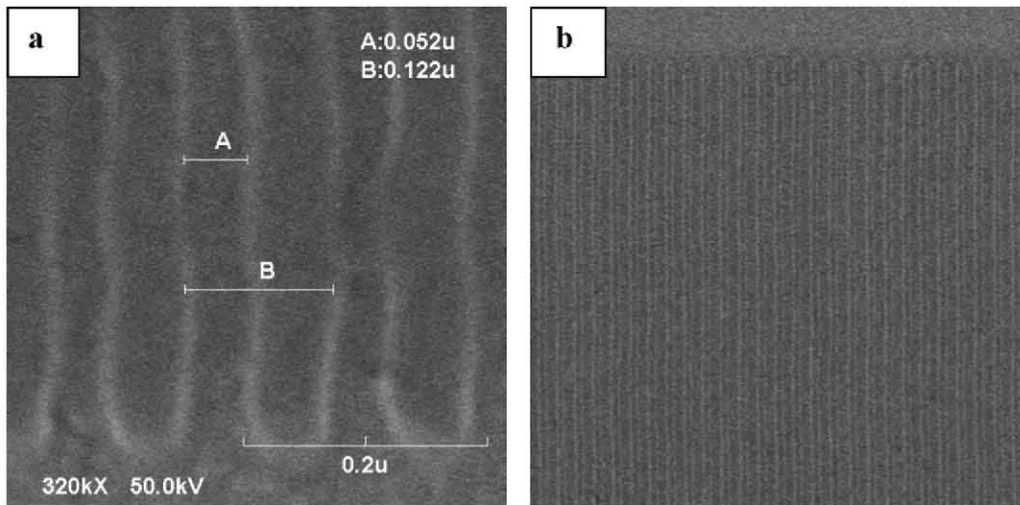


Fig. 3. (a) 50 nm and (b) 30 nm wide electrodes with (on the pattern) 100 nm pitch on a platinum (Pt) substrate, patterned with 65  $\mu\text{s}$  and 70  $\mu\text{s}$  dose times, respectively.

voltage is 5 kV, and the beam current can be varied from 5 pA to 100 nA. A beam position stability of  $\pm 30\text{ nm}/5\text{ h}$  is guaranteed as well as a 2 nm work stage resolution.

When working with insulating substrates, an organic anti-static layer (Espacer 300Z, Showa Denko) is used to avoid the charge accumulation. The layer scarcely influences the resolution of the e-beam lithography when this is done on semiconducting or metallic substrates, but it strongly influences the minimum resolution when working directly on insulating substrates.

Details of the process are as follow:

1. Spin coating of e-beam resist (ZEP520, Zeon) on a cleaned substrate: The thickness of the resist layer is chosen properly considering the trade-off between the required resolution and the electrode thickness. That is, it is empirically known that the resist layer thickness should be at least 100 nm thicker than the metal thickness for the following lift-off process, though the resolution increases with a decrease in the resist layer thickness.
2. Hard-baking: The resist was hard baked for 2 min at 190  $^{\circ}\text{C}$ .
3. Spin coating of antistatic layer (Espacer 300Z, Showa Denko), when required (only for insulating substrates): The thickness of the anti-static layer is of about 20 nm when spinned at 3000 rpm for 60 s.
4. E-beam exposure: The dose amount should be decided properly by taking into account the substrate material. See Table 1 for other parameters used.
5. When required, removal of anti-static layer: This process is performed by simply immersing the specimen in distilled water for a few seconds.
6. Resist development by dipping in ZED-N50 (Zeon) developer for 60 s and rinse by blowing with  $\text{N}_2$  for a few seconds.
7. Deposition of a very thin (5 nm) Cr film for adhesion improvement and a 20 nm thin Al film on the specimen by vacuum evaporation.
8. Removal of the resist layer (lift-off) by immersion in 1-methyl-2-pyrrolidinone at 85  $^{\circ}\text{C}$ .

### 3. Results and discussion

The results obtained on each of the five different substrates are analyzed either after resist development or after lift-off for reasons explained in each particular case. In the following, the IDT will be named after the line width or pitch used; e.g.,  $W100$  stands for electrode line width of 100 nm and  $P200$  stands for electrode line pitch

of 200 nm, where pitch is defined here as the distance resulting from the sum of the electrode width and the space in-between the sides of two adjacent electrodes facing each other.

#### 3.1. Platinum (Pt)

Fig. 2 shows the range of times in  $\mu\text{s}$  suggested for several combinations of IDT line width ( $W$ ) and pitch ( $P$ ). Some results are shown in Fig. 3.

E-beam times of 0.40  $\mu\text{s}$  and 0.45  $\mu\text{s}$  were too low and did not delivered good results. A 0.50  $\mu\text{s}$  dose time was enough for  $W100:P200$ , but  $W100:P160$  was not resolved even using the longest time (0.70  $\mu\text{s}$ ). The  $W80:P160$  ratio required a Dt of at least 0.60  $\mu\text{s}$ .

In summary, for lithography on Pt substrate, the best results are usually achieved using dose times of 0.70  $\mu\text{s}$ . Shorter times as low as 0.50  $\mu\text{s}$  were good enough for 100 nm wide electrodes on a 200 nm pitch, and could be used to speed up the e-beam lithography process. Line widths of 20 nm and below would require further optimization.

#### 3.2. Silicon (Si)

As shown in Fig. 4, Dt of at least 0.65  $\mu\text{s}$  is suggested for  $W100:P200$ . Line widths down to 20 nm could be obtained on a 100 nm pitch, but the electrode edges were not resolved. Lines

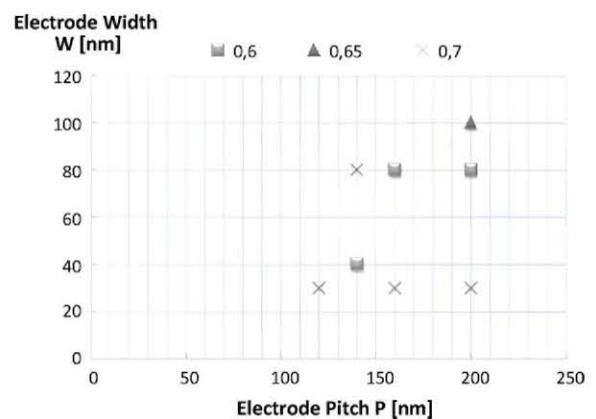


Fig. 4. Minimum Dt ( $\mu\text{s}$ ) for e-beam lithography suggested for several IDTs on Si substrates.

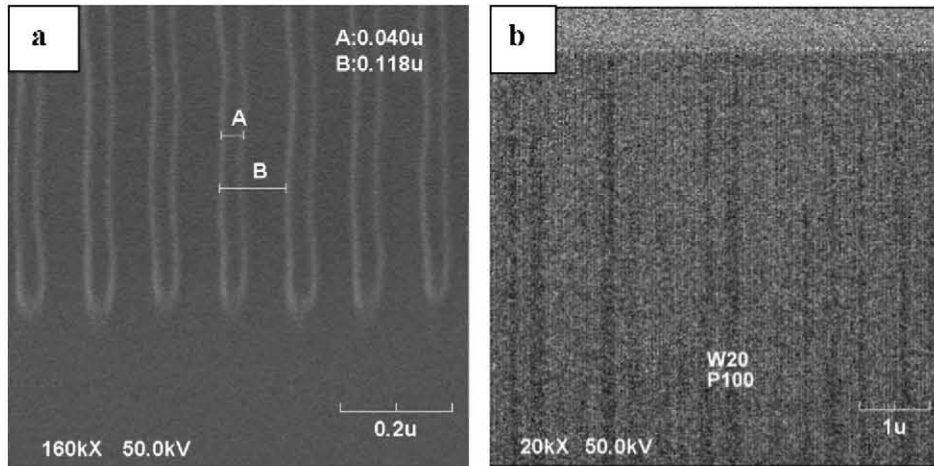


Fig. 5. Silicon substrate: (a) 40 nm electrodes on a (on the pattern) 100 nm pitch (60  $\mu$ s). (b) 20 nm electrodes on a 100 nm pitch showing some discontinuity (70  $\mu$ s).

below 20 nm in width require special optimization. Some results are shown in Fig. 5.

### 3.3. AlN on Si

In this section we describe the patterning of IDTs on AlN layers, 1.5  $\mu$ m thick, deposited by reactive sputtering on Si substrates. Despite the non-conductive nature of the AlN film, the AlN/Si system does not require the use of an antistatic layer for successful e-beam lithography.

However, due to charging effects, SEM cannot be used to analyze the sample after resist development. We tried to spin the antistatic layer to a higher speed in order to make it thinner (less than 20 nm) in an attempt to analyze the lines obtained. The charging effect could not be avoided; moreover, the resist tends to get slightly wider after a long exposure to the e-beam during SEM analysis. Therefore, no SEM analysis of the “as developed” samples could be done. Instead, the lift-off step was done, and the analysis of the results by SEM was used to determine the achievable electrode width–electrode pitch ratio under each dose time. As shown in Fig. 6, higher times are required on the AlN/Si system as compared to the Pt or Si systems.

Dose times below 0.65  $\mu$ s are not recommended on the AlN/Si substrate system, at least without using an antistatic layer.

Line widths below 50 nm require special optimization and/or the use of an antistatic layer. The manufacture of 100 nm wide

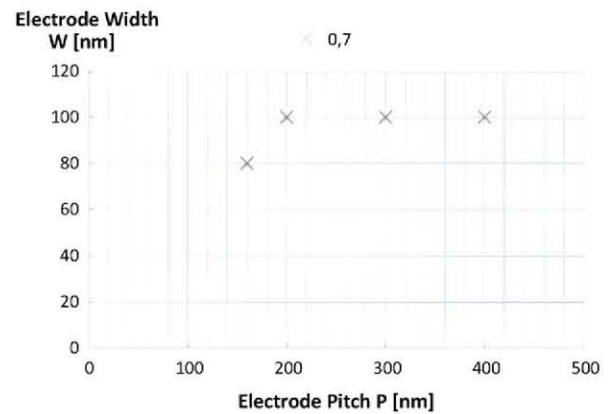


Fig. 6. Minimum Dt ( $\mu$ s) suggested for e-beam patterning of IDTs on AlN/Si structures.

electrodes required pitches above 200 nm, but 80 nm wide lines at 160 nm pitch could be defined by lift-off at very good yield (Fig. 7).

### 3.4. Al<sub>2</sub>O<sub>3</sub> and AlN/Al<sub>2</sub>O<sub>3</sub>

When fabricating IDTs on insulating materials by e-beam lithography, an antistatic polymer layer such as the Espacer 300Z (Showa Denko) should be used. This is the case discussed in this section

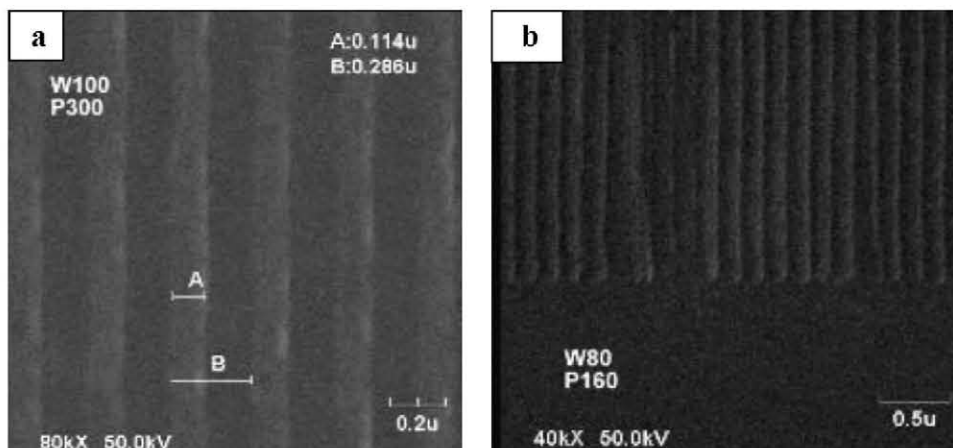


Fig. 7. E-beam patterning of IDTs on AlN/Si structures using 70  $\mu$ s dose times: (a) 100 nm electrodes on a 300 nm pitch, (b) 80 nm electrodes on a 160 nm pitch showing some discontinuity.

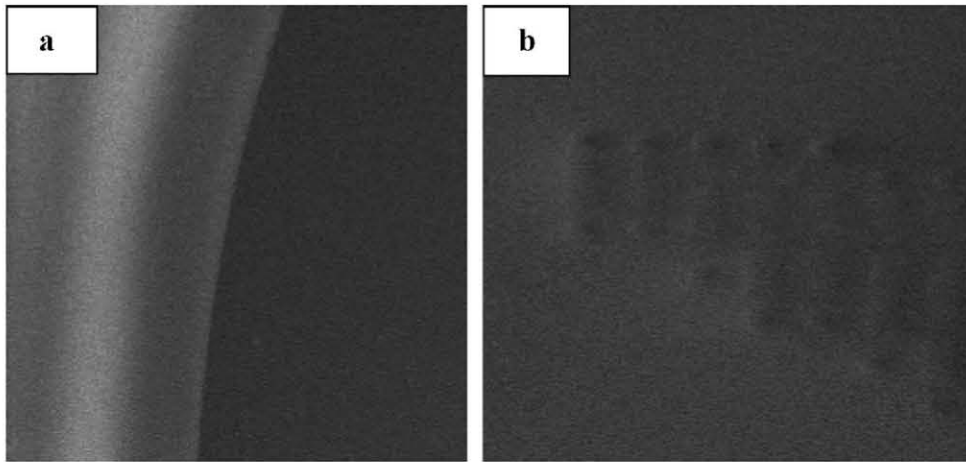


Fig. 8. (a) Charging effect shown on image's left half. (b) Use of Spacer 300Z (Showa Denko) for SEM analysis after resist development.

for the lithography and lift-off on  $\text{Al}_2\text{O}_3$  substrate and  $\text{AlN}/\text{Al}_2\text{O}_3$  structures. Actually, insulating substrates show a difficulty for SEM analysis after resist development of the achieved resolution due to charging effects. Fig. 8a shows a difference between an area where the antistatic layer is present (right half of the image), and an area where it was not used (left half of the image). Due to charging effects, SEM cannot be used directly to analyze the sample after resist development. Although the Spacer 300Z layer is only 20 nm thick, neither can it be used for SEM analysis after resist development. The 20 nm thin layer does not follow the contour of the developed resist lines, as shown in Fig. 8b. We tried to spin the antistatic layer to a higher speed in order to make it thinner (<20 nm) in an attempt to analyze the lines developed. The charging effect could not be avoided and hence no SEM analysis of the "as developed" samples could be done. Moreover, the resist tends to get slightly wider after a prolonged exposure to the e-beam during SEM analysis. For these reasons, the attempt to analyze the "as developed" structures was abandoned.

Instead, the lift-off step was done and the results of it, which could indeed be inspected under the SEM, were used to determine the achievable electrode width–electrode pitch ratio under each dose time.

As shown in Fig. 9, this substrate system showed to be more critical regarding the pitch. Thus, lift-off of electrode pitches below 100 nm could not be successfully done for sub-100 nm width

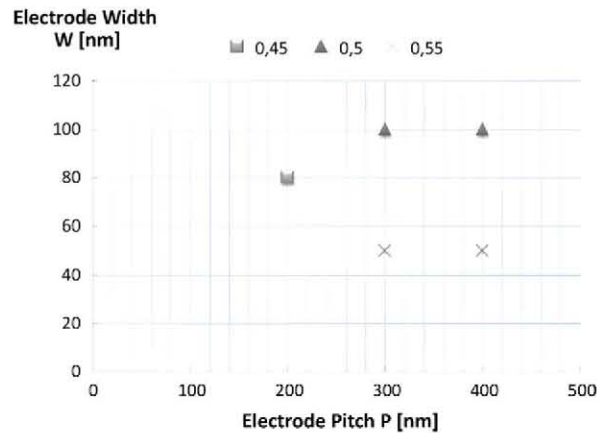


Fig. 9. Minimum doses ( $\mu\text{s}$ ) suggested on  $\text{AlN}/\text{Al}_2\text{O}_3$  and  $\text{Al}_2\text{O}_3$  substrate system.

electrodes. However, it is remarkable to see how widths as small as 60 nm and even 50 nm could be done using times as short as 0.50  $\mu\text{s}$  and 0.55  $\mu\text{s}$ . These good results are due to the use of the antistatic layer. ZEP520 resist has a sensitivity of  $220 \mu\text{C}/\text{cm}^2$ . According to this, the calculated dose for the field size ( $600 \mu\text{m} \times 600 \mu\text{m}$ ), voltage and current of e-beam used as well as for the amount of dots per

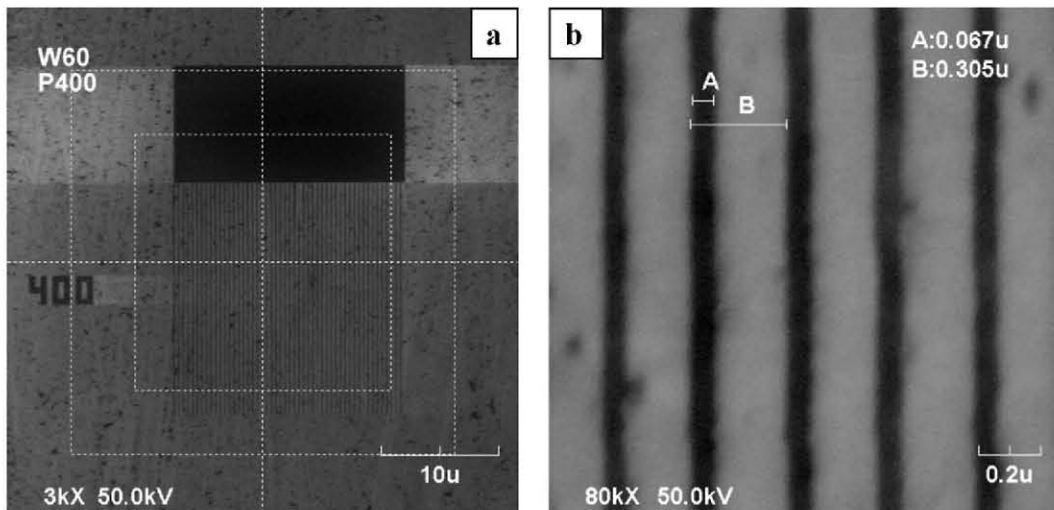


Fig. 10. Sapphire ( $\text{Al}_2\text{O}_3$ ) substrate: (a) 60 nm electrodes on a 400 nm pitch (dose time of 50  $\mu\text{s}$ ). (b) 60 nm electrodes on 300 nm pitch (dose time of 70  $\mu\text{s}$ ).

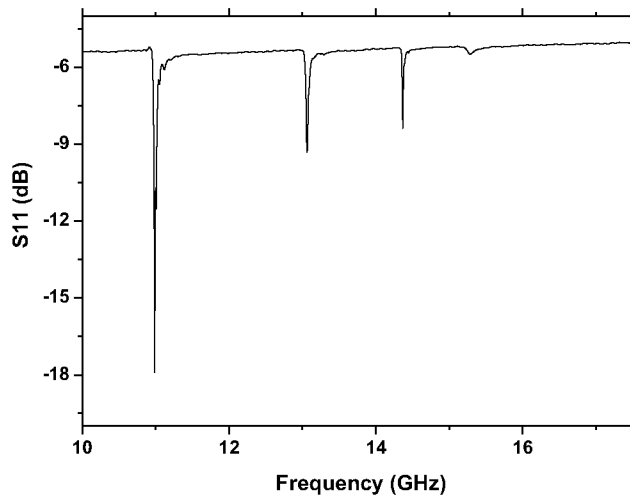


Fig. 11. Reflection coefficient of a 200 nm electrode width SAW resonator.

field used (60,000) should be  $0.44 \mu\text{s}$ , close to the dose times used for patterning the IDTs. As displayed in Fig. 10, IDTs with 60 nm wide electrodes after lift-off can successfully be manufactured on the AlN/Al<sub>2</sub>O<sub>3</sub> system, by using the techniques described above.

### 3.5. SAW device

In order to exploit the procedures discussed above, SAW devices with electrodes widths from 100 to 200 nm were processed on an AlN/diamond heterostructure in order to increase the frequency at which they operate. During e-beam exposure, the AlN/diamond heterostructure is equal to the Al<sub>2</sub>O<sub>3</sub> and AlN/Al<sub>2</sub>O<sub>3</sub> systems in terms of charge building effects. Thus the use of the antistatic layer was also required in this case.

AlN films 600 nm thick were deposited in a home built balanced magnetron sputter deposition system on microcrystalline diamond substrates. These substrates were fabricated by a chemical vapour deposition (CVD) and polished. The IDT of the device consists of 100 fingers with an electrode width of 200 nm. Fig. 11 shows the reflection coefficient of a SAW resonator showing three resonances, the Rayleigh mode at 11.0 GHz, and some other confined modes at 13.1 and 14.4 GHz, respectively. Improved devices are under way to further increase the operating frequencies.

## 4. Conclusions

This work shows that line widths of 100 nm and above can easily be resolved using the calculated dose of resists. However, the manufacture of sub 100 nm lines requires higher doses depending on the substrate as well as on the finger width/pitch ratio. The dose time required for the fabrication of IDTs of variable line width and line pitch patterned by e-beam lithography has been determined for five substrates of different conductive character. Platinum, silicon and AlN/Si substrates do not require the use of an antistatic layer to obtain line widths below 100 nm. However, e-beam patterning of these lines on insulating substrates (AlN/Al<sub>2</sub>O<sub>3</sub> and Al<sub>2</sub>O<sub>3</sub>) requires the use of such layer. We have used this procedure to fabricate SAW devices on AlN/diamond structures, operating above 10 GHz.

## Acknowledgements

GFI acknowledges the Spanish Ministerio de Ciencia e Innovación (MICINN) contract W050920B0. This work is supported by MICINN projects TEC2007-67065/MIC and TEC2010-19511.

## References

- Assouar, M.B., Elmazria, O., Kirsch, P., Mortet, V., Tiusan, C., Alnot, P., 2007. High-frequency surface acoustic wave devices based on AlN/diamond layered structure realized using e-beam lithography. *Journal of Applied Physics* 101, 114507.
- Hatekeyama, H., Omori, T., Hashimoto, K., Yamaguchi, M., 2004. Fabrication of SAW devices using SEM-based electron beam lithography and lift-off technique for lab use. In: *IEEE International Ultrasonics, Ferroelectrics, and Frequency Control Joint 50th Anniversary Conference*, pp. 1896–1900.
- Iriarte, G.F., 2009. Surface acoustic wave propagation characteristics of aluminium nitride thin films grown on polycrystalline diamond. *Journal of Applied Physics* 93 (12), 9604–9609.
- Kirsch, P., Assouar, M.B., Mortet, V., Alnot, P., Elmazria, O., 2006. 5 GHz surface acoustic wave devices based on aluminium nitride/diamond layered structure realized using electron beam lithography. *Applied Physics Letters* 88, 223504.
- Müller, A., Neculoiu, D., Konstantinidis, G., Deligeorgis, G., Dinescu, A., Stavrinidis, A., Cismaru, A., Dragoman, M., Stefanescu, A., 2010. SAW devices manufactured on GaN/Si for frequencies beyond 5 GHz. *IEEE Electron Device Letters* 31, 1398–1400.
- Neculoiu, D., Müller, A., Deligeorgis, G., Dinescu, A., Stavrinidis, A., Vasilache, D., Cismaru, A.M., Stan, G.E., Konstantinidis, G., 2009. AlN on silicon based surface acoustic wave resonators operating at 5 GHz. *Electronics Letters* 45, 23.
- Palacios, T., Calle, F., Monroy, E., Grajal, J., Eickhoff, M., Ambacher, O., Prieto, C., 2002. Nanotechnology for SAW devices on AlN epilayers. *Materials Science and Engineering B* 93, 154–158.
- Smith, H.I., 1974. Fabrication techniques for surface-acoustic-wave and thin-film optical devices. *Proceeding of the IEEE* 62 (10), 1361–1387.
- Yamanouchi, K., Cho, Y., Meguro, T., 1988. SHF-range surface acoustic wave interdigital transducers using electron beam exposure. In: *Proceeding IEEE Ultrasonic Symposium*, pp. 115–118.