Dynamical properties of electrical circuits with fully nonlinear memristors*†

Ricardo Riaza

Departamento de Matemática Aplicada a las Tecnologías de la Información
Escuela Técnica Superior de Ingenieros de Telecomunicación
Universidad Politécnica de Madrid - 28040 Madrid, Spain
ricardo.riaza@upm.es

Abstract

The recent design of a nanoscale device with a memristive characteristic has had a great impact in nonlinear circuit theory. Such a device, whose existence was predicted by Leon Chua in 1971, is governed by a charge-dependent voltage-current relation of the form $v = M(q)i$. In this paper we show that allowing for a fully nonlinear characteristic $v = \eta(q, i)$ in memristive devices provides a general framework for modeling and analyzing a very broad family of electrical and electronic circuits; Chua's memristors are particular instances in which $\eta(q, i)$ is linear in i. We examine several dynamical features of circuits with fully nonlinear memristors, accommodating not only charge-controlled but also flux-controlled ones, with a characteristic of the form $i = \zeta(\varphi, v)$. Our results apply in particular to Chua's memristive circuits; certain properties of these can be seen as a consequence of the special form of the elastance and reluctance matrices displayed by Chua's memristors.

Keywords: nonlinear circuit, memristor, differential-algebraic equation, semistate model, state dimension, eigenvalues.

AMS subject classification: 05C50, 15A18, 34A09, 94C05.

*Supported by Research Projects MTM2007-62064 of Ministerio de Educación y Ciencia, MTM2010-15102 of Ministerio de Ciencia e Innovacion, and CCG10-UPM/ESP-5236 of Comunidad de Madrid/UPM, Spain.

†This is a pre-peer reviewed of the following article, *R. Riaza, Dynamical properties of electrical circuits with fully nonlinear memristors. Nonlinear Analysis: Real World Applications, Vol. 12 (2011) 3674-3686.*

1 Introduction

In 1971 Leon Chua predicted the existence of a fourth basic circuit element which would be governed by a flux-charge relation, having either a charge-controlled form $\varphi = \phi(q)$ or a flux-controlled one $q = \sigma(\varphi)$ [10]. This characteristic was somehow lacking in electrical circuit theory, since resistors, capacitors and inductors are defined by voltage-current, charge-voltage and flux-current relations, respectively. The design of such a *memory-resistor* or *memristor* at the nanometer scale announced by an HP team in 2008 [37] has driven a lot of attention to these devices. Many applications are being developed (cf. [9, 21, 36, 38, 40] and references therein). Memristive devices pose challenging problems at the device and circuit modeling levels [4, 28, 33, 39] but also from a dynamical perspective [20, 25, 26, 27, 31].

The memristor reported in [37] is governed by a relation of the form

$$v = M(q)i, \tag{1}$$

being framed in the charge-control setting postulated by Chua in his seminal paper [10]; indeed, assuming ϕ to be C^1, taking time derivatives in the equation $\varphi = \phi(q)$ and using the relations $\varphi' = v$, $q' = i$, we are led to (1) with $M(q) = \phi'(q)$. Chua and Kang considered in [11] the more general characteristic

$$v = M(q, i)i. \tag{2}$$

Both (1) and (2), but also the maps governing other devices such as capacitors or resistors, are particular instances of the fully nonlinear relation

$$v = \eta(q, i) \tag{3}$$

to be discussed in this paper. The general characteristic (3) will give a deeper insight into the mathematical properties that underly several dynamical features of memristive circuits. In particular, memristors increase the dynamical degree of freedom regardless of their actual location in the circuit, contrary to capacitors or inductors which in certain (so-called topologically degenerate) configurations do *not* increase the state dimension; additionally, memristors have been observed to introduce null eigenvalues in the linearization of different circuits [25, 31]. This kind of problems can be nicely addressed in the framework here introduced.

This will be possible because of the fact that (3), together with its dual relation

$$i = \zeta(\varphi, v) \tag{4}$$

and their time-varying counterparts, allow for a surprisingly simple, albeit general, model for the dynamics of nonlinear circuits including resistors, memristors, capacitors, inductors,

and voltage and current sources. Indeed, such a model can be written as

$$\begin{aligned} q' &= i_q && \text{(5a)} \\ \varphi' &= v_\varphi && \text{(5b)} \\ v_q &= f(q, i_q, t) && \text{(5c)} \\ i_\varphi &= g(\varphi, v_\varphi, t) && \text{(5d)} \\ 0 &= B_q v_q + B_\varphi v_\varphi && \text{(5e)} \\ 0 &= D_q i_q + D_\varphi i_\varphi, && \text{(5f)} \end{aligned}$$

where $B = (B_q \; B_\varphi)$ and $D = (D_q \; D_\varphi)$ stand for the reduced loop and cutset matrices of the circuit (cf. subsection 3.1). The circuit elements (and hence B and D) are divided into so-called q- and φ-devices, as detailed in Section 2. The key aspect supporting the model (5) is that e.g. (5d) accommodates a great variety of devices, including flux-controlled memristors, linear inductors, Josephson junctions, *pn* and tunnel diodes, independent current sources, voltage-controlled current sources, etc.; similar remarks apply to (5c).

The goal of our research is two-fold: first, from a modeling point of view, we want not only to accommodate in circuit theory general devices governed by (3) or (4), but also emphasize the fact that these characteristics allow for a very general description of the circuit dynamics, providing in turn a framework for the analysis of different nonlinear phenomena; from an analytical standpoint, we wish to tackle several dynamical properties of circuits with fully nonlinear memristors. The structure of the paper reflects the two main aspects that drive this research: we address modeling issues in Section 2, and dynamical properties in Section 3. Section 4 compiles some concluding remarks.

2 Device models

2.1 q-devices

Definition 1. *A q-device is a circuit element which admits a C^1 description of the form*

$$v = \eta(q, i, t). \tag{6}$$

The terminology comes from the fact that q-devices may be controlled by the charge q (this will be the case for capacitors), its time derivative $q' = i$ (for current-controlled resistors) or both (for q-memristors). Voltage sources will be included in this group for the sake of completeness.

The relation (6) is a time-varying generalization of (3). Depending on the actual form of the map η in (6), q-devices particularize to the ones listed in Table 1. It is worth noting that η need not be a scalar map; this accommodates coupling effects within the different types of q-devices. Keep also in mind that e.g. $\partial\eta/\partial q \not\equiv 0$ (resp. $\equiv 0$) means that this derivative

does not vanish (resp. does vanish) identically; in the first case, it may find a zero at certain points, though; for instance, it vanishes at $i = 0$ in Chua's memristor, for which $v = M(q)i$.

1. A *q-memristor* is a q-device for which

$$\frac{\partial \eta}{\partial q} \not\equiv 0, \quad \frac{\partial \eta}{\partial i} \not\equiv 0.$$

The map governing the set of q-memristors will be denoted by $v_m = \eta_1(q_m, i_m, t)$.

2. A *capacitor* is a q-device for which

$$\frac{\partial \eta}{\partial q} \not\equiv 0, \quad \frac{\partial \eta}{\partial i} \equiv 0.$$

The relation governing the set of capacitors will be denoted by $v_c = \eta_2(q_c, t)$.

3. A *current-controlled resistor* is a q-device for which

$$\frac{\partial \eta}{\partial q} \equiv 0, \quad \frac{\partial \eta}{\partial i} \not\equiv 0.$$

The map governing the set of current-controlled resistors will be written as $v_r = \eta_3(i_r, t)$.

4. An independent *voltage source* is a q-device for which

$$\frac{\partial \eta}{\partial q} \equiv 0, \quad \frac{\partial \eta}{\partial i} \equiv 0.$$

The relation governing independent voltage sources will be denoted by $v_u = \eta_4(t)$.

Table 1: q-devices.

In a time-invariant setting, if η is linear in i then we get Chua's memristor, for which $v = M(q)i$. For this reason we use the expression "fully nonlinear" to label memristors with the general form $v = \eta(q, i)$. This should cause no misunderstanding with the nonlinear nature of the original flux-charge relation $\varphi = \phi(q)$ in Chua's setting. Note also that these memristors are referred to in the literature either as *charge-controlled memristors* or as *current-controlled memristors*; with the expression "q-memristor" we want to emphasize that the charge q is the dynamic variable actually involved in the description of the device, as it will happen with the flux φ in φ-memristors.

2.2 φ-devices

Definition 2. *A φ-device is a circuit element which admits a C^1 description of the form*

$$i = \zeta(\varphi, v, t). \tag{7}$$

The different types of φ-devices are enumerated in Table 2.

1. A *φ-memristor* is a φ-device for which

$$\frac{\partial \zeta}{\partial \varphi} \not\equiv 0, \quad \frac{\partial \zeta}{\partial v} \not\equiv 0.$$

The map governing the set of φ-memristors will be denoted by $i_w = \zeta_1(\varphi_w, v_w, t)$.

2. An *inductor* is a φ-device for which

$$\frac{\partial \zeta}{\partial \varphi} \not\equiv 0, \quad \frac{\partial \zeta}{\partial v} \equiv 0.$$

The relation governing the set of inductors will be denoted by $i_l = \zeta_2(\varphi_l, t)$.

3. A *voltage-controlled resistor* is a φ-device for which

$$\frac{\partial \zeta}{\partial \varphi} \equiv 0, \quad \frac{\partial \zeta}{\partial v} \not\equiv 0.$$

The map governing the set of voltage-controlled resistors will be written as $i_g = \zeta_3(v_g, t)$.

4. An independent *current source* is a φ-device for which

$$\frac{\partial \zeta}{\partial \varphi} \equiv 0, \quad \frac{\partial \zeta}{\partial v} \equiv 0.$$

The relation governing independent current sources will be denoted by $i_j = \zeta_4(t)$.

Table 2: φ-devices.

Again, Chua's flux-controlled memristor [10], for which $i = W(\varphi)v$, is obtained in particular when ζ is time-independent and linear in v.

We do not impose any condition on the time derivatives, either for q- or φ-devices. If they vanish in memristors, resistors, capacitors and inductors we would be led to a time-invariant setting, with η_k, ζ_k $(k = 1, 2, 3)$ being independent of t. For sources this assumption would model DC ones. It is also worth remarking that current-controlled voltage sources (CCVS's)

could be easily included in the above taxonomy as q-devices and, similarly, voltage-controlled current sources (VCCS's) can be modeled as φ-devices.

2.3 Characteristic matrices and passivity

The matrices of partial derivatives of the maps introduced above define the so-called *characteristic matrices* of the different devices.

Definition 3. *The incremental* memristance, elastance *and* resistance *matrices of q-memristors, capacitors and current-controlled resistors, respectively, are defined as*

$$M(q_m, i_m, t) = \frac{\partial \eta_1(q_m, i_m, t)}{\partial i_m}, \quad E_c(q_c, t) = \frac{\partial \eta_2(q_c, t)}{\partial q_c}, \quad R(i_r, t) = \frac{\partial \eta_3(i_r, t)}{\partial i_r}.$$

Additionally, the incremental elastance *of q-memristors is*

$$E_m(q_m, i_m, t) = \frac{\partial \eta_1(q_m, i_m, t)}{\partial q_m}.$$

In Chua's memristor, for which $v = M(q)i$, the incremental memristance depends only on the charge q. The fact that $q(t) = \int_{-\infty}^{t} i_m(\tau)d\tau$ makes this element behave as a resistor in which the resistance depends on the device history; the "memory-resistor" name stems from this.

If the elastance of capacitors is non-singular at a given operating point, then because of the implicit function theorem these devices admit (at least locally) a voltage-controlled description

$$q_c = \gamma(v_c, t).$$

The incremental *capacitance* matrix is then defined as

$$C(v_c, t) = \frac{\partial \gamma(v_c, t)}{\partial v_c} = (E_c(\gamma(v_c, t), t))^{-1}.$$

Note that when a given set of devices (memristors, capacitors or resistors) does not exhibit coupling effects, the corresponding characteristic matrix is a diagonal one, with diagonal entries defined by the memristances, elastances or resistances of the individual devices.

The characteristic matrices of φ-devices are defined analogously, as detailed below.

Definition 4. *The incremental* memductance, reluctance *and* conductance *matrices of φ-memristors, inductors and voltage-controlled resistors, respectively, are defined as*

$$W(\varphi_w, v_w, t) = \frac{\partial \zeta_1(\varphi_w, v_w, t)}{\partial v_w}, \quad \mathcal{R}_l(\varphi_l, t) = \frac{\partial \zeta_2(\varphi_l, t)}{\partial \varphi_l}, \quad G(v_g, t) = \frac{\partial \zeta_3(v_g, t)}{\partial v_g}.$$

The incremental reluctance *of φ-memristors is*

$$\mathcal{R}_w(\varphi_w, v_w, t) = \frac{\partial \zeta_1(\varphi_w, v_w, t)}{\partial \varphi_w}.$$

As for capacitors, if the reluctance of inductors is non-singular, then via the implicit function theorem these devices can be shown to admit a local current-controlled description

$$\varphi_l = \xi(i_l, t),$$

and the incremental *inductance* matrix is defined as

$$L(i_l, t) = \frac{\partial \xi(i_l, t)}{\partial i_l} = (\mathcal{R}_l(\xi(i_l, t), t))^{-1}.$$

In order to define the local notions of passivity and strict passivity, we make use of the concept of a positive (semi)definite matrix; a square matrix P is positive semidefinite (resp. definite) if $u^T P u \geq 0$ (resp. > 0) for every non-vanishing vector u. We do not assume P to be symmetric.

Definition 5. *We call the q-memristors, capacitors, current-controlled resistors, φ-memristors, inductors or voltage-controlled resistors* locally passive *(resp.* strictly locally passive*) at a given point if the incremental memristance, elastance, resistance, memductance, inductance or conductance matrix is positive semidefinite (resp. definite) at that point.*

It is easy to check that a positive definite matrix is non-singular, and that its inverse is itself positive definite; this means that the capacitance and inductance matrices are positive definite if the elastance and reluctance matrices of capacitors and inductors are so. No condition is imposed on the elastance and reluctance matrices of q- and φ-memristors, except for the fact that they cannot vanish identically since otherwise these devices would amount to (current- or voltage-controlled) resistors. Note finally that, with terminological abuse, the adverb "locally" is often omitted when a given set of devices satisfies the (semi)definiteness requirement everywhere. Similarly, the term "incremental" is very often omitted in the characteristic matrices.

3 Analytical results: nondegeneracy, null eigenvalues

The general framework introduced in Section 2 makes it possible to address different analytical properties of memristive circuits in broad generality. After introducing some background material in subsection 3.1, we tackle in subsections 3.2, 3.3 and 3.4 two particular problems which rely on linearization, emphasizing the role of the form of the different characteristic matrices discussed above; specifically, the absence of memristance (resp. memductance) in capacitors (resp. inductors), namely, the conditions $\partial \eta / \partial i \equiv 0$, $\partial \zeta / \partial v \equiv 0$ holding for them, together with the form of the elastance and reluctance matrices for different memristors, will explain certain dynamical features of memristive circuits. Our approach should also be useful in future analyses of many other aspects of memristive circuit dynamics, including e.g. stability properties, oscillatory phenomena or bifurcations.

3.1 Some auxiliary results from digraph theory

Many aspects of our analysis will rely on the properties of the *directed graph* or *digraph* underlying a given electrical circuit. We compile below some background material on digraph theory. The reader is referred to [1, 2, 5, 14, 30] for additional details.

We will work with a directed graph having n nodes, m branches and k connected components. A subset K of the set of branches of a digraph is a *cutset* if the removal of K increases the number of connected components of the digraph, and it is minimal with respect to this property, that is, the removal of any proper subset of K does not increase the number of components. In a connected digraph, a cutset is just a minimal disconnecting set of branches. The removal of the branches of a cutset increases the number of connected components by exactly one. Furthermore, all the branches of a cutset may be shown to connect the same pair of connected components of the digraph which results from the deletion of the cutset. This makes it possible to define the orientation of a cutset, say from one of these components towards the other. The cutset matrix $\tilde{D} = (d_{ij})$ is then defined by

$$d_{ij} = \begin{cases} 1 & \text{if branch } j \text{ is in cutset } i \text{ with the same orientation} \\ -1 & \text{if branch } j \text{ is in cutset } i \text{ with the opposite orientation} \\ 0 & \text{if branch } j \text{ is not in cutset } i. \end{cases}$$

The rank of $\tilde{D}$ can be proved to be $n-k$; any set of $n-k$ linearly independent rows of $\tilde{D}$ defines a *reduced cutset matrix* $D \in \mathbb{R}^{(n-k)\times m}$. In a connected digraph, any reduced cutset matrix has order $(n-1)\times m$.

The space spanned by the rows of D equals the one spanned by the rows of the so-called *incidence matrix*, defined as $A = (a_{ij})$ with

$$a_{ij} = \begin{cases} 1 & \text{if branch } j \text{ leaves node } i \\ -1 & \text{if branch } j \text{ enters node } i \\ 0 & \text{if branch } j \text{ is not incident with node } i. \end{cases}$$

Similarly, chosen an orientation in every loop, the *loop matrix* $\tilde{B}$ is defined as (b_{ij}), where

$$b_{ij} = \begin{cases} 1 & \text{if branch } j \text{ is in loop } i \text{ with the same orientation} \\ -1 & \text{if branch } j \text{ is in loop } i \text{ with the opposite orientation} \\ 0 & \text{if branch } j \text{ is not in loop } i. \end{cases}$$

The rank of this matrix equals $m-n+k$. A *reduced loop matrix* B is any $((m-n+k)\times m)$-submatrix of $\tilde{B}$ with full row rank.

We denote by B_K (resp. $B_{\mathcal{G}-K}$) the submatrix of B defined by the columns which correspond to branches belonging (resp. not belonging) to a given set of branches K; the same applies to the cutset matrix D. Certain submatrices of B and D characterize the existence of so-called K-cutsets and K-loops (that is, cutsets or loops just defined by branches belonging to K), as stated below (cf. [30, Sect. 5.1]).

Lemma 1. *Let K be a subset of branches of a given digraph $\mathcal{G}$. The set K does not contain cutsets if and only if B_K has full column rank or, equivalently, iff $D_{\mathcal{G}-K}$ has full row rank.*

Analogously, K does not contain loops if and only if D_K has full column rank or, equivalently, iff $B_{\mathcal{G}-K}$ has full row rank.

Actually, the dimensions of the spaces $\ker B_K$ and $\ker D_K$ are defined by the number of linearly independent K-cutsets and K-loops, respectively.

The proof of the following result can be found e.g. in [14, Sect. 7.4].

Lemma 2. *If the columns of the reduced loop and cutset matrices B, D of a digraph are arranged according to the same order of branches, then $BD^T = 0$, $DB^T = 0$.*

The relations $\operatorname{im} D^T = \ker B$ and $\operatorname{im} B^T = \ker D$ hold true. This expresses that the *cut space* $\operatorname{im} D^T$ spanned by the rows of D can be described as $\ker B$ and, analogously, the *cycle space* $\operatorname{im} B^T$ spanned by the rows of B equals $\ker D$ [5]. These spaces are orthogonal to each other since $(\operatorname{im} D^T)^\perp = (\ker B)^\perp = \operatorname{im} B^T$.

Finally, when applying these results to circuit analysis, we will split the columns of B and D according to the nature of the devices accommodated in the corresponding branches; B_q, B_φ, D_q, D_φ describe the submatrices of B and D defined by q- and φ-devices; these matrices will be further split into B_m, B_c, B_r, B_u, B_w, B_l, B_g, B_j (resp. D_m, D_c etc.), according to the division of q- and φ-devices into q-memristors, capacitors, current-controlled resistors and voltage sources, and φ-memristors, inductors, voltage-controlled resistors and current sources, respectively. With this notation, the identity $BD^T = 0$ in Lemma 2 can be written as

$$B_m D_m^T + B_c D_c^T + B_r D_r^T + B_u D_u^T + B_w D_w^T + B_l D_l^T + B_g D_g^T + B_j D_j^T = 0. \tag{8}$$

3.2 Nondegenerate problems and the order of complexity

The *order of complexity* or *state dimension* of an electrical circuit is the number of variables that can be freely assigned an initial value. Stemming from the work of Bashkow and Bryant [3, 7, 8], a circuit composed of capacitors, inductors, resistors and voltage and current sources is said to be *nondegenerate* if its order of complexity equals the number of reactive elements (capacitors and inductors). A necessary condition for a circuit to be nondegenerate is its *topological* nondegeneracy, that is, the absence of VC-loops (loops formed only by voltage sources and/or capacitors) and IL-cutsets (cutsets defined only by current sources and/or inductors). Different sufficient conditions can be given, involving e.g. the strict passivity of the circuit matrices or the structure of the circuit spanning trees [12, 30, 32, 34, 35].

In Theorem 1 we address the characterization of the order of complexity of circuits with fully nonlinear memristors, under strict passivity assumptions and restricting the discussion to cases without VC-loops and IL-cutsets. We show that memristors, even under a fully nonlinear assumption, do *not* introduce topological degeneracies; this means that every memristor increases by one the order of complexity, regardless of its location in the

circuit. The key difference with capacitors and inductors, which actually introduce degeneracies when entering VC-loops or IL-cutsets, is made by the fact that the characteristics of these, namely, $v_c = \eta_2(q_c, t)$ and $i_l = \zeta_2(\varphi_l, t)$, do not involve the current i_c or the voltage v_l, respectively.

Note, in this regard, that the equations $q_r' = i_r$, $q_u' = i_u$, $\varphi_g' = v_g$, $\varphi_j' = v_j$ will be excluded from the dynamical description of the circuit, since the variables q_r, q_u, φ_g, φ_j are decoupled from the rest of the system and are hence irrelevant from the dynamical point of view. This means that the circuit dynamics will be defined by the model

$$\begin{aligned} q_{mc}' &= i_{mc} && \text{(9a)}\\ \varphi_{wl}' &= v_{wl} && \text{(9b)}\\ 0 &= v_q - f(q_{mc}, i_q, t) && \text{(9c)}\\ 0 &= i_\varphi - g(\varphi_{wl}, v_\varphi, t) && \text{(9d)}\\ 0 &= B_q v_q + B_\varphi v_\varphi && \text{(9e)}\\ 0 &= D_q i_q + D_\varphi i_\varphi, && \text{(9f)} \end{aligned}$$

in the understanding that q_{mc} and φ_{wl} stand for $(q_m,\, q_c)$ and $(\varphi_w,\, \varphi_l)$, respectively. The same splitting applies to i_{mc} and v_{wl}. Notice that f and g group together the maps η_k, ζ_k $(k = 1, \ldots, 4)$ arising in Tables 1 and 2 for the sets of q- and φ-devices.

Theorem 1. *Consider a circuit without VC-loops and IL-cutsets in which the memristance, resistance, memductance and conductance matrices M, R, W, G are positive definite. Then its order of complexity is given by the total number of q- and φ-memristors, capacitors, and inductors.*

Proof. We will check that the relations (9c)-(9f) make it possible to write explicitly all the branch voltages and currents in terms of q_m, q_c, φ_w, φ_l, and that these relations impose no constraint among these variables in the absence of VC-loops and IL-cutsets. The way to do so is to check that the matrix of partial derivatives of (9c)-(9f) with respect to the branch voltages and currents v_q, i_q, v_φ, i_φ, is non-singular; a straightforward application of the implicit function theorem yields the result.

This matrix of partial derivatives has the form

$$J = \begin{pmatrix} I_q & -M_q & 0 & 0 \\ 0 & 0 & -W_\varphi & I_\varphi \\ B_q & 0 & B_\varphi & 0 \\ 0 & D_q & 0 & D_\varphi \end{pmatrix} \qquad (10)$$

with

$$M_q = \frac{\partial f}{\partial i_q}, \quad W_\varphi = \frac{\partial g}{\partial v_\varphi}.$$

Using a Schur reduction [19, 30], it is easy to see that (10) is non-singular if and only if so it is

$$J_{\text{red}} = \begin{pmatrix} B_q M_q & B_\varphi \\ D_q & D_\varphi W_\varphi \end{pmatrix}. \tag{11}$$

According to the classification of q-devices into q-memristors, capacitors, resistors and voltage sources, the matrix M_q has the block-diagonal structure block-diag$\{M, 0_c, R, 0_u\}$, where M and R are the incremental memristance and resistance matrices. Analogously, W_φ reads as block-diag$\{W, 0_l, G, 0_j\}$. This confers the matrix J_{red} in (11) the form

$$\begin{pmatrix} B_m M & 0 & B_r R & 0 & B_w & B_l & B_g & B_j \\ D_m & D_c & D_r & D_u & D_w W & 0 & D_g G & 0 \end{pmatrix}. \tag{12}$$

Assume that (12) has a non-trivial left-kernel; that is, suppose that there exists a non-vanishing $(x^T\ y^T)$ such that the following relations hold:

$$\begin{aligned} x^T B_m M + y^T D_m &= 0 && \text{(13a)} \\ y^T D_c &= 0 && \text{(13b)} \\ x^T B_r R + y^T D_r &= 0 && \text{(13c)} \\ y^T D_u &= 0 && \text{(13d)} \\ x^T B_w + y^T D_w W &= 0 && \text{(13e)} \\ x^T B_l &= 0 && \text{(13f)} \\ x^T B_g + y^T D_g G &= 0 && \text{(13g)} \\ x^T B_j &= 0. && \text{(13h)} \end{aligned}$$

Multiply the identity (8) from the left by x^T and from the right by y. Using (13b), (13d), (13f) and (13h), we get

$$x^T (B_m D_m^T + B_r D_r^T + B_w D_w^T + B_g D_g^T) y = 0.$$

This equation can be recast,using (13a), (13c), (13e) and (13g), as

$$x^T B_m M^T B_m^T x + x^T B_r R^T B_r^T x + y^T D_w W D_w^T y + y^T D_g G D_g^T y = 0. \tag{14}$$

Be aware of the fact that M^T and R^T are positive definite since so they are M and R. Together with the positive definiteness of W and G, this implies that the relations

$$\begin{aligned} x^T B_m &= 0 && \text{(15a)} \\ x^T B_r &= 0 && \text{(15b)} \\ y^T D_w &= 0 && \text{(15c)} \\ y^T D_g &= 0 && \text{(15d)} \end{aligned}$$

follow from (14). These relations yield, in turn,

$$y^T D_m = 0 \tag{16a}$$
$$y^T D_r = 0 \tag{16b}$$
$$x^T B_w = 0 \tag{16c}$$
$$x^T B_g = 0. \tag{16d}$$

Now, the identities (13f), (13h), (15a), (15b), (16c) and (16d) imply that $x = 0$, because of the absence of VC-loops and Lemma 1. Similarly, (13b), (13d), (15c), (15d), (16a) and (16b), together with Lemma 1 and the absence of IL-cutsets, yield $y = 0$. This means that (12) and so J in (10) are indeed non-singular; therefore, the implicit function theorem makes it possible to write v_q, v_φ, i_q, i_φ in terms of q_m, q_c, φ_w and φ_l, and this in turn yields an explicit ODE formulated in terms of the charges of q-memristors and capacitors and the fluxes of φ-memristors and inductors. The state dimension of this ODE is obviously defined by the number of memristors, capacitors and inductors and the proof is complete. □

Note that this result applies to fully nonlinear memristors, regardless of the actual form of the maps η_1 and ζ_1, as far as the memristance M and the memductance W are positive definite. It holds true, in particular, for Chua's memristors.

The different role played in this regard by q-memristors and capacitors, on the one hand, and by φ-memristors and inductors, on the other, becomes apparent in the light of the form of the matrix (12). Indeed, the fact that the characteristic $v_c = \eta_2(q_c, t)$ of capacitors does not involve the current i_c is responsible for the vanishing block over D_c in (12). Together with the null block over D_u, this explains the key role of VC-loops in the state dimension problem. By contrast, the presence of the M matrix within (12) makes the location of memristors irrelevant in this problem, showing that q-memristors cannot introduce topological degeneracies. In particular, VCM-loops (with at least one q-memristor) do not reduce the state dimension of the problem. The same reasoning applies to φ-memristors, inductors, IL-cutsets and ILW-cutsets.

With more technical difficulties it is possible to show, assuming the elastance of capacitors and the reluctance of inductors (or, equivalently, the capacitance and the inductance) to be positive definite, that the order of complexity of topologically degenerate circuits with fully nonlinear memristors is given by the total number of memristors plus the number of capacitors in a normal tree (that is, a tree including all voltage sources, the maximum possible number of capacitors, the minimum possible number of inductors and no current source) and the number of inductors in a normal cotree. This provides an extension of Bryant's results [7, 8] to circuits with fully nonlinear memristors.

3.3 Null eigenvalues; regular equilibrium points

Many qualitative properties of dynamical systems at equilibria can be characterized in terms of the linearized problem. In particular, zero eigenvalues of the linearization may be responsible for stability changes and bifurcation phenomena. In particular, within the context of memristive systems, some particular circuits with Chua-type memristors have been shown in the literature to display null eigenvalues [25, 31]. Below we tackle this problem for general circuits with fully nonlinear memristors, addressing Chua's memristors as a particular case with distinctive properties.

System (9) is a semiexplicit differential-algebraic equation (DAE) [6, 22, 23, 29, 30]. Equilibrium points are defined by the vanishing of its right-hand side, and the linearization at a given equilibrium leads to the *matrix pencil* [15] $\lambda H - K$, where $H = \text{block-diag}\{I, 0\}$ and K is the Jacobian matrix of the right-hand side at equilibrium. The *spectrum* of the matrix pencil is the set of values of λ which make $\lambda H - K$ singular. In particular, the pencil has null eigenvalues if and only if the Jacobian matrix K is singular.

An equilibrium point is said to be *regular* if and only if K is a non-singular matrix. Regular equilibria are important regarding DC-solvability and Newton-based computations [13]. The following result extends to systems with fully nonlinear memristors a property already known for RLC circuits [16, 17, 24]. With the same terminological convention, a VLW-loop is a loop defined by voltage sources, inductors and/or φ-memristors, and an ICM-cutset is a cutset including only current sources, capacitors and/or q-memristors.

Theorem 2. *Consider a memristive circuit with positive definite incremental resistance and conductance matrices R, G. An equilibrium point of this circuit is regular if and only if*

- *the elastances E_m, E_c of q-memristors and capacitors, as well as the reluctances $\mathcal{R}_w$, $\mathcal{R}_l$ of φ-memristors and inductors, are non-singular at the equilibrium; and*
- *the circuit does not have either VLW-loops or ICM-cutsets.*

Proof. The Jacobian matrix K reads as

$$K = \begin{pmatrix} 0 & 0 & 0 & I_{mc} & I_{wl} & 0 \\ -E_{mc} & 0 & I_q & -M_q & 0 & 0 \\ 0 & -\mathcal{R}_{wl} & 0 & 0 & -W_\varphi & I_\varphi \\ 0 & 0 & B_q & 0 & B_\varphi & 0 \\ 0 & 0 & 0 & D_q & 0 & D_\varphi \end{pmatrix} \tag{17}$$

with

$$E_{mc} = \begin{pmatrix} E_m & 0 \\ 0 & E_c \\ 0 & 0 \\ 0 & 0 \end{pmatrix}, \; \mathcal{R}_{wl} = \begin{pmatrix} \mathcal{R}_w & 0 \\ 0 & \mathcal{R}_l \\ 0 & 0 \\ 0 & 0 \end{pmatrix} \tag{18}$$

and

$$I_{mc} = \begin{pmatrix} I_m & 0 & 0 & 0 \\ 0 & I_c & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix}, \; I_{wl} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ I_w & 0 & 0 & 0 \\ 0 & I_l & 0 & 0 \end{pmatrix}.$$

It is clear that the elastances E_m, E_c and the reluctances $\mathcal{R}_w$, $\mathcal{R}_l$ must be non-singular for K to be so; if these requirements are met, the non-singularity of K relies on that of

$$\begin{pmatrix} 0 & 0 & I_r & -R & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -G & 0 & 0 & 0 & I_g \\ B_m & B_c & B_r & 0 & 0 & B_g & B_j & 0 & 0 & 0 \\ 0 & 0 & 0 & D_r & D_u & 0 & 0 & D_w & D_l & D_g \end{pmatrix}$$

and, by means of a Schur reduction, on the non-singularity of

$$K_{\text{red}} = \begin{pmatrix} B_m & B_c & B_r R & 0 & B_g & B_j & 0 & 0 \\ 0 & 0 & D_r & D_u & D_g G & 0 & D_w & D_l \end{pmatrix}. \tag{19}$$

The blocks comprising B_m, B_c, B_j show, in the light of Lemma 1, that the absence of ICM-cutsets is necessary for K_{red} to be non-singular; analogously, the blocks including D_u, D_w, D_l rule out the presence of VLW-loops. Conversely, in order to show that the absence of these configurations guarantees K_{red} to be non-singular, it suffices to check that a column-reordering gives this matrix the form of J_{red} in (11); proceeding exactly as in the proof of Theorem 1, and using only the positive definiteness of R and G, it is easy to check that in the absence of VLW-loops and ICM-cutsets the matrix K_{red} (and then K) is actually non-singular, as we aimed to show. □

More is true, actually; proceeding as in Theorem 3 below, one can show that, in problems in which the elastance of q-memristors and capacitors and the reluctance of φ-memristors and inductors are non-singular, the geometric multiplicity of the zero eigenvalue of K equals the number of independent VLW-loops and independent ICM-cutsets, where the notion of independence relies on the cut- and cycle-spaces described in subsection 3.1.

3.4 Null eigenvalues in circuits with Chua-type memristors

A distinct feature of Chua's memristors is that the elastance $E_m = \partial\eta_1/\partial q_m$ and the reluctance $\mathcal{R}_w = \partial\zeta_1/\partial\varphi_w$ do vanish at equilibrium points, because $\eta_1(q_m, i_m) = M(q_m)i_m$ and $\zeta_1(\varphi_w, v_w) = W(\varphi_w)v_w$ are linear in i_m and v_w, respectively, and the identities $i_m = 0$, $v_w = 0$ hold at equilibria. Theorem 2 above then predicts the existence of null eigenvalues in Chua-type memristive circuits owing to this zero-crossing property, as already observed in specific examples [25, 31]. The number of memristive devices actually characterizes the

geometric multiplicity of the zero eigenvalue in a broad class of circuits with Chua-type memristors, as detailed below.

Theorem 3. *Consider a circuit in which the elastance E_m of q-memristors and the reluctance $\mathcal{R}_w$ of φ-memristors do vanish at equilibria. If the resistance and conductance matrices R, G are positive definite at a given equilibrium, and the elastance E_c of capacitors and the reluctance $\mathcal{R}_l$ of inductors (equivalently, the capacitance and the inductance) are non-singular, then the geometric multiplicity of the null eigenvalue equals the number of memristors, independent VL-loops and independent IC-cutsets.*

Proof. Making $E_m = 0$ and $\mathcal{R}_w = 0$ in (18), the corank of the matrix K can be easily seen to equal the number of (q- and φ-) memristors plus the corank of

$$\begin{pmatrix} 0 & 0 & I_m & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -E_c & 0 & 0 & I_c & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & I_r & -R & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_w & 0 & 0 \\ 0 & -\mathcal{R}_l & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_l & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -G & 0 & 0 & 0 & I_g \\ 0 & 0 & B_m & B_c & B_r & 0 & 0 & B_g & B_j & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & D_r & D_u & 0 & 0 & D_w & D_l & D_g \end{pmatrix}. \tag{20}$$

The corank of (20) in turn equals that of

$$\begin{pmatrix} B_c E_c & 0 & B_r R & 0 & B_g & B_j \\ 0 & D_l \mathcal{R}_l & D_r & D_u & D_g G & 0 \end{pmatrix}. \tag{21}$$

Contrary to (19), (21) is not a square matrix, and its corank is defined by the dimension of its (right) kernel. A vector (u, v, w, x, y, z) of the kernel of this matrix verifies

$$\begin{aligned} B_c E_c u &= 0 && \text{(22a)} \\ B_r R w &= 0 && \text{(22b)} \\ B_g y &= 0 && \text{(22c)} \\ B_j z &= 0 && \text{(22d)} \\ D_l \mathcal{R}_l v &= 0 && \text{(22e)} \\ D_r w &= 0 && \text{(22f)} \\ D_u x &= 0 && \text{(22g)} \\ D_g G y &= 0. && \text{(22h)} \end{aligned}$$

The relations (22) imply that $(0, E_c u, Rw, 0, 0, 0, y, z) \in \ker (B_m\ B_c\ B_r\ B_u\ B_w\ B_l\ B_g\ B_j) = \ker B$, and $(0, 0, w, x, 0, \mathcal{R}_l v, Gy, 0) \in \ker (D_m\ D_c\ D_r\ D_u\ D_w\ D_l\ D_g\ D_j) = \ker D$. Use then

the identities $\ker B = \operatorname{im} D^T$ and $\ker D = \operatorname{im} B^T$ to derive the existence of vectors p, q satisfying

$$0 = D_m^T p,\ E_c u = D_c^T p,\ Rw = D_r^T p,\ 0 = D_u^T p,\ 0 = D_w^T p,\ 0 = D_l^T p,\ y = D_g^T p,\ z = D_j^T p,$$
$$0 = B_m^T q,\ 0 = B_c^T q,\ w = B_r^T q,\ x = B_u^T q,\ 0 = B_w^T q,\ \mathcal{R}_l v = B_l^T q,\ Gy = B_g^T q,\ 0 = B_j^T q.$$

Pre- and post-multiplying (8) by q^T and p, respectively, we get, in the light of these identities,

$$w^T R w + y^T G^T y = 0,$$

that is, $w = y = 0$ because of the positive definiteness of R and G. Then $(E_c u, z)$ belongs to $\ker (B_c\ B_j)$ and $(x, \mathcal{R}_l v)$ belongs to $\ker (D_u\ D_l)$. Due to the non-singular nature of E_c and $\mathcal{R}_l$, this means that the corank of (20) equals the number of independent IC-cutsets plus the number of independent VL-loops (cf. subsection 3.1). Hence, the corank of the matrix K, and therefore the geometric multiplicity of its null eigenvalue, equals the number of (q- and φ-) memristors plus the number of independent VL-loops and the number of independent IC-cutsets, as we aimed to show. □

In particular, in circuits without VL-loops and IC-cutsets, the geometric multiplicity of the null eigenvalue matches exactly the number of memristors; this is the case in the examples arising in [25, 31].

4 Concluding remarks

The fully nonlinear characteristics (3) and (4) introduced in the present paper might accommodate future devices arising in nonlinear circuit theory and displaying memristive effects, or provide more accurate models for already existing devices. The general form of these relations and their time-varying counterparts allows for a simple description of a very broad class of electrical and electronic circuits; different dynamical features of these can be then addressed in great generality. Several of these features can be understood to follow from the special form of the characteristic matrices of the different devices arising in the analysis. For instance, the zero-crossing property of Chua-type memristors makes them display a vanishing elastance and reluctance at equilibria; from Theorems 1 and 3, it then follows that in strictly passive circuits with Chua-type memristors, not exhibiting VC-loops, IL-cutsets, VL-loops or IC-cutsets, the order of complexity equals the number of memristors plus reactive elements, every memristor introducing a vanishing natural frequency in the linearized problem. Similarly, the absence of null eigenvalues is characterized, for general memristive circuits and in terms of the circuit matrices and the digraph topology, in Theorem 2. The characterization of other analytical properties of memristive circuits within the framework here introduced defines the scope of future research.

References

[1] B. Andrásfai, *Introductory Graph Theory,* Akadémiai Kiadó, Budapest, 1977.

[2] B. Andrásfai, *Graph Theory: Flows, Matrices,* Adam Hilger, 1991.

[3] T. R. Bashkow, The A matrix, new network description, *IRE Trans. Circuit Theory* **4** (1957) 117-119.

[4] S. Benderli and T. A. Wey, On SPICE macromodelling of TiO_2 memristors, *Electronic Letters* **45** (2009) 377-379.

[5] B. Bollobás, *Modern Graph Theory*, Springer-Verlag, 1998.

[6] K. E. Brenan, S. L. Campbell and L. R. Petzold, *Numerical Solution of Initial-Value Problems in Differential-Algebraic Equations*, SIAM, 1996.

[7] P. R. Bryant, The order of complexity of electrical networks, *Proceedings of the IEE, Part C* **106** (1959) 174-188.

[8] P. R. Bryant, The explicit form of Bashkow's A matrix, *IRE Trans. Circuit Theory* **9** (1962) 303-306.

[9] X. Chen, G. Wu and D. Bao, Resistive switching behavior of $Pt/Mg_{0.2}Zn_{0.8}O/Pt$ devices for nonvolatile memory applications, *Appl. Phys. Lett.* **93** (2008) 093501.

[10] L. O. Chua, Memristor – The missing circuit element, *IEEE Trans. Circuit Theory* **18** (1971) 507-519.

[11] L. O. Chua and S. M. Kang, Memristive devices and systems, *Proc. IEEE* **64** (1976) 209-223.

[12] A. Encinas and R. Riaza, Tree-based characterization of low index circuit configurations without passivity restrictions, *Internat. J. Circuit Theory Appl.* **36** (2008) 135-160.

[13] D. Estévez-Schwarz and U. Feldmann, Actual problems of circuit simulation in industry, in *Modeling, Simulation, and Optimization of Integrated Circuits* (Oberwolfach, 2001), *Int. Ser. Numer. Math.* **146** (2003) 83-99.

[14] L. R. Foulds, *Graph Theory Applications*, Springer, 1992.

[15] F. R. Gantmacher, *The Theory of Matrices,* vols. 1 & 2, Chelsea, 1959.

[16] B. C. Haggman and P. R. Bryant, Geometric properties of nonlinear networks containing capacitor-only cutsets and/or inductor-only loops. Part I: Conservation laws, *Cir. Sys. Signal Process.* **5** (1986) 279-319.

[17] B. C. Haggman and P. R. Bryant, Geometric properties of nonlinear networks containing capacitor-only cutsets and/or inductor-only loops. Part II: Symmetries, *Cir. Sys. Signal Process.* **5** (1986) 435-448.

[18] E. Hairer and G. Wanner, *Solving Ordinary Differential Equations II: Stiff and Differential-Algebraic Problems*, Springer-Verlag, 1996.

[19] R. A. Horn and Ch. R. Johnson, *Matrix Analysis,* Cambridge Univ. Press, 1985.

[20] M. Itoh and L. O. Chua, Memristor oscillators, *Intl. J. Bifurcation and Chaos* **18** (2008) 3183-3206.

[21] M. Itoh and L. O. Chua, Memristor cellular automata and memristor discrete-time cellular neural networks, *Intl. J. Bifurcation and Chaos* **19** (2009) 3605-3656.

[22] P. Kunkel and V. Mehrmann, *Differential-Algebraic Equations. Analysis and Numerical Solution*, EMS, 2006.

[23] R. März, Differential algebraic equations anew, *Appl. Numer. Math.* **42** (2002) 315-335.

[24] T. Matsumoto, L. O. Chua and A. Makino, On the implications of capacitor-only cutsets and inductor-only loops in nonlinear networks, *IEEE Trans. Circuits and Systems* **26** (1979) 828-845.

[25] M. Messias, C. Nespoli and V. A. Botta, Hopf bifurcation from lines of equilibria without parameters in memristors oscillators, *Intl. J. Bifurcation and Chaos* **20** (2010) 437-450.

[26] B. Muthuswamy, Implementing memristor based chaotic circuits, *Intl. J. Bifurcation and Chaos* **20** (2010) 1335-1350.

[27] B. Muthuswamy and P. P. Kokate, Memristor-based chaotic circuits, *IETE Tech. Rev.* **26** (2009) 417-429.

[28] Y. V. Pershin and M. Di Ventra, Spin memristive systems: Spin memory effects in semiconductor spintronics, *Physical Review B* **78** (2008) 113309.

[29] P. J. Rabier and W. C. Rheinboldt, Theoretical and numerical analysis of differential-algebraic equations, *Handbook of Numerical Analysis* Vol. VIII, 183-540, North-Holland (2002).

[30] R. Riaza, *Differential-Algebraic Systems. Analytical Aspects and Circuit Applications*, World Scientific, 2008.

[31] R. Riaza, State-space description of memristive systems, preprint, 2010.

[32] R. Riaza and A. Encinas, Augmented nodal matrices and normal trees, *Discrete Appl. Math.* **158** (2010) 44-61.

[33] R. Riaza and C. Tischendorf, Semistate models of electrical circuits including memristors, *Internat. J. Circuit Theory Appl.*, accepted, in press, 2010.

[34] A. M. Sommariva, State-space equations of regular and strictly topologically degenerate linear lumped time-invariant networks: the multiport method, *Internat. J. Circuit Theory Appl.* **29** (2001) 435-453.

[35] A. M. Sommariva, State-space equations of regular and strictly topologically degenerate linear lumped time-invariant networks: the implicit tree-tableau method, *IEEE Proceedings Circuits and Systems* **8** (2001) 1139-1141.

[36] G. S. Snider, Spike-timing-dependent learning in memristive nanodevices, *Proc. IEEE Intl. Symp. Nanoscale Architectures 2008*, pp. 85-92.

[37] D. B. Strukov, G. S. Snider, D. R. Stewart and R. S. Williams, The missing memristor found, *Nature* **453** (2008) 80-83.

[38] X. Wang, Y. Chen, H. Xi, H. Li and D. Dimitrov, Spintronic memristor through spin-torque-induced magnetization motion, *IEEE Electron Device Letters* **30** (2009) 294-297.

[39] J. Wu and R. L. McCreery, Solid-state electrochemistry in molecule/TiO_2 molecular heterojunctions as the basis of the TiO_2 memristor, *Journal of the Electrochemical Society* **156** (2009) 29-37.

[40] J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart and R. S. Williams, Memristive switching mechanism for metal/oxide/metal nanodevices, *Nature Nanotechnology* **3** (2008) 429-433.