System-on-Chip monitoring networks targeting nanometer technologies

CMOS Emerging Technologies

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POLITÉCNICA

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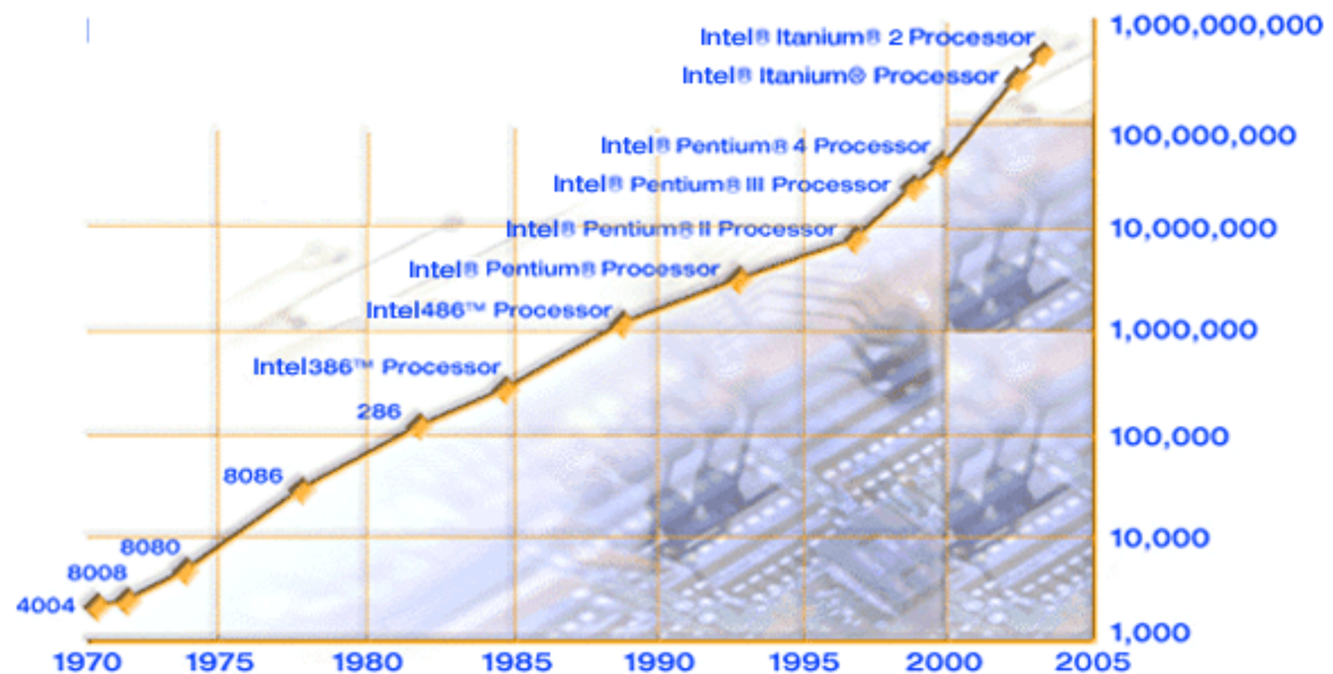
Outline

- Introduction
- Monitors taxonomy
- Other approaches
- Proposal
- Conclusions

Introduction

- Millions of transistors in a single die allow the implementation of very complex architectures:
  - SoC, MPSoC, NoC, Multi-core processors



Source: http://www.intel.com/research/silicon/mooreslaw.htm

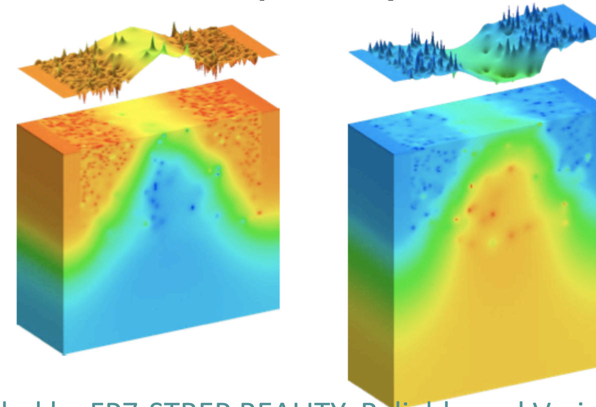
However…

Aggressive technology scaling comes at the cost of significant yield reduction

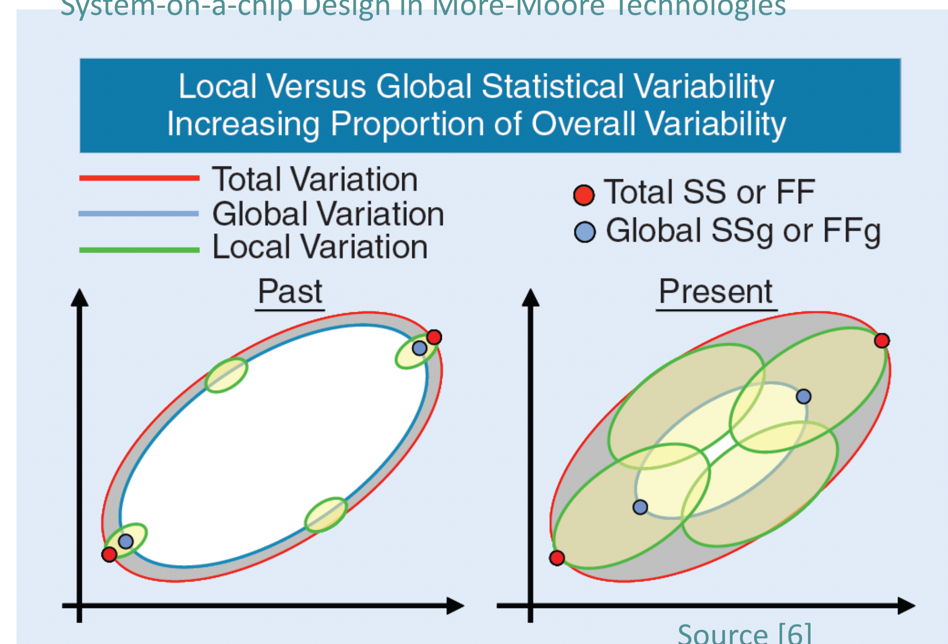
- Increased process variations
  - Variability-aware design becomes a must
- Tackling with higher power densities
  - Hot-spots mitigation through DTM
- Worse aging behavior
  - DFR

Process variations

- Within-die variations make the design of reliable complex systems more complicated
  - Line edge roughness
  - Interface roughness
  - Random discrete dopants
  - Gate tunneling…
- Effects
  - Critical path variations
  - Static power
  - VT variations
  - Yield,
  - Noise robustness
- Solutions
  - Variations-aware design
  - Design For Manufacturability
  - Critical path monitoring
  - Calibration



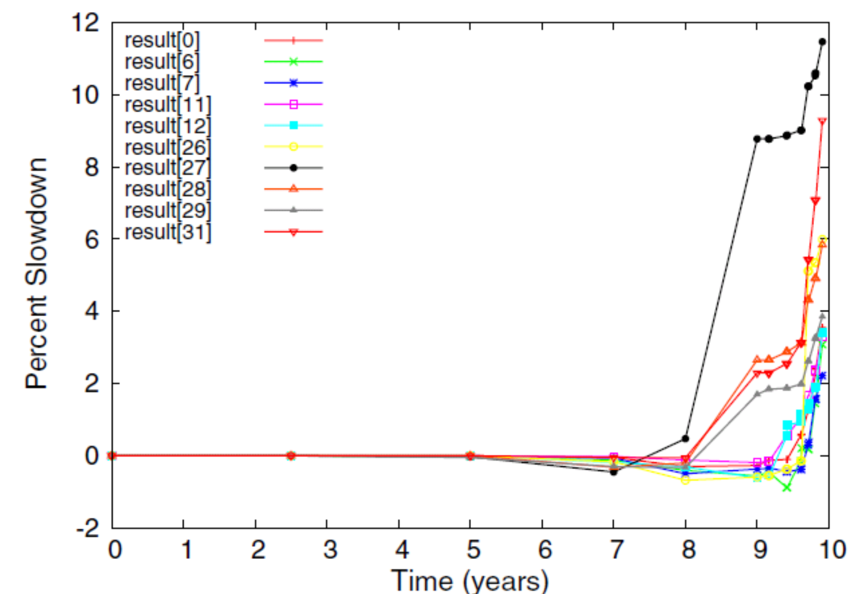
Funded by FP7-STREP REALITY: Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies



Aging

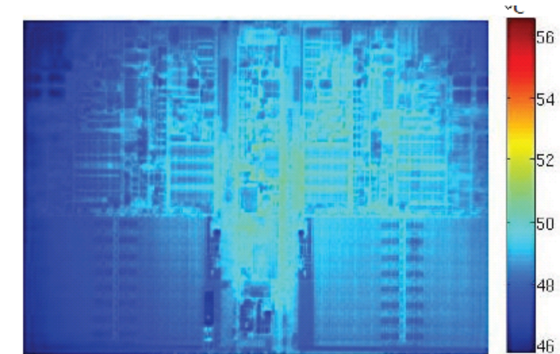
- Aging causes
  - NBTI: negative-bias temperature instability
  - TDDB: time-dependent dielectric breakdown
  - Electromigration
- Aging effects
  - Critical path delay
  - Leakage power increase
  - Failures (reduced reliability)
- Aging-aware design
  - Autonomous computing
  - Dynamic Reliability Management, DRM

Source [9] Blome, J., Feng, S., Gupta, S., and Mahlke, S. Self-calibrating Online Wearout Detection. 2007 Intl. Symposium on Microarchitecture

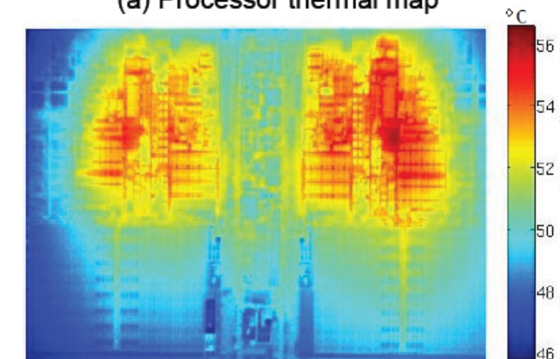


Temperature issues

- Spatial and time distributed hotspots
- Adverse effects
  - NBTI, TDDB, increased leakage, reliability, mechanical strains
- Thermal-aware design
  - Cooling
  - Temperature sensing and monitoring
  - Dynamic Thermal Management (DTM)
    - DVFS schemes
    - Workload management



(a) Processor thermal map



(c) Processor thermal map

A. N. Nowroz R. Cochran and S. Red., Thermal Monitoring of Real Processors: Techniques for Sensor Allocation and Full Characterization. DAC 2010

On-chip monitoring and calibrating network

- After fabrication, all techniques conceived to mitigate these adverse effects require
  - In-situ monitors
    - Sensors are more reliable
  - Ultra light-weight interconnection infrastructure
    - Reduced area, power overhead
    - Transparent to the designer
    - Multi-purpose
      - Monitoring and calibrating functions
      - Targeting all previous needs

Required monitors

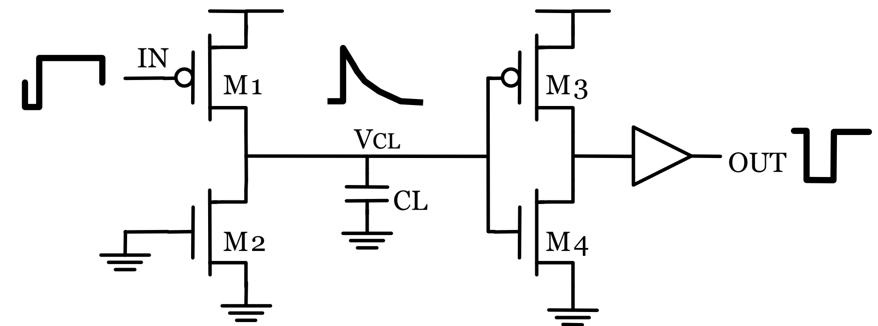
- Very reduced area and power
- Digital output
- Linear response
- Simple interface
- Transparent
- Easy to integrate in CMOS

Temperature monitors

- Efficiently allocated in the silicon to detect hotspots
- Low self-heating especially important
- Range: depends on the application.
  - For example, intel i5 20-111ºC
- Accuracy: 1 ºC
- Resolves in the order of milliseconds
- Spatial constant: 1 mm

Example of Temperature Sensor

- Based on the thermal dependence of the leakage currents
- Time to digital
- Digital interface with a logarithmic counter
  - 0.35 um AMS Technology
  - 10250 nm2
  - 1.05-65.5 nW at 5 samples/s
  - Resolution 0.28ºC
  - Maximum error (3σ) = ±1.97ºC



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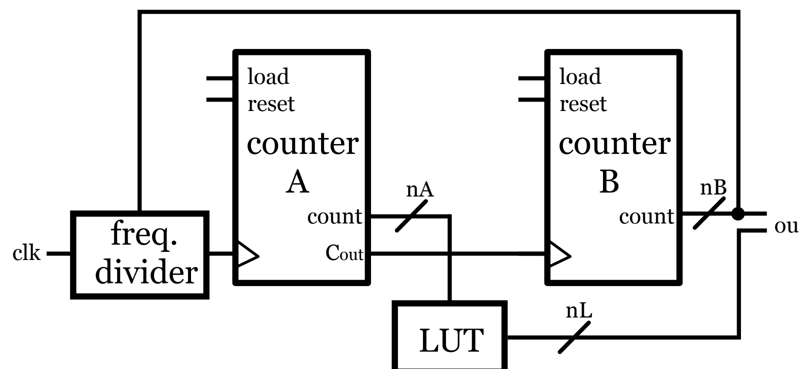
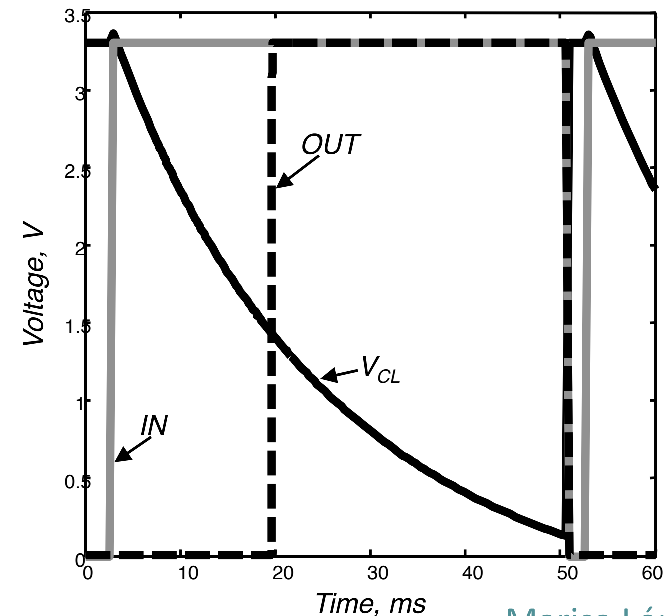
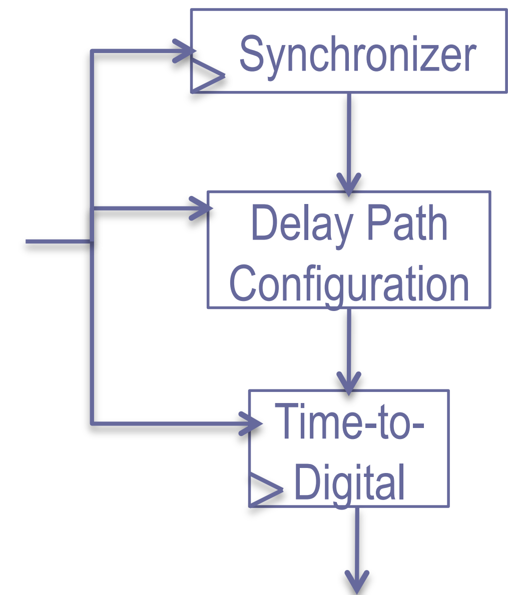




Critical path monitors

- Provide real- time performance information based upon the variation of the delay in a path
- Time to digital conversion
- Output provided to DVFS techniques
- Range-Accuracy:
  - F.i. 25 mV AC and 10 mV DC (65nm)
- Time period: depends on the application.
  - From 1/clk to 1/Mclk
  - Slow monitors record worst/average delay
- Quantization: few bits
- Spatial distribution: up to hundreds



Supply voltage monitors

- Power supply behind safety threshold can be due to
  - Resistive path
  - High instant current
- Monitors avoid unreliable operation of the chip
- Time constant: short
  - Quick actions are demanded
- Range-accuracy: 10-20 mV
- Spatial distribution: only close to the circuits that demand higher currents

Aging monitors

- Digitally quantify reliability/performance/power degradation due to aging
  - TDDB, NBTI, hot-carrier effect…
- Most of them based on critical path monitors
- Quantization: few bits
- Time period: large
- Spatial distribution: up to thousands

Monitors Taxonomy Summary

Magnitude	Time Period	Density	Quantization needs
Temperature	Milliseconds	Hundreds/chip	≈ 8 bits
Critical path	Microseconds	Hundreds/chip	≈ 7 bits
Supply voltage	Nanoseconds	Few/chip	≈ 6 bits
Aging	Long	Thousands/chip	≈ 4 bits

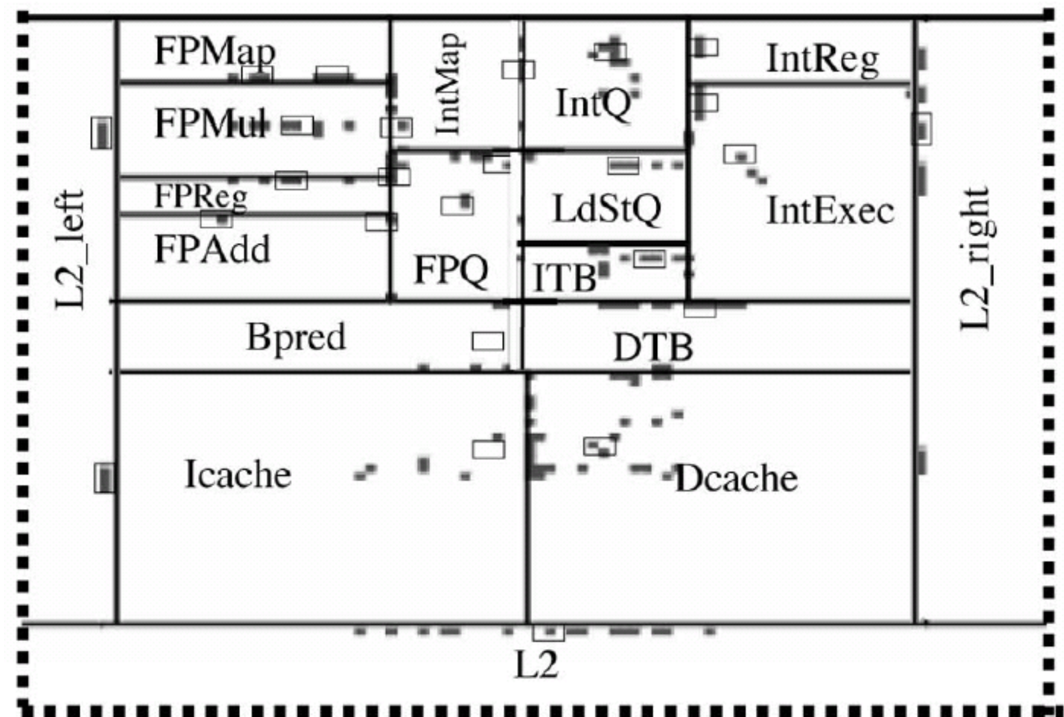
Network justification

- Current complex designs may need up to thousand sensors for monitoring
- Flexibility to deal with
  - Calibration and monitoring
  - Different monitors
- No previous design of a common infrastructure
  - Only for thermal monitoring
- But a clear need is shown in the literature

System using temperature monitors

Previous works study the number and allocation of temperature sensors for DTM

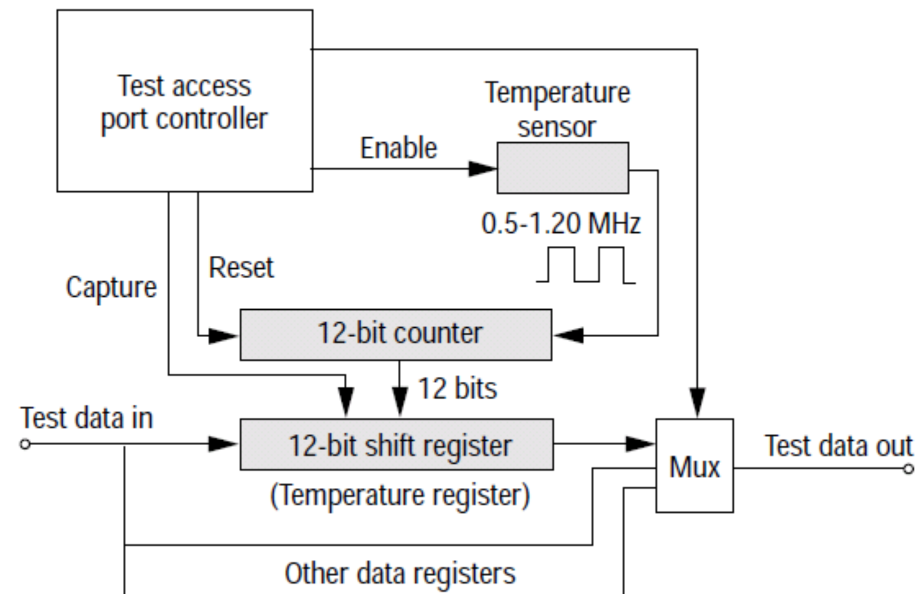
No information on the way they are connected is provided



Memik, S.O., Mukherjee, R., Min Ni, Jieyi Long, "Optimizing Thermal Sensor Allocation for Microprocessors," *IEEE Trans. on CAD of Integrated Circuits and Systems,*, vol.27, no.3, pp. 516-527, March 2008

System using temperature monitors: previous approaches

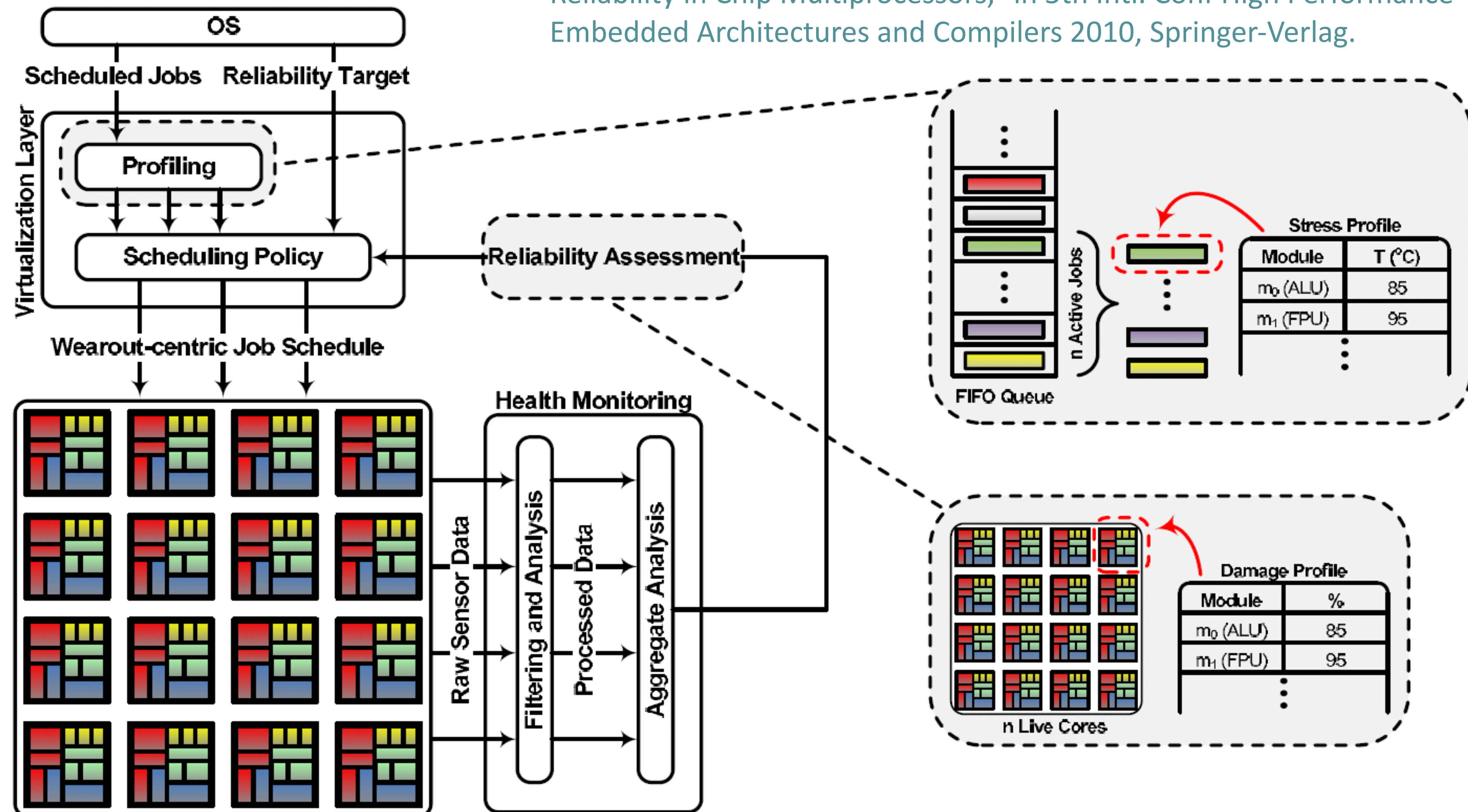
- Evolution:
  - From a single sensor per die to hundreds
- Previous approaches
  - Boundary-scan like



Szekely, V.; Rencz, M.; Courtois, B.; , "Tracing the thermal behavior of ICs," *Design & Test of Computers, IEEE* , vol.15, no.2, pp.14-21, Apr-Jun 1998

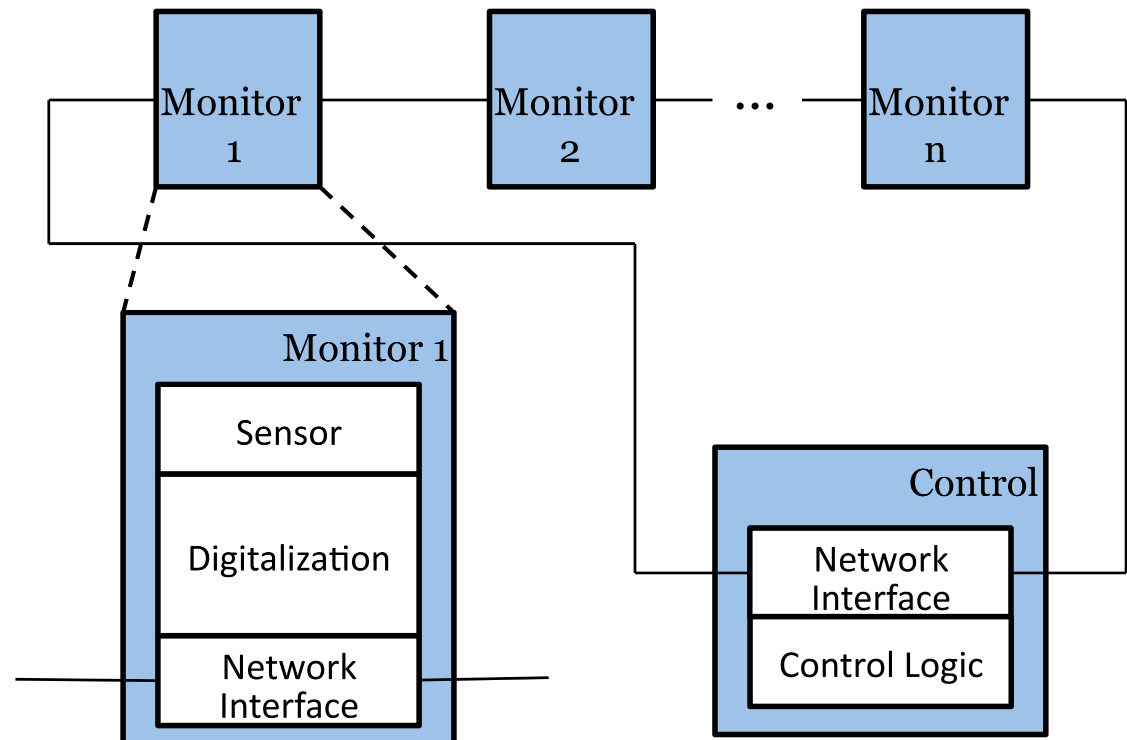
Maestro: reliability-aware system

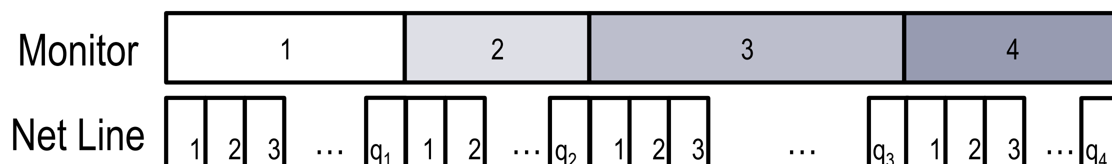
S. Feng, S. Gupta, A. Ansari, and S. Mahlke, “Maestro: Orchestrating Lifetime Reliability in Chip Multiprocessors,” in 5th Intl. Conf High Performance Embedded Architectures and Compilers 2010, Springer-Verlag.



Previous approaches

- Only targeting temperature sensors for DTM
- Boundary scan-like
- Replicated digitalization stage





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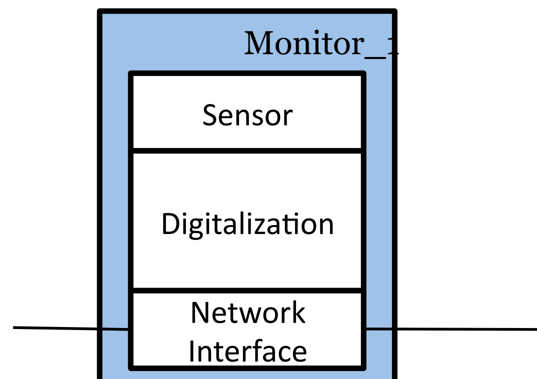
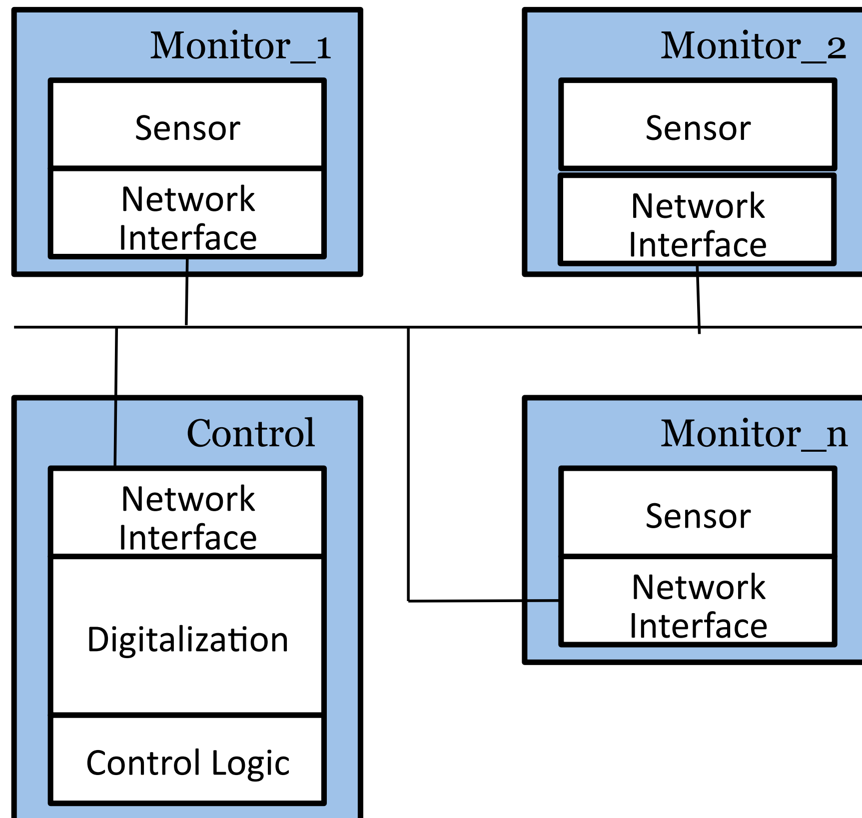
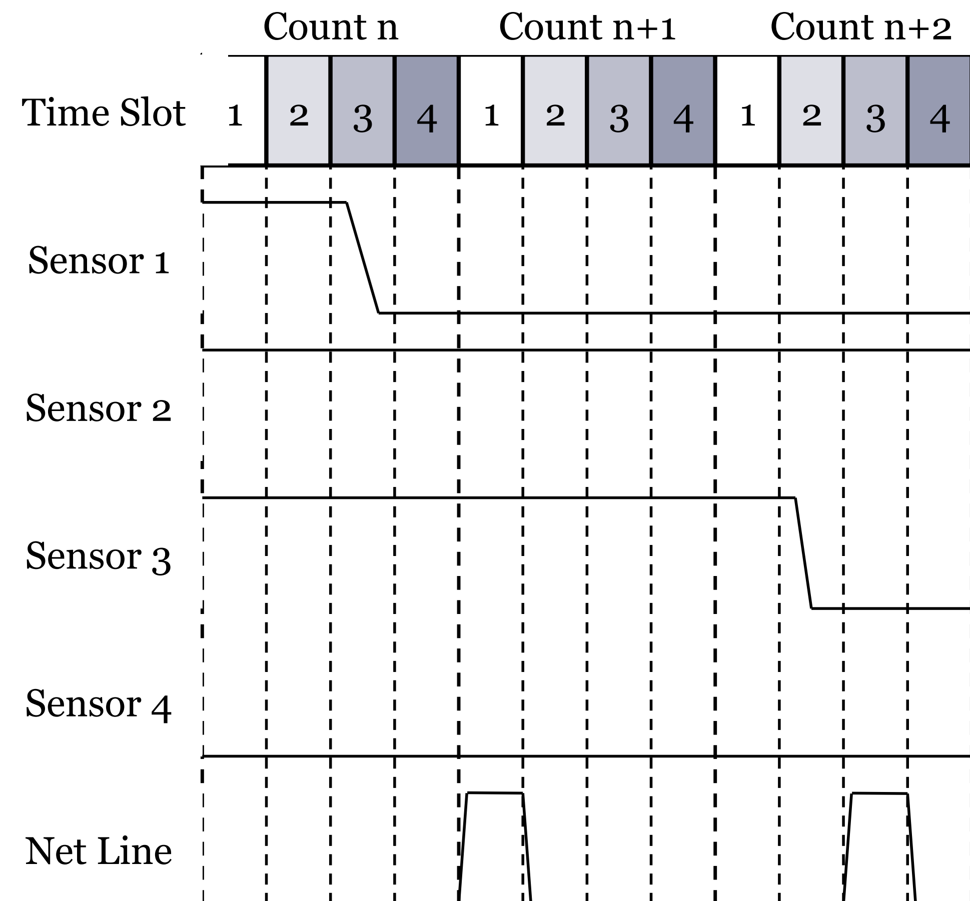
Our proposal

- Ultra light-weight network
  - Simplicity is the key to succes
- Constrained to:
  - Monitors with time-to-digital conversion
  - Common interface
- Shared digitalization for all monitors
- Time-multiplexing scheme to improve performance



Monitoring network





Comparison

- 32 monitor network
- 90 nm UMC Library
- Area savings: 25% each monitor + 16% net
- Power savings: 16%

	Area			Power		
Architecture	Single monitor	Control	Net	Single monitor	Control	Net
Boundary-ScanLike	504	9140	25227	1.39	20.50	61.85
Digital Resource Sharing	374	9294	21207	1.02	21.33	52.00

Conclusions

- Current nanometer technologies allow the integration of million of transistors at the cost of
  - Increased power densities
  - Lower reliability
- Designers should take care of all adverse effects
  - DFM, DTM, DPM
- Need of a common infrastructure for monitoring and callibrating the increased amount of sensors required by nowadays circuits
- Proposed network
  - Digitalization sharing, time multiplexing based
  - Common interface
  - Low area and power overhead
  - Scalability, flexibility

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