Selection of the appropriate winding setup in planar inductors with parallel windings

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Abstract.-. The use of parallel windings in high frequency planar inductors is a common practice. Since the planar technology, commonly PCB layers, limits the maximum layer thickness, the use of parallel windings is usually required in order to reduce the current density and losses. The distribution of the current through each parallel winding depends on the winding positioning and the frequency effects. This effect is especially important in gapped inductors, because the energy stored in the gap region determines the current distribution through the windings. Therefore, the winding positioning is a critical task in order to obtain a balanced current distribution through all the parallel windings.

This work presents a methodology that can be applied for determining the appropriate winding positioning in order to obtain a balanced current distribution through the parallel windings. This methodology allows reducing both, the power loss and the temperature in the magnetic component.

The results of the proposed methodology are presented using several examples.

I. INTRODUCTION

Paralleling devices is a well known approach to reduce losses and/or current stresses in power electronics. Current unbalance is a persistent issue, whereas the sharing mechanism is known in diodes and transistors, it is not that evident among the paralleled windings of a high-frequency inductor.

In fact, it is a very real problem because many planar components today are designed and manufactured using parallel turns in order to reduce the resistance of the winding. There are some works where the analysis of these components design is covered [1-3]. However, the goal of this paper is to describe the problem of designing planar inductors with parallel windings and to provide a methodology to select the appropriate winding setup in order to optimize the current sharing.

II. DESCRIPTION OF THE PROBLEM

Figure 1 illustrates the problem in the case of a planar inductor with gap. Figure 1(a) shows the section of the inductor where

the core and the winding layers are shown. There are two windings connected in parallel (the yellow and red ones).





Figure 1. (a) Inductor section. Red and yellow windings (5 turns each) are connected in parallel. (b) Current distribution at 50 Hz. (c) Current distribution at 1 MHz.

A gapped EI core has been used in this case. The EI core shape is a common shape used in planar components because of its low profile. Since the El cores are composed by an 'E' and an 'I' core parts, the gap in this kind of cores is placed at the upper part of the central leg of the core. Therefore, there is a no symmetrical distribution of the two windings with respect the position of the gap. This means that one of the parallel windings (the yellow one in this case) is placed closer to the gap than the other one (the red one). Beyond a particular frequency, this asymmetrical distribution of the currents. At low frequency, i.e. 50 Hz, the current through each parallel winding is almost the same (Figure 1(b)). However, at 1 MHz, there is a significant difference on both, the magnitude and the phase (Figure 1(c)).

Therefore, this parallel connection of the windings is not working on the sense of reducing the resistance. Additionally, this effect is frequency dependent. Therefore, it is necessary to establish a procedure to determine the appropriate winding setup in order to create a balanced distribution of the currents through the parallel windings. This paper presents a proposal in order to solve this problem. Although the effect is illustrated with an EI shape, the same effect appears in other shapes like the EE, where the gap is placed at the central part of the core legs.

III. PHYSICAL REASON FOR THE CURRENT UNBALANCE

Electric current produces ohmic losses (energy losses), and magnetic fields (energy storage). Current always flows through the lower impedance path. The lower impedance path is that one that produces minimum voltage drop (R i + L di/dt). This means, minimum loss and minimum variation of energy. Both effects are frequency dependent. In DC circuits, there is not variation of energy (frequency is null), and therefore current flows according to the DC resistance of the possible alternative paths (or differential cross sections of a single conductor). In AC circuits, there are ohmic losses and additionally energy (magnetic field) variation of the system. Therefore current flows so that the energy variation and power losses are minimized. According to the Ampere's law, the smaller is the area for the current flowing; the lower will be the energy. There is an optimum current distribution which optimizes these two opposite effects at each frequency. This effect is stronger as frequency increases, because there is energy variation at a higher rate and its effect becomes greater than the ohmic voltage drop.

In inductors with air gap, most of the energy is stored at the gap region (inside and around it). There is also energy in the rest of the area between the conductors (current carriers) and the gap (according to the Ampere's law). At high frequency, as explained above, the effect of the energy variation becomes predominant. The current distribution will be the one that reduces the energy; reducing the area where the energy is stored. Therefore, the current will flow as close as possible to the gap, increasing the ohmic losses. If two windings are connected in parallel and one of them is placed closer to the gap, the current will flow primarily through that winding beyond a particular frequency. The way to solve this problem is trying to distribute the parallel windings symmetrically with respect the gap. This can be done applying interleaving. However, the optimal layer distribution (optimal interleaving application) is not easy to determine without a theoretical basis as will be illustrated in the following section. This paper presents a proposal to determine the optimal layer distribution.

IV. DESIGN CONSIDERATIONS

a. General recommendations

Two simple rules of thumb can be applied to obtain reasonable results:

- Select the track width smaller than the skin depth for the current harmonic under consideration (normally the switching frequency of the power converter)
- Place parallel windings in "symmetrical" positions: they all have to be subjected to the same flux and field distribution around them, whichever it be. That is, each parallel winding should occupy an equivalent position with respect to the source of magnetic field or energy storage (in inductors, the gap).

b. Proposed procedure to determine the optimal winding distribution

The steps that should be followed to apply the proposed method are as follows:

Step 1:

It is needed to design the planar inductor in terms of selection of the core size and material, the number of turns and number of parallel layers of the winding, and the gap. As an example, the electric connections of the winding of an inductor are represented in Figure 2(a).

The layers numbered from 1 to 4 represent the layers of a PCB and all have the same structure to allow the maximum number of series and parallel combinations of layers. Winding A is made connecting in series layers 1 and 2. Winding B is made connecting in series layers 3 and 4. Finally, windings A and B are connected in parallel to build the complete inductor winding.

For this low number of layers, only 3 different winding configurations are possible. In other examples with a high number of layers, much more winding layouts can be evaluated.

Step 2:

Assume that all the layers are disconnected in order to obtain their self and mutual complex impedances. Since the current distribution depends on the gap effect, the impedance calculation method should consider this effect. Layers close to the gaps have high induced losses due to the proximity to the gap, while the effect on further layers is smaller. A high working frequency increases the effect. A Finite Element analysis tool is used in this work to evaluate these effects [4], but other methods are valid. Figure 2(b) represents the inductor of Figure 2(a) with the layers disconnected. As it can be seen, the inductor has become a set of 4 coupled inductors (self impedances are \underline{Z}_{I} , \underline{Z}_{2} , \underline{Z}_{3} , and \underline{Z}_{4} and mutual impedances are \underline{Z}_{12} , \underline{Z}_{13} , \underline{Z}_{14} , \underline{Z}_{23} , \underline{Z}_{24} , and \underline{Z}_{34}).



Figure 2. Example winding layout, unconnected layers of the example, and individual parallel windings.

It must be remarked that the finite element analysis tool (or any other selected method to calculate the impedance value) is used only once for the calculation of the self and mutual layer impedances. Once these impedances are known, finite element analysis is not necessary again, because the same impedances are used during the whole optimization process. Therefore, the optimization procedure is very fast: a great number of layers connections can be evaluated in very short time to obtain the optimal solution.

Using these self and mutual layer impedances, the self and mutual impedances of the parallel windings that form the inductor can be obtained. For the example represented in Figure 2(a), self impedances \underline{Z}_4 and \underline{Z}_B and mutual impedance \underline{Z}_{AB} of the windings in Figure 2(a) are calculated using the classical theory of coupled inductances represented in equations (1-3):

$$\underline{Z}_{\mathcal{A}} = \underline{Z}_{l} + \underline{Z}_{2} + 2\,\underline{Z}_{l2} \tag{1}$$

$$\underline{Z}_{B} = \underline{Z}_{3} + \underline{Z}_{4} + 2 \, \underline{Z}_{34} \tag{2}$$

$$\underline{Z}_{AB} = \underline{Z}_{13} + \underline{Z}_{14} + \underline{Z}_{23} + \underline{Z}_{24}$$
(3)

Note that the impedances for any possible connection of layers can be calculated using analogous equations.

Once the model of the parallel windings has been obtained, the condition for equal current share is derived. To do this, the equations of the parallel windings are written. For the example, using the references in Figure 2(c), equations (4-5) are obtained.

$$\left(\underline{U}_{A};\underline{U}_{B}\right) = \left(\underline{U};\underline{U}\right) = \left(\underline{Z}_{4};\underline{Z}_{AB};\underline{Z}_{AB};\underline{Z}_{B}\right)\left(\underline{I}_{4};\underline{I}_{B}\right) (4)$$

$$\left(\underline{I}_{4};\underline{I}_{B}\right) = \left(\underline{Z}_{4};\underline{Z}_{AB};\underline{Z}_{AB};\underline{Z}_{B}\right)^{-1}; \left(\underline{U};\underline{U}\right) =$$

$$= \left(\underline{Y}_{4};\underline{Y}_{AB};\underline{Y}_{AB};\underline{Y}_{B}\right)\left(\underline{U};\underline{U}\right) =$$

$$\left(\underline{Y}_{4}+\underline{Y}_{AB},\underline{U};(\underline{Y}_{AB}+\underline{Y}_{B})\underline{U}\right) = \left(\underline{Y}_{eqd};\underline{Y}_{eqB},\underline{U}\right) (4)$$
(5)

 \underline{U}_{4} and \underline{U}_{B} are the parallel winding voltages (equal to \underline{U} because both windings are connected in parallel) and \underline{I}_{4} and \underline{I}_{B} are their currents. In the 2 winding example, a perfect current share is obtained if equation (6) is verified.

$$\underline{Y}_{\mathcal{A}} + \underline{Y}_{\mathcal{A}\mathcal{B}} = \underline{Y}_{\mathcal{A}\mathcal{B}} + \underline{Y}_{\mathcal{B}}$$
(6)

For a two windings case, equation (6) is simplified as $\underline{Y}_4 = \underline{Y}_B$. If more than two windings are connected in parallel, similar conditions can be obtained. In any case, there are N sums of impedances which should have the same value to get an optimal current share (N is the number of windings in parallel). If the sums are not equal, current share becomes unbalanced.

Step 3:

The final step of the optimization process consist in selecting different layers connections, like Figure 2(a), and verifying (6) (or its equivalent for another number of parallel windings). The layer connection which matches the equation with the best accuracy is the optimal solution. As mismatch increases, imbalance in currents gets higher. Note that the FEA process is run only once for the impedance generation; the rest of calculations are based on analytical expressions.

This methodology is adequate to optimize using different criteria. For example, taking into account that the inductor power losses are calculated using (7).

$$P_{I} = \underline{U}_{A} \underline{I}_{A}^{*} + \underline{U}_{B} \underline{I}_{B}^{*} = \underline{U} (\underline{I}_{A} + \underline{I}_{B})^{*} =$$
$$= (G_{A} + 2 G_{AB} + G_{B}) U^{2}$$
(7)

Where a conductance G represents the real part of its corresponding admittance \underline{Y} and U is the RMS values of voltage \underline{U} . The minimum losses design is that with the lowest value of $G_{eg} = G_A + 2G_{AB} + G_B$.

V. EXAMPLES

The proposed methodology was used to design some magnetic components. Some results are presented here.

a. Example 1

An inductor for a full-bridge SMPS switching at 100 kHz was designed. Core shape is EI 32/6/20, core material is Ferroxcube 3C92, gap is 0.52 mm, and there are two parallel windings, A and B, with 5 turns each (each turn fills one layer).





Figure 3. Non-interleaved layout and currents in the parallel windings.

As the core halves are different, an 'E' and an 'I', the core gap cannot be placed in the middle of the central column. It is placed at the upper part of the central leg, as shown in Figure 3(a). As commented in section II, it has an important effect in the current sharing of the parallel windings: turns close to the gap suffer the effect of the fringing flux of the gap.

Figure 3(b) shows a representation of the windings of Figure 3(a).

Winding A (black) is composed of layers 1 to 5 connected in series and winding B (white), of layers 6 to 10. A current of 1 A has been injected in the inductor. Theoretically, 500 mA should flow through each parallel winding. However, the transient representation of currents in the parallel windings at 200 kHz, represented in Figure 3(c), shows a bad current sharing: not only the amplitudes of the currents are different, but also phases are opposite. Almost all the current circulates across the parallel winding which is closest to the gap. Note that adding both currents produce a sinusoid of 1 A peak value: that is the total injected current.

Figure 4 shows a full interleaving of the layers and the corresponding currents in the windings. Winding A is composed of layers 1-3-5-7-9 and winding B, of layers 2-4-6-8-10.



Figure 4. Fully-interleaved layout and currents in the parallel windings.

Since the gap is placed at the upper part of the central leg, this configuration is not providing a symmetrical distribution of both windings with respect to the gap. Therefore, a fully interleaved solution is not the optimal one for this case. Although the situation has been improved with respect to the previous case, it can be seen in Figure 4 that there is still an unbalance current distribution with this solution.

Figure 5 shows the layout optimized using the proposed methodology based on equations (5-6).



Figure 5. Optimal layout and currents in the parallel windings.

Winding A is composed of layers 1-4-6-7-9 and winding B, of layers 2-3-5-8-10. The waveforms shown in Figure 5 illustrate that both currents are equal.

The values of the winding admittances in (6), which are used to select the best designs in (6), take the following values:

$$\underline{Y}_{eqA} = 44.30 \sqcup -89.6^{\circ} \text{ mS}$$

 $\underline{Y}_{eqB} = 44.17 \sqcup -88.9^{\circ} \text{ mS}$

Their similar values produce the in phase currents which appear in Figure 5. The inductor equivalent admittance and impedance are:

$$\underline{Y}_{eq} = 1.09 - j 88.46 \text{ mS}$$

$$\underline{Z}_{eq} = 0.14 + j 11.30 \Omega$$

The minimum losses design gives an almost equal result. Winding A layers are 1-3-7-8-9, and winding B layers are 2-4-5-6-10. Now:

b. Example 2

The gap of the previous example was divided by two and placed in the inner and outer columns of the core, as can be seen in Figure 6.



Figure 6. Core section of example 2. Gap divided at both core legs.

For the equal current sharing condition, winding A layers are 1-3-7-8-9 and winding B layers are 2-4-5-6-10. The admittances and impedances take the following values:

 \underline{Y}_{eq4} = 39.04 ∟ -87.1° mS \underline{Y}_{eqB} = 38.09 ∟ -92.5° mS \underline{Y}_{eq} = 0.35 - j 77.04 mS \underline{Z}_{eq} = 0.06 + j 12.98 Ω

For the minimum losses design condition, winding A and B layers are 1-4-6-7-9 and 2-3-5-8-10 respectively. The admittances and impedances are:

Note that layer connections are almost the same in both examples. The admittances and impedances are quite different due to the reduced fringing flux from the gap.

c. Example 3

This is an inductor for a push-pull SMPS which switches at 100 kHz. There are 5 parallel windings and the PCB has 10 layers with a turn in each one. Therefore, each parallel winding has two turns in series.

There core shape is EI 22/6/16, the material is Ferroxcube 3C96 and the gap length is 0.27 for the inner and outer gaps. The cross section is shown in Figure 7.



Figure 7. Core section of example 3.

For the equal current share, windings A, B, C, D, and E layers are 1-10, 3-9, 6-7, 4-5, and 2-8 respectively. The admittances are:

$$\underline{Y}_{eqA} = 541.69 \sqcup -63.1^{\circ} \text{ mS}$$

$$\underline{Y}_{eqB} = 386.72 \sqcup -176.8^{\circ} \text{ mS}$$

$$\underline{Y}_{eqC} = 462.84 \sqcup 126.9^{\circ} \text{ mS}$$

$$\underline{Y}_{eqD} = 375.51 \sqcup -60.4^{\circ} \text{ mS}$$

$$\underline{Y}_{eqE} = 396.61 \sqcup -52.4^{\circ} \text{ mS}$$

$$\underline{Y}_{eq} = 7.47 \text{ - j } 775.99 \text{ mS}$$

$$\underline{Z}_{eq} = 0.012 \text{ + j } 1.29 \Omega$$

For the minimum losses design, the layers of windings A, B, C, D, and E are 1-10, 4-7, 2-9, 5-6, and 3-8 respectively.

$$\underline{Y}_{eqA} = 517.98 \sqcup -63.9^{\circ} \text{ mS}$$

$$\underline{Y}_{eqB} = 54.90 \sqcup -176.8^{\circ} \text{ mS}$$

$$\underline{Y}_{eqC} = 250.74 \sqcup -102.1^{\circ} \text{ mS}$$

$$\underline{Y}_{eqC} = 33.48 \sqcup 144.5^{\circ} \text{ mS}$$

$$\underline{Y}_{eqE} = 118.53 \sqcup -138.5^{\circ} \text{ mS}$$

$$\underline{Y}_{eq} = 4.52 - j \ 772.73 \text{ mS}$$

$$\underline{Z}_{eq} = 0.007 + j \ 1.29 \ \Omega$$

The equal current sharing gives a worse result than in examples 1 and 2. As there is high number of parallel windings and the number of layers in series is low, it is difficult to modify the winding impedances to get better results. In any case the current sharing for this configuration is better than for any other configuration analyzed during the optimization procedure.

VI. CONCLUSIONS

Parallel windings in inductors allow reducing losses and/or current stresses, but selecting the best connection of the layers of the windings is not easy because gap effect can create imbalances in the current share of the parallel windings.

A procedure to obtain the appropriate connection of layers that allows the best current share has been presented. The procedure takes into account the couplings between each pair of the parallel windings and compensates the aforementioned gap effects.

Some application examples were presented and the proposed method was compared with a design based on general recommendations. The proposed method allowed a great improvement and showed the limitation of the general recommendation.

The examples show two optimization methods: one based on equalizing the current sharing of the parallel windings and another based on minimizing the losses in the parallel windings. The first method gives good results when a high number of series turns allow a wide range of variation of the self and mutual impedances of the windings. Results are worse if it is not the case.

In any case, the results that are obtained with this methodology are better than the results from the general recommendations analyzed in section IV.a, therefore, this is an useful tool for the improvement of the design of planar inductors with parallel windings.

VII. REFERENCES

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