Multiple-output Class E Isolated dc-dc Converter

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Abstract - **This paper presents a multiple output class-E isolated dc-dc converter that regulates the output voltages at fixed switching frequency. The two output converter is simulated at operating frequency of 5 MHz. The converter output power is 40 W and the output voltages are 15 V and 5 V. All the switches operate at zero voltage switching (ZVS) conditions for the full load range. The circuit configuration is simple with small passive components which reduce the size of the converter. The circuit also has very good cross-regulation and an inherent short circuit protection with preserved ZVS conditions.**

I. INTRODUCTION

Using high switching frequencies leads to a significant reduction of size of passive components. However, very fast voltage and current transitions mean increasing influence of the layout, the interconnections and packaging on the circuit behavior. Semiconductor devices are exposed to very high di/dt during commutations because of the energy stored in their parasitics which increase switching losses and electromagnetic interference and may cause breakdown of the device. Parasitic inductances and capacitances cause significant problems as the frequency of the circuit is increased. To address these problems in the design of high-frequency operating dc-dc converters topologies that incorporates these parasitics into circuit elements are a good alternative.

The class-E resonant inverter topology, [1]-[5], addresses these problems which allow its operation in the megahertz order frequencies with zero-voltage switching and zero-voltage slope at turn-on if the switching conditions are met. The class-E topology also absorbs the power MOSFET's parasitic capacitance into the circuit elements and can be implemented with few components. These characteristics, in theory, allow achieving high power densities and high efficiency and reducing the size and weight of the converter.

Since class-E inverter can operate at very high frequency with very high conversion efficiency it can be used in designing resonant dc-dc converters [6]-[10]. The isolated dc-dc converter shown in Fig. 1, [11], [12], regulates the output voltage at fixed switching frequency by controlling the conduction time of the auxiliary switch in the rectifier stage connected at the secondary side of the transformer. Based on this concept, in this paper we analyze the extension of this topology to the multiple output power supply, Fig. 2.

Each rectifier at the transformer's secondary side has its own controller, therefore all of the output voltages can be regulated for the entire load range variations and the input line voltage variations.

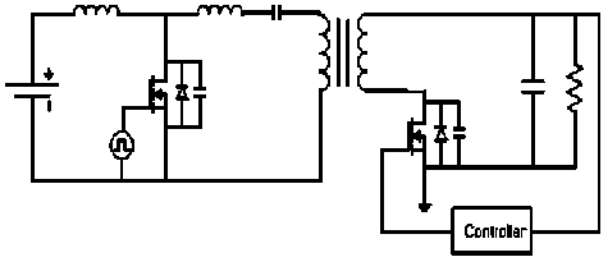

Fig. 1. The class-E isolated dc-dc converter

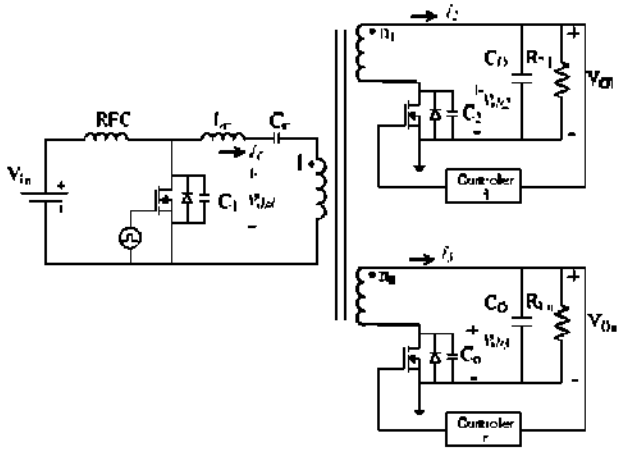

Fig. 2. Multiple output class-E isolated dc-dc converter

The analysis and evaluation of the impact that very high switching frequency has in multiple output power supplies is of special interest in the satellite applications. The launch cost is very high and there is a permanent interest in efficiency improvement and in the reduction of the mass and volume of the satellite's equipment. Switching at such a high frequency reduces significantly the size of the converter but can

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increase the switching losses to an unacceptable level. In this sense, it is important to analyze topologies different to those ones used for lower frequencies (hundreds of kHz), [13]-[16], and to evaluate the reduction of converter's size when switching at high frequency. In this paper, the circuit operation is reviewed and the two output class E converter is designed and validated with PSpice simulation results. Basic circuit operation is also tested on a preliminary prototype.

II. CIRCIUT OPERATION

The multiple output class-E dc-dc converter shown in Fig. 2 consists of a class-E series resonant inverter at the primary side of a high frequency transformer and the controllable synchronous rectifiers at its secondary sides. The class-E inverter consists of a RF choke that injects a dc current into transistor's drain node, the switching transistor with a shunt capacitor and a series resonant tank with a high quality factor, Q, that makes the resonant tank current approximately sinusoidal. The transistor is driven with the signal at fixed switching frequency and fixed duty cycle. Zero voltage switching conditions, ZVS, are satisfied in both turn-on and turn-off and in the entire range of operation, from-full load to open-circuit.

All the synchronous rectifier stages consist of one secondary winding of the transformer, the switching transistor with its parallel capacitor and the filter formed by the output capacitor and the load. Fig. 3 shows the rectifier model where the secondary winding is replaced with two current sources which represent the dc output current, that is magnetizing current I_M, and the rectifier driving current, i_{AC}. The principle of operation of the rectifier can be explained from the Fig. 4. The duty cycle D of the controlled switch is changing in the range of $D_{min} \leq D \leq D_{max}$ in order to regulate the output power at the desired level. When the transistor is off, the negative secondary current charges the parallel capacitor and the voltage V_{DS} increases. The positive current discharges this capacitor, its voltage decreases, and at the time when its voltage crosses through zero the transistor is turned on. The averaged value of the voltage V_{DS} is the output voltage since the averaged value of the transformer's secondary winding is zero. A change in the load resistance means changes in the currents I_M and i_{AC} and that leads to different negative peak of the transformer's secondary current and change the phase shift between the inverter's and synchronous rectifier's driving signal. Hence, the duty cycle D has to be changed to maintain the desired output power. The minimum value D_{min} corresponds to the maximum output power when all the negative current is charging the shunt capacitor. In case of the short circuit at the output the duty cycle of the driving signal sets to the maximal value, D_{max}, which is equal to 100 %. In this way the output current I_M is equal to zero. The drawbacks of the topology are high circulating currents that increase as the load decreases deteriorating the converter's efficiency at low load.

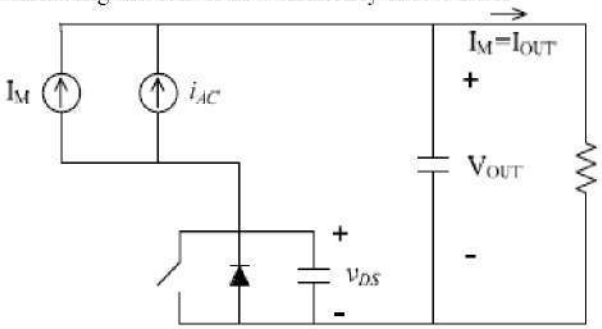


Fig. 3. Synchronous rectifier model

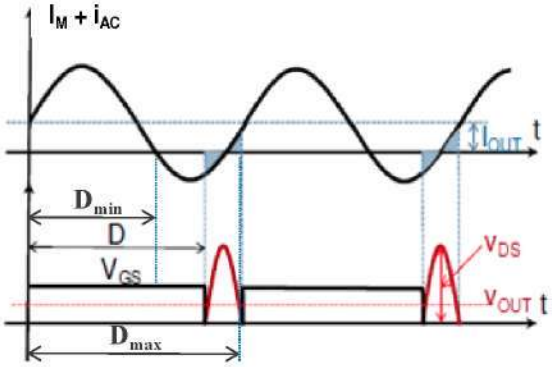


Fig. 4. The waveforms of transformer's secondary current switch driving signal and drain-to source voltage

III. DESIGN PROCEDURE

A detailed analysis of the synchronous rectifier is given in [8]. Here, the design procedure will be explained briefly for a two output class-E isolated dc-dc converter with the specifications given in Table I:

TABLE I
CONVERTER'S SPECIFICATIONS

Parameter	*Symbol*	*Value*
Input voltage	V_{in}	22 – 35 V
Output voltage 1	V_{OUT1}	15 V
Output current 1	I_{OUT1}	2 A
Output voltage 2	V_{OUT2}	5 V
Output current 2	I_{OUT2}	2 A
Switching Frequency	f_{SW}	5 MHz

The design of the converter is conducted for the minimal value of the input voltage because the circulating currents are the lowest in that case. In Fig. 5 the synchronous rectifier transistor's current and voltage stresses are given. The product of those two curves that represents the reciprocal value of the power output capability has its minimum when the duty cycle is equal to 50 %. Therefore, the minimal value of the duty cycle, D_{min}, is 50 % for both the rectifiers. For the

same reason, the fixed duty cycle for the inverter's switch is 50 % as well.

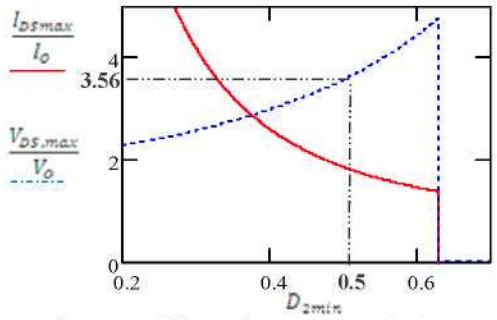


Fig.5. Synchronous rectifier transistor's current and voltage stresses

Using [8] and the minimum load resistance for both the stages, R_{L1} and R_{L2}, needed for nominal output voltage we obtained the parallel capacitors values of C_2 and C_3 as the function of selected D_{min} from the equation:

$$wC_2R_{Lmin} = \frac{1}{4\pi sin^2 4\pi D_{min}} \cdot \{(2\pi - 2\pi D_{min})(2sin4\pi D_{min} + 4sin2\pi D_{min}) + 2(2\pi - 2\pi D_{min})^2(1 + cos2\pi D_{min}) - ((2\pi - 2\pi D_{min})^2 - 4)sin^2 2\pi D_{min}\} \quad (1)$$

Now the input impedances of the rectifiers can be calculated using the describing function method as the RC series network seen at the fundamental harmonic. The turn ratio, n_1/n_2, is obtained from the relation between the transformer's voltages:

$$v_{prim} = \frac{Z_{rc2} \cdot i_2}{n_1} = \frac{Z_{rc3} \cdot i_3}{n_2} \quad (2)$$

where the v_{prim} is the fundamental harmonic of the transformer's primary side voltage, Z_{rc2} and Z_{rc3} are the equivalent impedances seen at the outputs of the transformer's secondary sides and i_2 and i_3 are the rectifiers' driving current. The amplitudes of i_2 and i_3 are the same since that are the output currents and duty cycles, so the ratio n_1/n_2 is:

$$\frac{n_1}{n_2} = \frac{Z_{rc2}}{Z_{rc3}} \quad (3)$$

The values for n_1 and n_2 are obtained in order to minimize the inverter's circulating current, i_1:

$$i_1 = n_1 \cdot i_2 + n_2 \cdot i_3 \quad (4)$$

To design class-E inverter we used [2], [3] and the values for the resonant tank elements L_r and C_r and shunt capacitance C_1 were obtained. The resonant tank capacitance C_r in series combination with the transformer's input capacitance makes the class-E inverter resonate with ZVS conditions. Loaded quality factor (Q) for the resonant tank network was selected to be high so the current through the tank was approximately sinusoidal although ZVS for all the switches can be satisfied with lower Q factor. The values for all the components are summarized in Table II.

TABLE II
CONVERTER COMPONENTS VALUES

Component	*Symbol*	*Value*
Minimal load resistance 1	R_{L1}	2.5 Ω
Minimal load resistance 2	R_{L2}	7.5 Ω
Resonant inductor	L_r	1.13 uH
Resonant capacitor	C_r	2.1 nF
Parallel capacitor 1	C_1	1 nF
Parallel capacitor 2	C_2	4 nF
Parallel capacitor 3	C_3	1.4 nF
Transformer´s turn ratio	$1:n_1:n_2$	1:0.75:0.25
Output filter capacitor	C_O	10 uF
Choke	RFC	6 uH

IV. DESIGN OF THE MAGNETIC COMPONENTS

The design of the inductors and the transformer is critical for the desirable operation of the converter. The circuit is strongly influenced by the parasitic components of the magnetics at the operating frequency. The design and optimization of these components is conducted by the help of the PEmag finite element analysis (FEA) based tool, [18], and the resulting configurations are given in the following paragraphs.

A. Choke

The choke inductor acts as a current source in the class E inverter and has a very small current swing. In case of the converter analyzed here the current swing is approximately 10 % of the input current so the ac resistance of the windings does not result critical. Two possible designs of the input choke are given in Fig. 6 and both have the same EP7 – 4F1 core from Ferroxcube without gap and with the difference in winding strategy. The inductor on the left side of Fig. 6 has 10 turns of AWG29 wire and two parallel windings while the inductor on the right side has 4 parallel windings of 10 planar conductor turns. The design with round wire has higher dc and ac resistances of the windings (29 mΩ and 283 mΩ) comparing to the design with planar conductors (16 mΩ and 201 mΩ) which also has the clear possibility to be integrated in the printed circuit board (PCB). The choke inductance value is 7.27 uH.

B. Resonant inductor

The high circulating current of the resonant tank inductor makes it impossible to be implemented with the reasonable

size of the magnetic core. The selected way to build it is to use air core inductor. At 5 MHz switching frequency the ac resistance of the resonant air core inductor (Lr=1.13 uH) is unacceptable large, therefore the resonant tank network has to be designed with lower Q factor. The lowest value for the resonant tank inductor is obtained when the impedance of the tank network is almost equal to the impedance of the resonant inductor. This means that the resonant capacitor should be increased in order to be seen as a short circuit at the operating frequency. The new values for the resonant inductor and capacitor are L_r=450 nH and C_r=70 nF. The resonant inductor is built as a solenoid with 7 turns of AWG22 wire on a 1 cm diameter air core and has a 140 mΩ of ac resistance at 5 MHz. The change in the resonant tank design has no influence on the nominal operating conditions of the converter. However, when the load is changed, the current that circulates through the tank is no longer a sinusoidal as it is at nominal load but has significant harmonic content. These currents increase the power losses in the resonant inductor and the transformer since the ac resistance of the windings at the harmonic frequencies is significantly higher than at the fundamental frequency. In order to reduce this effect a small second harmonic parallel LC filter is added is series with the resonant tank. The filter inductor and capacitor values are L_{2f} = 30 nH and C_{2f} = 8.44 nF. Fig. 7 shows the resonant tank current with and without filter applied when the output powers are P_{OUT1}=0 and P_{OUT2}=10 W. As it can be observed the filter significantly reduces the tank current harmonic content and, consequently, the converter's conduction losses.

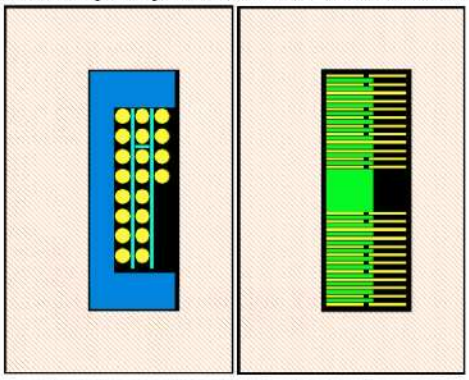


Fig. 6. Two possible designs of the input choke

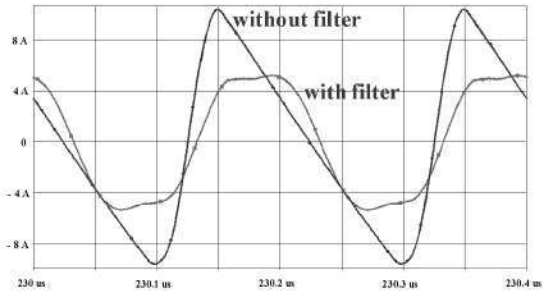


Fig. 7. The resonant tank current with and without filter added when the output powers are P_{OUT1}=0 and P_{OUT2}=10 W

C. *Transformer*

The transformer is designed with 8:6:2 turn ratio on EP13-4F1 core from Ferroxcube. Several winding strategies have been considered in order to minimize the ac resistance of the windings. In Fig. 8, two winding strategies with different number of layers and turns per layer are shown. The design on the left side of the Fig. 7 has much higher ac resistance in primary and first secondary winding comparing to the design on the right side. The second one is more complicated to integrate in PCB due to the higher number of layers but since it has lower ac resistance of the windings this design is chosen. The ac resistance obtained from PEmag for the primary winding is 83 mΩ and for the secondary windings are 83 mΩ and 28 mΩ (comparing to 127 mΩ, 101 mΩ, 28 mΩ for the left side design). The designs with the round wires have significantly higher ac resistances.

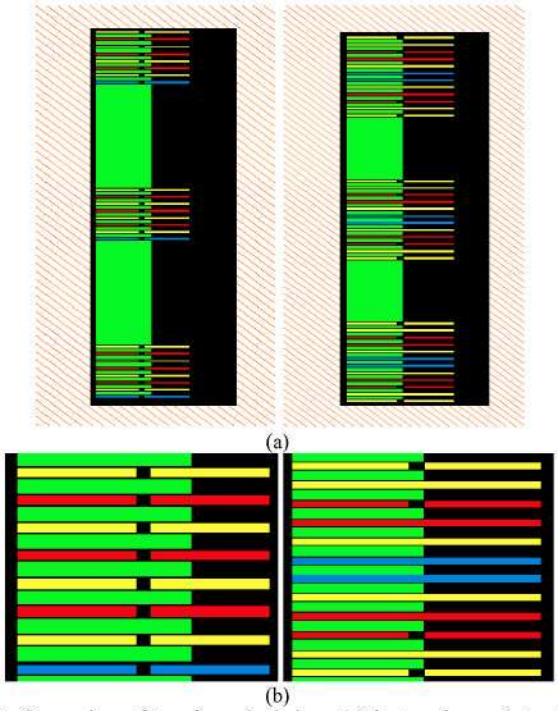


Fig. 8. Comparison of transformer's designs: (a) the transformers' structures with 8 primary turns (yellow), 6 first secondary turns (red) and 2 second secondary turns (blue), and (b) detail of the segments replicated 3 times in both structures

V. SIMULATION RESULTS

The two output class-E isolated dc-dc converter was simulated in PSpice circuit simulator using the elements designed in the previous section. An equivalent electrical circuit model for the transformer is obtained in PEmag and is exported to PSpice. The choke and resonant inductors are represented with their inductances in series with dc and ac resistances, respectively. The leakage inductance at the

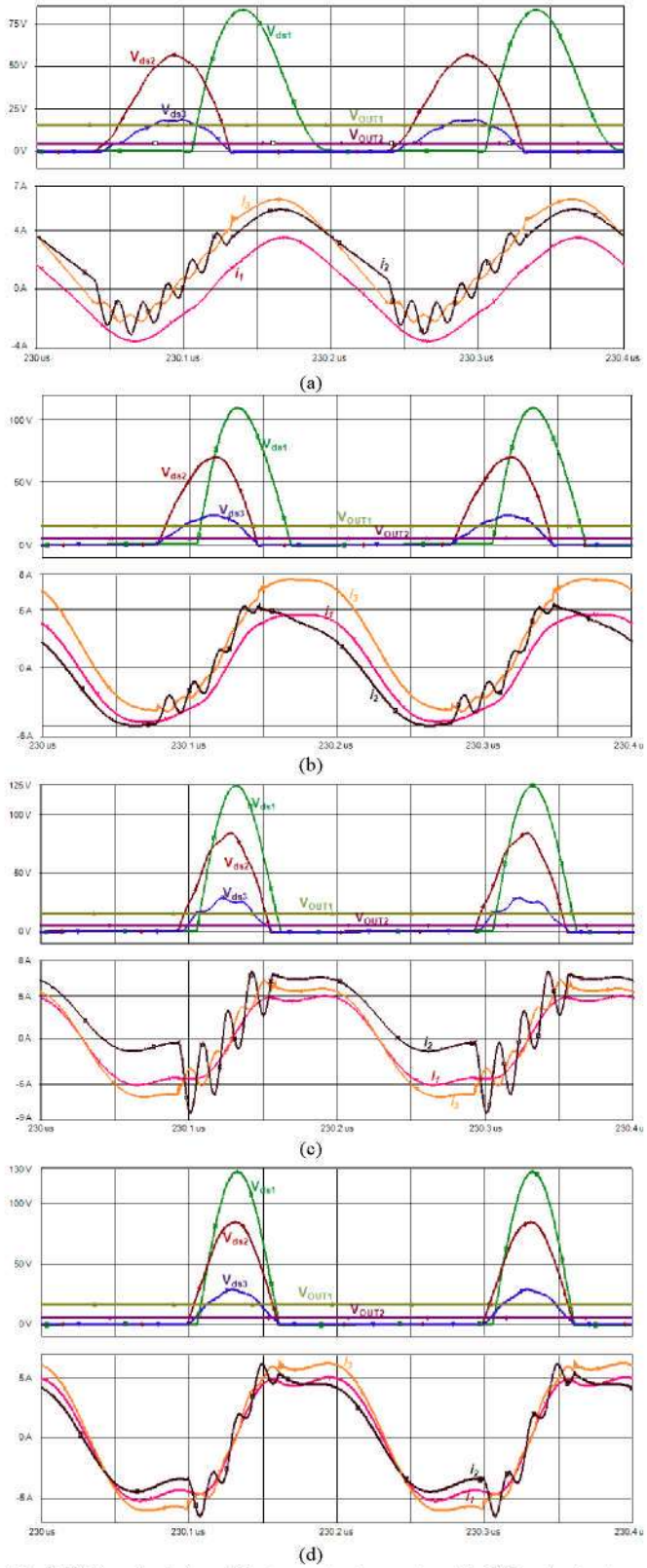


Fig. 9. PSpice simulation of the two output converter with different output powers: (a) P_{OUT1}=30 W, P_{OUT2}=10 W, (b) P_{OUT1}=30 W, P_{OUT2}=0 W, (c) P_{OUT1}=0 W, P_{OUT2}=10 W, and (d) P_{OUT1}=0 W, P_{OUT2}=0 W.

transformer's primary side is included in the simulation and it is absorbed in the resonant tank inductance. For that reason the resonant inductance had to be decreased. The value of the shunt capacitor C_1 was also decreased in order to attain full ZVS condition in the inverter's switch. The new values for those elements are L_r=420 nH and C_1=740 pF. Fig. 8 shows the voltages across the switches v_{ds1}, v_{ds2}, v_{ds3}, the output voltages V_{OUT1} and V_{OUT2}, and the transformer's currents i_1, i_2, i_3 at different loads. The Fig. 9 reveals that all the switches are turned at ZVS conditions for the full-load to open-circuit. It can be observed from Fig. 9 that the harmonic content of the circulating current i_1 is depending on the load; the higher the load, the higher is the harmonic content. When the output is open-load the value of the third harmonic reaches 1 A which further affects the losses. The driving signals for both the rectifiers are the same which means that the circuit has very good cross regulation and only one control circuit can be implemented for both rectifiers. The maximum variation of V_{OUT1} is +4 % when the V_{OUT2} is fixed to its nominal value. The output voltages can also be independently adjusted to the nominal values with slight difference in duty cycles of the gating signals. The losses distribution for the switches and the magnetic elements is given in the Table III for the minimal input voltage and full-load.

TABLE III
POWER LOSSES DISTRIBUTION IN THE CONVERTER

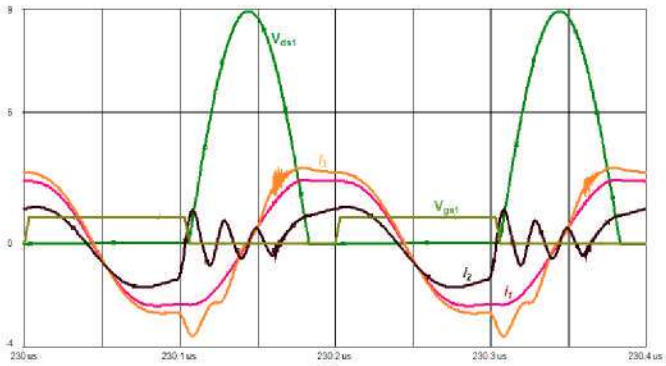
Component	*Losses*
Choke	0.15 W
Switch 1	0.75 W
Resonant inductor	0.85 W
Transformer	1.7 W
Switch 2	0.33 W
Switch 3	0.27 W

The converter's efficiency is summarized in Table IV for different loads and without driving circuitry losses included. The converter's efficiency is high at nominal input voltage and nominal load. When the input voltage is increased, the circulating currents are higher and it strongly affects the efficiency out of the nominal operating conditions.

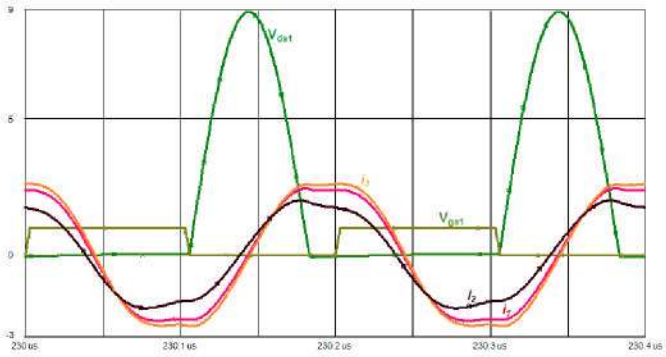
TABLE IV
CONVERTER'S EFFICIENCY FOR DIFFERENT LOADS

Output power	*Efficiency*
P_{OUT1}=30 W, P_{OUT2}=10 W	91 %
P_{OUT1}=30 W, P_{OUT2}=0 W	81 %
P_{OUT1}=0 W, P_{OUT2}=10 W	54 %
P_{OUT1}=0 W, P_{OUT2}=0 W	9.3 W power loss

The circuit also has short circuit self protection as can be seen on the Fig. 10 in the case of short circuit in one stage or in both stages. The ZVS condition of the inverter switch at turn on and off is preserved even in this case. The power losses in both cases are approximately 1.3 W.



(a)



(b)

Fig. 10. PSpice simulation of the converter in case of short circuit at one output (a) and at two outputs (b). The v_{ds1} voltage attenuation is equal to 10.

VI. EXPERIMENTAL VERIFICATION

A. *Concept and design validation on a preliminary prototype*

In order to validate the feasibility of the converter switching at such a high frequency and due to the complexity of the circuit we have opted to design first the converter with one output concentrating all the 40 W of the output power at the output of V_{OUT}=15 V. The input voltage specifications and the switching frequency are the same as they are given in Table I.

B. *Design details*

In this prototype the selected main switch FQD18N20V2 (200 V, 140 mΩ, Q_g=20 nC) as the main switch and STD10NF10 (100 V, 115 mΩ, Q_g=16 nC) as the synchronous rectifier's switch. The input choke was built with an EP7 core with 4 parallel windings of 8 turns of Litz 1x20x0.05 wire. The transformer was built with an EP13 core with 8 parallel windings of Litz 1x20x0.05 wire and a 4:3 turn ratio. The core material was 3F3 for both the choke and transformer since the 4F1, which is the most appropriate for the operating frequency, was not available. The resonant inductor was built as a solenoid with 8 turns of AWG22 wire on a 1 cm diameter air core. The photograph of the prototype is given in Fig. 11.

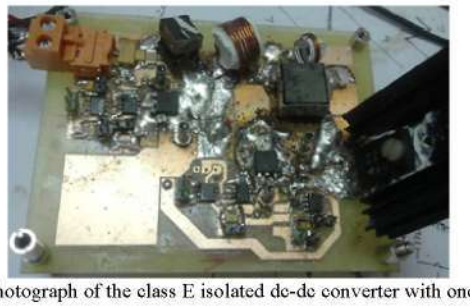
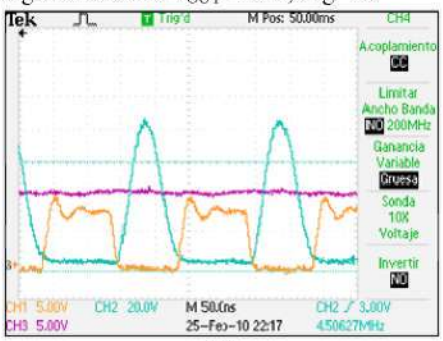


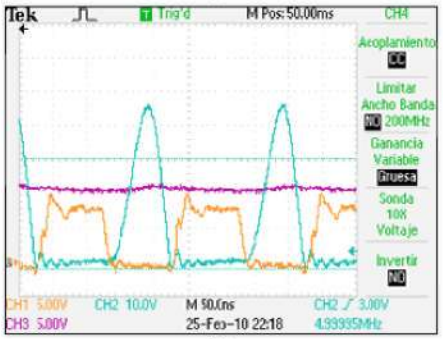
Fig. 11. Photograph of the class E isolated dc-dc converter with one output

C. *Measurement results*

Fig. 12, 13 and 14 show experimental waveforms of the converter's voltages at full load, open circuit and short circuit, respectively, and at V_{in}=22 V. As it can be observed from these diagrams, ZVS conditions are satisfied for both the switches at each of the operating conditions. The maximal values of the drain-source voltages are as it was expected from the simulation. However, the losses are higher than expected due to the poor PCB design and inappropriate use of both the 3F3 magnetic material specified for the order of magnitude lower switching frequency and the litz wire. For the full load output (R_{Lmin}=5.6 Ω) the total losses are 14 W when the output voltage is V_{OUT}=15 V. The efficiency is this case is η=74 %. Due to high losses the temperature rise is significant and the output voltage drops to V_{OUT}=11 V in steady state, Fig. 12, while the efficiency drops to η=71.4 %. When the output is open circuit the losses are higher due to higher circulating currents and are equal to 16.5 W but the output voltage is stable at V_{OUT}=15 V, Fig. 13.



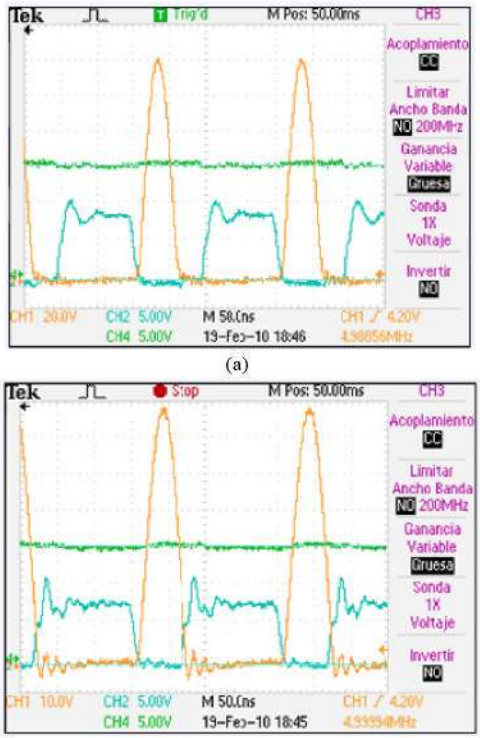
(a)



(b)

Fig. 12. Voltage diagrams when the input voltage is V_{in} = 22 V and the output is full load: (a) v_{gs1} (Ch. 1), v_{ds1} (Ch. 2) and v_{out} (Ch. 3) and (b) v_{gs2} (Ch. 1), v_{ds2} (Ch. 2) and v_{out} (Ch. 3)

The circuit also has short circuit self protection as can be seen on the Fig. 14 in the case when V_{in}=33 V. The ZVS conditions of the inverter switch at turn on and off are preserved even in this case. The duty cycle of the synchronous rectifier's driving signal is set to 100% in order to minimize the losses. The power losses in this case are 6.9 W.



(a)

(b)

Fig. 13. Voltage diagrams when the input voltage is V_{in} = 22 V and the output is open circuit: (a) v_{gs1} (Ch. 1), v_{ds1} (Ch. 2) and v_{out} (Ch. 3) and (b) v_{gs2} (Ch. 1), v_{ds2} (Ch. 2) and v_{out} (Ch. 3)

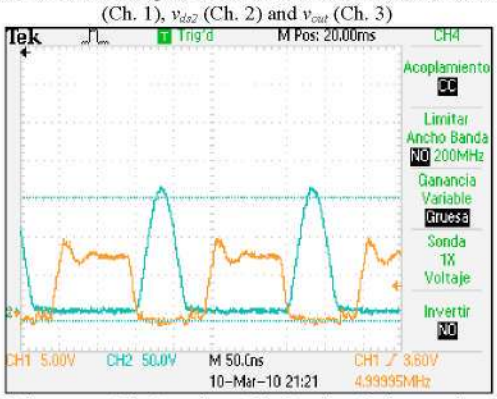


Fig. 14. Voltages v_{gs1} (Ch. 1) and v_{ds1} (Ch. 2) when the input voltage is V_{in} = 33 V and the output is short circuit

VII. CONCLUSION

The class E isolated dc/dc converter with synchronous rectification and two outputs is analyzed in this paper. The advantages of this topology are:

- operation at fixed switching frequency. Besides, the class E inverter driving signal has fixed duty cycle and hence the gate driver can be built in the form of resonant circuit which means lower losses in the converter.
- circuit can work with ZVS conditions in all the transistors and for the entire load range.
- it has very good cross regulation which reduces the number of control circuits at the secondary side of the transformer.
- the converter has short circuit self protection and the inverter's switch operates at ZVS condition even in this case.

The main drawbacks of this topology are high circulating currents that:

- increase the design complexity of the magnetic components. Due to this, the resonant inductor should be designed with an air core.
- increased influence of the PCB parasitics
- decrease efficiency when the input voltage is changed from its nominal value and at low load since the circulating currents are higher comparing to those ones at nominal load.

Experimental results that confirm expected circuit operation at full load, open circuit and short circuit were obtained for a converter with one output. The preliminary prototype has shown a high design complexity of the circuit due to very high circulating energy that makes the converter's optimization quite difficult. Efficiency improvements are expected in a two output prototype where the choke and transformer will be integrated in the PCB and the magnetic material will be the most appropriate for the operating frequency (4F1).

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