"Fast control technique for high frequency DC/DC integrated converter based on non-invasive output capacitance current estimation"

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***Abstract*— High switching frequency allows the integration of low power DC/DC converters. Although a high switching frequency would make feasible a voltage mode control with 1MHz bandwidth, parasitic effects and robustness don't allow such a high bandwidth. This paper proposes a fast control to optimize the dynamic response of high frequency DC/DC converters. The proposed control is based on the peak current mode control of the output capacitor current. The output capacitor current loop provides fast dynamic response while the voltage loop provides accurate steady state regulation. Experimental results have validated the fast dynamic response of the proposed control under load steps.**

Keywords: DC/DC converters, high switching frequency, fast dynamic response, output capacitor current, integration.

I. INTRODUCTION

Nowadays, many power supplies applications demand fast dynamic response. The implementation of a linear control system with fast dynamic response involves an increase in the switching frequency, and it benefits the whole system integration. On the other hand, the high bandwidth needed in linear controls is difficult to obtain because of parasitic effects, component variation and non-idealities of the error amplifier. One technique to face up to these limitations is the combination of non-linear and linear control [1], [2].

Well known non-linear strategies are V^2 [2], [3] or hysteretic control [3] of the output voltage. Both require sensing the output voltage ripple, which is very small compared to the dc value and it is very sensitive to parasitic variations. It is also required to have a triangular output ripple given by the ESR (ESR must be dominant or it is required an additional resistor that worsens the regulation under load changes).

The non-linear and linear control proposed in [1] is based on a hysteretic control of the output capacitor (C_{out}) current of a Buck converter. It achieves a faster control action under load steps since the output capacitor current responds instantaneously (Figure 1). The problem is to measure the output capacitor current but it can be estimated with the non-invasive method described in [4]. Although this method has very fast dynamic response under load steps with low bandwidth, it suffers some limitations: variable frequency, restricted operation and control by the hysteretic bandwidth and high sensitivity to current sensor mismatches [4].

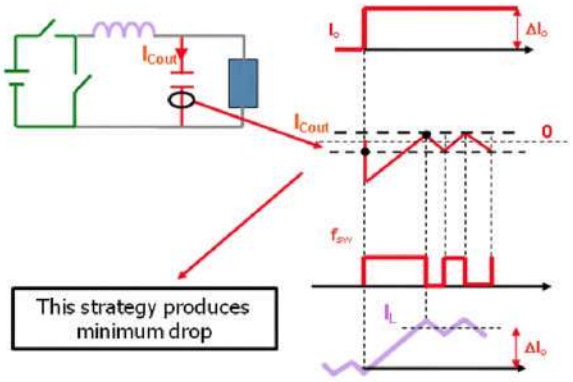

Figure 1. Hysteretic control of the output capacitor current.

The control proposed in this paper avoids these problems. It is based on the capacitor current-injected control described in [5] but using a non-invasive output capacitor current sensor [4]. The sensor used in [5] is invasive (current transformer) and would have effect on the control dynamic response. With the control proposed the dynamic response is fast and the required bandwidth low, so the components can be reduced, mainly the output capacitor, making easier the integration.

II. NON-INVASIVE OUTPUT CAPACITANCE CURRENT ESTIMATION

The non-invasive capacitor current estimation method described in [4], and used in the control proposed in this paper, consists of a RLC network. The basic idea is to use an RLC network in parallel with the output capacitor to measure the current by matching phases, time constants and scaling impedances. The current in the parallel network of the output capacitor is proportional to the C_{out} current (Figure 2). The physical implementation of the RLC network is done with a

transimpedance amplifier as shown in Figure 3 and the voltage obtained at the sensor output (V_S) is proportional to the output capacitor current (I_{Cout}).

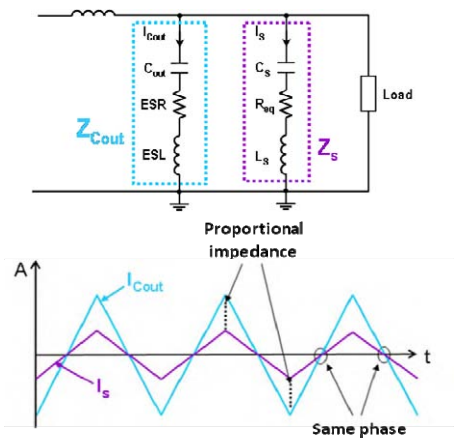

Figure 2. RLC network and sensor matching. [4]

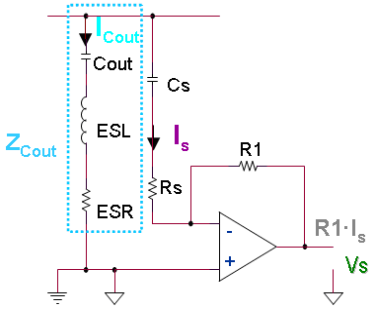

Figure 3. Physical implementation of the capacitor current sensing method (RLC network). [4]

III. PROPODED CONTROL

A. *Operating principle of the proposed control*

The control proposed and analyzed in this paper is based on the peak current mode control of the output capacitor current [5] of a Buck converter (Figure 4).

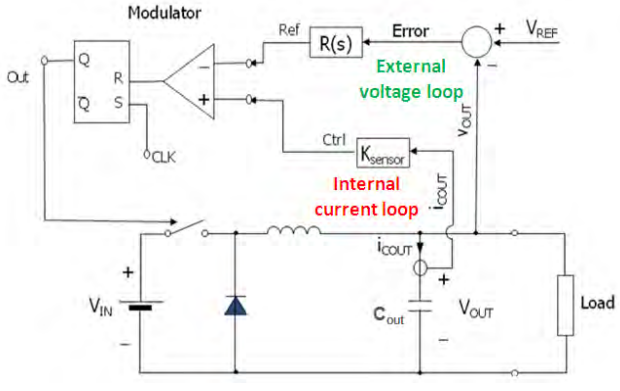

Figure 4. Peak current mode control of the C_{out} current.

Unlike the method described in [5], in this proposed control the output capacitor current is sensed with the non-invasive method described in [4]. The output signal of the current sensor is compared with the error signal from the voltage loop error amplifier. When the sensor signal reaches the reference, the main MOSFET switches off. Then, due to the RS latch, when the period finishes the main MOSFET switches on (Figure 5). Hence, this control prevents from the problem of variable frequency and the control based on the measurement of the output capacitor current improves the transient response. The output capacitor current loop provides fast dynamic response to load transitions since it behaves as a feed-forward of the load current while the voltage loop provides accurate steady state regulation. The limitation of the current mode control is that for duty cycles greater than 50% appears a sub-harmonic oscillation, so compensating slope must be added (Figure 5) to prevent it. Besides, this compensating slope helps to desensitize this technique to current sensor mismatches and parasitic effects. On the other hand, the higher the slope compensation, the worst the dynamic response.

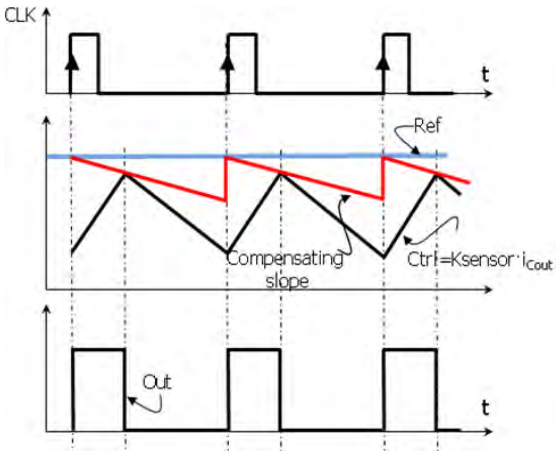

Figure 5. Modulator. Slope compensation.

B. *External voltage loop design*

One of the advantages of the control proposed is that the voltage loop doesn't need a high bandwidth since the current loop behaves as a feed-forward of the output current.

The design of the voltage loop has been done with a simplified averaged model of the peak current mode control [7] of a buck converter (Figure 6 and Figure 7). The compensating slope is not included in the model since the slope is small and the model is good enough, as shown in the simulations (Figure 8).

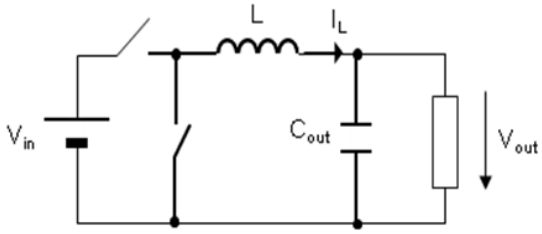

Figure 6. Buck converter.

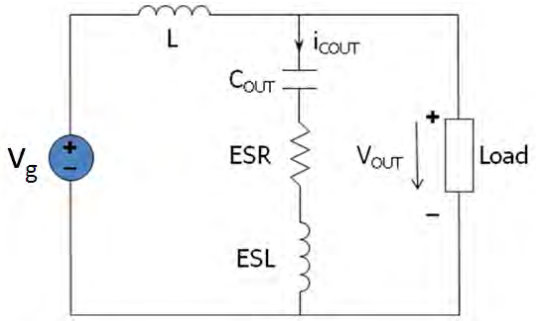

Figure 7. Buck converter averaged model.

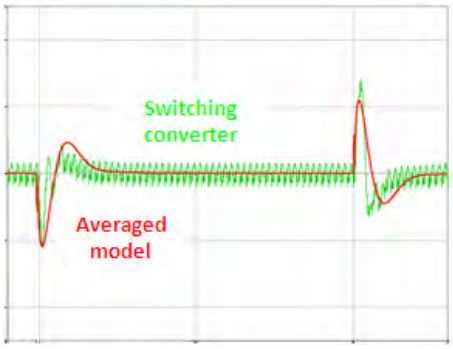

Figure 8. Closed loop output voltage response under load step.

The power supply <v_g> in the averaged model (Figure 7) is a dependent source whose value is:

$$\langle v_g \rangle = v_{in} \cdot 2 \cdot L \cdot f_{sw} \cdot \frac{I_{ref} - \langle i_{Cout} \rangle}{v_{in} - v_{out}} \quad (1)$$

where v_{in} is the instantaneous input voltage, v_{out} the instantaneous output voltage, L the output filter inductance, f_{sw} the switching frequency, <ic_{out}> the mean value of the output capacitor current and I_{ref} the output reference of the voltage regulator. The steady state value of I_{ref} is calculated as the output capacitor current peak value considering mean values and assuming <i_{Cout}>=0. Its value is calculated (2).

$$I_{ref} = \frac{V_{in} - V_{out}}{2 \cdot L \cdot f_{sw}} \cdot \frac{V_{out}}{V_{in}} \quad (2)$$

The voltage regulator has been designed for two external voltage loop bandwidths: 10 kHz and 50 kHz. Being V_{in}=3V, V_{out}=1V, f_{sw}=500kHz, L=700nH and C_{out}=50µF, Figure 9 and Figure 10 show the simulated response of the proposed control with the slow (B=10 kHz) and fast (B=50 kHz) voltage regulators.

The voltage drop is similar in both cases and very low (20mV) (Figure 9) providing faster recovery time the faster voltage loop (B= 50 kHz), as expected. The control response is very fast and the inductor current changes rapidly (Figure 10).

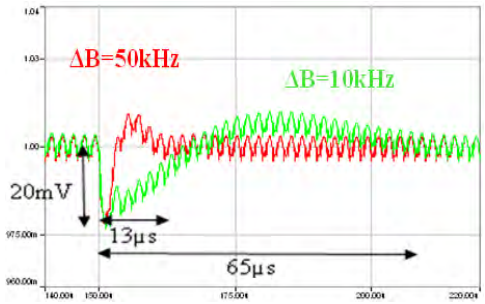

Figure 9. Output voltage response under a 10A/µs load step (2 A).

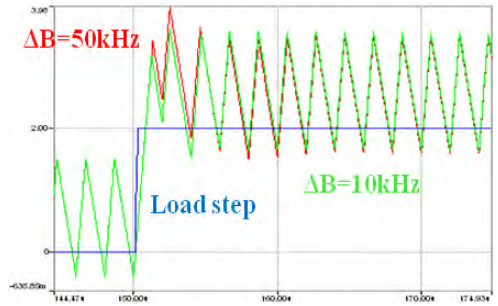

Figure 10. Inductor current response under a 10A/µs load step (2 A).

IV. Comparison Of The Proposed Control With A High Bandwidth Voltage Mode Control

The proposed control (with an external voltage loop designed with a bandwidth of 50 kHz) is compared with a fast voltage mode control. This comparison is done through simulations being V_{in}=3V, V_{out}=1V, f_{sw}=500kHz, L=700nH and C_{out}=50µF (Figure 6).

As shown in simulations (Figure 11 and Figure 12), a similar dynamic response and voltage drop have been achieved comparing the proposed control with an external voltage loop of 50 kHz and a voltage mode control with a bandwidth of 200 kHz. That means four times less bandwidth in the proposed control making easier the implementation and integration.

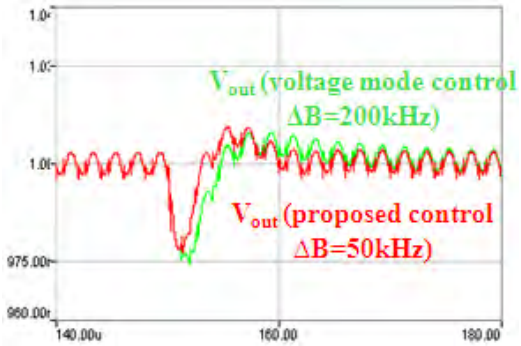

Figure 11. Output voltage response under a 10A/µs load step (2 A).

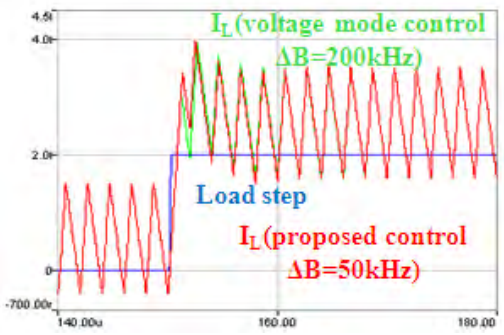

Figure 12. Inductor current response under a 10A/µs load step (2 A).

If the converter switching frequency is 5 MHz, the comparison becomes more interesting. In this case, V_{in}=3V, V_{out}=1V, f_{sw}=5MHz, L=100nH, C_{out}=10µF (Figure 6). In order to compare the control response at high switching frequency with the previous 500 kHz switching frequency the bandwidths should be 2 MHz in the voltage mode control and 50 kHz in the proposed control. However, at high frequencies, the maximum bandwidth is limited by the output capacitor parasitics. The capacitor used has the following parasitic values: ESR=2m• and ESL=1nH. The open loop response of the voltage mode control is shown in Figure 13. 2MHz is very close to the resonant frequency due to the parasitic ESL of the output capacitor (f_{res}=1.6MHz), so the bandwidth has to be reduced to avoid instabilities in closed loop.

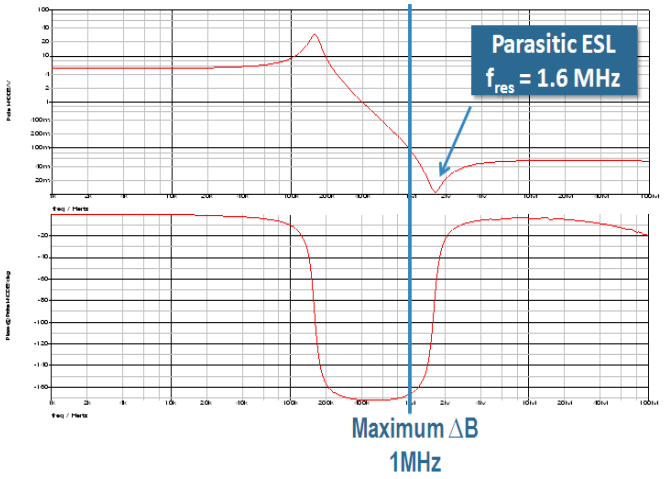

Figure 13. Effect of Cout parasitics on the duty cycle to output voltage frequency response.

Hence, he comparison is now done between the proposed control with a bandwidth of 50 kHz and the voltage mode control with a bandwidth of 1MHz, far enough of the resonant frequency to avoid instabilities. As shown in Figure 14 and Figure 15, the proposed control has the same voltage drop as a 1 MHz bandwidth voltage mode control. Their dynamic responses are also similar. From the practical point of view the implementation of 1 MHz linear control is difficult due to parasitic effects. With the proposed control the bandwidth is 20 times lower, making easier the implementation. In addition, the components size can be reduced. Since the components size and control bandwidth is reduced the implementation and integration of the whole system, power converter and control, is more feasible.

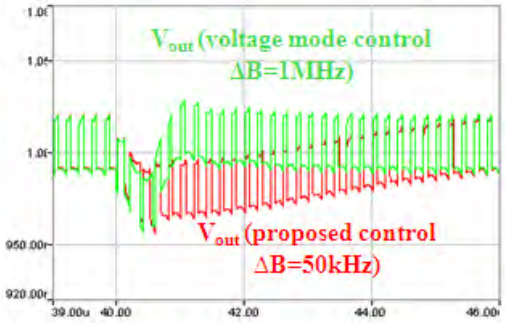

Figure 14. Output voltage response under a 10A/µs load step (6 A).

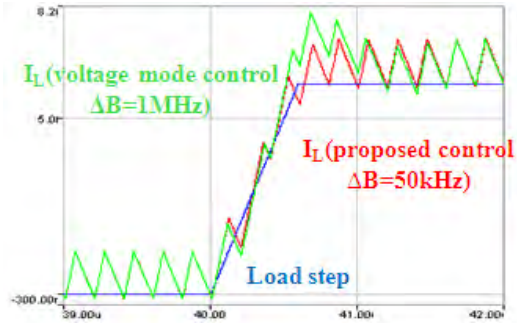

Figure 15. Inductor current response under a 10A/µs load step (6 A).

V. Experimental Results

The experimental results have been obtained on a converter with the specifications shown in Figure 6, being V_{in}=3V, V_{out}=1V, f_{sw}=500kHz, L=700nH and C_{out}=4µF.

As expected and shown in Figure 16 and Figure 17, the control response is very fast. When the load step occurs the control reacts instantaneously saturating the duty cycle (Figure 16) or keeping the main switch off (Figure 17). Only two switching cycles are needed to reach the new steady state. The output voltage drop is 200 mV, but it must be taken into account that the output capacitor value is only 4µF.

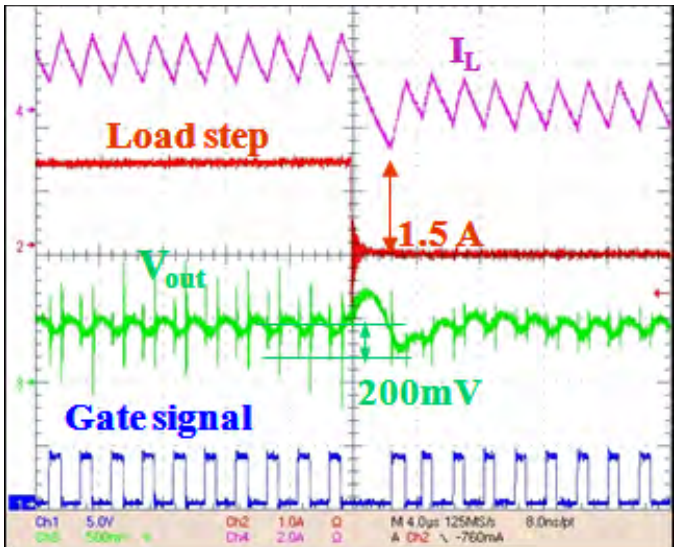

Figure 16. Experimental results. Load step up of 1.5A (1A/div), inductor current I_L (2A/div), output voltage V_{out} (500mV/div) and gate signal (5V/div).

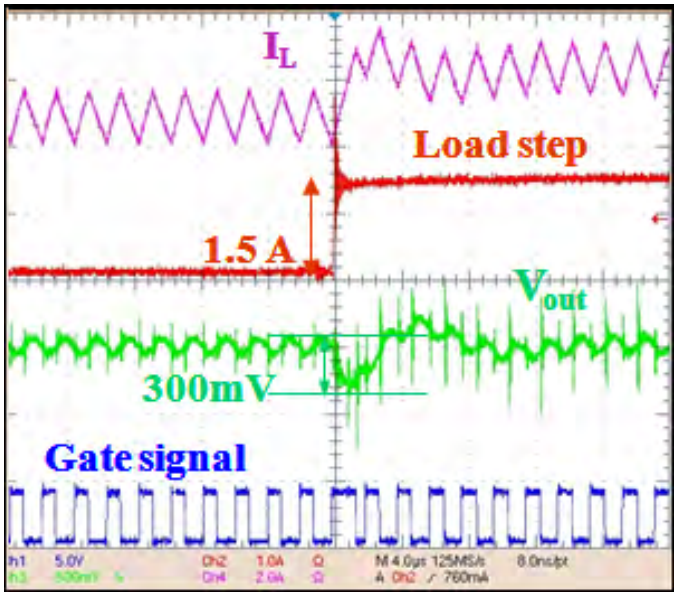

Figure 17. Experimental results. Load step down of 1.5A (1A/div), inductor current I_L (2A/div), output voltage V_{out} (500mV/div) and gate signal (5V/div).

VI. Conclusion

The control proposed is based on the capacitor current-injected control described in [5] but using a non-invasive output capacitor current sensor [4]. The advantages of this control are: constant switching frequency, fast dynamic response, since it behaves as a feed-forward of the load current, and low sensitivity to parasitic effects due to slope compensation. As shown in simulations at 5 MHz switching frequency, the proposed control with a voltage loop of 50 kHz bandwidth has the same voltage drop as a 1 MHz bandwidth linear voltage mode control. Their dynamic responses are also similar. That means 20 times less bandwidth making easier the implementation and design of the control. This control is very appropriate for high switching frequency applications like integrated DC/DC converters. Finally, experimental results have verified the fast dynamic response of the proposed control under load steps.

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