"Fast control technique for high frequency (5MHz) DC/DC integrated converter"

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ABSTRACT

A switching frequency of 5 MHz allows the integration in a chip of a low power (10W) DC/DC converter. Although this switching frequency would make feasible a voltage mode control with 1MHz bandwidth, the parasitics and robustness don't allow such a high frequency bandwidth. This paper proposes a fast control technique that helps to optimize the dynamic response of high frequency DC/DC converter. The control proposed and analyzed in this paper is based on the peak current mode control of the output capacitor current of a Buck converter. The output capacitor current loop provides fast dynamic response to the control since it behaves as a feed-forward of the load current while the voltage loop provides accurate steady state regulation. Experimental results have validated the fast dynamic response of the proposed control under load steps.

1 Introduction

Nowadays, many power supplies applications demand fast dynamic response. The implementation of a linear control system with fast dynamic response involves a frequency switching increase, and it benefits the whole system integration. On the other hand, the high bandwidth needed in linear controls is difficult to obtain because of parasitics, component variation and non-idealities of the error amplifier. One technique to face up to these limitations is the combination of non-linear and linear control [1], [2].

Well known non-linear strategies are V^2 [2] or hysteretic control of the output voltage. Both require sensing the output voltage ripple, which is very small compared to the dc value and it is very sensitive to parasitics. It is also required to have a triangular output ripple given by the ESR (ESR must be dominant or it is required an additional resistor that worsens the regulation under load changes).

The non-linear and linear control scheme proposed in [1] is based on a hysteretic control of the output capacitor (C_{out}) current of a Buck converter. It achieves a faster control action under load steps since the output capacitor current responds instantaneously (**Figure 1**). The problem is to measure the output capacitor current but it can be estimated with the non-invasive method described in [4]. This control technique has very fast dynamic response under load steps. However, this method suffers some limitations: variable frequency, restricted operation and control by the hysteretic bandwidth and high sensitivity to current sensor mismatches [4].

The control proposed in this paper avoids these problems. It is based on the capacitor current-injected control described in [3] but using a non-invasive output capacitor current sensor [4]. The sensor used in [3] is invasive (current transformer) and would have effect on the control dynamic response .

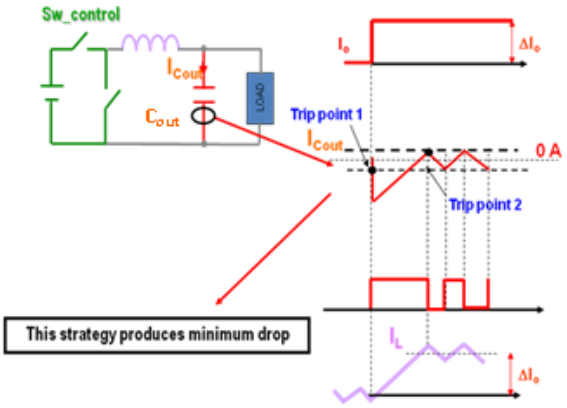

Figure 1 Hysteresis control of the C_{out} current.

2 Proposed solution

The control proposed and analyzed in this paper is based on the peak current mode control of the output capacitor current of a Buck converter (**Figure 2**).

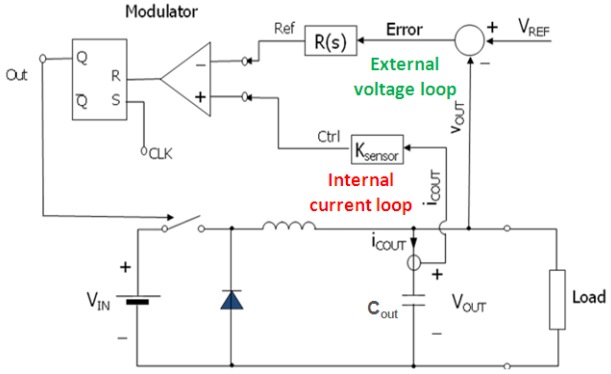

Figure 2 Peak current mode control of the C_{out} current.

The output capacitor current is sensed with the method described in [4]. The output signal of the current sensor is compared with the error signal from the voltage loop error amplifier. When the sensor signal reaches the reference, the main MOSFET switches off. Then, due to the RS latch, when the period finishes the main MOSFET switches on (**Figure 3**). Hence, this control prevents from the problem of variable frequency and the control based on the measurement of the output capacitor current improves the transient response. The output capacitor current loop provides fast dynamic response to load transitions since it behaves as a feed-forward of the load current while the voltage loop provides accurate steady state regulation. The limitation of the current mode control is that for duty cycles greater than 50% appears a sub-harmonic oscillation, so compensating slope must be added (Figure 3) to prevent it. Besides, this compensating slope helps to desensitize this technique to current sensor mismatches and parasitic effects. On the other hand, the higher the slope compensation, the worst the dynamic response.

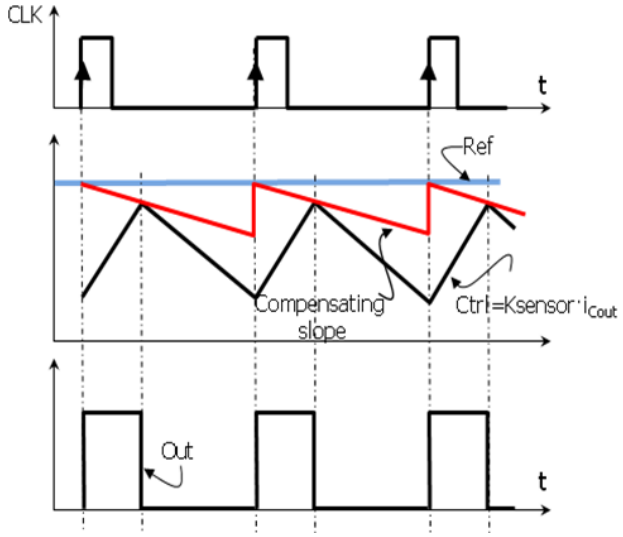

Figure 3 Modulator. Slope compensation.

3 External voltage loop design

The design of the voltage loop has been done with a simplified averaged model of the peak current mode control [6] of a buck converter (**Figure 4**). The compensating slope is not included in the model since the slope is small and the model is good enough as shown in the simulations.

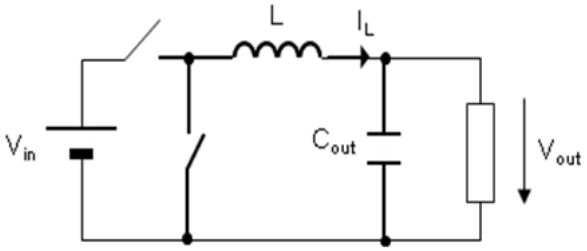

Figure 4 Buck converter.

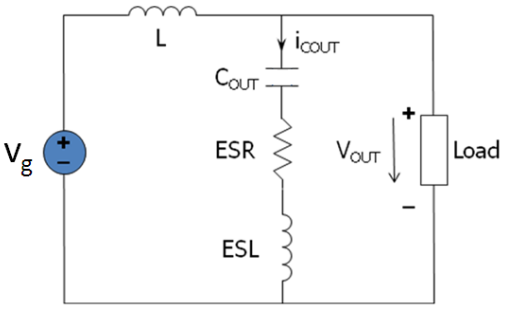

Figure 5 Buck converter averaged model.

The power supply v_g in the averaged model (**Figure 5**) is a dependent source whose value is:

$$v_g = v_{in} \cdot 2 \cdot L \cdot f_{sw} \cdot \frac{I_{ref} - \langle i_{Cout} \rangle}{v_{in} - v_{out}} \qquad (1)$$

where v_{in} is the instantaneous input voltage, v_{out} the instantaneous output voltage, L the output filter inductance, f_{sw} the switching frequency, $\langle ic_{out} \rangle$ the mean value of the output capacitor current and I_{ref} the output reference of the voltage regulator. The steady state value of I_{ref} is calculated as the output capacitor current peak value considering mean values and assuming $\langle i_{Cout} \rangle = 0$. Its value is calculated with equation 2:

$$I_{ref} = \frac{V_{in} - V_{out}}{2 \cdot L \cdot f_{sw}} \cdot \frac{V_{out}}{V_{in}} \qquad (2)$$

The voltage regulator has been designed for two external voltage loop bandwidths: 10 kHz and 50 kHz. Regarding the specifications shown in fig. 4 and being V_{in}=3V, V_{out}=1V, f_{sw}=500kHz, L=700nH and C_{out}=50µF, **Figure 6** and **Figure 7** show the simulated response of the proposed control with the slow (ΔB=10 kHz) and fast (ΔB=50 kHz) voltage regulators. The voltage drop is similar in both cases and very low (20mV) (Figure 6) providing faster recovery time the faster voltage loop (ΔB= 50 kHz), as expected. The control response is very fast and the inductor current changes rapidly (Figure 7), thanks to the output capacitor current loop, taking only two cycles to reach the new steady state.

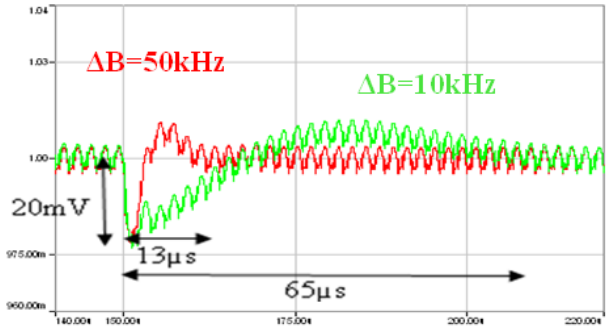

Figure 6 Output voltage response under a 10A/µs load step (2 A).

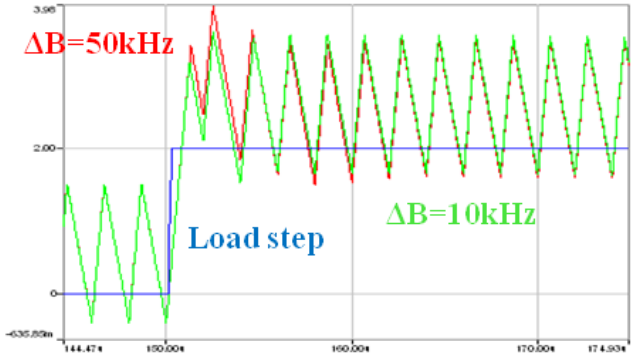

Figure 7 Inductor current response under a 10A/µs load step (2 A).

The response of the control with the 50 KHz bandwidth regulator is detailed in **Figure 8**. The control signal is the sensed output capacitor current with the addition of the compensating slope. The compensating slope amplitude should be high enough to avoid sub-harmonic oscillations over 50% duty cycles and parasitic effects, but also it should be low enough to reduce the influence on the system dynamic response. When the load step occurs this control signal goes down immediately, as it does the output capacitor current. The reference signal obtained in the external voltage loop changes since there is an error between the output voltage and the reference voltage until the new steady state is reached.

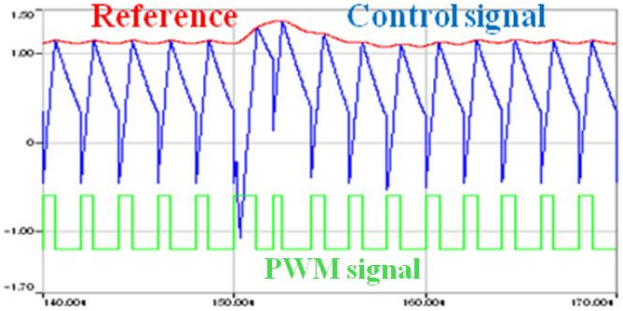

Figure 8 Reference, control and gate signal response under a 10A/µs load step (2 A). Control signal is the sensed I_{Cout} with the addition of the compensating slope.

4 Comparison of the proposed control with high bandwidth voltage mode control

The proposed control (50 kHz bandwidth external voltage loop) can be compared with the voltage mode control. This comparison is done through simulations being V_{in}=3V, V_{out}=1V, f_{sw}=500kHz, L=700nH and C_{out}=50µF (Figure 4). As shown in simulations (**Figure 9** and **Figure 10**), a similar dynamic response and voltage drop has been achieved comparing the proposed control scheme with an external voltage loop of 50 kHz and a voltage mode control with a bandwidth of 200 kHz. That means four times less bandwidth in the proposed control making easier the implementation and integration of the system.

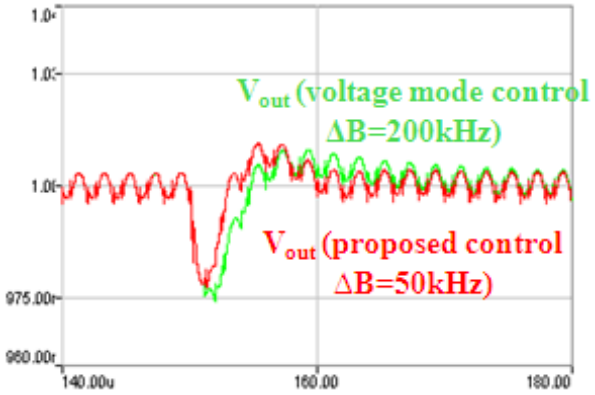

Figure 9 Output voltage response under a 10A/µs load step (2 A).

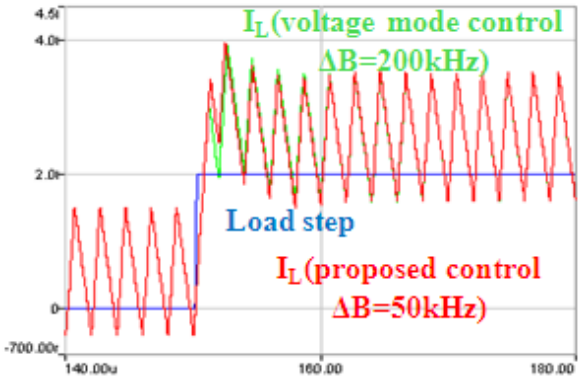

Figure 10. Inductor current response under a 10A/µs load step (2 A).

If the converter switching frequency is 5 MHz, the comparison becomes more interesting. In this case, V_{in}=3V, V_{out}=1V, f_{sw}=5MHz, L=100nH, C_{out}=10µF (Figure 4). The comparison is now done between the proposed control with a bandwidth of 50 kHz and the voltage mode control with a bandwidth of 1MHz (limited in this case by the output capacitor parasitic, in other situations could be even higher).

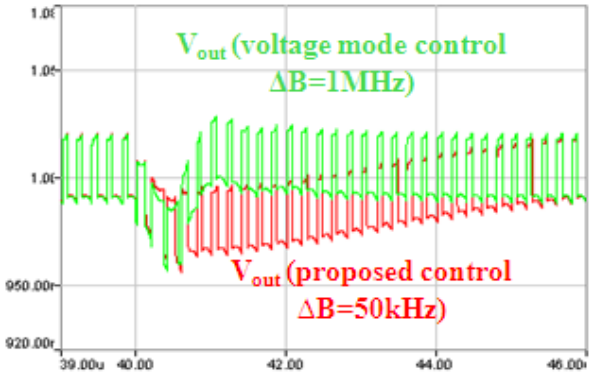

Figure 11 Output voltage response under a 10A/µs load step (6 A).

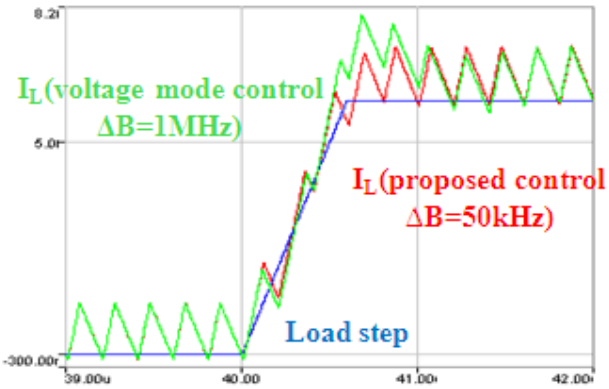

Figure 12 Inductor current response under a 10A/µs load step (6 A).

As shown in **Figure 11** and **Figure 12**, the proposed control with an external voltage loop of 50 kHz bandwidth has the same voltage drop as a 1 MHz bandwidth voltage mode control. Their dynamic responses are also similar. From the practical point of view the design and implementation of 1 MHz linear control is difficult due to parasitics effects. With the proposed control the bandwidth is 20 times lower, making easier the implementation. In addition, the switching frequency can be increased and therefore the components size reduced. Since the components size and control bandwidth is reduced the implementation and integration of the whole system, power converter and control, is more feasible.

5 Experimental results

The experimental results have been obtained on a converter with the specifications shown in Figure 4, being V_{in}=3V, V_{out}=1V, f_{sw}=500kHz, L=700nH and C_{out}=4µF.

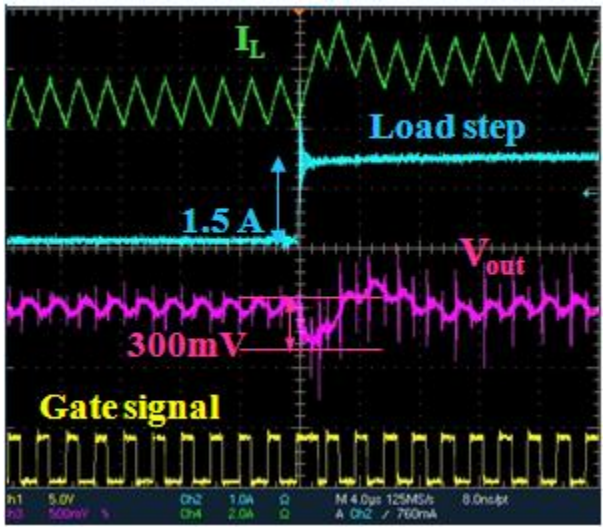

Figure 13 Experimental results. Load step up of 1.5A (1A/div), inductor current I_L (2A/div), output voltage V_{out} (500mV/div) and gate signal (5V/div).

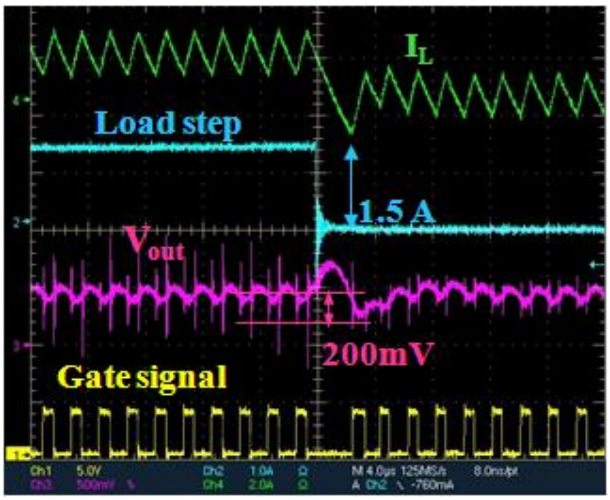

Figure 14 Experimental results. Load step down of 1.5A (1A/div), inductor current I_L (2A/div), output voltage V_{out} (500mV/div) and gate signal (5V/div).

As expected and shown in **Figure 13** and **Figure 14**, the control response is very fast. When the load step occurs the control reacts instantaneously saturating the duty cycle (Figure 13) or keeping the main switch off (Figure 14). Only two switching cycles are needed to reach the new steady state. The output voltage drop is 200 mV, but it must be taken into account that the output capacitor value is only 4µF.

6 Conclusions

The control proposed is based on the capacitor current-injected control described in [3] but using a non-invasive output capacitor current sensor [4]. The advantages of this control are: constant switching frequency, fast dynamic response, since it behaves as a feed-forward of the load

current and low sensitivity to parasitics due to slope compensation. As shown in simulations at 5MHz switching frequency, the proposed control with a voltage loop of 50 kHz bandwidth has the same voltage drop as a 1 MHz bandwidth linear voltage mode control. Their dynamic responses are also similar. That means 20 times less bandwidth making easier the implementation and design of the control. This control is very appropriate for high switching frequency applications like integrated DC/DC converters. Finally, experimental results have verified the fast dynamic response of the proposed control under load steps.

7 References

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