Fast control technique based on peak current mode control of the output capacitor current

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***Abstract* -- The control proposed and analyzed in this paper is based on the peak current mode control of the output capacitor current of a Buck converter. The output capacitor current loop provides fast dynamic response to the control since it behaves as a feed-forward of the load current while the voltage loop provides accurate steady state regulation. A simulation oriented averaged model of the proposed control has been developed to design the external voltage loop. As shown in simulations, with the converter switching at 5 MHz, the proposed control with a voltage loop of 50 kHz bandwidth has the same voltage drop and a similar dynamic response as a 1 MHz bandwidth voltage mode control. The reduction of the bandwidth makes easier the control implementation and integration. Finally, experimental results have been achieved verifying the fast dynamic response of the proposed control under load steps.**

***Index Terms*-- DC/DC converters, high switching frequency, fast dynamic response, output capacitor current and integration.**

I. INTRODUCTION

Nowadays, many power supplies applications demand fast dynamic response. However, the high bandwidth needed, if a linear control is used, is difficult to obtain because of parasitic effects, component variation and non-idealities of the error amplifier. One technique to face up to these limitations is the combination of non-linear and linear control [1], [2].

Well known non-linear strategies are V^2 ([2] and [3]) or hysteretic control [3] of the output voltage. Both require sensing the output voltage ripple, which is very small compared to the dc value and it is very sensitive to parasitic effects. It is also required to have a triangular output ripple given by the ESR (ESR must be dominant or it will be required an additional resistor that worsens the regulation under load changes).

The non-linear and linear control scheme proposed in [1] is based on a hysteretic control of the output capacitor (C_{out}) current of a Buck converter. It achieves a faster control action under load steps since the output capacitor current reacts instantaneously (Fig. 1). The problem is to measure the output capacitor current but it can be estimated with the non-invasive method described in [4]. This control technique has very fast dynamic response under load steps. However, this method suffers some limitations: variable frequency, restricted operation by the hysteretic bandwidth and sensitivity to current sensor mismatches [4].

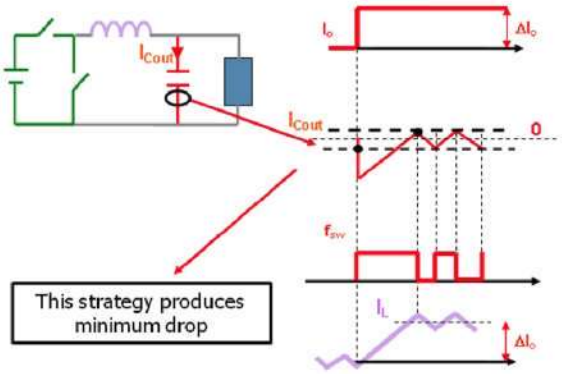

Fig. 1. Hysteretic control of the output capacitor current.

The control proposed in this paper avoids these problems. It is based on the capacitor current-injected control described in [5] but using a non-invasive output capacitor current sensor [4]. With the proposed control the dynamic response is fast and the required bandwidth in the voltage loop is low. This fast response can be used in high frequency converters (5MHz) to reduce the output capacitor, making easier the integration.

The main contribution of this paper is the development of a simulation oriented averaged model and the real implementation in a prototype of the peak current mode control of the output capacitor current based on a non-invasive sensor.

II. NON-INVASIVE OUTPUT CAPACITOR CURRENT ESTIMATION

The non-invasive capacitor current estimation method described in [4], and used in the control proposed in this paper, consists of a RLC network. The basic idea is to use an RLC network in parallel with the output capacitor to measure the current by matching phases, time constants and scaling impedances. The current in the parallel network of the output capacitor is proportional to the C_{out} current (Fig. 2). The physical implementation of the RLC network is done with a

trans-impedance amplifier as shown in Fig. 3 and the voltage obtained at the sensor output (V_S) is proportional to the output capacitor current (I_{Cout}).

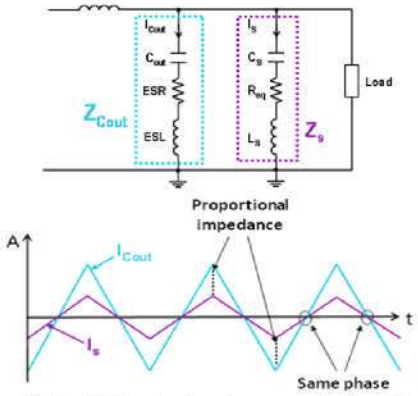

Fig. 2. RLC network and sensor matching. [4]

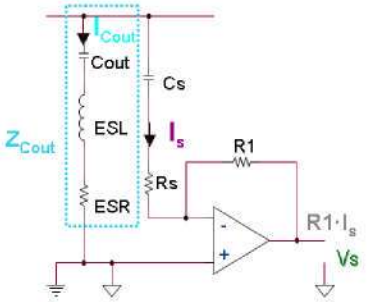

Fig. 3. Physical implementation of the capacitor current sensing method (RLC network). [4]

III. Proposed Solution

A. *Operating principle of the proposed control*

The control proposed and analyzed in this paper is based on the peak current mode control of the output capacitor current [5] of a Buck converter (Fig. 4).

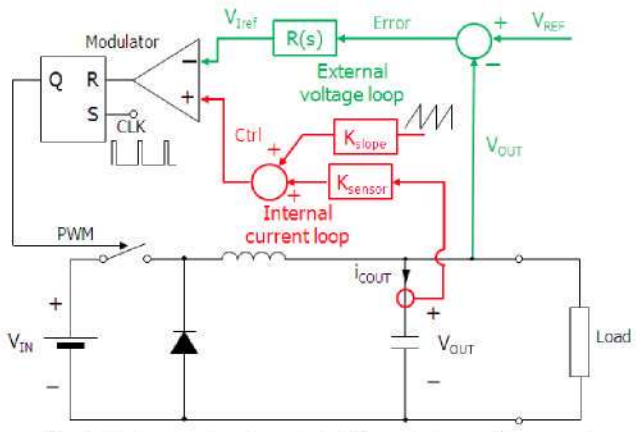

Fig. 4. Peak current mode control of the output capacitor current.

The output capacitor current is sensed with the non-invasive method described in [4]. The control signal (addition of the sensor signal and the compensating slope) is compared with the output signal from the voltage loop error amplifier (V_{Iref}). When the control signal reaches the reference, the main MOSFET switches off. Then, due to the RS latch, when the period finishes the main MOSFET switches on (Fig. 5). Hence, this control prevents from the problem of variable frequency. The output capacitor current loop provides fast dynamic response to load transitions since it behaves as a feed-forward of the load current while the voltage loop provides accurate steady state regulation. The limitation of the current mode control is that for duty cycles higher than 50% a sub-harmonic oscillation appears, so compensating slope must be added (Fig. 5) to prevent it. Besides, this compensating slope helps to desensitize this technique to current sensor mismatches and parasitic effects. On the other hand, the higher the slope compensation, the worst the dynamic response, being a design trade-off

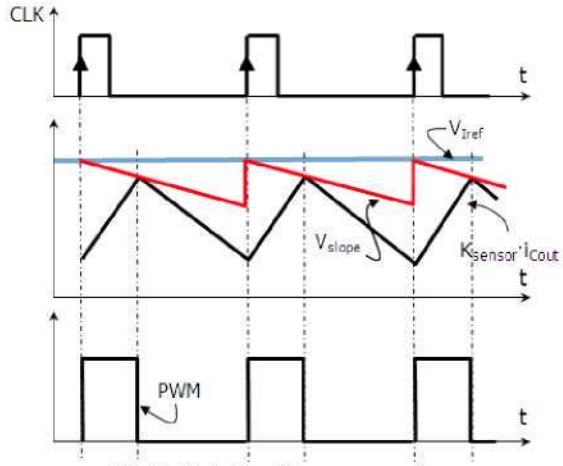

Fig. 5. Modulator. Slope compensation.

B. *Averaged model of the proposed control*

One of the advantages of the control proposed is that the voltage loop doesn't need a high bandwidth to achieve fast dynamic response since the current loop behaves as a feed-forward of the output current.

A simulation oriented averaged model of the peak current mode control [7] of a buck converter (Fig. 6) has been developed in order to obtain the reference (V_{Iref}) to output voltage (V_{out}) frequency response and design a regulator to close the external voltage loop.

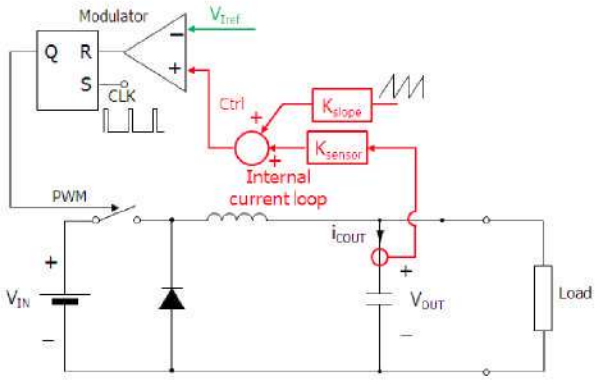

Fig. 6. Circuit to be modeled: buck converter with peak current mode control of the output capacitor current.

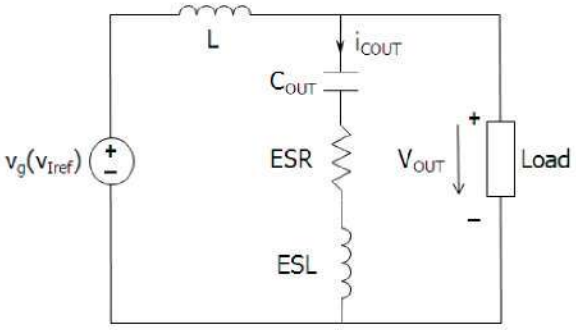

Fig. 7. Averaged model of the proposed control with the current loop closed.

The power supply v_g in the averaged model (Fig. 7) is a dependent source whose mean value is:

$$\langle v_g \rangle = v_{in} \cdot d \tag{1}$$

where v_{in} is the instantaneous input voltage and d the instantaneous duty cycle.

The instantaneous value of the reference (v_{Iref}) is calculated as the output capacitor current peak value with the addition of a compensating slope (Fig. 6) as shown in (2):

$$v_{Iref} = K_{sensor} \cdot \left(< i_{Cout} > + \frac{v_{in} - v_{out}}{2 \cdot L \cdot f_{sw}} \cdot d \right) + V_{DC\_slope} + V_{pp\_slope} \cdot (d - 0.5) \tag{2}$$

where K_{sensor} is the sensor gain, $<ic_{out}>$ the mean value of the output capacitor current, v_{in} the instantaneous input voltage, v_{out} the instantaneous output voltage, L the output filter inductance, f_{sw} the switching frequency, d the instantaneous duty cycle, V_{DC_slope} the compensating slope DC value and V_{pp_slope} the compensating slope peak to peak value.

Finally, the value of $<v_g>$ is obtained working out the variable d in (2) and introducing it in (1).

In Fig. 8 is shown the reference (V_{Iref}) to output voltage (V_{out}) frequency response obtained for a buck converter with the simulation oriented model and the following specifications: V_{in}=3V, V_{out}=1V, f_{sw}=1MHz, L=830nH and C_{out}=130µF.

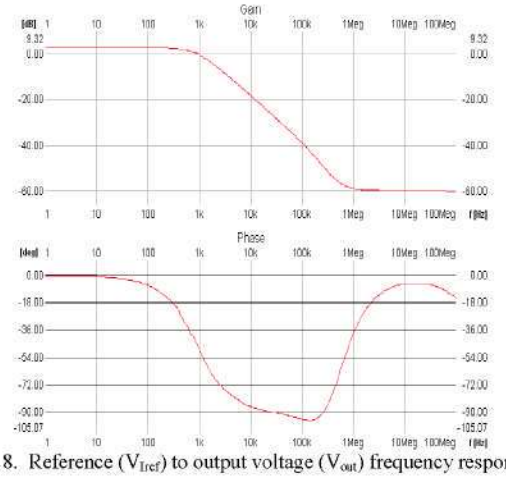

Fig. 8. Reference (V_{Iref}) to output voltage (V_{out}) frequency response.

Finally, the accuracy of the averaged model has been validated in simulation (Fig. 9) with a regulator designed for a bandwidth of 10kHz.

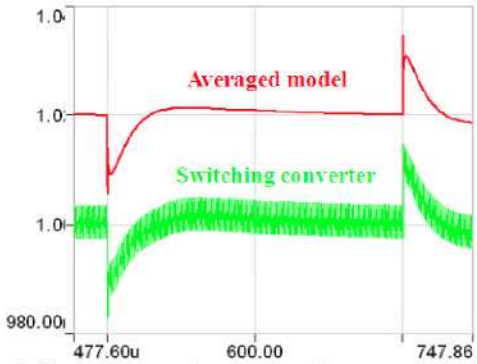

Fig. 9. Switching converter and averaged model output voltage response in closed loop under load step (2A).

C. *External voltage loop design*

Regarding the averaged model developed the voltage regulator has been designed for two external voltage loop bandwidths: 10 kHz and 50 kHz. With a buck converter with V_{in}=3V, V_{out}=1V, f_{sw}=1MHz, L=830nH and C_{out}=130µF, Fig. 10 and Fig. 11 show the simulated response of the proposed control with the slow (ΔB=10kHz) and fast (ΔB=50kHz) voltage regulators. The voltage drop is similar in both cases and very low (18mV) (Fig. 10) providing faster recovery time the faster voltage loop (ΔB= 50kHz), as expected. The control response is very fast and the inductor current changes rapidly (Fig. 11), thanks to the output capacitor current loop.

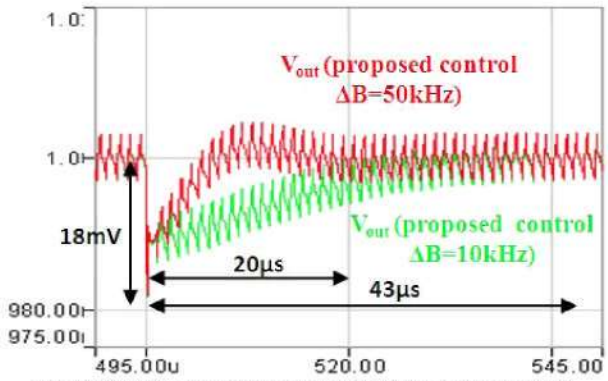

Fig. 10. Output voltage response under a 10A/µs load step (2 A).

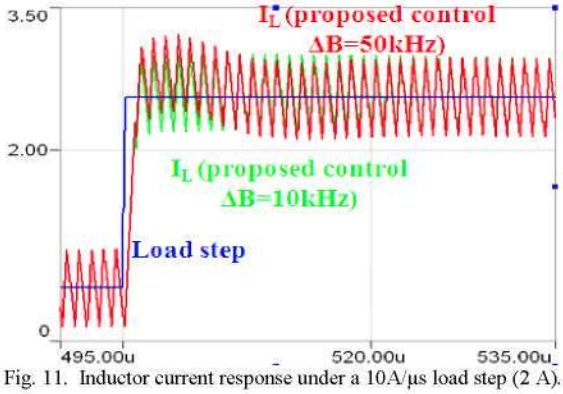

Fig. 11. Inductor current response under a 10A/µs load step (2 A).

The response of the control with the 50KHz bandwidth regulator is detailed in Fig. 12. The control signal is the sensed output capacitor current with the addition of the compensating slope. The compensating slope amplitude should be high enough to avoid sub-harmonic oscillations over 50% duty cycles and parasitic effects, but also it should be low enough to reduce the influence on the system dynamic response. When the load step up occurs this control signal goes down immediately, as it does the output capacitor current. The reference signal obtained in the external voltage loop changes since there is an error between the output voltage and the reference voltage until the new steady state is reached.

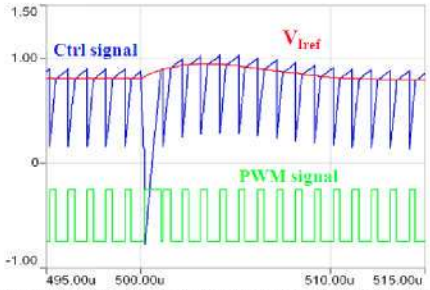

Fig. 12. Reference, control and gate signal response under a 10A/µs load step (2 A). Control signal is the sensed I_{Cout} with the addition of the compensating slope.

IV. Comparison Of The Proposed Control With A High Bandwidth Voltage Mode Control

The proposed control (with an external voltage loop designed with a bandwidth of 50 kHz) is compared with a fast voltage mode control. This comparison is done through simulations in a buck converter being V_{in}=3V, V_{out}=1V, f_{sw}=1MHz, L=830nH and C_{out}=130µF.

As shown in simulations (Fig. 13 and Fig. 14), a similar dynamic response and voltage drop have been achieved comparing the proposed control scheme with an external voltage loop of 50kHz and a voltage mode control with a bandwidth of 200kHz. That means a bandwidth four times lower with the proposed control, making easier the implementation and integration of the system.

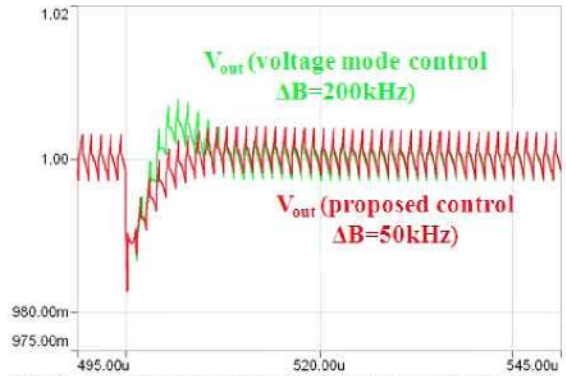

Fig. 13. Output voltage response under a 10A/µs load step (2 A).

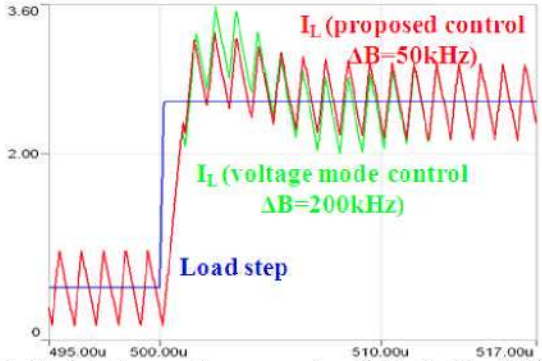

Fig. 14. Inductor current response under a 10A/µs load step (2 A).

In Fig. 15 and Fig. 16 the Bode plots of the closed loop response of both controls are shown.

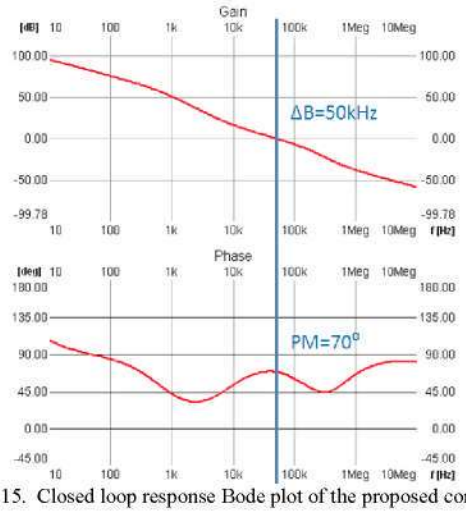

Fig. 15. Closed loop response Bode plot of the proposed control.

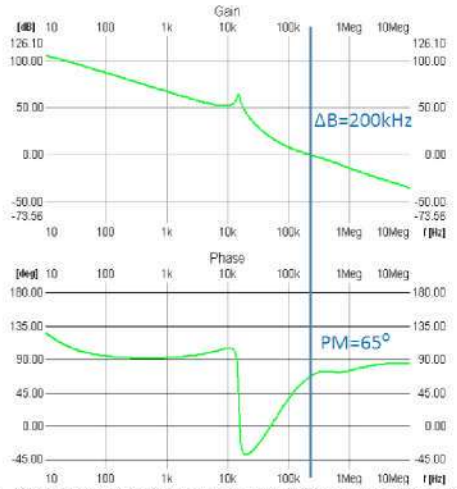

Fig. 16. Closed loop response Bode plot of the voltage mode control.

If the converter switching frequency is 5MHz, the comparison becomes more interesting. In this case, V_{in}=3V, V_{out}=1V, f_{sw}=5MHz, L=100nH, C_{out}=10µF. In order to compare the control response at 5MHz switching frequency with the previous 1MHz switching frequency the bandwidth should be higher in the voltage mode control. However, at high frequencies, the maximum bandwidth is limited by the output capacitor parasitic components and tolerances. The capacitor used has the following parasitic values: ESR=2m• and ESL=1nH. The open loop response of the voltage mode control is shown in Fig. 17. The maximum bandwidth is limited by the resonant frequency due to the parasitic ESL of the output capacitor (f_{res}=1.6MHz), hence the bandwidth has to be reduced to avoid instabilities in closed loop.

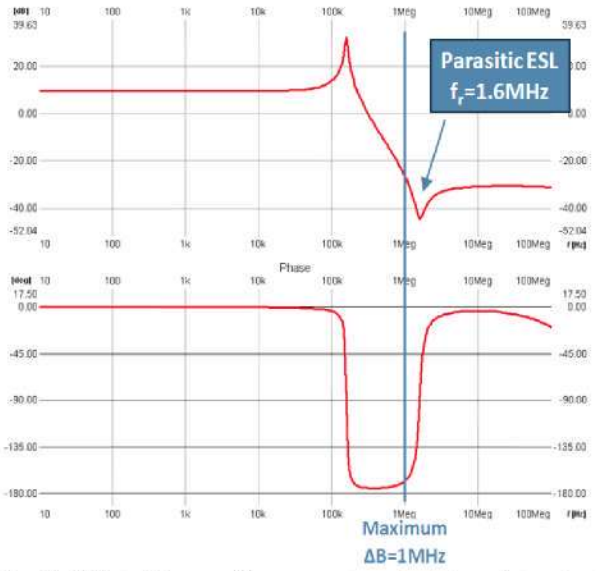

Fig. 17. Effect of C_{out} parasitic components on the duty cycle to output voltage frequency response.

Hence, the comparison is now done between the proposed control with a bandwidth of 50 kHz and the voltage mode control with a bandwidth of 1MHz, far enough from the resonant frequency to avoid instabilities. As shown in Fig. 18 and Fig. 19, the proposed control with an external voltage loop of 50kHz bandwidth has the same voltage drop as a 1MHz bandwidth voltage mode control. Their dynamic responses are also similar. With a switching frequency of 5MHz and 1MHz bandwidth in the voltage mode control the components size can be reduced. From the practical point of view the design and implementation of 1MHz linear control is difficult due to parasitic effects, while 50kHz is easier to obtain (20 times less bandwidth). Since the bandwidth and components size are reduced the implementation and integration of the whole system, power converter and control, is more feasible.

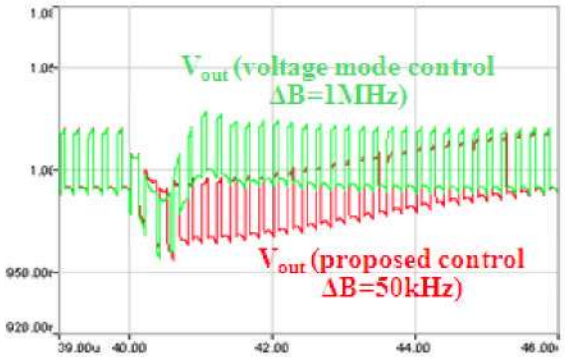

Fig. 18. Output voltage response under a 10A/µs load step (6 A).

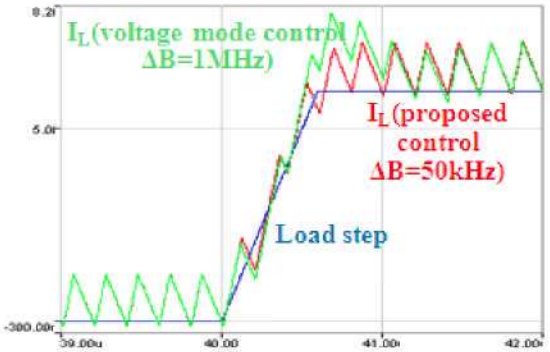

Fig. 19. Inductor current response under a 10A/µs load step (6 A).

V. Experimental Results

The experimental results have been obtained on a buck converter being V_{in}=3V, V_{out}=1V, f_{sw}=1MHz, L=830nH and C_{out}=130µF and an external voltage loop designed for 50kHz. In order to implement the control, a commercial integrate has been used. The maximum switching frequency allowed in these controllers is 1MHz, for that reason this is the switching frequency selected.

As expected and shown in Fig. 20 and Fig. 21 the control response is very fast. When the load step occurs the control reacts instantaneously saturating the duty cycle (Fig. 20) or keeping the main switch off (Fig. 21). The experimental results can be compared with the simulations with the same specifications, obtaining practically same results as shown in Fig. 22 and Fig. 23. The little differences are due to mismatches in the sensor and real bandwidth different to calculated in the experimental prototype. The advantage of the proposed control is that it works properly under these situations.

Since the experimental results agree with the simulations, the same results can be expected at a switching frequency of 5MHz.

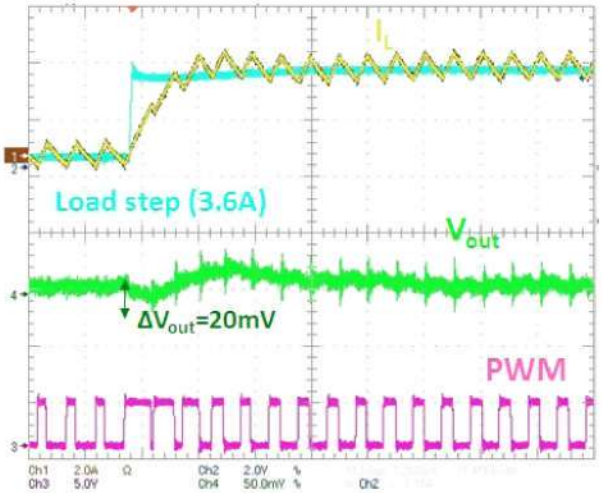

Fig. 20. Experimental results. Load step up of 3.6A (2A/div), inductor current I_L (2A/div), output voltage V_{out} (50mV/div) and gate signal (5V/div) with 2µs/div time scale.

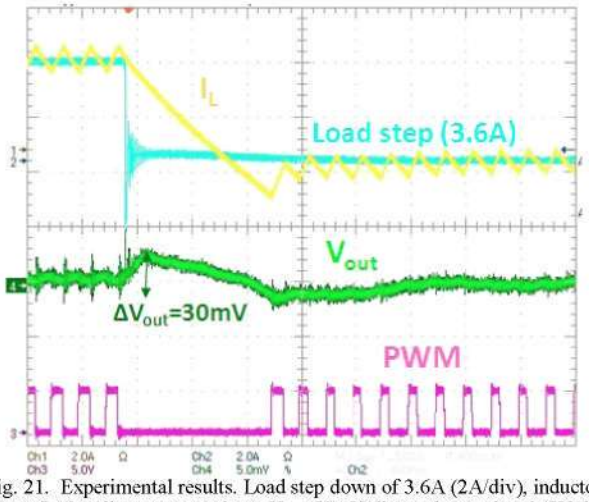

Fig. 21. Experimental results. Load step down of 3.6A (2A/div), inductor current I_L (2A/div), output voltage V_{out} (50mV/div) and gate signal (5V/div) with 2µs/div time scale.

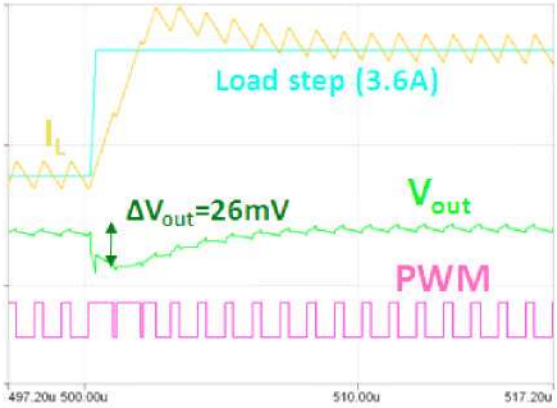

Fig. 22. Simulation results. Load step up of 3.6A

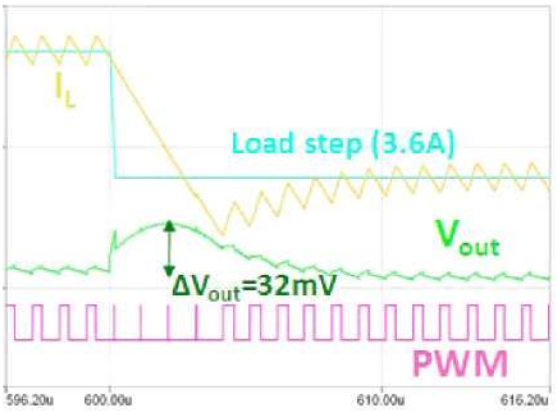

Fig. 23. Simulation results. Load step down of 3.6A.

VI. Conclusions

The proposed control is based on the capacitor current-injected control described in [5] but using a non-invasive output capacitor current sensor [4]. The advantages of this control are: 1) constant switching frequency, 2) fast dynamic response, since it behaves as a feed-forward of the load

current, and 3) low sensitivity to parasitic effects and mismatches due to slope compensation. As shown in simulations, at 5MHz switching frequency, the proposed control with a voltage loop of 50 kHz bandwidth has the same voltage drop as a 1 MHz bandwidth linear voltage mode control. Their dynamic responses are also similar. That means 20 times less bandwidth making easier the implementation and design of the control, avoiding parasitic effects. This control is very appropriate for high switching frequency applications like integrated DC/DC converters since the fast dynamic response allows a reduction in the output capacitors required. Finally, experimental results have verified the fast dynamic response of the proposed control under load steps.

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