Core-less Multiphase Converter with Transformer Coupling

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***Abstract*—A coupled multiphase converter where the coupling among the phases is done using core-less planar transformers is presented in this paper. Operating principle of the transformer-coupled converter has been presented previously in the literature and in this paper this concept is applied to develop a core-less converter. Two prototypes operating at high frequency (4 MHz), with low profile (3mm - 4mm) and 60 W of output power, with two different core-less transformers are presented. Main advantages of applying this concept at high frequency are size reduction and operation with core-less transformers. This topology can be considered as a dc-dc transformer and applications for this topology can be 'dc-dc transformers' for two-stage power supply systems and voltage scaling power supplies.**

I. Introduction

Among the reasons for the interest in core-less converters, reduction of cost and increase of power density are the most outstanding ones. Although design and modeling of core-less transformers is difficult, the lack of ferrite core enables the integration of the whole magnetic element in a silicon die or in PCB tracks, thus enabling important cost reduction and power density improvement. Due to these attractive advantages, several papers in state of the art deal with the design and optimization of core-less magnetic components ([1],[2],[3]).

One of the issues in the design of core-less transformers is that there is not a defined path for the flux in comparison with magnetic-core transformers ([1]). Hence, achievable values for open circuit inductance are much lower than those achieved with the presence of a magnetic core. Open circuit inductance values obtained with core-less transformers and reported in state of the art are typically in the range of nH and up to a few μH. Besides, there are several factors that influence the value of the short circuit inductance in core-less transformers; apart from the winding strategy, the construction technology, the separation between primary and secondary, plus the shape and dimension of the turns ([1], [2]) have a great influence over the short circuit inductance in core-less transformers.

Implementations of core-less power converters can be found in [4]-[7], which are typically operated at high frequencies (MHz range). Multiphase coupled converters can be good candidates for high frequency operation since low phase ripple can be achieved while maintaining a good transient response [8], [9]. Since low ripple helps to keep power losses (both conduction and switching losses) in a low level, high frequency operation could be implemented while achieving acceptable efficiency. This advantage has been considered in [10], where a coupled inductor converter with micro-fabricated magnetic substrates has been implemented and operated at 5 MHz.

In this paper, the design and implementation of a multiphase converter where the coupling among the phases is done by core-less transformers is presented, this topology is operated at high frequency (4 MHz) being the concept previously presented in state of the art ([11], [12]). The main characteristic of this topology is that the coupling between two consecutive phases is done by using transformers instead of coupled-inductors. Since transformers are (ideally) not energy storing elements, the converter can be operated without energy storage, hence, the dynamic response is decoupled from the switching frequency. If the switching frequency and the dynamic response are decoupled, switching frequency becomes a degree of freedom for designing a converter. The main drawback of this topology is that, in order to use transformers as coupling elements, the energy flowing into the transformers should be controlled in certain way, hence, the proposed topology can only be operated at certain duty cycles (operating nodes) and it lacks of regulation capability. The operating principle, advantages and drawbacks of this concept are presented in [11] and [12] (a brief review is done in section II of this paper).

The paper is organized as follows. Main features of the topology are reviewed in section II. Previous to the design of the core-less converter, a prototype has been implemented and tested under two different operating conditions: with EE14 cores and without cores. The details on this setup are presented in section III. The design of the core-less converter is presented in section IV and its experimental validation is presented in section V. Finally, conclusions are given in section VI.

II. Basic operation of transformer coupling topology

As said before, The topology presented in this paper is based on a multiphase transformer-coupled converter. Operating principle of this topology, along with its operating features have been presented in [11] and [12].

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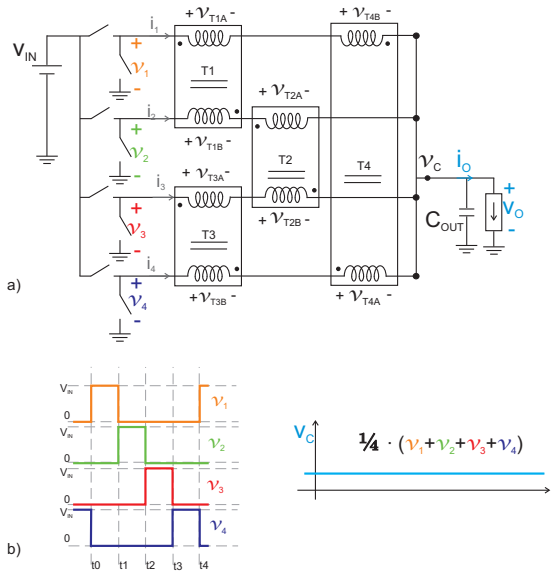

Fig. 1. Proposed multiphase topology with transformer coupling

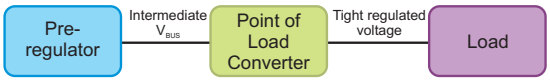

Fig. 2. Proposed topology can be considered to be a good candidate for a pre-regulator in a two-stage power architecture

The main characteristic of this multiphase topology is that the coupling among phases is done using transformers instead of coupled-inductors. Since transformers are considered to be not energy storing elements (ideally), it can be said that the converter operates (ideally) with no energy storage.

The main advantage of 'no energy storage' operation is that the switching frequency and the transient response of the converter are decoupled. If the switching frequency does not limit the dynamic response, it can be chosen in order to optimize, for example, the size or the efficiency of the converter. The main drawback of 'no energy storage' concept is that the converter lacks of regulation capability.

In order to operate the converter (ideally) under no energy storage operation, two conditions must be accomplished:

- For all time, it should be accomplished that the sum of the input voltages to the magnetic structure should be kept constant for every instant of time ($\sum v_i = constant$).
- Mean value of the **voltage across each transformer of the magnetic structure should be zero**, limiting the voltage waveforms (v_i) that can be applied to the input of the magnetic structure.

If the sum of the input voltages to the magnetic structure are constant at any time, output voltage to the magnetic structure (v_C) will be also constant and no output filter will be needed. Output voltage (V_O) is then equal to v_C which is given by:

$$v_C = \frac{\sum v_i}{n} \tag{1}$$

where n is the number of phases. In figure 1 an example of a four-phase converter is presented. Input voltages to the magnetic structure (v_i) are: v_1, v_2, v_3 and v_4. The particularization of equation 1 for a four-phase converter gives that $v_C = \frac{v_1+v_2+v_3+v_4}{4}$ should be kept constant at any time.

The value of $\sum v_i$ is defined by the number of phases that are connected to V_{IN} for a given time. Being k the number of phases connected simultaneously to V_{IN} at any instant of time, it is given that:

$$\sum v_i = k \cdot V_{IN} \tag{2}$$

Substituting 2 into 1 and regarding that $V_O = v_C$:

$$V_O = \frac{k \cdot V_{IN}}{n} \tag{3}$$

This equation can be particularized for a four-phase topology with $n = 4$ and available values for k are integers from 0 to 4. This implies that a four-phase topology with transformer coupling can be operated only at the following duty cycles: 0%, 25%, 50%, 75% and 100%. It is important to point out that the multiphase transformer-coupled topology is always operated in open loop.

Input and output voltages to the transformers for a four-phase converter ($n = 4$) operating with 25% duty cycle are shown in Figure 1b. For this duty cycle, only one phase is connected to V_{IN} at any instant of time, hence, $k = 1$. Output voltage level is given in equation 4 which is obtained by substituting these values in eq. 3:

$$V_O = \frac{1 \cdot V_{IN}}{4} \tag{4}$$

The response of the converter is, ideally, instantaneous regardless of the switching frequency, the equivalent short circuit inductance of the transformers, actually limits the transfer of the energy in the converter. An analysis on the impact of this inductance in the dynamic response is done in [12].

Due to its features, this kind of converter can be used as a step-down converter in two-stage architectures ([13]). An example of this kind of power architecture is shown in figure 2. In examples of state of the art, first stage or pre-regulator is usually a high efficiency topology ([14]) used to step down the input voltage. If the two-stage system is well designed, it can improve the overall efficiency of single stage power supplies, as done in [14]. Another example of application for the proposed topology can be in systems where input voltage modulation leads to energy savings (for example DVS or RF systems power modulation technique - such as Envelope Elimination or Restoration [15]). An example of an application of the proposed converter for power modulation in an RF system is shown in [16].

Based on transformer-coupling topology, a high frequency prototype has been designed. With high frequency operation, it is possible to use low inductance values, which enables the

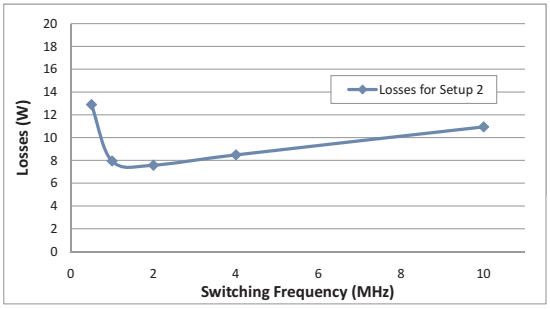

Fig. 3. Power losses calculation for specifications of Setup 2. Based on this analysis, the frequency where the converter operates with less losses is around $2MHz$ - $4MHz$

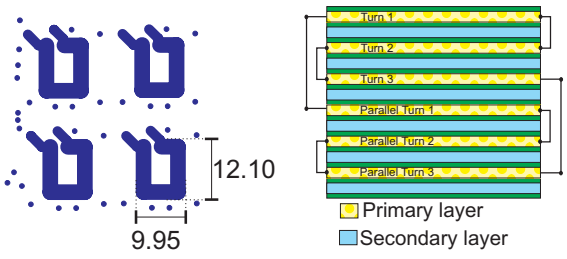

Fig. 4. Layout of the transformers in the PCB (dimensions are in mm). Four transformers are identical. Construction details are also illustrated.

use of core-less transformers. In this paper, two prototypes with different core-less transformers configurations are presented. Since the prototype is intended for high current (10 A), it is very important to keep conduction losses in low level. Hence, one of the main constraints when designing the core-less transformers is to find an adequate trade-off between the open circuit inductance and the equivalent series resistance.

III. Comparison of Multiphase Transformer-Coupled Converter Using Core and Core-less Transformers

In this section, the use of core-less transformers in the proposed topology is explored with an experimental approach. In order to evaluate advantages and drawbacks of a core-less topology implementation, a four-phase prototype has been designed using multilayer technology. In this prototype, the turns for the transformers are integrated into the PCB. One turn for layer has been placed. The shape of the turns can be seen in fig. 4. Both setups have been tested using the same PCB. A picture of this 12-layer PCB is shown in figure 5 and the details on the construction of the transformer are shown in figure 4. From this figure, it can be seen that there is only one turn per layer. The primary (as well as the secondary) is comprised by three turns connected in series. There are two identical windings connected in parallel for the primary, and two identical parallel windings for the secondary. Turns ratio of the transformer is 1:1 and height of the copper layers is $70\mu m$ for all the tracks.

Although the design of the transformer windings is the same

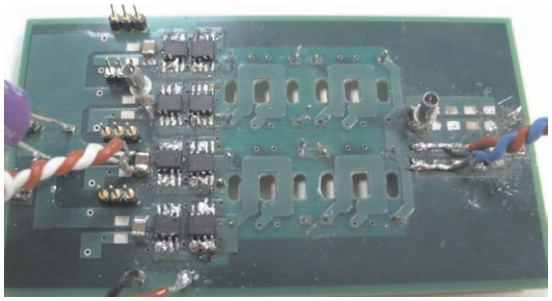

Fig. 5. PCB for testing setups 1 and 2: in *Setup 1* EE14-3F4 cores have been used, while in *Setup 2* no magnetic core is used.

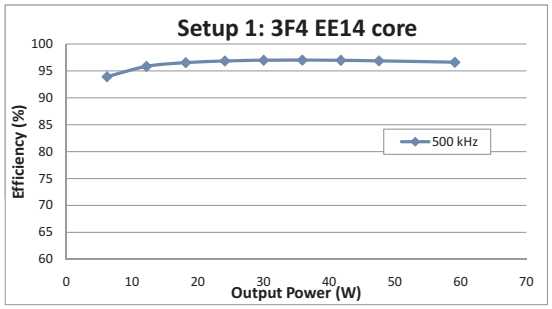

Fig. 6. Efficiency for optimum operating frequency (500 kHz) of *Setup 1*. Open circuit inductance is equal to $6\mu H$. Input voltage is $12V$ and output voltage is $6V$

for both *Setup 1* and *Setup 2*, the values for the measured open circuit inductances are different, regarding if the magnetic core is placed or not. For *Setup 1*, EE14-3F4 cores are used while for *Setup 2* no core is placed. Since for both setups the value of the open circuit inductance is different, the nominal operating frequency for each setup is also different.

A. Setup 1: EE14 core converter

Setup 1 is built based on the following specifications:

- V_{IN}=12 V. Since it is a four phase converter, available output voltage levels (according to the operation principle of this topology) are: $3V$, $6V$ and $9V$.
- I_{OUT}= 10 A is the maximum output current for this converter.
- $EE14-3F4$ core is used in this setup.
- $L_{OC}=6\mu H$ is the open circuit inductance with $N=3$ and the selected core.
- $f_{SW}=500kHz$
- Profile: $7.2mm$

Efficiency measurement for this converter at $500kHz$ and with 50% duty cyle ($12V$ to $6V$) is shown in figure 6. It can be seen that efficiency is very high for a wide load frequency; it is higher than 95% for a wide load range: from $2A$ to $10A$ ($12W$ to $60W$).

In figure 7, a load step has been applied to *Setup 1*. With a $22\mu F$ ceramic multilayer capacitor at the output of the converter, the voltage deviation at the output is around 5% of

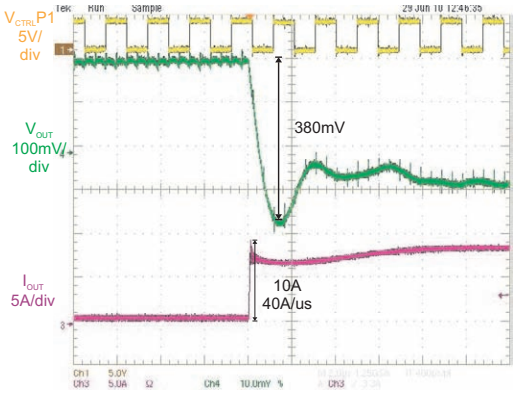

Fig. 7. $10A$ load step has been applied to *Setup 1*. Operating frequency is $500kHz$ and dv/dt of the load step is $\approx 40A/\mu S$

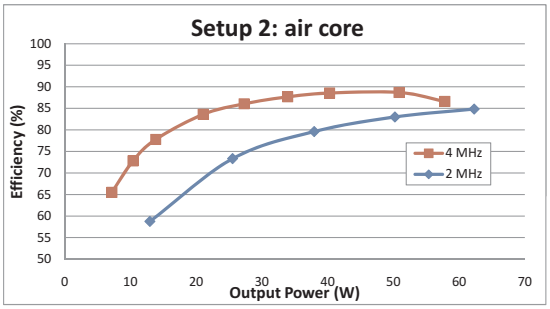

Fig. 8. Efficiency for $2MHz$ and $4MHz$ of *Setup 2*. Open circuit inductance is equal to $70nH$. Input voltage is 12 V and output voltage is 6 V.

output voltage. The input capacitor is formed by one $470\mu F$ oscon and 4x22μF ceramic multilayer capacitors.

B. Setup 2: core-less configuration

For *Setup 2*, input voltage, output voltage and current specifications are the same than for *Setup 1*, however and as mentioned above, no magnetic core is used. With the same winding configuration ($N = 3$ and turns ratio of 1:1) than that for *Setup 1*, but without core, measured open circuit inductance (L_{OC}) is around $70nH$. With this inductance value, a power loss analysis has been done in order to estimate operating frequency where less power losses are obtained. This losses model accounts for conduction losses and switching losses in the converter. Switching losses are calculated based on a model reported in state of the art ([17]). It was found that operating frequency for minimum losses is around $2MHz$.

Efficiency measurements for these operating frequencies are presented in figure 8. Compared to *Setup 2*, lower efficiency is achieved; from output power of $30W$ to full load ($60W$) frequency is higher than 85%.

A load step of $10A$ is applied to this setup and the response of the converter is shown in the waveform of figure 9. If the responses of both setups are compared, it can be seen that, under the same load step, both responses are similar, since the short circuit inductance measured in both setups is very similar (around $40nH$).

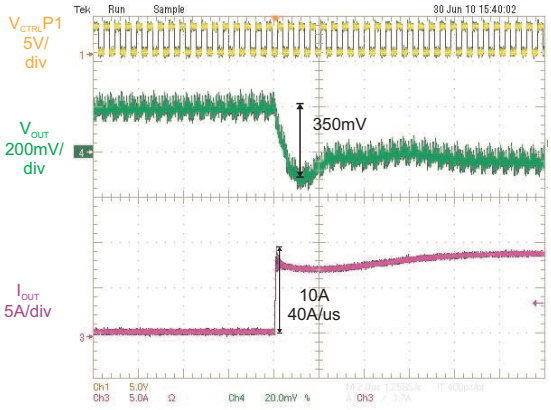

Fig. 9. $10A$ load step has been applied to *Setup 2*. Operating frequency is $2MHz$ and dv/dt of the load step is $\approx 40A/\mu S$

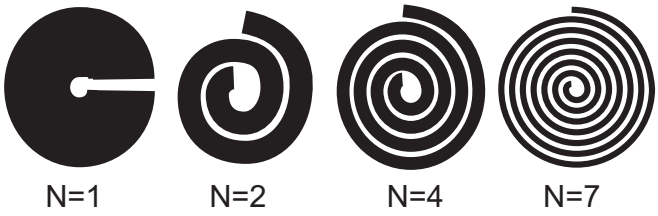

Fig. 10. Spiral-shaped turns for core-less transformer design. Inner and outer dimensions are fixed while turns number and width of the tracks have been changed. Separation between the tracks is defined by the PCB technology ($200\mu H$)

Although with *Setup 2*, lower efficiency is achieved, the profile of the converter has been reduced, from $7mm$ to $3mm$ while keeping the same output power. This result motivates the development of a core-less converter with the aim of obtaining further improvements in efficiency and size. In order to do this, a core-less transformer has to be designed. This design is based in results from state of the art ([2],[3]). The design process is aided by a 2D Finite Element Analysis simulator, PEmag ([18]) and it is presented in the following section.

IV. Design of Core-less Multiphase Converter with Transformer Coupling

Based on the design guidelines given in [2] and [3], the design for a core-less transformer is done in agreement with the requirements of the topology presented in section II. In this case, the main criteria for designing the transformers is to maximize the open circuit inductance while minimizing the short circuit inductance and the resistance of the windings. Multilayer technology is chosen for the design of this core-less prototype. Evaluated setups for these transformers are shown in figure 10. These setups have been evaluated with the 2D FEA modeler, PEmag [18]. For the design of this transformers, all the turns for the primary winding are going to be placed in the same layer; same consideration is applied to the secondary, since both windings are identical for all the analyzed cases. In order to reduce DC resistance, placing identical layers and connecting them in parallel was the final stage of the design.

TABLE I
SIMULATED VALUES FOR: OPEN CIRCUIT INDUCTANCE (L_{OC}), DC RESISTANCE (R_{DC}), SHORT CIRCUIT INDUCTANCE (L_{SC}), AND AC RESISTANCE (R_{AC}) FOR WINDINGS WITH DIFFERENT TURNS NUMBER

	$N=1$	$N=2$	$N=4$	$N=7$
L_{OC}	$8nH$	$35nH$	$155nH$	$500nH$
R_{DC}	$2m\Omega$	$8.9m\Omega$	$37m\Omega$	$130m\Omega$
L_{SC}@$2MHz$	$1.5nH$	$6nH$	$27nH$	$86nH$
L_{SC}@$4MHz$	$1.4nH$	$6nH$	$27nH$	$84nH$
L_{SC}@$8MHz$	$1.4nH$	$6nH$	$27nH$	$81nH$
R_{AC}@$2MHz$	$4m\Omega$	$23m\Omega$	$100m\Omega$	$300m\Omega$
R_{AC}@$4MHz$	$5.4m\Omega$	$30m\Omega$	$140m\Omega$	$410m\Omega$
R_{AC}@$8MHz$	$7.5m\Omega$	$42m\Omega$	$195m\Omega$	$583m\Omega$

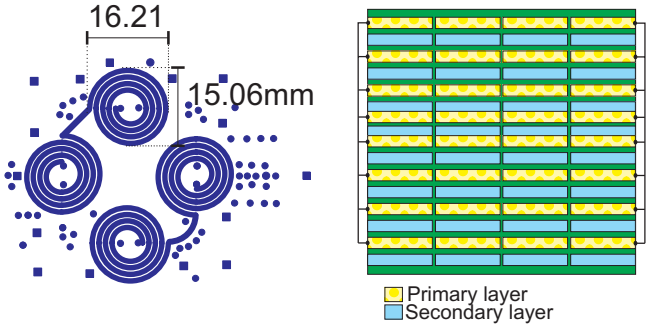

Fig. 11. Layout of the core-less transformers and construction details. The transformer is comprised by 16 layers: Eight parallel layers have been placed for primary winding; secondary is also formed of 8 parallel layers. 4 serial Turns are placed in each copper layer.

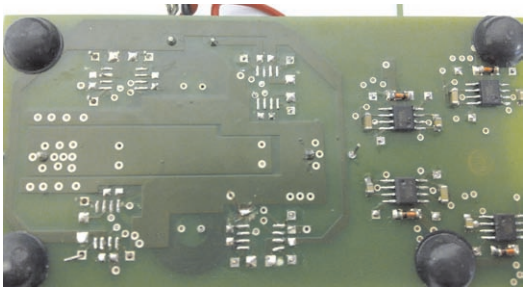

Fig. 12. Picture for core-less prototype. Output power for this converter is 60W and a very low profile is achieved (4 mm)

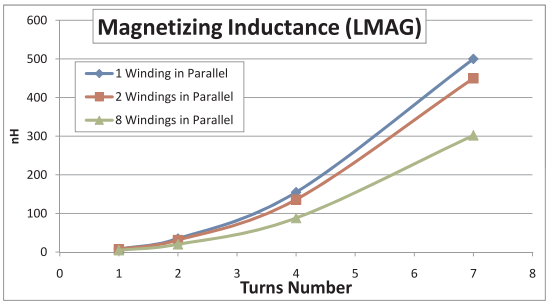

Fig. 13. Open circuit inductance reduces with parallel windings. In this graph, the effect of the parallel windings for different number of turns is presented

Fixed parameters for doing this analysis are:

- turns ratio, which is 1:1
- shape of the transformer
- inner diameter
- outer diameter
- separation between copper (fixed by the chosen technology to $200\mu m$)
- separation between primary and secondary (fixed by the chosen PCB technology)

The parameters that are changed in order to do this analysis are:

- turns number
- number of parallel windings
- width of the turns

Width and number of the turns are changed together, in order to keep constant the inner and outer radio of the core-less transformer. Less number of turns means wider tracks and vice versa. First of all, different number of turns are evaluated using 2 layers construction; evaluated turns number are $N =$ 1, 2, 4 and 7, these setups are shown in figure 10. As said before, the aim of the design of this core-less transformer, is to achieve a high open circuit inductance (L_{OC}) while keeping resistances (both DC and AC) in a low level. Besides, it is important to reduce short circuit inductance (L_{SC}) with the use of an appropriate interleaving strategy and by minimizing the distance between primary and secondary. The results of this analysis are reflected in table I. Conclusions obtained from this analysis are the following:

- Open circuit inductance. The value of L_{OC} is directly proportional to the number of turns.
- DC resistance. This resistance is also proportional to the number of turns, achieving a higher inductance means an increment in the DC resistance and hence in the losses related to it.
- AC resistance. High frequency effects are more noticeable when width of the tracks is smaller. Since, increasing turns for a fixed area implies a reduction in the width of the track, it can be said that for this application, less turns are preferred from the point of view of the AC resistance.
- Short circuit inductance. L_{SC} is higher when the number of the turns is increased. As mentioned before, higher number of turns means smaller width. Both effects contribute to increase short circuit inductance. In order to minimize short circuit inductance, less turns are preferred. It is important to point out, that when parallel windings are considered, the use of an interleaving strategy will contribute to reduce the value of L_{SC}.

From this analysis, the chosen configuration for building the transformer is $N = 4$. It is considered that this winding setup has a convenient trade-off between L_{OC} and resistance. Regarding parallel windings, the transformer is comprised

by eight paralleled primary windings and eight paralleled secondary windings. By doing this, the R_{DC} is divided by 8. In figure 11, the layout and the construction details of the core-less transformers are shown.

V. Experimental results

As a result of the previous analysis, a four-phase converter with four core-less transformers is implemented. These transformers are built with 16 layers and the construction details along with the layout of the four transformers is shown in figure 11. A picture of the prototype is shown in figure 12. Core-less prototype specifications are the following:

- Measured open circuit inductance (L_{OC}) is $90nH$
- Switching frequency of the converter is $2MHz$ - $4MHz$
- Profile of this converter is: $4mm$

It is important to point out, that the measured value for the open circuit inductance is much lower than that predicted by the FEA simulator with the 2-layer setup. In order to explain this, simulations featuring the complete transformer (all 16 layers) were run. The result of this simulations is shown in figure 13. It can be seen that the obtained open circuit inductance decreases when more parallel windings are placed. For higher number of turns, this effect is more pronounced. With the result of this analysis it is necessary to point out, that another trade-off between open circuit inductance and DC resistance has to be considered for future designs. It is important to point out that simulated value for L_{OC} when 8 parallel windings are considered for each winding (both primary and secondary) corresponds accurately with the measured open circuit inductance.

Since open circuit inductance is very similar to the one in *Setup 2* from section III, the results obtained with this converter are also very similar to those achieved with *Setup 2*. Efficiencies for 25% and 50% duty cycle are shown in figures 14 and 15 respectively. It can be seen that for 50% duty cycle, efficiency is higher than 85% from 30 W to full load, however, efficiency is almost 90% from 35 W to 50 W of output power.

Dynamic response of this topology is also very similar to the response of the former prototype; less than 5% of output voltage deviation is achieved with one $22\mu F$ capacitor at the output and $470\mu F$ plus four $22\mu F$ ceramic capacitors at the input. Applied load step is 10 A with a di/dt of approx. $40A/\mu s$. This waveform is shonw in figure 16.

Steady state waveforms of the current of all phases and the output voltage are provided in figures 17 and 18.

VI. Conclusions

In this paper, a multiphase transformer-coupled converter is proposed for high frequency operation. In this topology, the coupling of the phases is done with transformers. Since transformer do not store energy (ideally), the converter operates without energy storage and the dynamic response is decoupled from the switching frequency. Switching frequency then becomes a degree of freedom and it can be selected in order to optimize efficiency or size. Based on this topology, a

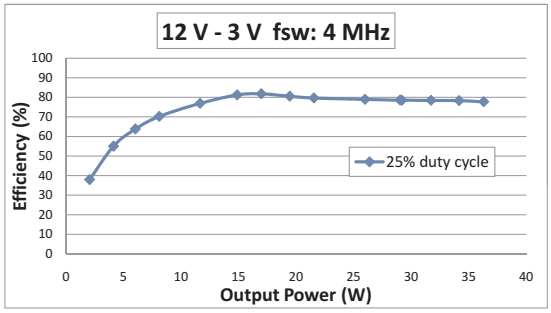

Fig. 14. Experimental measurements for core-less prototype, 12 V input and 3 V output

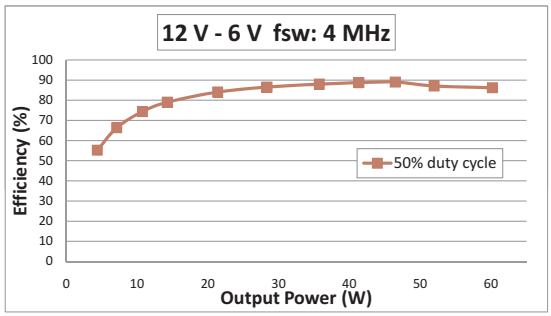

Fig. 15. Experimental measurements for core-less prototype, 12 V input and 6 V output

prototype where efficiency is prioritized in the design, provides a very high efficiency in a wide load range ($\eta > 95\%$ from $12W$ to $60W$), being 500 kHz the f_{SW}. On the other hand, another prototype based on the same topology is designed in order to optimize size and to minimize the profile of the converter. Based on this criteria, a converter with very low profile ($4mm$) and high frequency ($4MHz$) operation is designed. Output power of this converter is also $60W$ and the efficiency is almost 90% from 35 W to 50 W. Also, design guidelines for core-less converters for the proposed topology

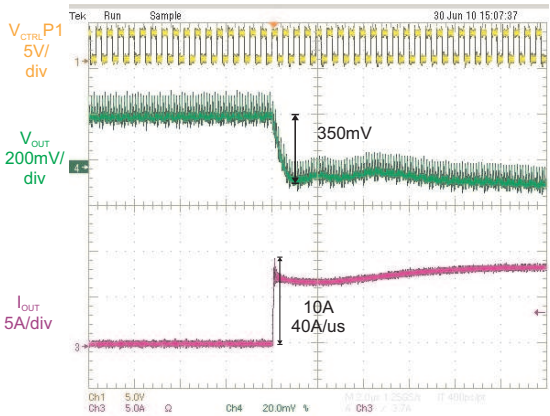

Fig. 16. $10A$ load step has been applied to core-less prototype. Operating frequency is $500kHz$ and dv/dt of the load step is $\approx 40A/\mu S$

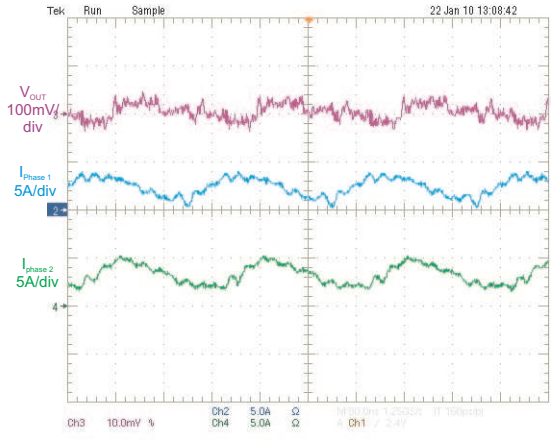

Fig. 17. Steady state waveforms of core-less converter. Output voltage ripple is shown. Currents of phases 1 and 2 are also shown when load is $10A$ and output voltage is $3V$

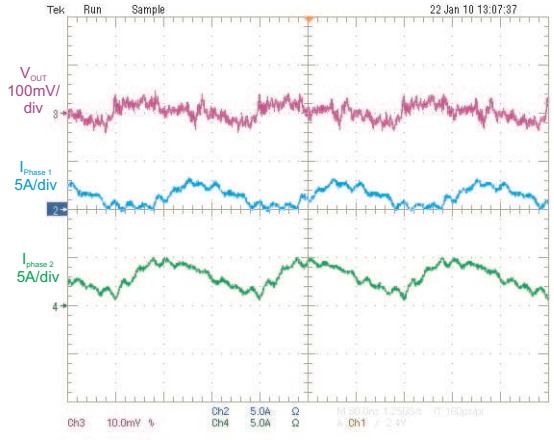

Fig. 18. Steady state waveforms of core-less converter. Output voltage ripple is shown. Currents of phases 3 and 4 are also shown when load is $10A$ and output voltage is $3V$

are obtained. From this guidelines it is concluded that the key parameters in order to obtain the desired open circuit inductance (L_{OC}) are: number of turns, length of the tracks and parallel layers. In order to minimize the losses in the converter, these parameters should be carefully designed to obtain the adequate trade-off between open circuit inductance and resistance. It is important to take into account that adding parallel windings can reduce the L_{OC}.

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