

High Power Wideband Class-E Power Amplifier

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Abstract—This letter shows a high-power, high-efficiency, wideband Class-E RF power amplifier designed upon the load admittance synthesis concept and built using an uncomplicated low-loss load network with a low loss wideband admittance transformer as the main component. It uses a power Silicon LDMOS transistor to provide up to 145 W at 28 V peak power, up to 86% drain efficiency over 35% fractional bandwidth (from 85 to 120 MHz) and 15.6 dB gain at peak power without any adjustments. These are clear performance advantages over previous published works and commercially available amplifiers at a similar frequency band and power level. The amplifier applications include FM broadcast, aeronautical communications, nuclear, MRI, heating or RF power stage for Envelope Elimination and Restoration transmitters.

Index Terms—Aeronautical, broadband amplifiers, broadcasting, Class-E, EER, power amplifiers (PAs).

I. INTRODUCTION

HIGH efficiency, wideband power amplifiers (PAs) can help to reduce power consumption, size and thermal requirements of communications equipments better than any other circuit or system. In practice, the maximum efficiency that can be achieved for an RF PA depend on several factors such as working frequency, fractional bandwidth, maximum power and linearity, in such a way that the higher the frequency, output power, bandwidth and linearity the lower the efficiency of the amplifier.

Although several circuits and techniques have been devised to design high efficiency PAs, in practice the performance of those amplifiers is usually lower than expected, and the improvement over conventional, less complicated PAs is limited. As a consequence, it is still usual to find new PA designs based on techniques dating from the thirties [1] that do not take advantage of new design concepts and advancements.

There are several reasons that practical RF PAs are unable to achieve the high efficiency levels predicted by theory [2], most of them direct or indirect consequences of the low load impedances required by high power transistors at the fundamental and harmonics. Among the so called high efficiency amplification classes, Class-E [3] has proven to be specially suitable for RF and microwave high efficiency power amplification because of

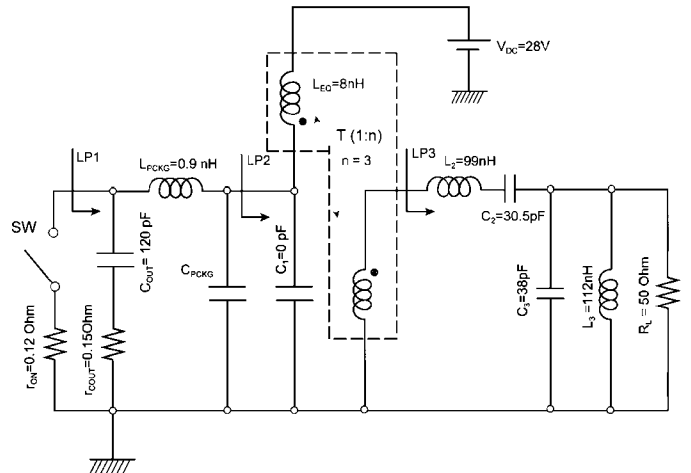


Fig. 1. Scheme of the amplifier output circuit.

its inherent tolerance to active-device parasitics, specially evidenced at high frequencies, such as the transistors output capacitance C_{OUT} and non-zero switching times. There are interesting examples in the technical literature of wideband Class-E VHF PAs but all of them are in the tens of watts power range [4], [5], or they do not offer unquestionable efficiency improvement in comparison to conventional Class-C designs at this frequency band [6]. In this letter, a new wideband high power Class-E VHF amplifier is shown. Its output power is in the hundreds of watts range and its peak measured drain efficiency is 86%. To the best of the author's knowledge this is a significant improvement on previously published high efficiency, high power, wideband amplifiers for the VHF frequency band. Improving drain efficiency of high PAs does not only provide benefits on power savings but on heat management as well, allowing the design of more compact and reliable transmitters.

This amplifier is designed upon the load admittance synthesis concept. This means that the load admittance required by the transistor for close to nominal Class-E operation [7] is provided by a low-loss load network, specially designed to minimize losses and to take advantage of parasitic effects of components to synthesize the load admittance required by the transistor.

II. AMPLIFIER DESCRIPTION

The schematic of the amplifier output circuit is shown in Fig. 1. The amplifier comprises the following few parts:

A. Transistor

The transistor used in this amplifier is a power Silicon LDMOS (MRF6V4300N from Freescale Semiconductors). As of 2010 commercially available Silicon LDMOS technology for VHF combines a relatively high breakdown voltage (about

110 V), an important advantage for Class-E designs that exhibit high peak drain to source voltages 3.56 times higher than the power supply voltage V_{DC} , with low output capacitance and moderate cost in comparison to other solid state technologies such as GaN or SiC. Besides, the MRF6V4300N does not contain a built-in matching network that could preclude the synthesis of the load required for nominal Class-E operation at the fundamental and harmonics. However, the parasitics of the package of this transistor have important influence on the load that can be synthesized at the die load plane of the transistor.

For the sake of simplicity a sinusoidal voltage is used for driving this amplifier but more sophisticated drivers could be used to increase its gain. In this way, the transistor is driven hard enough to make it switch, as required by switch-mode amplification classes such as Class-E.

The transistor is modeled by a simple yet effective model for switching transistors [8] that provides accurate results for switch-mode PAs. Its simplicity is based on the fact that it is focused on modeling the “on” and “off” operation regions of the transistor. This model uses a non linear resistor “ r_{ON} ” to model the transistor in the “on” region and a “lossy capacitance” made of a nonlinear capacitance “ C_{OUT} ” in series with a nonlinear resistor “ r_{COU} ” for modeling the “off” region of the transistor. Fig. 1 shows the schematic of the amplifier; it also shows the transistor die modeled, as explained before, along with a basic model for its package made of an inductance “ L_{PKG} ” and a capacitor “ C_{PKG} .”

As shown in Fig. 1 three load planes are defined in this amplifier; load plane “LP1” is a virtual load plane located inside the transistor, at the right hand of the switch “SW”. This is the load plane where the load admittance required for Class-E operation needs to be synthesized. Load plane “LP2” is located right at the output of the transistor package where actual load measurements can be obtained. L_{PKG} is the most disturbing package parasitic providing the load required by SW at load plane “LP1” because it adds an inductive reactance in series to the load impedance synthesized at the load plane “LP2” by the load network. Load plane “LP3” is located after the wideband admittance transformer “T.”

B. Admittance Transformation Network

The most important component of the load network of this amplifier is the wideband admittance transformer “T” located right at the output port of the power transistor. It is used to lower the load admittance requirements at load plane “LP2” down to the admittance synthesized at “LP3”. This transformer is a low-loss, magnetic-flux coupling design with a measured loss of 0.24 dB at 100 MHz. It is made of three rings of low impedance (15 Ω) semirigid coaxial cable. The cable outer jackets are connected in parallel to form the primary of the transformer; the inner conductors are connected in series to form the secondary. The diameter of the transformer, 10 mm for this design, determines the inductance of the primary L_{EQ} that is used as a component of the amplifier load network. In order to reduce losses to a minimum, no magnetic core is used. This fact reduces coupling between the primary and secondary of the transformer giving a transformation ratio lower than the value expected from its geometry; its bandwidth is about 400 MHz. Transformers

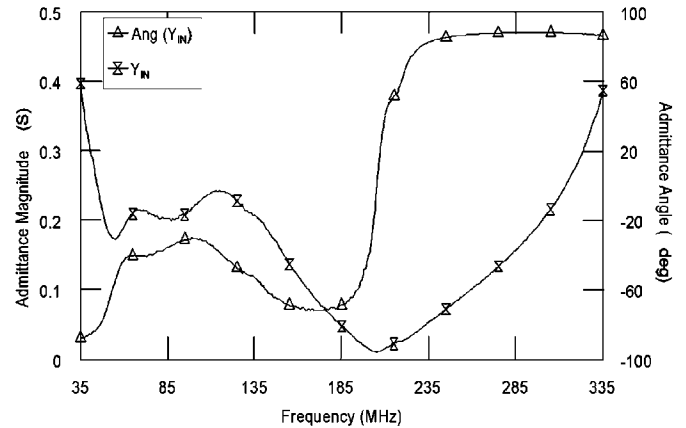


Fig. 2. Measured load admittance at load planes LP2 at $V_{DC} = 16$ V.

of different sizes using different cable diameters were built to find the most suitable one for this application. A model was extracted from its measured “S” parameters, their more significant parameters are the following few ones: Magnetizing inductance $L_M = 8.8$ nH, primary leakage inductance L_{KP} negligible, secondary leakage inductance $L_{KS} = 26$ nH, primary copper loss $R_{CP} = 0.08$ Ω , secondary copper loss $R_{CS} = 0.3$ Ω , primary intra winding capacitance $C_{IP} = 16$ pF, secondary intra winding capacitance $C_{IS} = 1.5$ pF, inter-winding capacitance $C_{PS} = 6$ pF and turn ratio $n = 2.7$.

C. Harmonic Termination Network

A lumped component network is located after the transformer at load plane “LP3” to provide both proper loads at the harmonics and admittance phase rotation at the fundamental for nominal Class-E operation. The network comprises components C_2, L_2, C_3 and L_3 located at “LP3”, and C_{OUT} and L_{EQ} located at “LP2”. The admittance transformation provided by the transformer ($1 : n^2$) allows using higher reactance components for L_2, C_2, L_3, C_3 at the load plane “LP3” than if they were located at a lower impedance plane such as “LP2”. Having higher reactance, these components exhibit higher quality factors (Q) and self resonance frequencies (SRF) than the lower reactance counterparts required at load plane “LP2” to perform the same function.

III. DESIGN, SIMULATION AND TESTING

The harmonic termination network of the amplifier was designed starting from a six element Chebyshev band-pass filter. The components were modified using computer optimization to approximately provide the load phase angle required for nominal Class-E operation from 75 to 135 MHz, the goals of the computer optimization also included keeping load admittance purely reactive at the second and third harmonics as shown in [7]. The load network and PCB of the amplifier were carefully built to reduce parasitic effects that have a noticeable effect on the amplifier performance. The admittance provided by the load network measured at “LP2” at $V_{DC} = 16$ V is shown in Fig. 2. It must be noted that the admittance changes with V_{DC} because the nonlinear nature of C_{OUT} .

After load network optimization the amplifier was simulated using Agilent’s Advanced Design System (ADS). In spite of

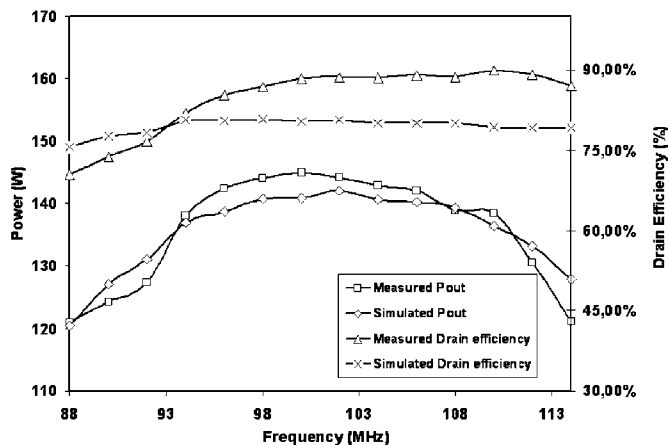


Fig. 3. Measured and simulated output power P_{OUT} and drain efficiency η_D .

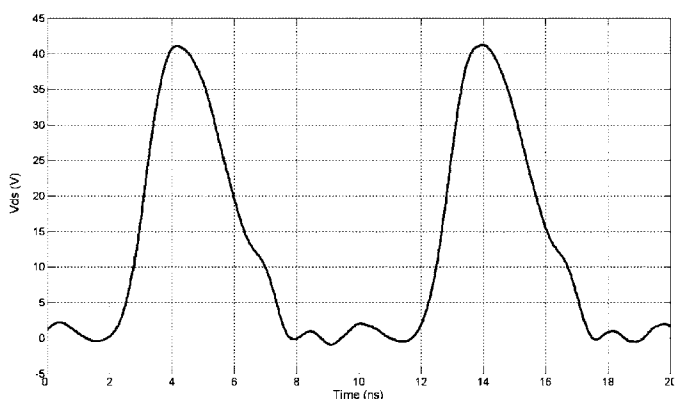


Fig. 4. Measured $v_{DS}(t)$ at 100 MHz and 12 V_{DC} .

this circuit containing a pure switch that may cause harmonic balance convergence problems, the simulation ran smoothly in this case. The simulation results for drain efficiency and output power are shown in Fig. 3.

The amplifier output power and the drain efficiency were tested using a Bird 5000EX wattmeter with an accuracy of 5%. Output power was proportional to the second power of drain bias and drain efficiency decreased with drain bias (maximum AM- V_{DC} rms error is 2% and PM- V_{DC} ranges from -90° at 0.05 V to 0° at 20 V). Measured output power P_{OUT} and drain efficiency η_D test results are shown in Fig. 3 along with simulation results for better comparison. As can be observed there is a good correspondence between simulated and measured output power, while measured efficiency is better than expected from simulated results. This is attributed to transistor model imperfections, instrument uncertainty and harmonic power influence on power tests.

In order to check that the amplifier was really operating close to nominal Class-E conditions, drain to source $v_{DS}(t)$ waveforms were measured at load plane LP2 using a 1 GHz bandwidth, 4 GSa/s oscilloscope fitted with a 650 MHz 3 dB bandwidth oscilloscope probe over the amplifier bandwidth. Fig. 4 shows the $v_{DS}(t)$ waveform measured at 100 MHz (middle of the amplifier band) while the amplifier was powered at $V_{DC} = 12$ V, approximately half of the power supply voltage required for maximum output power, in order to not to exceed the maximum voltage of the oscilloscope probe.

TABLE I
MEASURED GAIN AT PEAK POWER AND AVERAGED TRANSISTOR SWITCHING CURRENT VERSUS FREQUENCY

Frequency (MHz)	88	100	114
I_{DC} (A) @ 28V	6.13	5.86	4.97
Gain at peak power@28V (dB)	14.5	15.3	14.5
$2f$ attenuation (dBc)	14.6	19	21

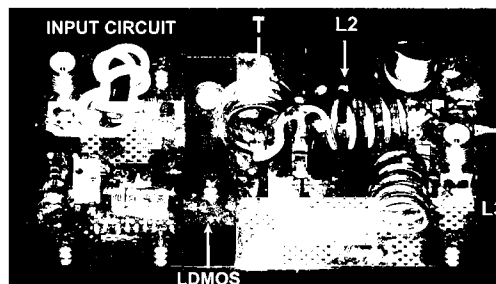


Fig. 5. Photograph of the amplifier.

Measured gain at peak power and averaged transistor switching current versus frequency are shown in Table I.

A photograph of the amplifier is shown in Fig. 5. The size of the circuit is 80×50 mm. This relatively low size for a power VHF amplifier makes easy the combination of several stages for achieving high output levels usually required at this band by some applications such as broadcasting.

IV. CONCLUSION

A high efficiency, wide-band, high power VHF PA has been shown. To the best of the author's knowledge, the performance of this amplifier is an advance over published or commercial amplifiers at this frequency band and power level. It has been designed providing the approximate load admittance required for Class-E nominal operation both at the fundamental and harmonics using a low-loss, uncomplicated load network, whose main component is a low-loss, wideband transformer that elevates the load impedance right at the drain of the transistor.

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