Current Sensorless Power Factor Correction based on Digital Current Rebuilding

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***Abstract*- A new digital control technique for power factor correction is presented. The main novelty of the method is that there is no current sensor. Instead, the input current is digitally rebuilt, using the estimated input current for the current loop. Apart from that, the ADCs used for the acquisition of the input and output voltages have been designed ad-hoc. Taking advantage of the slow dynamic behavior of these voltages, almost completely digital ADCs have been designed, leaving only a comparator and an RC filter in the analog part. The final objective is obtaining a low cost digital controller which can be easily integrated in an ASIC along with the controller of paralleled and subsequent power sections.**

I. INTRODUCTION

There is no doubt in the interest of digital control for switch mode power supplies (SMPS). Some of its advantages are valid for any application, like programmability, decreased components count, less sensitivity to changes or noise, reduced design time and, more recently, additional power management capabilities, such as PMBus [1-2] compatibility. Apart from these general advantages, some applications obtain specific advantages using digital control, like non-linear control algorithms seeking time-optimal performance in VRMs [3-5] or interleaving and current sharing in multiphase converters [6-9]. In power factor correction (PFC), most efforts of previous digital proposals have been done trying to increase the bandwidth of the voltage loop without interfering with the intrinsic output voltage ripple [10-13]. Although the results are quite promising, the increased output voltage bandwidth can hardly compensate the low cost of analog integrated controllers because the output voltage ripple will still be present even with high bandwidth voltage loops.

In some previous works, digital control was used to avoid some measurement in PFC. For instance, in [14-15] the input voltage is not measured, while in [16-17] the current is not measured and no current loop is used. In this work, looking for a low cost digital solution, a controller valid for continuous and discontinuous conduction mode (CCM and DCM) operation that does not need a current sensor is presented. This current sensor is commonly the most problematic and expensive of the three usual sensors (input/output voltages and input current) of a PFC.

This work has been partially supported by the TEC2008-01753/TEC project of the Spanish Ministry of Science and Technology.

The block diagram of the proposal is represented in Fig. 1. Both current and output loops are employed, substituting the current measurement by a digitally rebuilt current. Apart from that, and looking for a low cost solution that can be easily integrated in CMOS technology, the ADCs for the input and output voltages have been designed ad-hoc. The only analog components that have been used are a comparator and an RC filter, employing the ΣΔ technique. This is possible since the measured voltages have a slow behavior.

The rest of the paper is organized as follows. The ADCs are explained in the next section, and the current loop using the current rebuilding technique in section III. Experimental results are included in section IV and the main conclusions are highlighted in the last section.

II. AD-HOC ADCS

In the proposed controller, only the input and output voltages need to be measured. Both voltages dynamics are defined in a low frequency range (50 or 60 Hz for the input voltage and 100 or 120 Hz for the output voltage). We can take advantage of this fact in order to reduce the cost of the ADCs. Keeping this goal in mind, ad-hoc ADCs have been designed trying to reduce the analog components to a minimum. The proposed ADCs, which employ the ΣΔ principle [18], only need a comparator, a resistor and a capacitor as analog components, the last two used as a low-pass filter. The block diagram of the proposed ADC is shown in Fig. 2.

An up/down counter represents the measured voltage as a digital bus. This bus is converted into a bitstream using a ΣΔ modulator (dot line block). The bitstream is then converted to an analog voltage using an RC low-pass filter, which is compared to the analog input. Depending on this comparison, the counter is increased or decreased. The integral action of the ΣΔ modulator (the accumulator) forces the error to be zero in steady state. Therefore, the mean value of the counter (once translated to a voltage) has to be equal to the measured voltage.

The main drawback of the proposed ADC is that it is quite slow: when using *M* bits, the clock frequency is divided up to 2^M. However, the digital clock and the input or output voltages have so different dynamics (100 MHz and 100/120 Hz respectively in our case) that the slow nature of the ADC is not a problem.

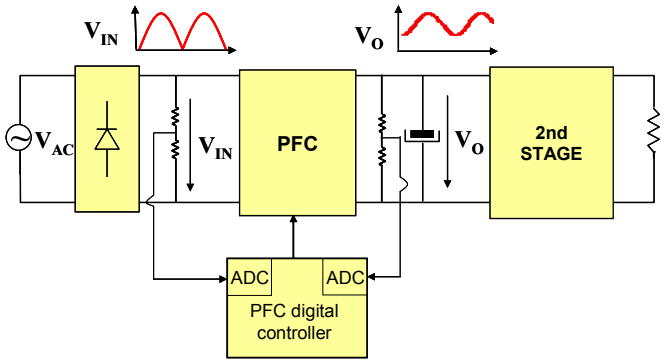


Figure 1. PFC controller proposal

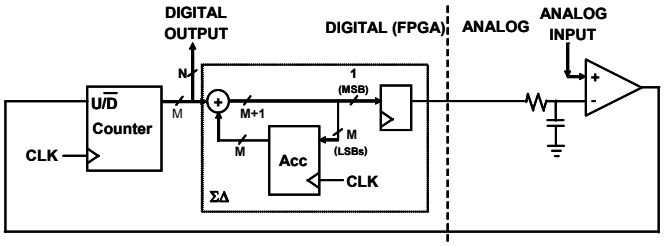


Figure 2. Ad-hoc ΣΔ ADC.

Regarding the RC filter, it must be chosen in order to filter the frequencies generated by the ΣΔ modulator. The clock frequency, f_{clk}, is obviously present because the modulator output is updated at this frequency. Sub-harmonics are also present, which can be as low as $f_{clk}/2^M$ (being M the number of bits). Given the slow behavior of the measured voltages, we could think that the best solution would be a big RC constant, enough to filter frequencies much below $f_{clk}/2^M$ (but not the measured voltage frequency, of course). However, using a big RC constant introduces oscillations in the measurement. This is because of the delay of the RC filter. On the other hand, reducing the RC constant diminishes precision because not all the sub-harmonics are filtered. A trade-off between precision and stability has to be achieved. Experimental results changing the RC values are shown in Table I, using a clock frequency of 50 MHz and 8 bits of resolution. Both the oscillation and the error are referred to the complete ADC resolution (i.e. error/256), giving the worst case in all the measurement range.

TABLE I
OSCILLATION AND ERROR USING DIFFERENT RC VALUES WITH M=8

R	C	Maximum Oscillation	Maximum Error
1 kΩ	22 pF	16%	7.4%
1 kΩ	220 pF	22%	1.5%
1 kΩ	2.2 nF	59%	1.1%

In order to decrease the relative oscillation there are two possible solutions. One is to increase the number of bits. The oscillation remains basically the same independently of the number of bits, but its percentage is halved with each additional bit. The other solution is to update the counter at a slower frequency, while keeping the same frequency in the modulator. The first solution has been used for the experimental results shown in the rest of the paper, choosing R=1 kΩ and C=220 pF for the filter. The ADCs have been implemented using M=13 bits. However, only N=8 bits have been used (the MSBs) because the oscillations affect the LSBs. In this way, 8 bits of resolution with almost no oscillation (noise) have been achieved.

III. DIGITALLY REBUILT CURRENT

The main contribution of the proposed controller is that the input current does not need to be measured. Instead of that, it is digitally rebuilt from the input and output voltages, and the on/off driving signal. In the case of a Boost converter, which has been used in the experimental results, the input current increases proportionally to V_{in} during the on-time, while it decreases proportionally to V_{in}-V_{out} during the off-time (see Fig. 3) The rebuilding algorithm changes slightly in each topology, but can be easily adapted. The on and off periods are known inside the controller because the driving signal is generated there, so a simple accumulator can represent the estimated current.

It must be taken into account that the rebuilding update frequency, which is the clock frequency in our case, sets the resolution of the PWM. Therefore, the rebuilding technique is more appropriate for custom hardware (FPGA or ASIC) implementation than for DSP or microcontroller implementation, like in [19-20].

The input current control loop shapes the rebuilt current, $i_{in\text{-}r}$, while the output voltage control loop generates the current reference, i_{ref}, for the utility period as depicted in Fig. 4.

Of course, the rebuilt current can not be perfect due to many factors: in DCM or peak current mode control, inductor value different from expected, input and output voltage measurement errors, driving signal delays, etc. If the converter were always in CCM, even the smallest error would lead to saturation because it would be integrated indefinitely. However, the converter enters DCM at zero-crossing, so the error is reset every 10 or 8.33 ms (50 or 60 Hz). Therefore, the rebuilding errors have an impact on the power factor but do not saturate the converter. Regarding the mean input current, any possible errors are compensated by the voltage loop.

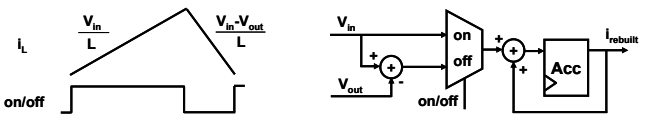


Figure 3. Current rebuilding concept. Waveforms (left) and HW architecture (right)

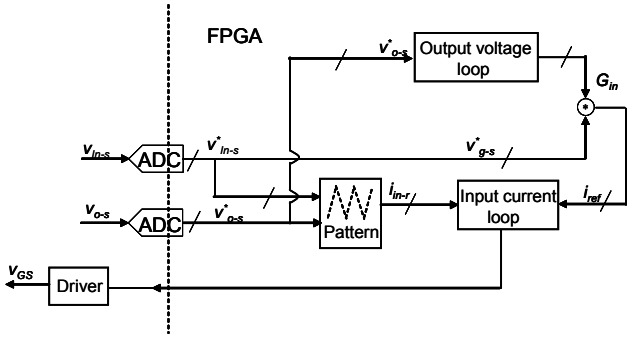


Figure 4. Schematic of the current sensorless controller

Despite that simulation of the converter model under the proposed control shows perfect current shaping, as is shown in Fig. 5, even considering inductance tolerances, the experimental results have shown that the most critical errors are due to: a) The driving signal delays, especially when the on-to-off delay is different from the off-to-on delay, because the effective duty cycle is changed, b) Measured voltage errors due to offsets and c) Measured voltage errors due to sample and hold and registering delays. An effect of the accumulative inductance volt-seconds error is shown in Fig. 6, where initially the volt seconds applied to the inductor in each switching period are lower than calculated. Therefore, the input current, i_{in}, does not grow as required and calculated by $i_{in\text{-}r}$. Later, since the low i_{in} affects the output voltage, the input current rise during the on-time is not properly compensated in the off-time and i_{in} raises more that desired. This effect is experimentally confirmed.

If the delay difference is known in advance or measured, it can be compensated in the rebuilding algorithm. Since the accumulative error to delays and offset is the difference between the volt-seconds applied to the inductor and the calculated by the digital circuit the compensating technique can be unified using a single variable.

Sample and hold and register delays, τ_{SH} and τ_R respectively, produced in the v_{in} and v_o data acquisition process, can not be compensated by compensation constants. As it is observed in Fig. 7, where the fundamental components of the digitally rebuilt v_{in} affected by τ_{SH} and τ_R are represented, the sign of the error depends on the voltage slope. The slow rate of change of the measured voltages allows implementing effective compensation by the linear extrapolation of the voltage acquired data. As an example, minimum linear extrapolation is given by

$$v_{in}[n+1] = 2v_{in}[n] - v_{in}[n-1] \tag{1}$$

Once the input current is rebuilt, any current loop can be used: average current, peak-current, hysteretic control, etc. In this proposal, one-cycle control is used [21-24], which has the advantage of using constant switching frequency and that can be easily implemented in digital hardware, because it is based on additions and comparisons.

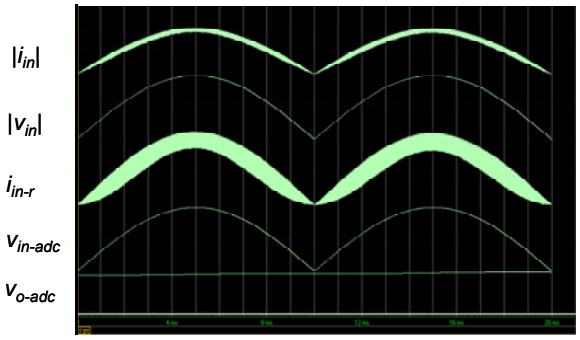
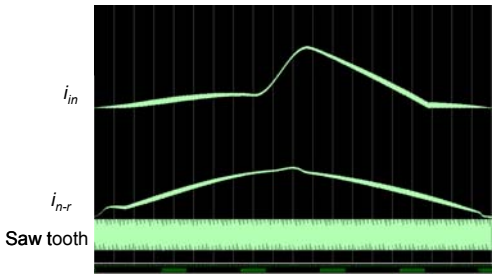
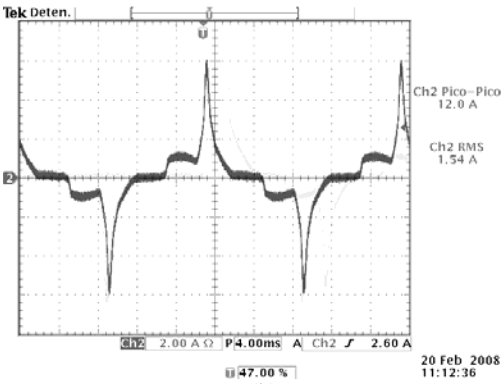


Figure 5. Simulation of the PFC under the proposed sensorless control. From top to down: input current, input voltage, rebuilt input current, digital samples of the input voltage and digital samples of the output voltage



(a)



(b)

Figure 6. (a), Simulation of the accumulative volts-seconds error in the rebuilt current. Top input current. Middle rebuilt current, bottom carrier control signal. (b), Experimental input current with the accumulated error effect.

Non linear one-cycle controllers compare a carrier signal with the variable under control, in this case the rebuilt input current, to determine the switch instant. Fig 8 shows the case for the Boost converter. The turn-off instant corresponds to

$$V_m - V_m \frac{t_{on}}{T_s} = r_s i_{Lpk},\ V_m(1-d) = r_s i_{Lpk}, \tag{2}$$

where r_s is the theoretical current sensor resistor and V_m is the maximum carrier signal value controlled by the outer loop. In CCM steady state, the control law is rewritten as

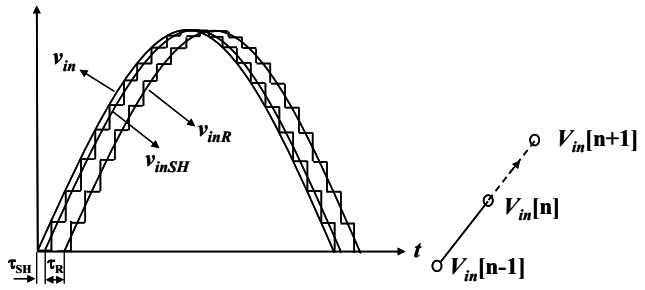


Figure 7. Left, representation of v_{in} affected by the sample and hold, and the register delays. Right, linear extrapolation.

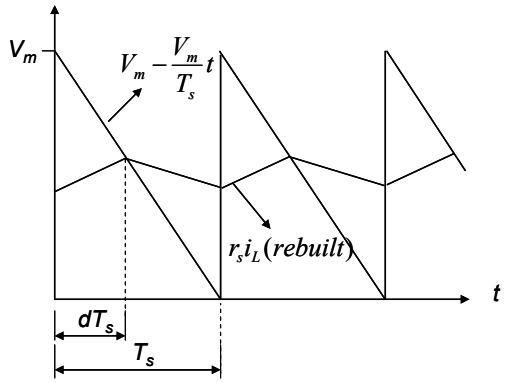


Figure 8. One-cycle control for the Boost converter controlled as PFC

$$V_m \frac{v_{in}}{V_o} = r_s i_{Lpk}, \tag{3}$$

and therefore the peak current follows the input voltage in each switching period, achieving power factor correction. One-cycle control can be modified in order to be adapted to other topologies. For example, in a Buck-Boost type converter, e.g. SEPIC, the turn-off instant corresponds to

$$V_m - V_m \frac{t_{on}}{T_s} = r_s i_{Lpk} \frac{t_{on}}{T_s},\ V_m \frac{1-d}{d} = r_s i_{Lpk}, \tag{4}$$

in order to achieve that the peak current follows the input voltage in each switching period.

The parameter V_m is the result of the outer output voltage control loop. In steady state V_m represents the line power.

$$P_{in} \cong V_m \frac{V_{in}^2}{r_s V_o} \tag{5}$$

Accumulative volt-seconds errors caused by v_{in} and v_{out} data deviations or by switching delays are compensated by generating the transition of the switch drive signal before the theoretical conditions arrive. Compensation times are introduced for the off-on and off-on switch times. The on-off transition is generated by the digital circuit $n_{dlon\text{-}off}$ clock cycles (T_{clk}) before reaching condition (2) and the off-on transition is generated $n_{dloff\text{-}on}$ clock cycles before the carrier ramp reaches zero. Fig. 9 represents the modification introduced in the one-cycle control algorithm to compensate the inductor volt-seconds error. The ideal driving signal should be the "non-compensated" one. In order to compensate the delays, the FPGA generates instead the "compensated" signals. Once it travels through the driver and switch, the real pulses will be almost identical to the "non-compensated" signal, which is the desired behavior.

IV. Experimental results

Before testing the converter, the controller was tested through simulation. The entire controller and the digital parts of the ADCs have been designed in VHDL. In order to perform closed-loop simulation, a simple VHDL model of the boost converter and the analog parts of the ADCs was used [25-26]. Using closed-loop simulation, the effects of the driving signal delay in the rebuilt current were studied.

After simulation, a boost prototype converter was built in order to test the proposed controller. The controller and the digital parts of the ADCs were implemented in a Spartan-3E XC3S500E Xilinx FPGA evaluation board. The ADCs have been implemented as explained in section II with M=13 bits of resolution, although only the N=8 MSBs have been used (the 5 LSBs exhibit high noise). The boost converter used in this experiment was designed for V_{in} up to 220 V_{rms}, 50 or 60 Hz, 500 W and f_{sw} 73 kHz (it was an existing prototype not designed for this purpose). No line filter is included for the experiments. The circuit implementation schematic is presented in Fig. 10 where details of the bitstream filter, unipolar comparators LM393N and connection between the FPGA and the power section through the MOSFET driver HCPL3120 are highlighted.

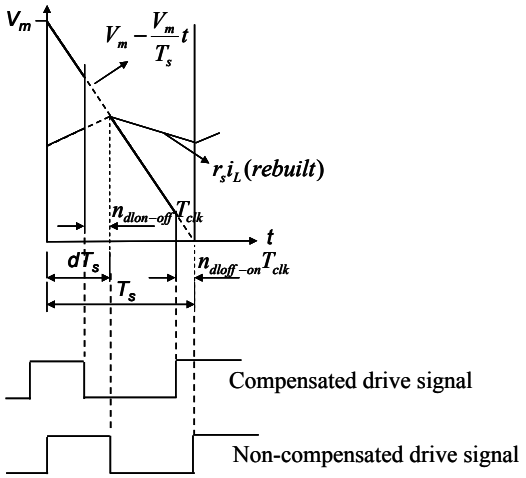


Figure 9. Modification of the one-cycle algorithm to compensate inductor volt-seconds errors

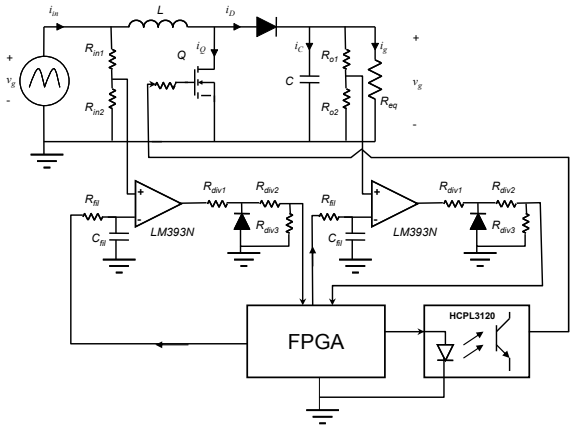


Figure 10. Experimental PFC circuit and control schematic

Figures 11 to 15 show different aspects of the PFC operation under the proposed control. In Fig. 11 the FPGA output (channel 1) that acts as the MOSFET drive signals is compared to the inductor voltage (channel 2). The measured delay time is 920 ns for the on-off transition and 620 ns for the off-on transition.

Figure 12 and 13 present the results of the data acquisition. The input and output voltages and the corresponding filtered bit streams obtained from the circuit in Fig. 2 are shown. No significant delay is observed although the noise may induce some perturbation to the input current.

Figure 14 shows the input voltage (channel 1) and current (channel 2), at 75 V_{rms}, 135 W. Figure 15 shows the same wave forms at 220 $V_{rms,}$ 400W. It can be seen that current shape is very good for low line; highline waveform shows some crossover distortion and a higher frequency current ripple (it should be pointed that no line filter is included in the prototype). Power factor correction was successfully achieved. Measurements of power factor were 0.98 in the first case and 0.96 in the latter. The harmonic content of this waveform complies with regulation EN61000-3-2 for class C lighting applications equipments

V. CONCLUSIONS

A digital controller for power factor correction has been proposed. Taking advantage of digital circuits capabilities, the input current is rebuilt from the input and output voltages instead of being measured. Avoiding the current measurement can be a significant advantage with respect to the analog controllers, which also helps to reduce the total cost. Furthermore, trying to reduce cost and taking advantage of the slow nature of the input and output voltages, cheap ad-hoc ΣΔ ADCs have being designed. Their only analog components are a comparator, a resistor and a capacitor. The rest are digital blocks, which are integrated with the rest of the controller. In fact, controllers of subsequent power stages could also be integrated. The experimental results show the feasibility of the method, obtaining a high power factor in spite of not measuring the input current.

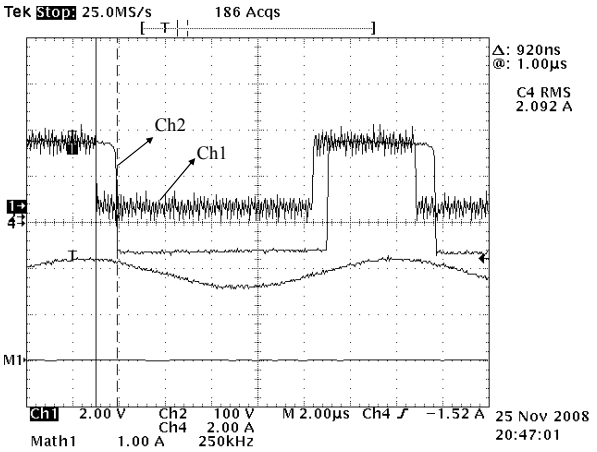


Figure 11. Experimental time switch transitions compared with the drive signals. Ch1, MOSFET drive signal FPGA output. Ch2, Inductor voltage

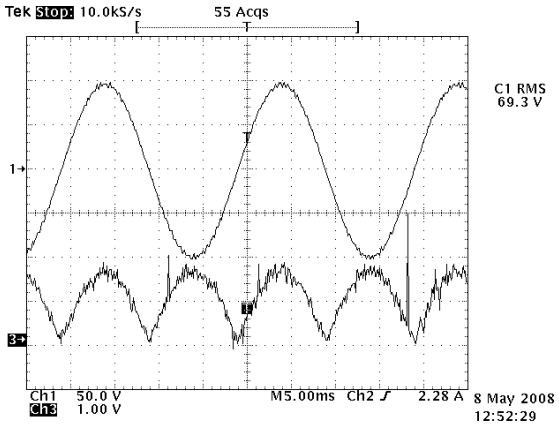


Figure 12. Experimental data acquisition on input voltage. Channel 1 input voltage, channel 2 filtered bitstream.

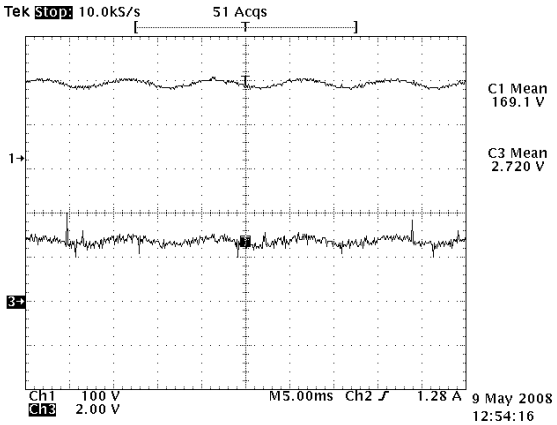


Figure 13. Experimental data acquisition on output voltage. Channel 1 output voltage, channel 2 filtered bitstream.

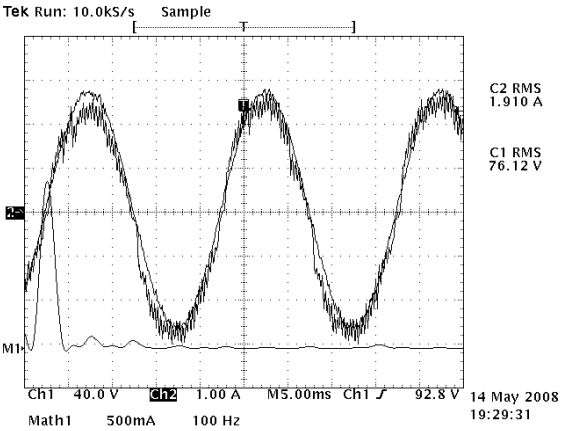


Figure 14. Experimental results. V_{in} 75 V_{rms}. Channel 1 input voltage, channel 2 input current, math 1 input current spectrum

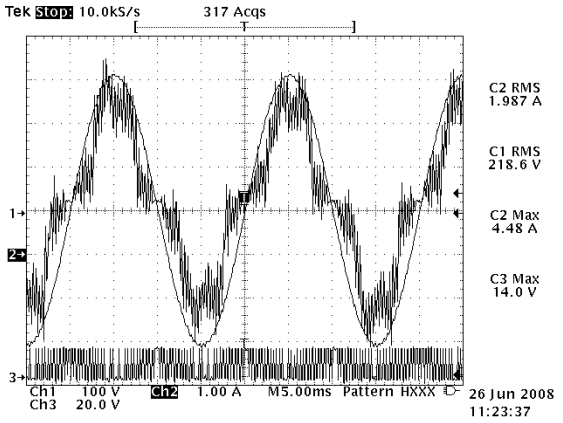


Figure 15. Experimental results. V_{in} 220 V_{rms}. Channel 1 input voltage, channel 2 input current, channel 3 MOSFET drive signal.

ACKNOWLEDGMENTS

The authors would like to thank you Víctor Manuel López, Pilar Montero and Alejandro García for their help with the experimental results.

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