Differential-Mode EMI Reduction in a Multiphase DCM Flyback Converter

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***Abstract*—Switched converters are a source of electromagnetic interference (EMI) due to the hard switching and abrupt edges in the current and voltage waveforms. Multiphase converters can reduce the EMI at the source, minimizing the conducted EMI generation, without changing dramatically the normal operation of the circuit. Input filter can be greatly reduced, radiated EMI is lower, and internal EMI problems are minimized. This paper is focused on exploring multiphase converters as a topological technique to reduce conducted differential-mode EMI generation at the source, considering some nonidealities of the multiphase converter.**

***Index Terms*—Electromagnetic conductive interference, power conversion, power conversion harmonics.**

I. Introduction

SWITCH-MODE converters manage the energy in a pulsating way but the use of interleaving technique [1]–[3] provides a more continuous energy flow. From the point of view of conducted differential mode (DM) electromagnetic interference (EMI), interleaved operation is very interesting, since the bad EMI behavior of switched converters is in part due to the fact that the energy is taken from the main source abruptly at high frequencies.

Paralleling and shifting power converters, known as interleaving technique, have been used widely in the recent years [4]–[8]. The goal is increasing the effective frequency of the converter by synchronizing several smaller converters (basic cells or phases) and operating them with relative time shifts. The effect seen from outside the multiphase power converter is a converter with higher switching frequency (n times the switching frequency of a single phase) and less peak-to-peak ripple. In Fig. 1, two input current waveforms are shown: single-phase operation (single phase or no phase shifting between parallel converters) and interleaved operation (phase shifting between paralleled converters).

A significant reduction of the EMI filter is expected based on the ripple cancellation effect and the rise of the effective ripple current (in theory proportional to the number of phases). This reduction yields to lower volume and weight what benefits the power density of the converter.

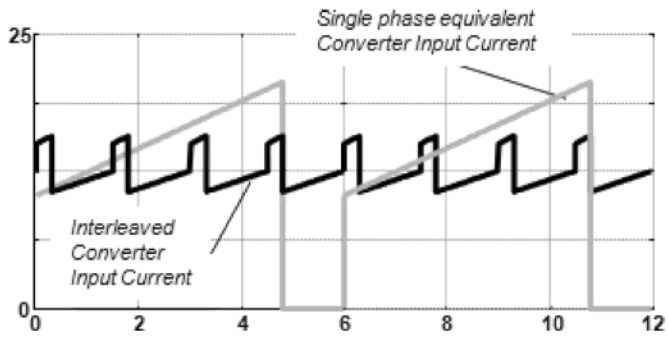


Fig. 1. Input energy flow in a multiphase converter.

The problem of increasing the number of phases can be solved by digital control implementations [5]–[7], [9]–[12], where additional advantages can be taken to optimize the efficiency of the converter [6], the bandwidth of the control loop [7], or improving current balance between phases [11], [13].

Nevertheless, the impact of interleaving in EMI is not always beneficial. Interleaving is used in [14] in a power factor correction (PFC) application, and it is shown that a two-phase interleaved boost converter in continuous conduction mode (CCM), in spite of the ripple cancellation, cannot improve the size of the EMI filter.

There are many techniques to minimize the EMI generation, some of them based on minimizing parasitic couplings [15], [16] and some others based on acting in the operation principle of the circuit [17], [18] (soft switching, random pulsewidth modulation (PWM) generation, etc.). Multiphase converters can be considered as a topological approach to DM EMI reduction, without changing the operation principle of the converter, as introduced in [1], [14], [19], and [20].

This paper is focused on the analysis of differential conducted EMI noise reduction of constant duty cycle PFC multiphase converters for a high number of phases, taking into account nonidealities. The analysis is based on a flyback converter in discontinuous conduction mode (DCM) as a power factor corrector while minimizing the generation of conducted EMI by a proper operation (shifting) of the converter (see Fig. 2).

II. Application Description: DCM Flyback Converter With PFC

Electromagnetic compatibility (EMC) considerations are especially important in the case of PFC converters, because they are connected to the ac mains. They must meet low-frequency regulations, up to 2 kHz, and high-frequency (EMI) regulations, from 150 kHz. Low-frequency requirements are met by

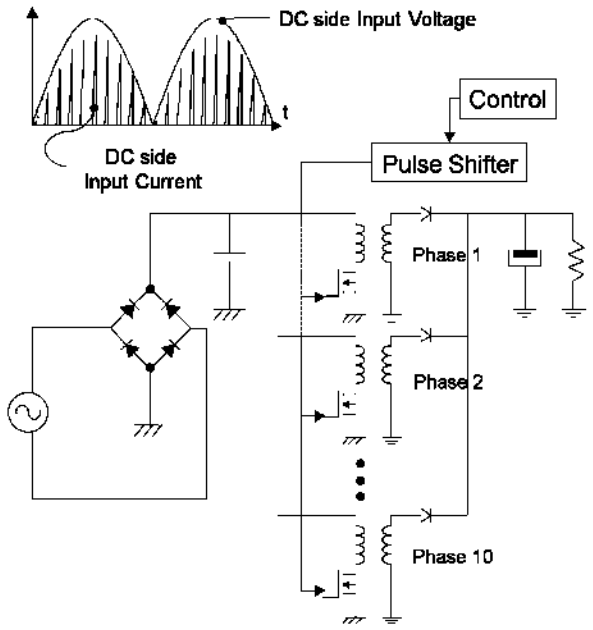


Fig. 2. Multiphase DCM flyback converter.

means of the converter control combined with a proper topology, matching the input current of the converter with the proper input current waveforms. The conducted EMIs generated by high-frequency operation are commonly rejected by means of EMI filters operating between the mains and the converter [21].

A flyback converter has been widely used for low-power and low-cost PFC providing simplicity, robustness, and isolation. However, the power range commonly suitable for this converter is relatively low (for example, 100–200 W). A flyback converter in DCM operation with constant duty cycle is a natural resistor emulator [22] with the input average current being proportional to the input voltage. However, it generates a high EMI content (due to the falling edge and rising slope of the discontinuous input current; see Fig. 2), which must be filtered in many cases.

Interleaving provides EMI reduction and higher output power capability, so a very simple topology such as DCM flyback can be used in a higher power range. However, paralleling without shifting increases not only the output current capability, but also the EMI emissions to be filtered.

On the other hand, interleaving acts at high-frequency level. This is why the output capacitor cannot be reduced by interleaving, because it is used for low-frequency energy storage.

A proper current sharing among phases is warranted by the topology, since in this case, the phase current is reset at every switching cycle due to the DCM operation. Therefore, the current mismatch due to component tolerances and different layout could be kept in an admissible value without any additional current sharing mechanism.

Gate signals for the phases should be quite similar to perform a proper harmonic cancellation. Digital controllers based on specific hardware, such as field-programmable gate arrays (FPGAs), provide an easy way to generate many signals [5], [7], [9], [10], [24], while the accuracy is higher than analog controllers. In this converter, a digital shifter for the pulses has been designed (see Fig. 3), and implemented in a low-range

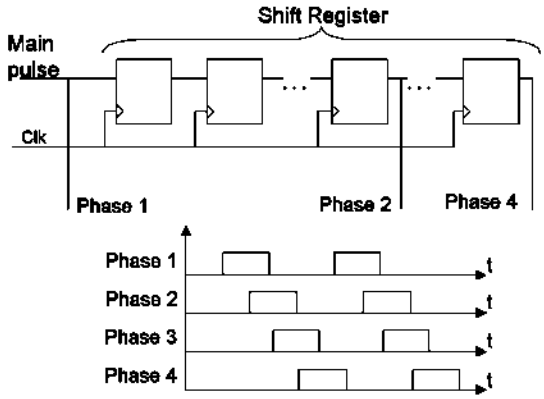


Fig. 3. Multiphase pulse generation scheme.

programmable logic device. The control digital blocks have been described using very high speed integrated circuits hardware description language (VHDL).

III. Input Current Harmonic Cancellation

The main concept involved in this paper is the cancellation of input current harmonics by means of interleaving. In terms of Fourier series, the input current is expressed in (1), where f_s is the frequency of the input current (switching frequency), n is the order of the harmonic, and c_n is the coefficient of the harmonic of order n

$$i(t) = \sum_{n=-\infty}^{n=+\infty} c_n \, e^{\,jn2\pi f_s t}. \tag{1}$$

Let us consider an M-phase dc–dc converter (constant input voltage, no input capacitor) operating without any shifting among phases (equivalent to a single phase) and with relative shifting between phases, i.e., operating with interleaving.

When the converter operates with interleaving, controller generates a time delay of the current of each phase equal to the switching period over the number of phases (uniform time shifting). This time delay produces a different angle delay for each harmonic. When the angle delay is the same for all harmonics, they are added and the resulting amplitude is larger. When the angle delay is different for each harmonic, the sum of all of them is equal to 0, and then, the harmonic cancellation is produced [23]. This feature of interleaved operation is described in expressions (2)–(4), where c_{n_p} is the harmonic of order n of the phase p, c_{n_total} is the harmonic of the total input current (sum of the current trough all phases), M in the number of phases, and p is the pth phase

$$c_{n\_p} = c_n \, e^{-j2\pi p \frac{n}{M}} \tag{2}$$

$$c_{n\_\mathrm{total}} = \sum_{p=0}^{M-1} c_n \, e^{-j2\pi p \frac{n}{M}} = c_n \sum_{p=0}^{M-1} e^{-j2\pi p \frac{n}{M}} \tag{3}$$

$$c_{n\_\mathrm{total}} = \begin{cases} Mc_n, & \text{if } \dfrac{n}{M} \in Z \\ 0, & \text{if } \dfrac{n}{M} \notin Z. \end{cases} \tag{4}$$

In the ideal case, when M phases are used, the first harmonic of the input current has a frequency M times higher than the

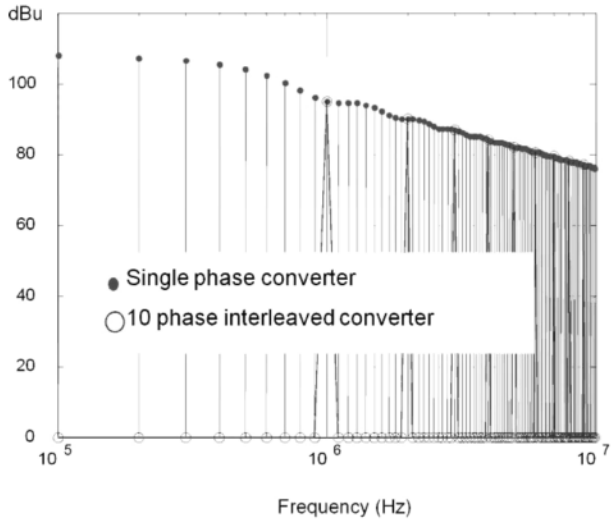


Fig. 4. Ideal harmonic cancellation in a multiphase converter with ten phases.

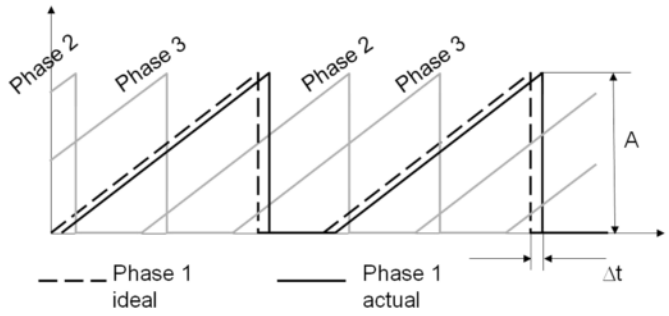


Fig. 5. Effect of a nonideal shifting in one phase.

switching frequency, and the amplitude is the same if all phases were not shifted. The first $(M-1)$ harmonics disappear. For higher order harmonics, there are only harmonics with an order multiple of the number of phases, as shown in Fig. 4. For a ten-phase converter switching at 100 kHz, harmonics from 100 to 900 kHz are cancelled, and the first one takes place at 1 MHz, the next at 2 MHz, and so on. Ideally, the frequency envelope of the harmonic spectrum is the same for both multiphase and equivalent single-phase operation, but with interleaving, a lot of harmonics disappear.

IV. Nonidealities

In order to evaluate the application of this technique in actual converters, several nonidealities must be considered, such as nonuniform pulse shifting, nonuniform phase current amplitude, and nonuniform duty cycle.

A. Nonuniform Pulse Shifting

It is caused by the different delays introduced by drivers, MOSFETs, and a nonideal phase shifter (see Fig. 5). The effect of this nonideality depends on the additional delay. In the case of an additional delay in a single phase, the perturbation is shown in Fig. 6, where $\Delta\alpha$ is the relative difference between the nominal phase shift and the actual phase shift. The influence of this nonideality in terms of harmonics is given by the

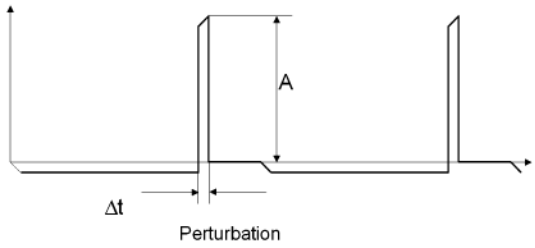


Fig. 6. Perturbation due to a nonideal shifting in one phase.

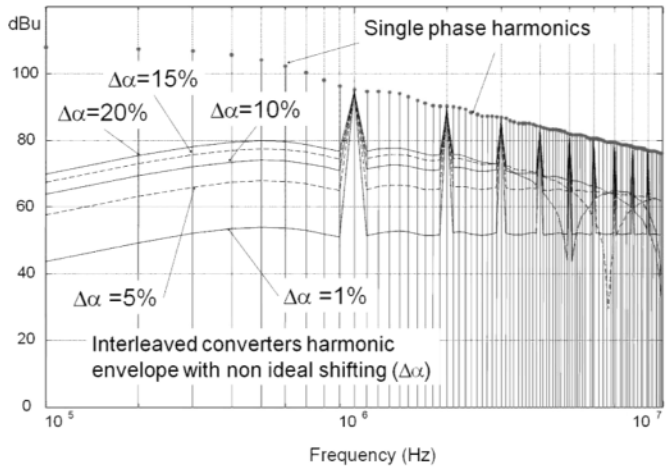


Fig. 7. One phase is not properly shifted.

relative duration of the delay, as shown in Fig. 7. In expression (5), the harmonic of order n is given when phase q has a difference in time of $\Delta t = \Delta\tau/f$, under the condition of the ideal phase shift for phase q, with $\Delta\alpha = \Delta\tau M$. The new coefficient c_{n_total} has two different parts: one of them corresponding to the ideal situation and the other one corresponding to the effect of the described nonideality. The amplitude of the harmonic corresponding to this nonideality in the worst case is given in (6), where $c_{n\_1\phi}$ is the amplitude of the harmonic of the equivalent single-phase converter (all phases working without phase shifting). Note that for ten phases, the amplitude of the harmonic is five times (14 dB) less than that the amplitude of the harmonic in the equivalent single phase

$$c_{n\_\text{total}} = c_n \left(\overbrace{e^{-j2\pi n \frac{q}{M}\left(e^{-j2\pi n \Delta\tau} - 1\right)}}^{\text{Nonideality}} + \overbrace{\sum_{p=0}^{M-1} e^{-j2\pi p \frac{n}{M}}}^{\text{Ideal}} \right) \quad (5)$$

$$c_{n\_\text{total}} = c_n \left(e^{-j2\pi n \frac{q}{M}}(-1-1) \right)$$

$$\Rightarrow c_{n\_\text{total}} = 2c_n = \frac{2c_{n\_1\phi}}{M} \qquad \forall \frac{n}{M} \notin Z. \quad (6)$$

B. Nonuniform Phase Current Amplitude

Due to the tolerance of inductors, there might be some variations in the amplitude of the current waveforms through each phase, as shown in Fig. 8. The effect of nonuniform amplitude is

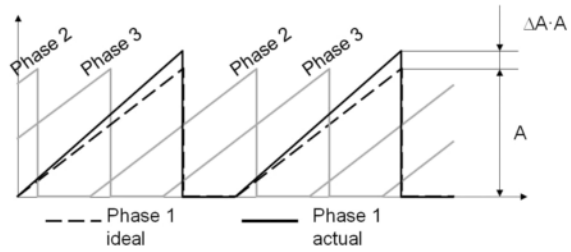


Fig. 8. One phase has current amplitude higher than the others.

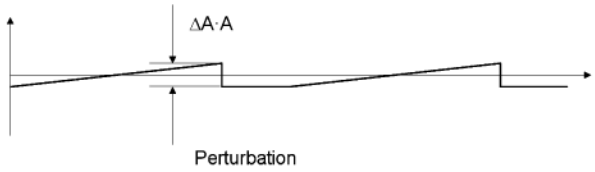


Fig. 9. Perturbation due to a mismatch in the current amplitude.

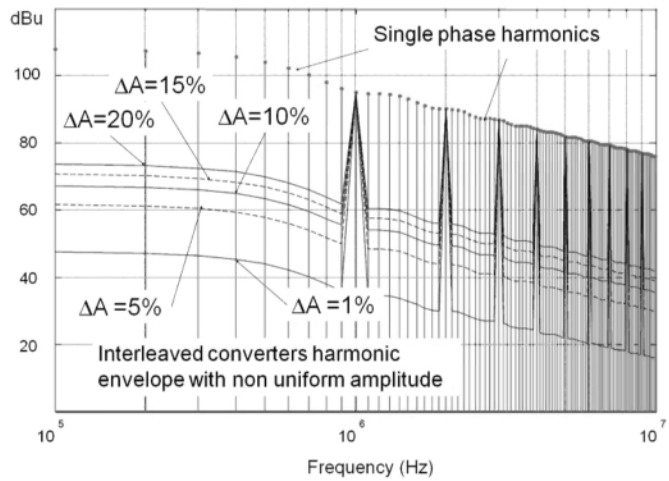


Fig. 10. One phase has current amplitude higher than the others.

the same for all harmonics, with the amplitude being the scaled version of the single-phase current (see Fig. 9).

The effect on the harmonics of the difference in the current amplitude of one phase is given in Fig. 10. In expression (7), the amplitude of the harmonic of order n is given when the amplitude of phase q is $A\ (1+\ \Delta A)$, where A is the amplitude in the ideal case. This harmonic is composed of two different parts: one of them due to the ideal operation and the other one due to the nonideality. In (8), the amplitude of the harmonic due to the nonideality is shown, for a harmonic n that is ideally cancelled. The attenuation $\mathrm{Att_{dB}}$ of the harmonic n, which is ideally canceled, is given in (9), as a function of the amplitude difference ΔA and the number of phases M

$$c_{n\_\mathrm{total}} = c_n \left(\Delta A\, e^{-j2\pi q \frac{n}{M}} + \sum_{p=0}^{M-1} e^{-j2\pi p \frac{n}{M}} \right) \tag{7}$$

$$c_{n\_\mathrm{total}} = c_n \Delta A e^{-j2\pi n \frac{q}{M}} \qquad \forall \frac{n}{M} \notin Z \tag{8}$$

$$\mathrm{Att_{dB}} = 20\ \log\left(\frac{c_{n\_1\phi}}{c_{n\_\mathrm{total}}}\right) = 20\ \log\left(\frac{M}{\Delta A}\right) \qquad \forall \frac{n}{M} \notin Z. \tag{9}$$

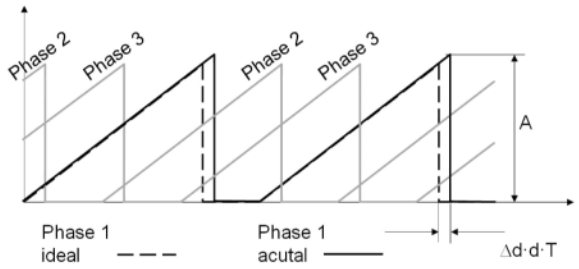


Fig. 11. One phase has higher duty cycle than the others.

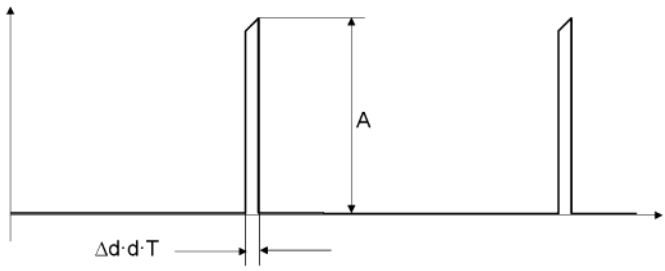


Fig. 12. One phase has higher duty cycle than the others.

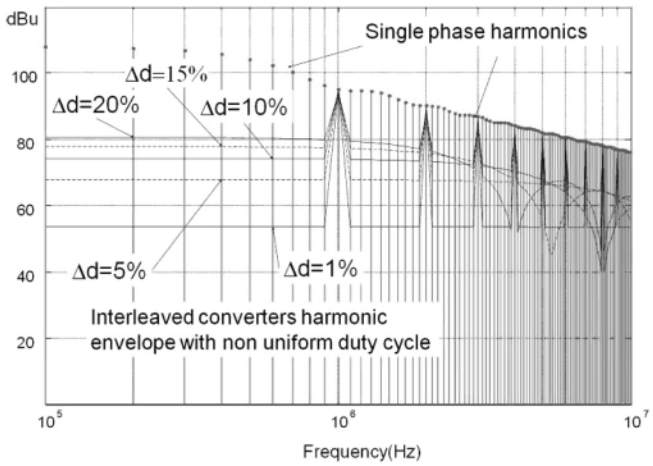


Fig. 13. One phase has different duty cycle than the others.

C. Nonuniform Duty Cycle

This is the result mainly of the dispersion of the characteristics of the controller, drivers, and MOSFETs (see Fig. 11). Digital control can reduce this error. The effect of the nonuniform duty cycle can be considered as an additional pulse of amplitude A (the peak current), at the switching frequency and duration of $\Delta d\, d\, T$ (see Fig. 12). The evaluation of the effect of this nonideality on the current spectra is given in Fig. 13. The expression of the amplitude of additional harmonics corresponding only to this nonideality can be approached by the expression (10), where the amplitude of the input current is A and the relative difference on the duty cycle is Δd

$$|c_{n\_\mathrm{total}}| = \frac{A}{2\pi n} \left| \left(e^{-j2\pi n \Delta d\, d} - 1 \right) \right|. \tag{10}$$

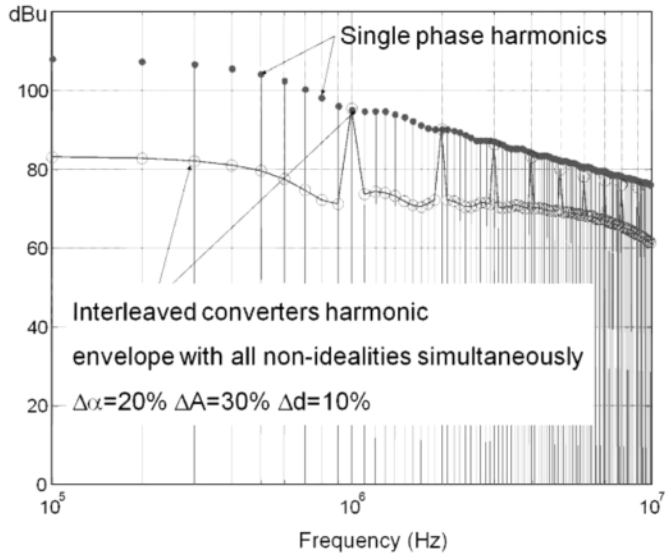


Fig. 14. Effect of nonidealities in the input current harmonic content. One phase is not properly shifted, has a current amplitude 1.3 higher than the others, and has 1.1 times the duty cycle.

The effects of all the aforementioned nonidealities are shown in Fig. 14. This is a worst-case estimation. In practice, all effects appear simultaneously with random distribution in all phases. One effect can act in the same way as another, and vice versa, two different effects can compensate themselves.

In spite of the nonidealities, the effect of the interleaving is positive from the point of view of EMI. For relatively rough tolerances, the attenuation of the first harmonics can easily be higher than 30 dB. Additionally, it is possible to minimize the effect of those nonidealities by reordering the switching sequence of the phases [10].

Another nonideality is the interaction between the converter and the impedance seen from the input terminal of the converter, i.e., EMI filter plus line impedance stabilization network (LISN). When the converter operates in interleaving, the interaction with EMI filter and LISN is not the same as that in single-phase operation, which is due to the fact that the converter presents different input impedance at high frequency in both cases.

V. Simulation and Experimental Results

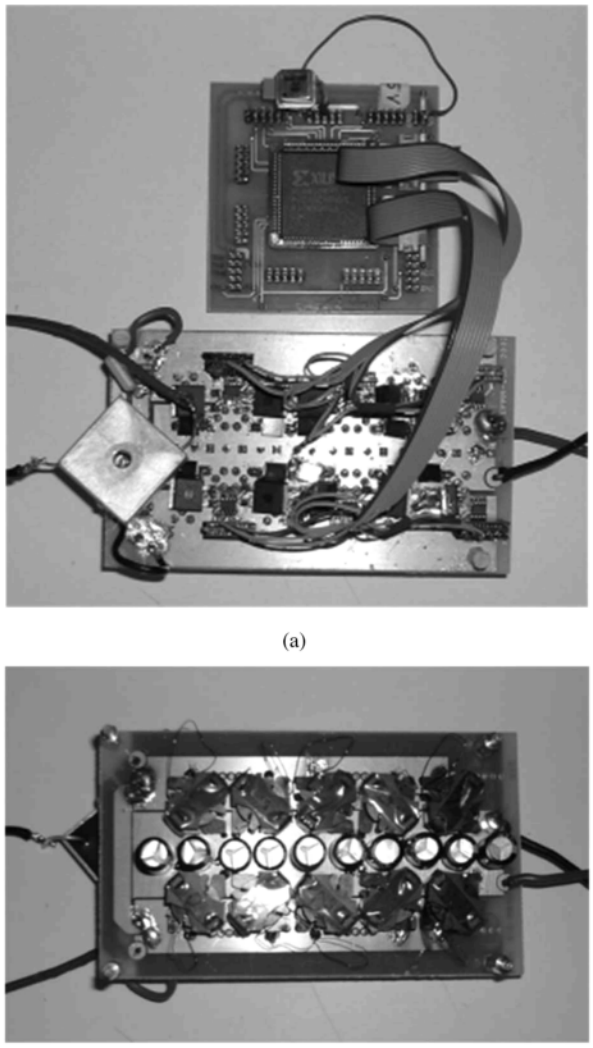
In this section, simulation and experimental results are presented in order to validate the theoretical predictions.

The number of phases (i.e., ten) has been chosen in order to have a significant attenuation of the harmonics and a significant increase of the frequency of the first harmonic in the ideal case. With ten phases ideally, the first harmonic appears at ten times the original switching frequency, which is one decade higher. Moreover, the amplitude of this tenth harmonic is lower compared with the first.

In a real application, the number of phases should be chosen taking into account many design issues, such as efficiency, size, control complexity, and many others, including EMI.

TABLE I
Specifications of the Designed Converter

Input AC Voltage	110 Vac
Output DC Voltage	48 Vdc
Output Power max.	150 W
Switching Frequency	100 kHz
Number of Phases	10



(a)

(b)

Fig. 15. Actual prototype. (a) Full view with control circuitry. (b) Power stage bottom view.

The power stage has the scheme shown in Fig. 2. The main specifications are shown in Table I. The control which has been implemented is a logic programmable device (complex programmable logic device (CPLD), Xilinx XC-9500) shown in Fig. 15. The main pulse is generated by a PWM modulator and then the phase shifting is applied. One of the advantages of using DCM flyback topology for the multiphase converter is that it is not necessary to include any current sharing method. It only depends on the tolerances of the inductors and the duty cycle [25].

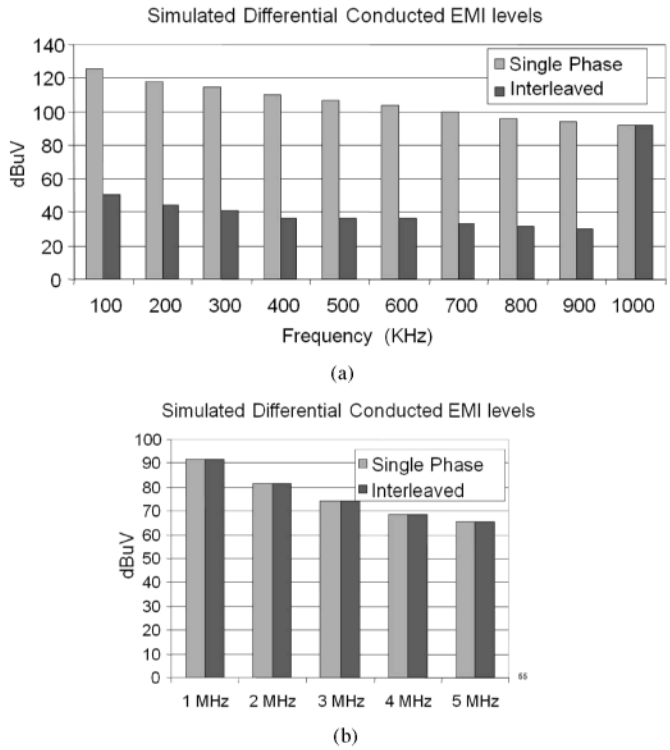


Fig. 16. Comparison of simulated differential conducted EMI levels with LISN ($f_{\text{switching}} = 100$ kHz).

Digital devices can provide control pulses for many phases in a very simple way. Digital hardware description languages provide a very simple way to customize digital controls, especially suitable for many multiphase converters. The converter has been tested in open loop.

A. Simulation Results

Fig. 16 shows the results of the simulation in PSpice of the aforementioned power stage with real component models (see Fig. 2). Results agree with the predictions. In this case, there is no full cancellation due to the simulator numerical errors. The experiment has been performed via simulation with an LISN (described in CISPR 16) to evaluate the DM EMI content.

The first harmonic in the case of the single-phase converter is 126 dBuV at the rate of 100 kHz, while in the case of the multiphase converter, the first significant harmonic is 91.9 dBuV at the rate of 1 MHz. The reduction in amplitude is relatively large; moreover, the frequency of the first harmonic to be filtered is ten times higher. The combined effect of lower amplitude and higher frequency can be observed considering a filter with, for example, an additional attenuation slope of 20 dB/decade. With this slope, the first harmonic of the multiphase converter referred to 100 kHz is 71.9 dBuV, which is 54.1 dB lower than the single phase.

B. Experimental Results

In Fig. 17, the low-frequency shape of the input current is shown. As predicted by theory, DCM flyback with constant duty cycle is a natural resistor emulator. The peak value of the input

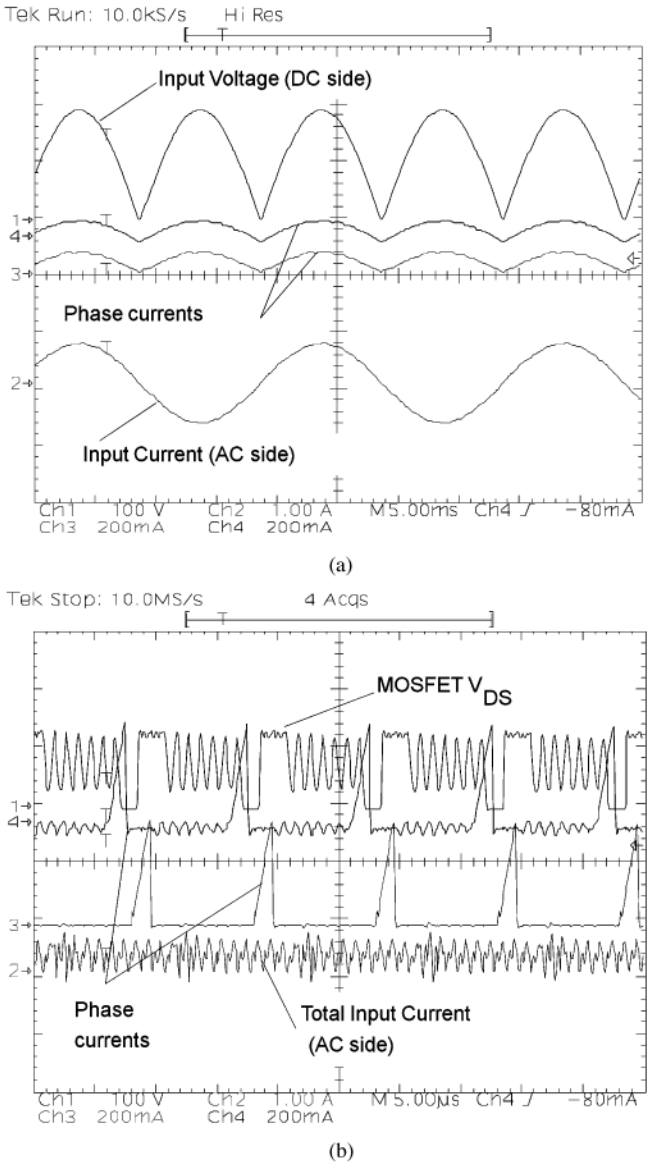


Fig. 17. (a) Measured input current over a line period and (b) in several switching cycles. No filtering has been used.

current is proportional to the input voltage. Since the frequency is constant and so is the duty cycle, the moving average of the input current is also proportional to the input voltage.

Fig. 17(b) shows a detail of the input current. Note that the current ripple in the case of the multiphase converter has a frequency ten times higher than the single-phase current ripple. Moreover, the amplitude is around ten times smaller than the single-phase case. Therefore, the input current is easier to be filtered.

Fig. 18 shows the EMI levels measured in the LISN of both single-phase operation and interleaved operation as well as a typical conducted EMI template (CISPR22). A single-stage EMI filter has been used. The harmonic content of the input current is dramatically reduced, as predicted by the theory. Nonideal effect of the converter (imperfect shifting due to semiconductors, inductance mismatch, effective duty cycle mismatch) produces

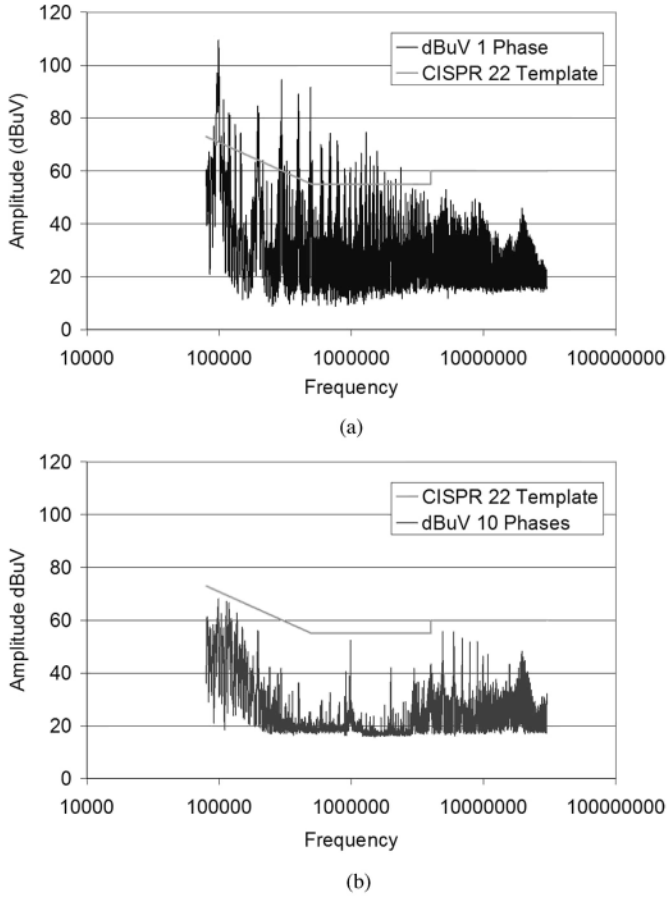


Fig. 18. Actual EMI levels measurements. (a) Single-phase operation with input EMI filter. (b) Multiphase operation with input EMI filter.

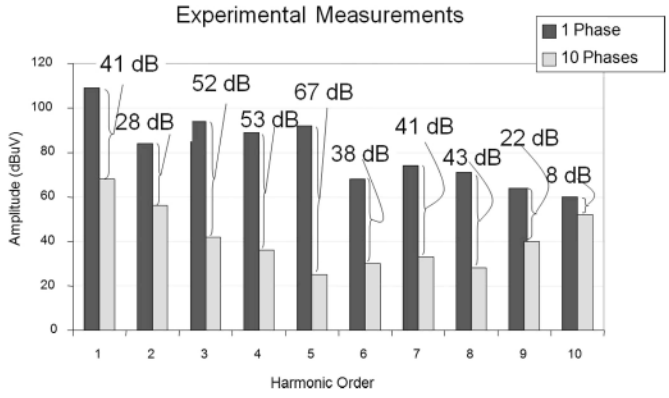


Fig. 19. Harmonic comparison.

the noncancellation of the harmonics nonmultiple of the number of phases, i.e., there should only be harmonics at the rate of 10 × 100 kHz, 20 × 100 kHz, etc. In terms of attenuation (see Fig. 19), the first nine harmonics exhibit attenuation between 22 and 67 dB. The tenth harmonic should be similar but a relatively small difference can be observed (nonlinearities of EMI filter, delays of the driving circuits, etc). Optimization of the power stage (layout, component repeatitivity) can improve this performance, thus providing higher attenuation.

Note that the required attenuation of the input filter is significant with interleaving operation. It means that using an *LC* filter, both the values of inductance and capacitance could be reduced significantly. It yields a significant saving in the EMI filter.

VI. Conclusion

Interleaving of converters can be considered as a topological solution to reduce DM EMI generation. The effect of the interleaving on DM EMI generation has been analyzed. The analysis in the frequency domain shows that interleaving provides harmonic cancellation and increasing of the existing harmonics without increasing of the switching frequency. From the EMI point of view, it means a dramatic reduction of the EMI filter size.

Nonidealities of the multiphase converter, such as nonuniform shifting, nonuniform phase current amplitude, and nonuniform phase duty cycle, limit some of the advantages provided by interleaving, but, in general terms, they provide a significant attenuation for the lowest order harmonics.

A ten-phase flyback converter has been simulated and built in order to verify the theoretical predictions. A significant reduction of the harmonic amplitude can be achieved by interleaving converters (between 22 and 67 dB for the first nine harmonics), while the switching frequency is not increased, as shown in the experimental measurements.

Generation of accurate shifted pulses can be implemented easily in standard digital devices, like FPGAs or CPLDs or standard CMOS technologies. The algorithms are simple and they can be described using hardware description languages, thus providing ease of design and flexibility.

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