BOOST-BASED MPPT FOR THE MTM PCDU OF THE BEPICOLOMBO MISSION

Lapeña, E.[(1)], Rueda, P.[(2)]; García, O.[(3)]; Cobos, J.A.[(3)]; Alou, P.[(3)]; Oliver, J.[(3)]; del Nuevo, M.A.[(1)]; M. de las Mulas, E.[(1)]; Soto, A.[(1)]; Rancaño, J.[(4)]

[(1)]EADS Astrium CRISA
c/ Torres Quevedo, 9 – Parque Tecnológico de Madrid - 28760, Tres Cantos, Madrid, Spain
Phone: +34 91 8068600 – e-mail: elapena@crisa.es; mdelnuev@crisa.es; emulas@crisa.es; asoto@crisa.es
[(2)]ESA-ESTEC
Keplerlaan, 1 - Postbus 299 – 2200 AG Noordwijk – The Netherlands
Phone: +31 71 5656565 – email: pablo.rueda.boldo@esa.int; jesus.rancano@esa.int
[(3)] Universidad Politécnica de Madrid. Centro de Electrónica Industrial (CEI), Universidad Politécnica de Madrid
c/ José Gutiérrez Abascal, 2 – 28006, Madrid, Spain
Phone: +34 91 4117517- e-mail: o.garcia@upm.es; ja.cobos@upm.es; pedro.alou@upm.es; jesusangel.oliver@upm.es
[(4)] ESA-ESTEC, formerly EADS Astrium CRISA

ABSTRACT

BepiColombo is an ESA mission to Mercury to be launched in 2013. A better knowledge of the origin and evolution of the planet, of its structure and vestigial atmosphere, of its magnetosphere, and of the origin of its magnetic field are the main objectives for the program. The journey to Mercury will last for approximately 6 years, and will be based on the gravity of the Earth, Venus and Mercury, and on the use of Solar Electric Propulsion. For the last, the use of the MPPT concept is essential for the mission.

A mission power demand of up to 14kW is foreseen in the cruise phase for the Mercury Transfer Module (MTM) PCDU, being the power subsystem based on a 100V bus. Under this scenario, the use of a classical step-down regulator for the implementation of the MPPT power cell would require to keep the worst case minimum solar array voltage over the bus for any mission operating condition. Then, the maximum solar array voltage would become as high as to overpass the insulating capability of the isolation layer between the solar array cells and the substrate, under the high temperature environment experienced by the spacecraft near Mercury.

As a result, the development of a step-up MPPT Array Power Regulator (APR) becomes a critical issue for the mission feasibility. Moreover, due to the hard environment that the solar array will be exposed to, the segregation of the solar array power is a very desirable feature. Furthermore, apart from the two classical operating modes of the APR – conductance or MPPT, depending on the spacecraft user loads demand and the available solar array power – the APR will have to operate in S3R mode for solar array voltages over the bus, with a fully autonomous transition between the three operating modes.

This paper covers all the aspects related with the design of the APR MPPT concept and its implementation: APR power cell topology, control scheme, control strategy, protections. The implications on the design of the MTM PCDU MEA will be also addressed. Finally, they will be presented the results of the test carried out over an 1/10 scaled-down engineering model of the BepiColombo PCU - including 3 APRs - in front of the real operating conditions foreseen for the MTM PCDU, including all the relevant issues related to the behaviour of the Electric Propulsion load like beam-out events and load transients.

1. MTM PCDU CONCEPT

The architecture of the PCDU for the Mercury Transfer Module is driven by the functionality, the solar generator segregation and the failure tolerance concept of the BepiColombo mission.

A wide range of environmental operating conditions are foreseen for the solar array in the trip between Earth and Mercury, leading to a broad variation in:

- Solar array voltages
- Solar array temperatures
- Other environmental conditions like radiation

leading to a challenging APR design.

To have the solar array voltage always over the bus becomes unpractical not only due to the maximum voltages on the power handling devices, but also due to the lack of capability of the isolation layer between the solar array cells & substrate to withstand simultaneously the high voltage and temperature conditions experienced during the mission.

The only possible solution is to design the solar array voltage to be under the bus voltage, but unfortunately it is not possible to guarantee this condition under all the

Proc. of the '8th European Space Power Conference', Constance, Germany, 14–19 September 2008 (ESA SP-661, September 2008)

mission phases. Fig.1 shows a simulation of the solar array voltage range foreseen near Earth and Mercury.

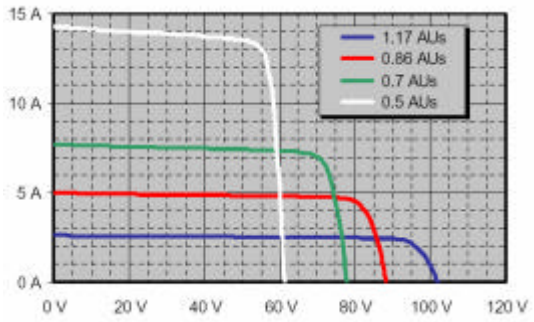


Figure 1. BepiColombo range of solar array I-V curves

The S^3R operational mode is a natural consequence of the solar array voltage evolution when exiting eclipse and the panel is cold.

A 14kW mission requires a large solar array that may experience significant differences in temperature and illumination along its structure. Then, its segregation into independent sections becomes a practical issue. The following boundary conditions define the design baseline:

- 30 independent solar array sections.
- Maximum power to be conditioned per section of 485W.
- Solar array input power to be clamped near Mercury, as power in excess of 600W will be available even if the solar array is de-pointed with respect to the Sun.

In this way, each APR has to face three operational modes: conductance, MPPT and S^3R. A fully autonomous transition – without external intervention – is required among them.

A 100V unregulated bus is the baseline for the mission – whose nominal voltage may fall down to 90V – and abnormally down to 40V, with the need for autonomous recovery capability. The Li-Ion battery management is based on the classical two operational modes: either charge at constant current (programmable to be C/2 or C/3) or taper charge when EOC voltage is reached. Again an autonomous transition between modes is required, based on reliable control electronics.

As mentioned before, the PCU shall restart autonomously from any abnormally low battery voltage – even without battery connected to the bus – thanks to the following autonomous start up sequence: 1) Start the APR auxiliary supply – provided with input under-voltage protection - from the solar array power as soon as it is available 2) Supply the MEA 3) Perform a soft start action of the APR converters under MEA control.

This means that the system is only enabled to start up if two conditions are met: 1) The APR auxiliary supply is formed, and 2) MEA is properly supplied.

The mass is a critical issue in the BepiColombo mission, in this way two massive elements are reduced to a minimum:

- The bus capacitor value, while being compliant with the bus quality figures, and
- The MTM battery size, meaning that it is not possible to rely on it for supporting the PCDU load transient behaviour, then a minimum MEA bandwidth is required

2. THE APR CONVERTER POWER CELL

Power dissipation is a critical issue for the feasibility of the proposed PCDU concept. To achieve an efficiency figure as high as possible for the APR converter, a passive lossless turn-on/turn-off snubber network is implemented for the boost PWM converter, Ref. [1]. Besides the benefit of small number of added components, all the devices block a voltage not higher than the output DC voltage.

The snubber is based on making use of the reflected voltage on a coupled inductor. In this way, only an additional winding of an existing inductor, three auxiliary diodes and one snubber capacitor are required in addition to the classical boost converter components. Although there is one more diode voltage drop in the power path from the solar array to the bus bar, the extra conduction losses are not significant compared with the switching losses reduction achieved. Moreover, this additional diode is required to protect the bus from SC in the output diode.

Fig.2 shows the basic elements of the proposed topology along with the names for the most relevant circuit variables. The leakage inductance of the coupled inductor that plays a relevant role in the converter behaviour is also shown in the figure as L_lk.

Next paragraphs will briefly describe the operation of the circuit with reference to the waveshapes shown on Fig. 3.

Initial conditions: The switch SW is on, carrying the magnetisation current of Lm. No current flows through Ds, Do, Da and Db, and Cs is charged at Vbus.

Voltage rise at the drain of SW, T0 < t < T1

The MOSFET SW is switched off. A driving of the gate as fast as possible is needed for an optimum efficiency. The capacitor Cs slows down the rate of rise of the voltage at the drain of SW, while the current on Lb_a is

"immediately" transfers to diode Do, which was at zero volts (no reverse recovery) thanks to the action of Cs.

This subinterval finishes when the voltage on Cs reaches 0 Volts, i.e., the drain to source voltage of the MOSFET equals Vbus. The rate of change of these voltages is imposed by the energy stored in the Lm inductor whose current is changing the voltage on Cs.

Note that Ds is kept reverse biased, hence current on it remains at zero.

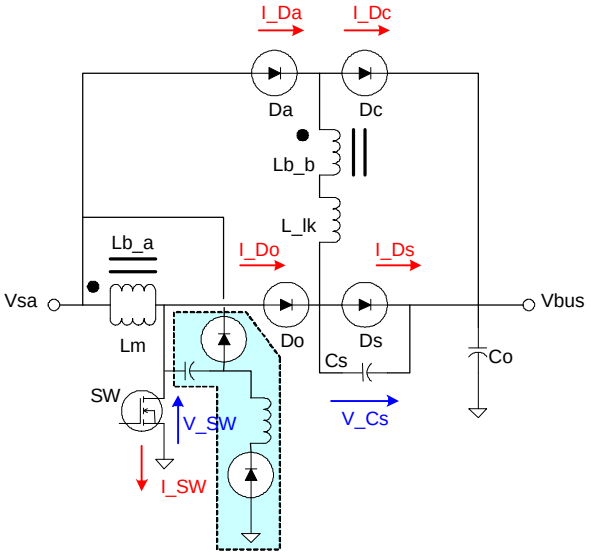


Figure 2. The APR converter power cell.

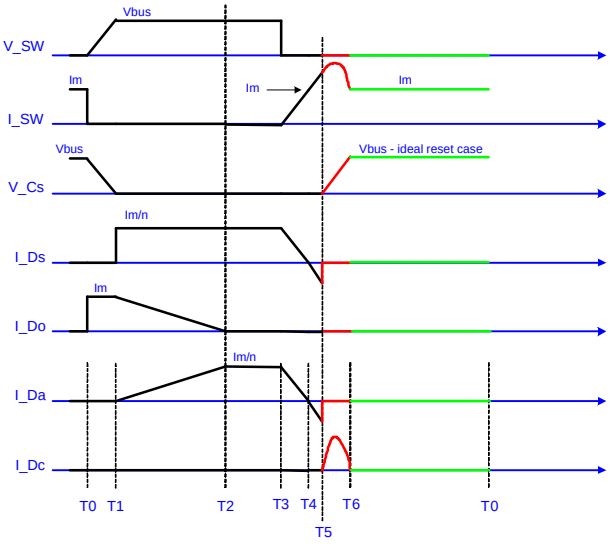


Figure 3. The APR converter switching waveforms.

Current shifting from Lb-a to Lb-b, T1 < t < T2

Now the diode Ds is ready for starting to drive current. Thanks to the coupled inductor turns ratio, the voltage reflected on Lb_b is slightly higher than the one on Lb_a, just to reverse bias the diode Do. But this process will not finish up to the moment on which the leakage inductance L_lk is forced to drive the whole Lm current affected by the turn ratio "n". During this process, the current interchange between Lb_a and Lb_b takes place.

The switching frequency, the coupled inductor leakage inductance, and the minimum (1-d) value must be compatible to get a complete reset of the Lb_a inductor at least for those cases where switching losses are higher.

No change takes place on Ds current during this subinterval, as the composition of Do and Da remains constant.

Waiting for switching SW back to on, T2 < t < T3

At T2, Do stops driving current and the circuit remains static for what respects the output current.

SW is set on, L_lk current drops to zero, T3 < t < T4

A fast driving signal on the gate of SW puts the device in on state, but no current still flows through it. First, the current on L_lk must drop to zero thanks to the voltage "n x Vsa" reflected by the coupled inductor whose "primary winding" Lb_a sees Vsa.

When the current on the L_lk inductance reaches zero, Da and Ds stop driving current. This means that the whole current was transferred to SW.

Note that up to T4 the voltage on Cs remains at zero volts and the diode Do is blocking Vbus.

Reverse recovery of Ds, T4 < t < T5

At T4 the current on L_lk reached zero Amps, but the current on it continues to negative to achieve the reverse recovery of Ds. The additional benefit of having L_lk is a limitation in the magnitude of the peak recovery current on Ds. The same current that achieves the recovery of Ds circulates through Da.

Resonant reset of Cs, T5 < t < T6

At T5 the reverse recovery current of Ds reaches its maximum value. The reflected voltage of Lb_a on Lb_b puts in conduction the Dc diode enabling a half cycle resonance between L_lk and Cs. The full recovery (reset) of Cs for the next switching cycle is only complete for certain range of the Vsa voltage, then the component sizing must ideally account for that in order to achieve full reset of Cs under the most dissipative working conditions.

T6 < t < T0

The last subinterval lefts all the converter variables "as we found at T0", hence a new switching cycle can start.

Note on classical resonant snubber

As mentioned above, the full reset of the Cs capacitor only takes place for some particular conditions of the input (solar array) and output (bus bar) voltages. The total reset condition takes place if

$$Vsa \times (n+1) > Vbus$$

Additionally, high power dissipations could take place if one of the components in the snubber is lost. In view of the above considerations, a second "classical" resonant snubber has been added to the design to solve potential issues. Fig. 2 shows dashed in light blue the practical implementation of this second snubber that provides reliable APR operation at the cost of some extra mass. This very well known snubber, classical in many converter applications, will not be described here.

Important note: it must be kept in mind that in the S^3R mode, the 2 plus 2 diode chains drive almost equal currents in DC, only different according to the parasitic resistance of the two power paths. In consequence all the diodes have been selected to have a TO254AA package or similar.

3. THE APR CONTROL ISSUES

As mentioned in the previous paragraphs, the APR converter and its control electronics has to face 3 different operation modes depending on the user power demand, the solar array voltage magnitude and the bus bar voltage. A fully autonomous transition among the three operation modes is required.

- Conductance mode: the APR performs like a constant current source proportional to the MEA voltage. An excess of solar array power is available with respect to the user & battery charge needs.
- MPPT: The maximum available solar array power is extracted. The MPPT control electronics overrides the conductance control when the APR operates in this mode. One independent MPP tracking circuit per SA section is implemented, according to the classical principle presented in Ref [3].
- S^3R: For those cases when the solar array voltage is over the bus.

The APR conductance operation takes place in the voltage region of the solar array I-V curve, as shown in Fig. 4, where it is also shown the transition point to MPPT mode.

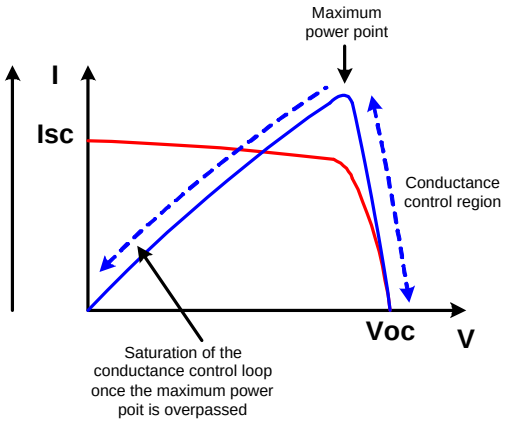


Figure 4. The APR mode vs. the solar array I-V curve.

A power clamping is required as long as near Mercury the available solar array power exceeds by far any possible (bus + battery charge) power demand. This fact is a consequence of sizing the solar array to be capable of operating at full power near Earth.

If all the APR converters are controlled in parallel by the same dynamic range of the MEA signal, sub-harmonic oscillations may take place in the power system when crossing the boundary between conductance and MPPT modes, as some dispersion will exist among the moment on which the different APR converters enter in MPPT mode in response to the same common MEA signal. In consequence, the following MEA plan is the baseline for the PCU design:

- Sequential organisation of the APR converters. In this way the system is always aware of the potential remaining power capabilities. This means 30 domains for "conductance/MPPT" + 30 domains for "S^3R", one per APR.
- Conductance / MPPT operation: for a given MEA voltage, 1) all APRs whose domain voltage range is lower are in MPPT mode, with the conductance loop saturated, 2) that APR whose domain voltage contains the MEA voltage is in conductance mode. See Fig. 5.
-

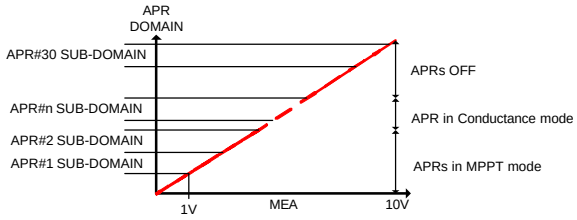


Figure 5. The conductance/MPPT range of the MEA.

May be one solar array section is “the first in being over the bus” while MEA is still in the conductance / MPPT range, then two options are possible:

1) MEA continues in the conductance / MPPT region, as the system finds a new equilibrium point accounting for the power coming from one section in S^3R mode (Isc x Vbatt), and reducing eventually the power provided in conductance/MPPT by the APRs in operation, or

2) The system power consumption is so low that sequentially al the APRs go to off and the MEA signal goes to S^3R sub-domain. See Fig.6.

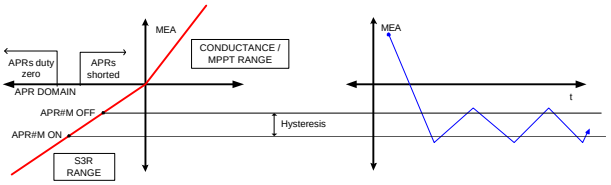


Figure 6. Conductance/MPPT to S^3R transition.

For what respects the S^3R mode, two main different scenarios are possible, see Fig.1 for reference:

1) The battery is fully charged and therefore the bus voltage is regulated by the Main Error Amplifier voltage loop to 100V. The maximum solar array section current defined for voltages higher than 100V is below 2 A.
2) The battery is partially discharged and its charge current is regulated by the Main Error Amplifier battery current loop. The bus voltage could be between 40V and 100V in nominal conditions. The maximum solar array section current defined for voltages higher than 40V is 15 A at most.

The S^3R mode implementation is based on the MEA voltage, in such a way that it has been designed in order to achieve the best compromise between a reasonable bus ripple and an acceptable power loss figure.

An important issue is the magnitude of the peak current on the solar array section when the APR converter operates in S^3R mode. The design enables for a soft-switching of the (solar array section worst case maximum effective output capacitance + APR input filter capacitance). The worst case maximum value for the peak current on the diode in series with the solar array section, for a solar array capacitance corresponding to the worst case operating conditions – 3uF according to best available model data - when exiting from an eclipse while orbiting Mercury, is lower than 35Amps.

Even if the Solar Array interface characteristics are still pending of consolidation, this number is compatible with the maximum repetitive peak current that the diode in series with the solar array section is able to withstand. Moreover, a control mean for the peak current is provided, that can be tailored to the final solar array section interface definition when available.

The APR overall control strategy is shown on Fig. 7.

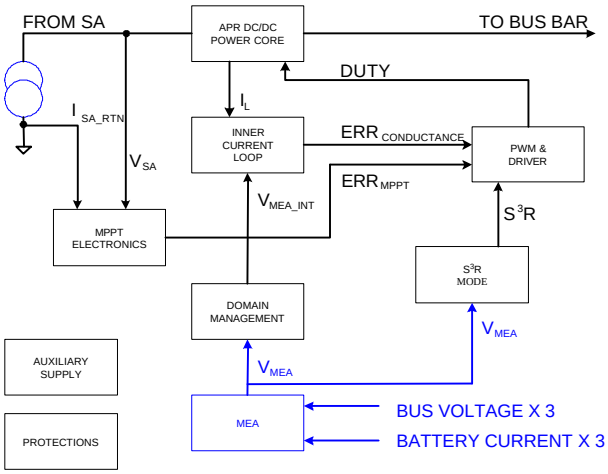


Figure 7. The APR control electronics.

The MEA controls the boost inductor current. This current is sensed in the converter power line with a low ohmic value resistor in series with the boost inductor to avoid any common mode noise problem.

It must be kept in mind that this current is not directly related to the converter output current. Then a control law has to be implemented to compensate MEA signal as a function of input (solar array) and output (bus) voltages to get an “APR output current to MEA conductance ratio” independent from the APR working conditions through the mission. This control strategy also provides compensation for the RHPZ issues intrinsic to the boost topology. Fig. 8 provides further details on the APR inner current loop implementation.

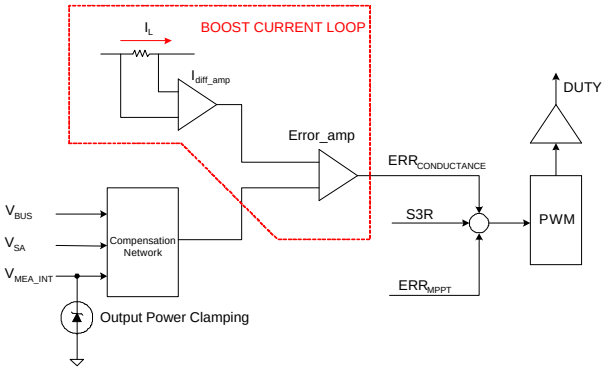


Figure 8. The APR inner current control loop.

Another important control issue is that related to the CCM/DCM operation. Analysis and measurements of the APR inner current control loop show the classical dramatic reduction in gain and bandwidth, inherent to the discontinuous conduction mode; nevertheless, gain and phase margin stays around a comfortable value. An exhaustive analysis and characterisation campaign has been run to demonstrate that the gain and phase margins remain stable along the DCM operation range and in the CCM/DCM boundary. The MEA EOC control loop shows a significant but not dramatic bandwidth reduction when the APR converter is in DCM, with comfortable gain and phase margins.

4. PROTECTIONS

The design of the protections is driven by the fact, coming from mission and power system architecture analysis, that it is acceptable to loss one solar array section at system level. In this way, the protections design – supported by the classical FMECA analysis - is focused on:

- Not propagating failures to the bus.
- Not propagating failures to the "contiguous APR", as three are implemented per PCB.

Thermal protection: One thermistor per APR is implemented, to cope with the APR converter failure modes leading to over-dissipation. The protection forces a duty cycle equal to 1 on both MOSFET in parallel that constitute the APR boost switch. In this way it is eliminated the source for power dissipation before the failure propagates. Independent driving sources are used for every MOSFET in parallel; hence a MOSFET in linear mode can be short circuited by the other in parallel. Note also that this protection is not intended for protecting any particular power device, but to avoid thermal failure propagation to the contiguous APR.

Bus over-voltage: The APR implements a bus over-voltage protection, only intended for operation on ground. The protection has an operating threshold and an actuation delay, to prevent from false triggering

Boost short circuit to the bus: It is a main issue not to propagate short circuits to the power bus rail, what would mean the loss of the mission. Note that the selected topology provides inherent protection against such events, thanks to the coupled inductor snubber implementation described above: two diodes in series are in any power path connected to the positive lead of the bus bar. Hence two consecutive failures in the same APR converter would be required to provoke a single point failure. Obviously, the APR output capacitor, as part of the distributed bus capacitor concept implemented in the PCU, is of the self-healing type. The low impedance path of the PCDU bus bar, designed to carry currents in excess of 140 Amps, and the capacitor bank that constitutes the bus capacitor, provides more than enough energy to carry out the self healing process.

APR and auxiliary DC/DC converter control loops: It is well known that the failure in open circuit or short circuit of one of the components in the converter control loop may lead to converter erratic performance or even oscillations. Following the CRISA heritage of the design made for the LISA Pathfinder PCDU MPPT electronics, the passive elements (resistors, capacitors) that define the converter feedback loop and gain are redounded with the sufficient number of elements in series and/or parallel such as to get that after a single component failure the converter control loop remain stable, maybe with some degradation in the gain and phase margin but still stable.

Eclipse protection: During an eclipse, the battery is discharging continuously due to the lack of power in the solar generator. The aim of this protection is to save power from the battery during eclipse periods. Once this situation is detected by the system, the duty cycle is fixed to one to avoid any extra consumption in the driving and the switching of the boost converter power MOSFETs.

APR output over-current: This failure mode may be caused by the APR control electronics improper performance, either due to an error in the acquisition of the output variable used for the feedback loop closure (inductor current), or due to a "saturation to high" condition in the conductance control reference signal to occur inside the APR module (remember that outside the module is not possible as the MEA signal is a one failure tolerant line).

When coming out from an eclipse, the battery voltage will be low, hence it is impossible to produce an over voltage condition in the bus due to an APR converter in over current condition. An excess of current coming from a single APR cannot provoke an over current condition on the battery, as the maximum battery current charge setting is C/2, what for a 30 Amp-h battery, means 15 A. The maximum achievable contribution of a single APR module is in the range of the maximum short circuit current of one solar array section, less than15 Amp according to Fig.1. Moreover, the output from the other APR modules will be adjusted by the Battery Control Management electronics to get the desired rate of charge.

In case of a boost in short circuit input-to-output, (i.e. MOSFET power switch permanently off, but output series diodes remaining operative), the only possibility for this APR to dump current from the solar generator

into the battery is that the solar generator voltage be higher than the battery voltage. This can take place only when the solar generator is cold, after an eclipse.

Let's assume the bus at EOC. If we intersect the solar generator characteristic with the constant battery voltage line, the resulting working point leads to a current drawn from the solar generator in the range of 1 Amp. This means around 100W of electrical power dumped on the power bus, which is less than the minimum user's power consumption of 140W stated for the PCDU. Hence, no overcharge or over voltage is foreseen under any circumstance. See Fig. 9 for reference.

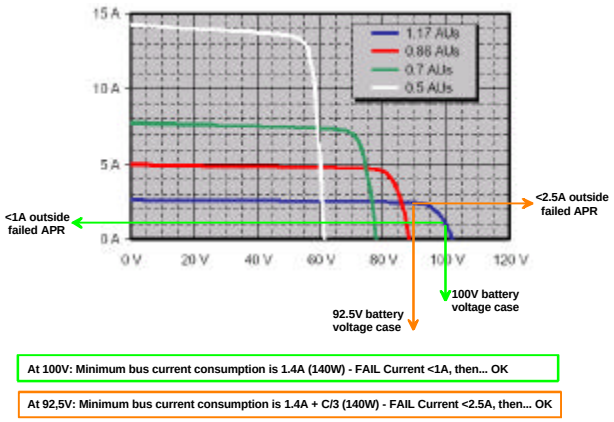


Figure 9. Maximum solar array section current on the bus with an APR failed.

MEA reliable error signal: the bus control is under the responsibility of the main error amplifier that controls the battery charge either in conductance control mode or by enabling the MPP Tracker mode or the S^3R mode. The main error amplifier generates the Reliable Error Signal for this purpose, as result of a {two out of three + majority voting} one failure tolerant system. Hence it is not possible to provoke an under voltage or over voltage condition in the bus due to improper operation of the MEA.

Auxiliary DC/DC converter short circuit to the bus: The APR auxiliary DC/DC converter takes the power from whatever the available power source be, either the solar array or the battery (bus) voltage. The input stage of the auxiliary DC/DC converter implements a non latching over-current protection that limits the current drawn by the converter in case of failure. As soon as failure condition disappears, the converter will re-start its operation in an autonomous way without need for external intervention.

Auxiliary DC/DC converter output over-voltage: The secondary voltages generated by the auxiliary converter are used to power the APR control electronics. Failure modes exist, for example in the PWM controller, leading to over-voltage in the secondary outputs. The most critical consequence of this failure mode is the erratic behaviour of the APR. Hence, every auxiliary power supply secondary voltage is equipped with an over-voltage protection. Again, the protection does not implement any latching mechanism, converter restarts automatically if the failure condition disappears.

5. CHARACTERISATION RESULTS

To validate design concept and system performances a 1/10 scaled down prototype of the 14kW PCU has been built, that is 3 APR in a single PCB which is the baseline modularity for the MTM PCDU. The prototype is fully representative of the intended flight design in all functional aspects and electrical interfaces, providing also capability to be thermally cycled. See Fig. 10.

Figure 10. The APR module with 3 x APR converters.

An exhaustive characterisation campaign has been run to demonstrate the compliance of the design to the applicable set of requirements. Only the most relevant test results are shown here.

Bode plots of APR inner current loop: The plots shown, see Fig.11, are for the following operating conditions: Bus voltage, 100V - Solar array voltage, 55V – APR Output power, 400W – No battery connected.

The blue line in the plots corresponds to the Matlab model of the APR inner current loop design, which fits very well with the measurement results. An important point to be taken into account is that the SAS source impedance presents a zero at 500Hz, and then only represents the solar array real impedance at low frequencies, so this test was made with a constant voltage source.

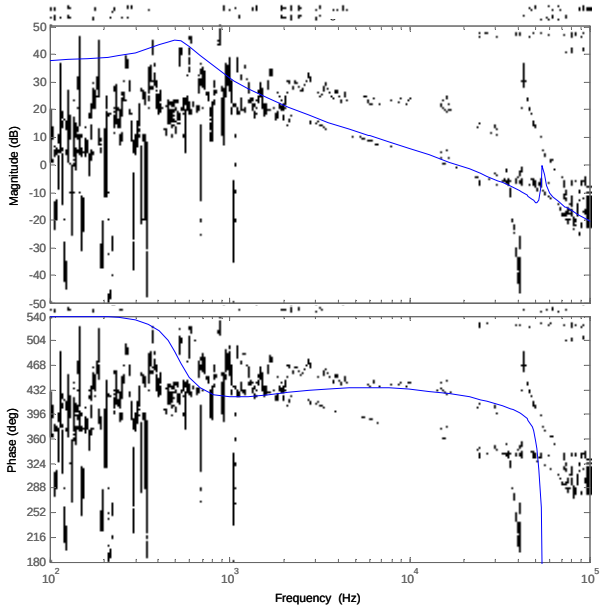


Figure 11. APR converter Bode plots of the inner current loop.

Bus quality @ MPPT mode: The plot shown, see Fig.12, is for the following operating conditions: Three APR in MPPT mode - SAS @ 0,86AU curve, that is Voc = 88V / Isc = 5A - Csa = 3uF – Bus voltage = 100V – Load = 1100W.

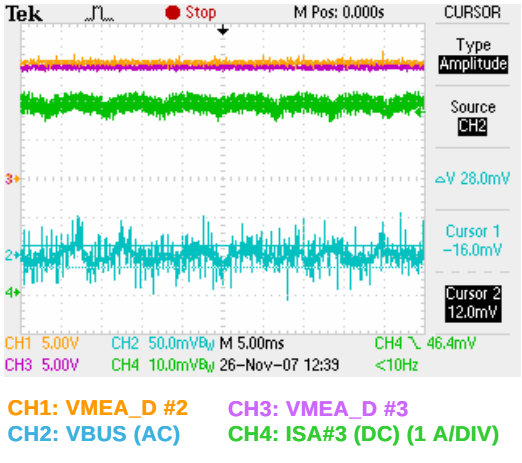


Figure 12. Bus ripple in MPPT mode.

MEA EOC loop: The plots shown, see Fig.13, are for the following operating conditions: Bus voltage, 100V – Solar array voltage, 60V – Output power, 400W – No battery.

The blue line in the plots corresponds to the Matlab model of the MEA EOC loop design, which fits very well with the measurement results.

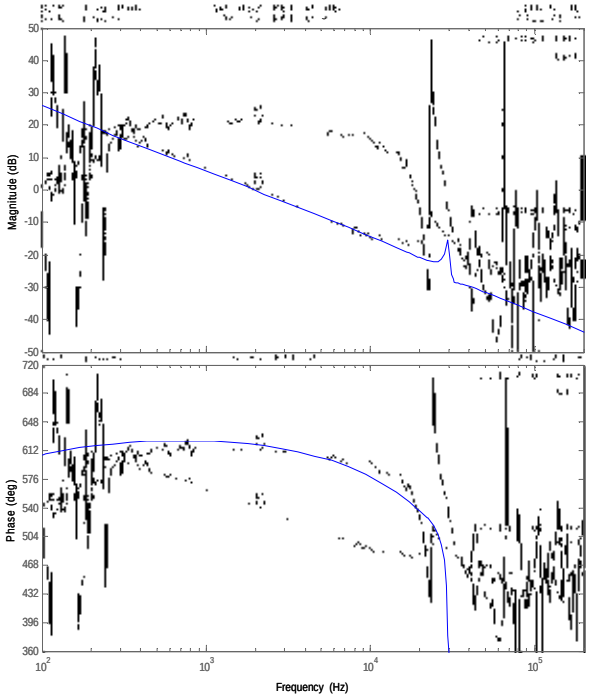


Figure 13. MEA EOC loop Bode plot.

Bus quality @ S^{3}R mode & MEA EOC loop: The plot shown, see Fig.14, is for the following operating conditions: Isc = 4A - Voc = 110V - Csa = 3uF – Bus voltage, 100V. In this operating point, APR#1 and APR#2 MOSFET are switched off, so they are delivering power from the SAS to the battery through the boost diodes, and APR#3 is regulating in S3R mode.

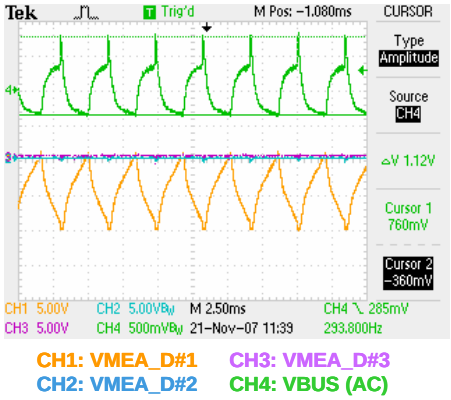


Figure 14. Bus quality in S^{3}R mode @ MEA EOC loop.

When the MEA is controlling the battery current charge, the worst case conditions are: Isc = 14A - Voc = 60V - Csa = 3uF – Bus voltage = 40V. With the battery under EOC, the plots exceed the required 1,5Vpk-pk figure on the bus. The dynamic response of the current loop will be improved and the battery current sense resistor shall be reduced to10mO (instead of the 20mO used in the tests), in order to comply with the requirement with a maximum solar array Isc of 14A.

The APR converter time-domain Matlab model shows very good correlation with test results for the 1/10 scaled down prototype. Then the Matlab simulations can be used for extrapolating the test results to the full power case representative of the real mission conditions.

Load transient +300W: The plot shown, see Fig.15, is for the following operating conditions: 1/10 scaled down load transient of +3000W - Isc = 5A - Voc = 45V - Csa = 3uF – Bus voltage = 100V.

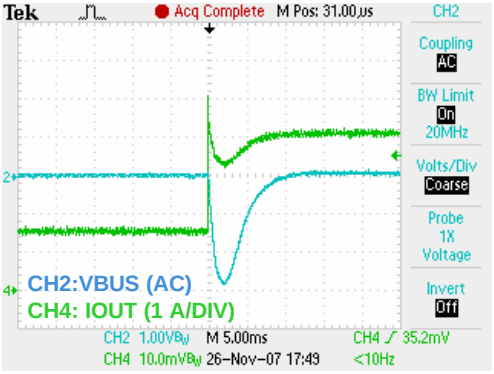


Figure 15. +300W 1/10 scaled down load transient.

Load transient -300W: The plot shown, see Fig.16, is for the following operating conditions 1/10 scaled down load transient of -3000W - Isc = 5A - Voc = 45V - Csa = 3uF – Bus voltage = 100V.

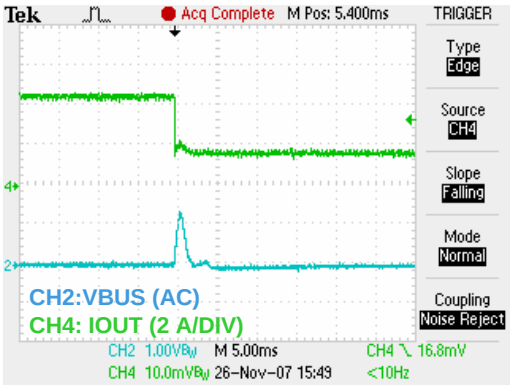


Figure 16. -300W 1/10 scaled down load transient.

Beam out event scaled down test: The main load of the MTM PCDU is the electric propulsion system, which may suddenly shut down when operating at full power. Then a load transient of -1300W (1/10 of real transient) is tested to see how the system behaves. The plot shown, see Fig.17, is for the following operating conditions - Isc = 7A - Voc = 85V - Csa = 3uF – Bus voltage = 100V.

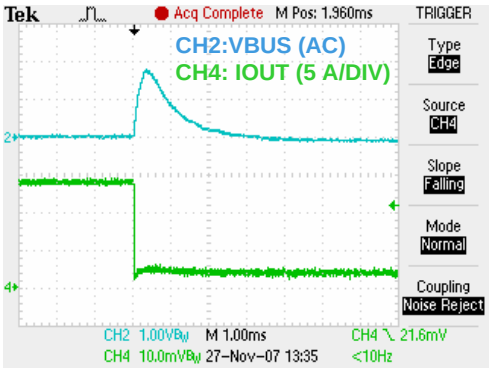


Figure 17. -1300W 1/10 scaled down beam out transient.

Transition to EoC: Fig.18 shows the smooth transition to EOC under MEA control.

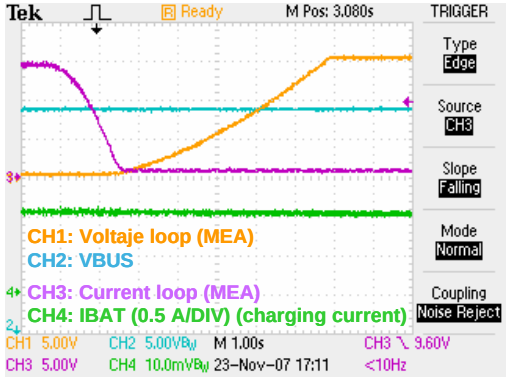


Figure 18. Transition to EOC.

Conductance to MPPT transition: The following transition is provoked in the system, see Fig.19.

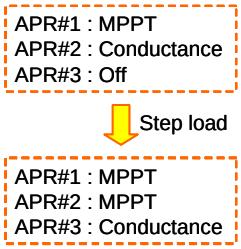


Figure 19. Conductance to MPPT transition.

The result is shown on Fig. 20.

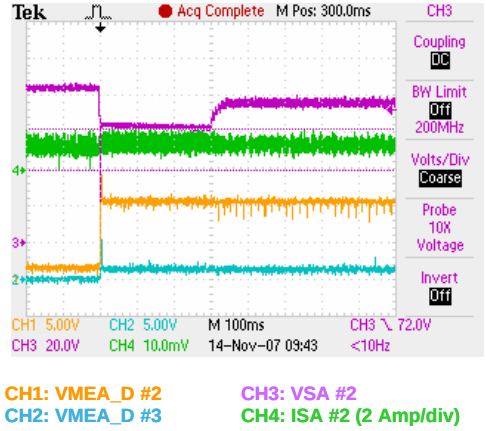
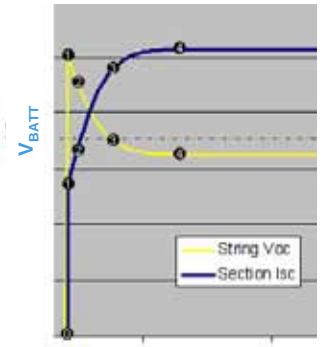


Figure 20. Conductance to MPPT transition.

Eclipse – sunlight near Mercury: According to the available mission data, the following eclipse – sunlight transition was simulated, see Fig. 21.



Step	Voc	Isc	Time (sec)
0	0	0	0
1	120	7.5	0.024
2	100	8	26
3	78	8.5	60.8
4	68	8.7	121.6
5	68	8.7	180

Figure 21. Eclipse to sunlight transition near Mercury.

Fig.22 shows the test results with the transition between the APR operating modes.

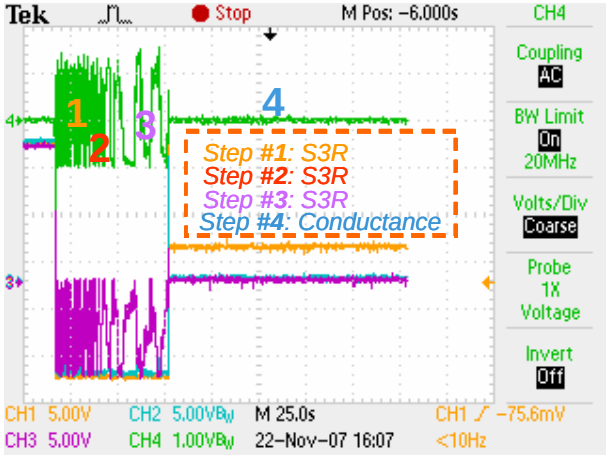


Figure 22. APR behaviour in an eclipse to sunlight transition near Mercury.

PCU output impedance: The plot shown, see Fig.23, is for the following operating conditions: No battery - Isc = 7A - Voc = 70V - Vmpp = 60V – Bus voltage = 100V.

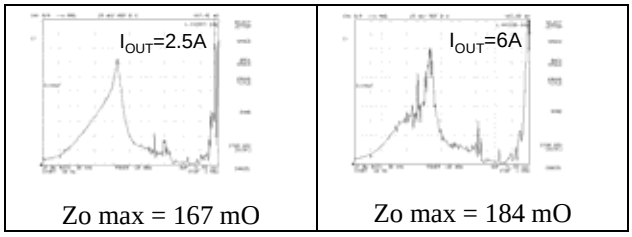


Figure 23. PCU output impedance in EOC.

Efficiency: provided at MPPT operation, see Fig.24, where more power is needed in the system, hence efficiency data is more representative of system behaviour.

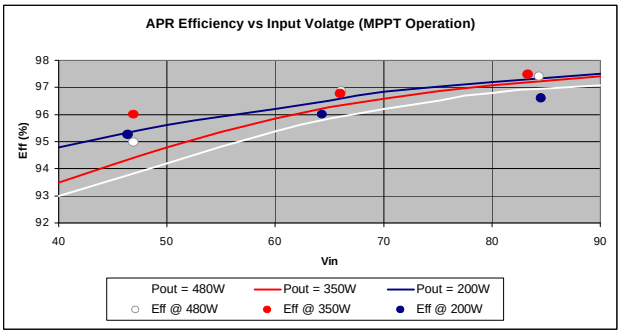


Figure 24. APR efficiency in MPPT mode.

AKNOWLEDGEMENTS

This activity has been developed under the ESA GSTP contract reference 20997/07/NL/JD/na. We wish to specially acknowledge to Mr. Bouke Van der Weerdt from ESA-ESTEC for his valuable contribution and useful technical discussions on the system architecture and performances.

REFERENCES

1. Rueda, P. Segregated Maximum Power Point Tracking based on Step-up Regulation. 7th ESPC, Stresa, Italy. May 2005. ESA-SP-369, pp. 171-174.
2. R.Martinelly, C.Ashley. Coupled Inductor Boost Converter with Input and Output Ripple Cancellation. APEC-91.
3. W. Denzinger Electrical Power Subsystem of Globalstar. 4th ESPC, Poitiers, France, September 1995. ESA SP-369, pp171-174