Aluminum nitride for heatspreading in RF IC's

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A B S T R A C T

To reduce the electrothermal instabilities in silicon-on-glass high-frequency bipolar devices, the integration of thin-film aluminum nitride as a heatspreader is studied. The AlN is deposited by reactive sputtering and this material is shown to fulfill all the requirements for actively draining heat from RF IC's, i.e., it has good process compatibility, sufficiently high thermal conductivity and good electrical isolation also at high frequencies. The residual stress and the piezoelectric character of the material, both of which can be detrimental for the present application, are minimized by a suitable choice of deposition conditions including variable biasing of the substrate in a multistep deposition cycle. Films of AlN as thick as 4 μm are successfully integrated in RF silicon-on-glass bipolar junction transistors that display a reduction of more than 70% in the value of the thermal resistance.

Keywords:
Aluminum nitride
Bipolar transistor
Electrothermal phenomena
Heatspreader
Piezoelectric characteristics
RF integration
Thermal instabilities
Thermal resistance

1. Introduction

Thermal management of silicon IC's has over the years become more and more challenging due to the ceaseless increase of power density caused by the continuous scaling and drastic isolation schemes being implemented throughout the whole semiconductor industry In SOI and substrate transfer processes, the separation of the devices from the thermally conductive Si substrate seriously aggravates the matter. For RF applications, substrate transfer processes are particularly interesting because the lossy Si substrate can be replaced by an insulator As a drawback, however, the aggressive electrical isolation of the Si devices with dielectric materials such as SiO_2 and SiN_x can also lead to a very high thermal resistance. This has been demonstrated in our in-house silicon-on-glass substrate transfer process described in in which bipolar transistors with record high thermal resistance values were realized. On a circuit level, such high thermal resistance seriously hampers reliable circuit design due to strong electrothermal phenomena. To tackle this problem at a device level, an attractive solution is to incorporate a heatspreader in the design. To be effective, this heatspreader must be in close proximity to the devices and be made of a material that has good thermal conductivity as well as good electrical insulation properties, so as not to deteriorate the electrical performance of the devices. Aluminum nitride answers to this description and, in the form of polycrystalline thin-films, it is fully compatible with standard silicon technology. The poly-films have been exploited in integrated surface- and bulk-acoustic-wave devices because AlN has the additional property of being a piezoelectric material, an aspect that has been receiving an increasing amount of attention For our purpose, however, piezoelectric behavior is undesirable since the application of electric signals to the circuits could then initiate additional stress in the AlN films as well as parasitic resonators that could interfere with the intended functioning of the devices. Suppressing piezoelectric behavior in AlN while preserving a sufficiently high thermal conductivity can be achieved by inducing the growth of grains with good crystal quality but with a random distribution of the polar momentum so that the net contribution of all the grains to the piezoelectric response of the film is negligible.

In the present work, a physical-vapor-deposited (PVD) low-stress AlN layer has been evaluated for the first time for use as heatspreader in RF devices and circuits. In a previous paper 0.8 μm-thick layers were integrated in our silicon-on-glass bipolar process and shown to have a heatspreading effect. Here, the layer thickness has been increased up to 4 μm and the films have been extensively characterized with respect to DC and high-frequency electrical performance including piezoelectric behavior. Since the overall properties of deposited films can be very equipment and process flow dependent, and, needless to say, very different from

the corresponding bulk properties, the structural and optical properties were also extensively monitored and reported here in brief. To minimize the piezoelectric effects, AlN films with grains of alternating polarity were fabricated by implementing a multilayer deposition scheme. At the same time, this scheme was configured to also minimize the residual stress of the AlN layers in a manner similar to methods previously reported for other material systems

The dielectric properties of the AlN that are important for applications in high-speed devices are determined for a wide range of layer thicknesses. For the actual integration in the silicon-on-glass technology, any residual stress in the thin-films can be very destructive, a fact that limited the maximum layer thickness, before substrate transfer to glass, to 4 μm. The benefits of applying several micrometer thick layers as heatspreaders are quantified by measuring the thermal resistance of individual transistors as well as by studying the electrothermal behavior of small circuits of two and three transistors operating in parallel.

2. Aluminum nitride deposition

Thin-films of AlN were deposited by reactively sputtering a pure aluminum target with a nitrogen and argon admixture at a total pressure of 5 mTorr. A 2 kW pulsed-DC power supply with a frequency of 250 kHz and a duty cycle of 40% was used to create the discharge. Before deposition the wafers were preheated at 380 °C for 1 min in Ar atmosphere at 1 Torr of pressure. The tensile in-plane residual stress of the AlN layers as a result of the above deposition conditions could be altered to compressive stress by applying an RF bias to the substrate. To reduce the stress of AlN layers of a few micrometers, a multi-step deposition process with alternating 0.2 μm-thick layers were deposited by turning off and on a substrate bias of 20 W. This provided AlN layers of up to 4 μm-thick with stress levels low enough to allow reliable integration in the silicon-on-glass process. In addition, this approach also annihilates the piezoelectric response, as will be described in next Section.

3. Aluminum nitride properties

3.1. Structural and piezoelectric characterization of AlN films

The structural properties of the AlN films were obtained by using X-ray diffraction (XRD) $\theta/2\theta$ patterns and the rocking-curves (RC) around the 00 · 2 AlN reflection [18.02° (θ)], while the piezoelectric activity was evaluated by the measurement of surface acoustic wave (SAW) devices.

XRD measurements indicated that the crystal quality of the AlN films was very good, as all the films exhibited a high degree of *c*-axis orientation. However, some small peaks corresponding to other orientations (10 · 1, 10 · 2, and 10 · 3) were also present in the XRD patterns, revealing the presence of tilted grains among the *c*-axis-oriented grains normal to the surface. This result was confirmed by infrared reflectance measurements, which exhibited the two characteristic modes of vibration associated with the grains normal to the substrate (A1(LO) at 890 cm^{-1}) and tilted grains (quasi-LO at 910 cm^{-1}), respectively. It is worth noting that the presence of tilted grains has been associated previously with a strong reduction of the piezoelectric activity of the films [13], which is what we wish to achieve in the present films. As a general rule, the crystal quality of the films deposited on bare silicon was better than that of those grown on SiO_2 and the quality worsened as the amount of tilted grains increased.

The frequency response (S_{ij}) of SAW devices built on top of the AlN films gave a means of deriving the piezoelectric activity of the films. A simulation model specifically developed to obtain accurate values of the electromechanical coupling factor (k_{31}^2), was used. As expected, the values of k_{31}^2 ranged from 0.1% to 1%, depending on the amount of tilted grains present in the AlN films. The explanation for this behavior is that the multistep deposition method, based on switching the RF bias to the substrate on and off, promotes the growth of grains with opposite polarities and thus reduces the overall piezoelectric response of the films.

The measurement of the curvature of the wafer before and after the AlN deposition provided an estimation of the in-plane residual stress by using Stoney's equation. A residual stress of less than 250 MPa was determined for 2 μm-thick AlN layers deposited on a SiO_2 layer in a process consisting of ten 0.2 μm-thick layers with alternating substrate biasing. All in all, from a structural point of view, the deposited AlN films appears to be appropriate for the targeted application, since they exhibit a reasonably good crystal quality along with both low-stress and low piezoelectric activity.

3.2. Electrical properties

Current–voltage (*I–V*) measurements were performed on a Cascade probe station with an Agilent 4156C parameter analyzer, and capacitance–voltage (*C–V*) results are obtained with an HP4284A Precision LCR-meter operating up to 1 MHz. Measurements on coplanar waveguides (CPW) are performed on a calibrated Cascade Microtech station using an HP8510C Network Analyzer; the probe is a coplanar ground-signal-ground HF probe with a 100 μm pitch.

The electrical resistivity of AlN layers of various thicknesses has been extracted from the differential resistance, that is from the slope at each point of the *V–I* graph, of aluminum-AlN-silicon capacitors. The results are summarized in Fig. 1. Below a thickness of 100 nm, the resistivity is high but very thickness dependent. At 100 nm, values above ~10^{12} Ω cm are obtained after which the resistivity increases with film thickness, reaching about 10^{13} Ω cm for the 300 nm case. For comparison it can be noted that the DC resistivity of the deposited materials most used in IC-technology, like silicon nitride and oxide, is in the order of 10^{14} Ω cm

The dielectric constant of AlN has been extracted from *C–V* measurements: it falls in the range 9–11.5 for the examined AlN thicknesses.

The behavior of AlN at microwave frequencies has been studied by fabricating 1.4 μm-thick Al CPWs on surface-passivated

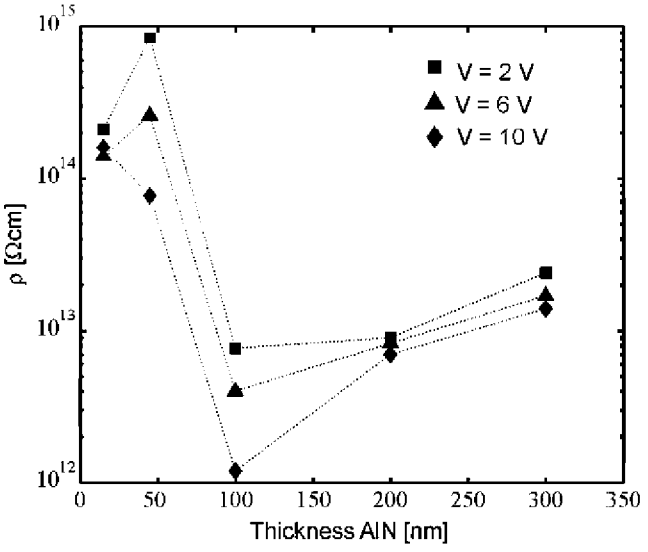

Fig. 1. Resistivity as a function of AlN thickness for different values of the voltage applied to the terminals of Al–AlN–Si capacitors.

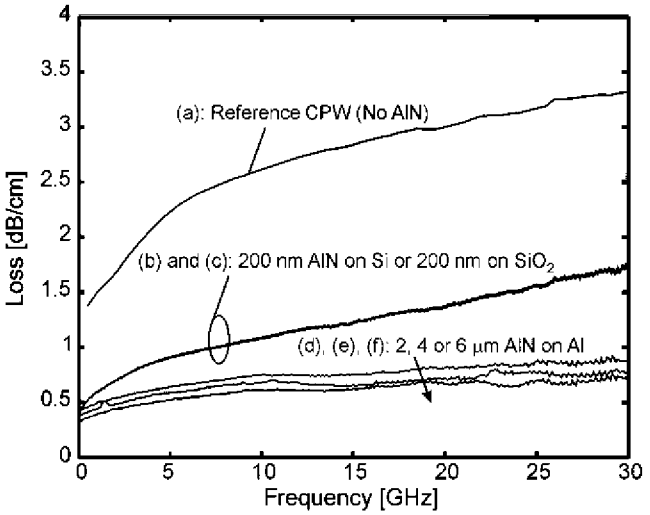

Fig. 2. Measured microwave losses for 5 different CPWs: (a) CPW on 330 nm SiO_2; (b) CPW on 200 nm AlN deposited directly on the silicon substrate; (c) CPW on 200 nm AlN deposited on 30 nm SiO_2; (d) 2 μm AlN, (e) 4 μm AlN, and (f) 6 μm AlN deposited on a CPW as in (a).

high-resistivity substrates (~4000 Ω cm) In Fig. 2 the measured losses up to 30 GHz are shown for five different samples: (a) is for a CPW fabricated on 330 nm silicon dioxide, (b) and (c) are for CPWs on a layer of AlN deposited directly on either the silicon substrate or on a thin 30 nm-thick layer of thermally grown SiO_2, respectively, and (d), (e), and (f) are for CPWs as (a) but with an AlN layer deposited on top of the Al of the CPW. The results show that the presence of AlN does not introduce additional losses at high frequency. This suggests that adding AlN layers when integrating active and passive devices on the same chip would not deteriorate the RF performances of the overall system.

3.3. Thermal properties

The lateral (in-plane) thermal conductivity of our AlN layers, as measured in on dedicated test structures, was determined to be about 12 $Wm^{-1} K^{-1}$. However, this value is lower than that suggested by measurements of the thermal resistance of bipolar junction transistors, as will be discussed in the next Section. It is plausible that the vertical thermal conductivity is significantly higher than the lateral one due to the columnar growth of the material during sputtering. An estimate of the overall thermal conductivity of the AlN films has been attempted by using thermal-only 3-D FEM simulations to reproduce the thermal resistance of silicon-on-glass devices with the same geometry as the transistors studied in the Section 4. A fitting within 10% between thermal resistances extracted by measurements and simulations has been obtained using a value of 50 $Wm^{-1} K^{-1}$ for the k_{TH} of AlN with thicknesses from 0.8 to 4 μm

4. AlN heatspreaders in silicon-on-glass bipolar transistors

PVD AlN is deposited directly on the first metal layer of NPN silicon-on-glass bipolar transistors in the manner described in [11]. The results reported in the following are for BJTs made in a silicon island of dimensions 12 × 25 × 0.94 μm^3. A cross-section of such a device is illustrated in Fig. 3.

When considering circuits of two or three bipolar transistors working in parallel, the emitter leads are shorted together and the base terminals are also connected. On the other hand, to allow monitoring of each individual collector current the collector leads

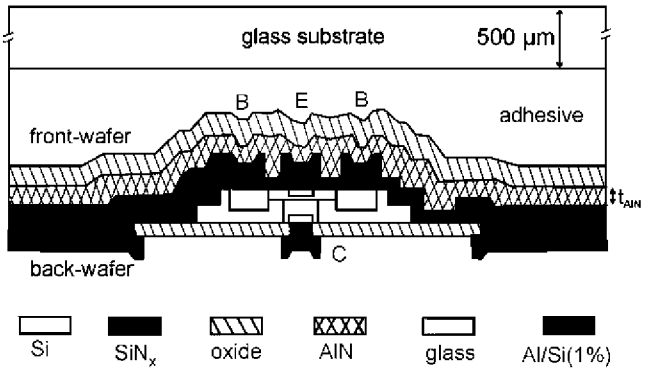

Fig. 3. Schematic cross-section of a silicon-on-glass bipolar junction transistor with an AlN layer deposited on the front-wafer.

are separated. Each transistor is insulated by the others by means of trenches filled with silicon nitride and oxide. In the simulations, the thermal coupling between the devices is also taken into account.

4.1. Single NPN bipolar junction transistor

Fig. 4 shows the collector current measured as a function of the base–emitter voltage for a single NPN BJT. The beneficial effect of the AlN layer for reducing the electrothermal feedback is increased as the layer thickness is increased. The values of thermal resistances are extracted by determining the point of onset of thermal instability, i.e., the starting point of negative differential resistance (also referred as flyback or snapback) and results are given in Table 1. The measurements have been compared with simulations based on analytical solutions of a system of non-linear algebraic equations that describe the BJT. This model accounts for all the relevant phenomena needed for an electrothermal analysis in a large range of currents The model parameters were adjusted by using the characteristics of the transistor measured in isothermal conditions at various temperatures. A 4 μm-thick AlN (device D in Table 1) produces a very significant reduction of the thermal resistance of more than 70%.

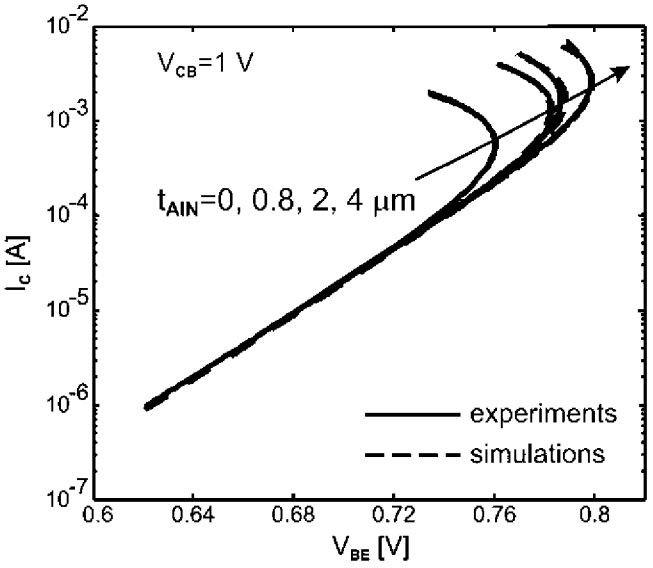

Fig. 4. Collector current as a function of the base–emitter voltage for an NPN covered with AlN layers of different thicknesses t_{AlN}.

Table 1
Thermal resistances extracted from BJT test structures, as in Fig. 3, with different thickness of AlN layer deposited on the front-wafer

Device	t_{AlN} (μm)	R_{TH} (K/W)	Benefit compared to device A (%)
A	0	19,000	/
B	0.8	9000	53
C	2	7300	62
D	4	5250	72

An even lower thermal resistance of devices can be obtained by also depositing AlN layers on the back of the silicon-on-glass devices after wafer transfer. This has been demonstrated for 0.8 μm layers in where also the benefit of adding thick copper heat sinks on top of this layer, but at a distance from the device, was illustrated. This latter experiment also confirmed the heatspreading nature of the AlN film.

4.2. Two NPN bipolar junction transistors

An important function of heatspreaders is to keep critical devices in a circuit at the same temperature. This function of the AlN has been investigated here by measuring two identical NPN BJTs where the emitters are 42.5 μm apart and are separated by otherwise thermally isolating materials. When such a pair is operated in parallel, it can suffer from electrothermal instabilities that lead to current hogging by the one transistor while the other switches off In Fig. 5a the measured collector currents are shown for an NPN pair with and without a 4 μm-thick AlN layer. Also in this case the experiments (solid lines) are compared with simulations (dashed lines) using values of 17,800 and 2200 K/W, respectively, for the self-heating resistance R_{TH} and the thermal coupling coefficient R_M (also referred as mutual thermal resistance) for the non-cooled pair, and 5000 and 1000 K/W for the pair cooled with 4 μm AlN. It can be noticed that, for the latter pair, the onset of thermal instability is shifted to a higher value of the dissipated power.

While the thermal resistance R_{TH}, as for the previous case of a single transistor, has been extracted from analytical calculations [19], the thermal coupling coefficient R_M is obtained by fitting the measurements (Fig. 5a, solid lines) with simulations (dashed lines).

The temperature increases above ambient as a function of the total collector current I_{CTOT} is illustrated in the simulations of Fig. 5b. It is clear that in presence of AlN heatspreaders (dashed lines) the two elementary transistors work at temperatures closer to each other and will be able to function in a larger current range. For example, the difference in the operating temperature of the two transistors, in absence of AlN layer (solid lines), is more than 130 K for I_{CTOT} = 5 mA, whereas it is only a few K for the same biasing condition when a 4 μm-thick AlN layer is added.

In the case of two BJTs working in parallel, it is known that an increased thermal coupling between the two devices improves the overall electrothermal behavior A figure of merit for such a circuit, from the electrothermal point of view, can be obtained with the inverse of the difference between the thermal resistance R_{TH} and the thermal coupling coefficient R_M. In fact, the onset of the thermal instability in a current controlled two-finger device, i.e. the onset of the current bifurcation, is described by the relationship

$$I_{C,crit} \propto \frac{1}{V_{CE}(R_{TH} - R_M)}, \quad (1)$$

where $I_{C,crit}$ is the collector current at which the thermal instability arises and V_{CE} is the collector–emitter voltage. The difference R_{TH}–R_M drops from 15,600, for the two-finger device without heatspreader, to 4000 K/W when a 4 μm-thick AlN layer is applied.

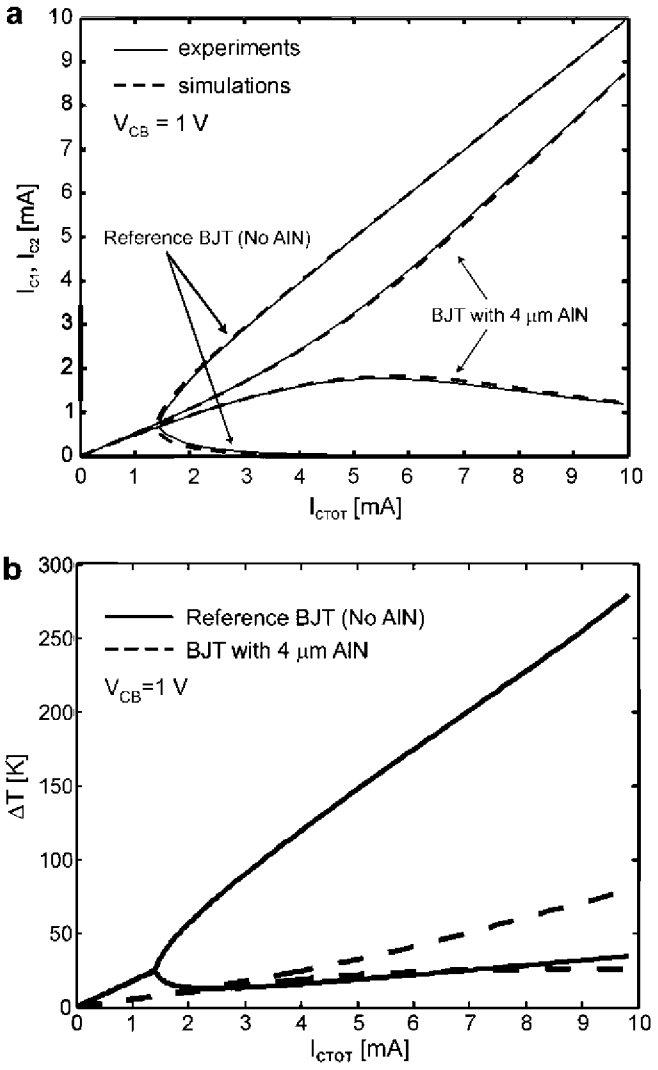

Fig. 5. (a) Measured (solid lines) and simulated (dashed lines) collector currents of the individual transistors of a pair operated in parallel as a function of the total collector current for the reference device and a device with a 4 μm-thick layer of AlN. (b) Simulated increase of temperature above ambient of the individual transistors of a pair, without (solid line) or with (dashed lines) a 4 μm-thick layer of AlN.

4.3. Three NPN bipolar junction transistors

In this sub-section, measurements are performed on three elementary transistors working in parallel. In other works theoretical studies of the electrothermal behavior of three BJTs in parallel have been carried out. For the three identical NPN BJTs, the emitters are 42.5 μm apart and are separated by trenches filled by thermally isolating materials.

The electrothermal feedback is very susceptible to all the small differences that are in practice always present in "identical" devices. For example, for the case considered here, an asymmetry of the three BJTs with respect to the position of the bondpads might be the main cause of differences in thermal resistance and, therefore, transistor #3 becomes hotter than the other two: it starts to take the total current while the other two switch off, as shown in the measurements of Fig. 6a (solid lines).

In Fig. 6 the comparison is made to a device with a 4 μm layer of AlN added. In this situation, the operating temperatures of the three devices become closer. The transistor #3 again bears the highest current, but, in the whole range examined in Fig. 6a, all the three devices still conduct a significant part of the total current. This will result in an increase of the reliability of the overall circuit. A figure

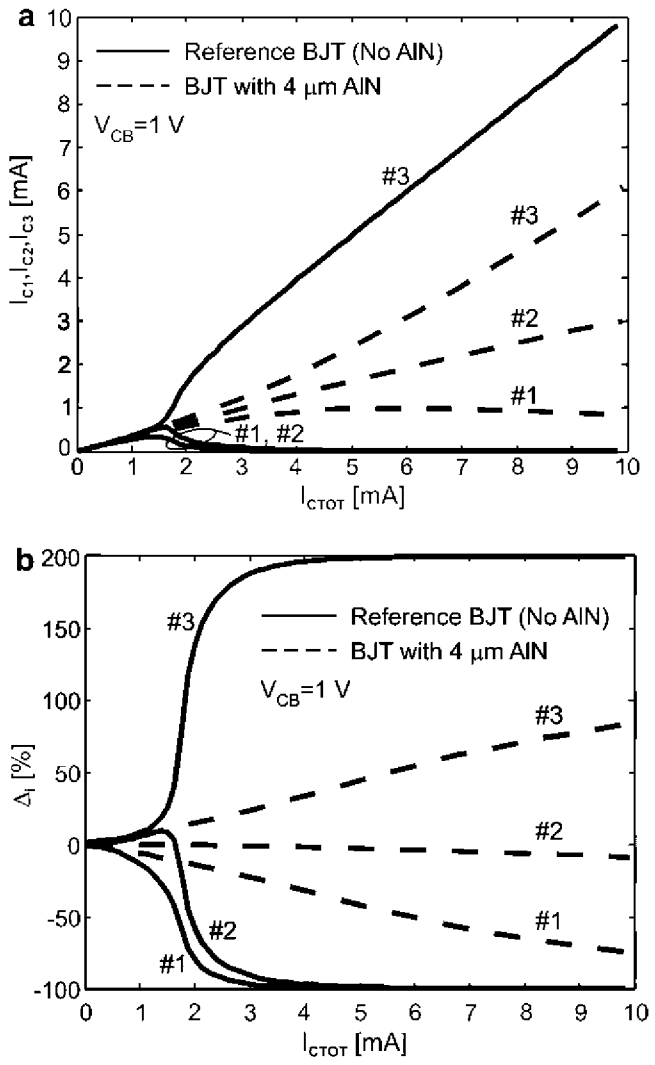

Fig. 6. (a) Measured collector currents of the individual transistors of a set of three operated in parallel as a function of the total collector current for the reference device (solid lines) and a device with a 4 μm-thick layer of AlN (dashed lines). (b) Discrepancy Δ_i of the individual collector currents with respect to the thermally ideal situation versus I_{CTOT}.

of merit for this case can be extracted from measurements considering the shift of the individual currents compared to an ideal case

$$\Delta_i = \frac{3I_{Ci} - I_{CTOT}}{I_{CTOT}} \times 100, \quad i = 1,2,3. \tag{2}$$

From Fig. 6b it becomes clear that, for example, while without using AlN Δ_i is above 50% for all the transistors even at I_{CTOT} = 2 mA, the shift Δ_i (with i = 1,2,3) is still within 50% up to I_{CTOT} = 6 mA.

5. Conclusions

The PVD AlN developed in this work was found to be very suitable for integration as heatspreader in RF IC processes both with respect to the electrical isolation properties (measured up to 30 GHz) and the electromechanical properties. Both mechanical stress and piezoelectric effects were effectively suppressed by alternating the growth conditions every 0.2 μm. In this way a suitable mixture of AlN grain sizes and orientation were achieved, which made it possible to reliably integrate layers up to 4 μm thick.

The thicker the AlN is, the more efficient the cooling of the devices. In silicon-on-glass NPN BJTs, a 4 μm-thick layer deposited before wafer transfer to glass gave a reduction of the thermal resistance of more than 70%, bringing it down to about 5000 K/W, which is a value typical of many of today's bipolar processes

Since the yield of the silicon-on-glass technology is much more sensitive to stress than more conventional processes, the present results indicate that a wider use of thick AlN heatspreading layers in RF IC's would certainly be feasible.

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