High temperature behaviour of GaN HEMT devices on Si(111) and sapphire substrates

R. Cuerdo , F. Calle , A. F. Braña , Y. Cordier , M. Azize , N. Baron , S. Chenot , and E. Muñoz

Instituto de Sistemas Optoelectrónicos y Microtecnología and Dpto. de Ingeniería Electrónica, E.T.S.I. Telecomunicación, Universidad Politécnica de Madrid, Ciudad Universitaria, 28040 Madrid, Spain
Centre de Recherche sur l'Hétéro-Epitaxie et ses Applications (CRHEA-CNRS), Rue Bernard Grégory, 06560 Valbonne, France
Picogiga International, Place Marcel Rebuffat, Parc de Villejust, 91971 Courtaboeuf, France

1 Introduction AlGaN/GaN high electron mobility transistors (HEMTs) have been used in power applications at X band and above for the last few years They take advantage of some interesting properties of III-nitrides, such as their high breakdown field and saturation velocity, good thermal conductivity, and intense piezoelectric fields, to provide high power at microwave frequencies and harsh environments. This includes high temperature (HT), either due to the environment or generated by the device operation. Different technological and design aspects, such as the substrate or the device geometry can influence the final transistor performance. This work focuses on the DC characterization of GaN/AlGaN/GaN HEMT devices, with different gate lengths, grown on sapphire and Si(111) substrates, at ambient temperature (T_a) from room temperature (RT) up to 350 °C.

2 Experimental AlGaN-GaN layers were grown by molecular beam epitaxy (MBE) on Si(111) and c-sapphire substrates. The active layers consist of an undoped GaN buffer of 1.7 μm on Si(111) substrates and of 0.5 μm on sapphire substrates, followed by 1 nm of AlN, an undoped 21 nm thick $Al_{0.29}Ga_{0.71}N$ barrier and a thin 5 nm GaN cap layer. The sheet carrier density (n_s) and Hall mobility (μ_H) were 8.9×10^{12} cm^{-2} and 1865 $cm^2/V\cdot s$ for samples on Si(111), and 10^{13} cm^{-2} and 2039 $cm^2/V\cdot s$ for samples on sapphire. Ti/Al/Ni/Au metallization was used for ohmic contacts and Ni/Au for gate contacts. Gate lengths (L_G) vary from 2 to 41 μm with constant drain-gate distances (L_{DG}) and gate-source distances (L_{GS}) of 3.5 μm. In addition, other devices with L_G = 2 μm have $L_{DG} = L_{GS}$= 1 μm. All HEMTs have a gate width of 150 μm. It is important to remark that transistors were not passivated.
All transistors had a single gate (G-TLMs), so that only DC measurements were performed. Drain current (I_D) and transconductance (g_m) characterizations were carried out each 50 °C from RT up to 350 °C and vice versa, in a specific designed HT station. Devices were encapsulated on TO-7 packages.

3 Results and discussion Both I_D and g_m parameters decrease as temperature increases for all the devices measured, as shown in Fig. 1 for a HEMT on Si(111) with L_G = 2 μm, mainly due to the reduction of mobility caused by polar optical phonon scattering This behaviour is reversible for every temperature in almost all devices under

study, so their initial performance is recovered after the thermal treatment. Nevertheless, different quantitative results are achieved depending on the substrate and the HEMT geometry (particularly, L_G).

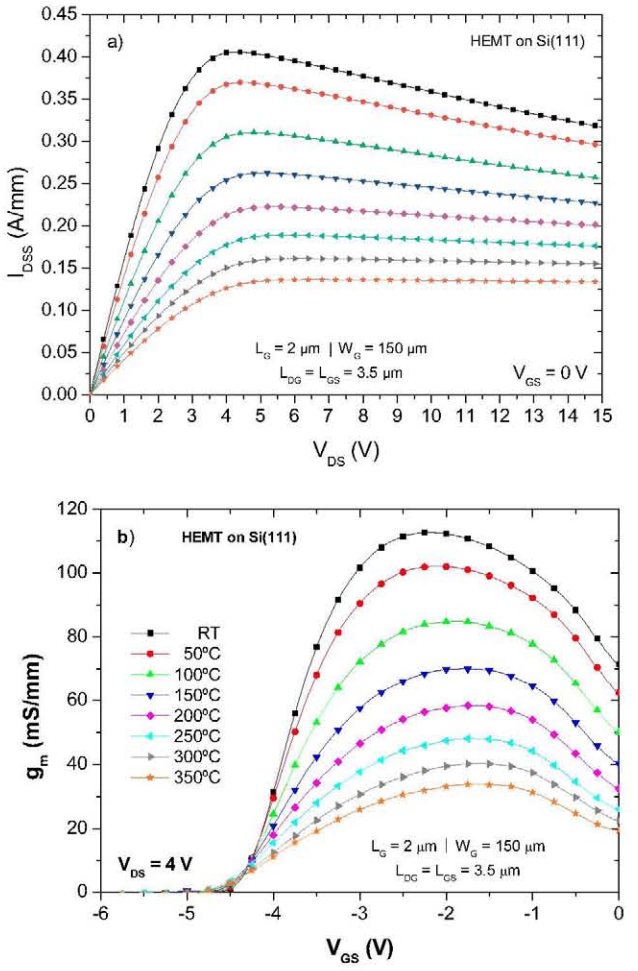

Figure 1 Evolution with temperature of the drain current at V_{GS} = 0 V (a) and transconductance at V_{DS} = 4 V (b), in a transistor on Si(111).

Regarding the substrate, it is well known that Si dissipates heat more easily than sapphire [4] due to its higher thermal conductivity (1.57 W/cm·K vs 0.35 W/cm·K). Thus, the self-heating effect in HEMTs on Si at RT is smaller than in HEMTs on sapphire, and I_D and g_m present higher values. In this study, transistors on sapphire have higher source and drain resistances (R_S and R_D) than Si ones, which can contribute additionally to their higher self-heating. Nevertheless, in order to obtain a direct and reliable comparison between HEMTs on both substrates (see Fig. 2), the effects of R_S and R_D have been removed from V_{DS}. The self-heating effect is reduced as T_a increases and becomes negligible above 300 ºC, where I_D curves can be considered flat in the saturation region. In addition, transistors on sapphire have the same or even a slightly higher I_D performance (since their higher n_s and μ_H) than Si ones at high temperatures; so, in absence of self-heating, this behaviour should be the same for all temperatures. Differences in the real performance between them, such as the 14% lower current of the HEMT on sapphire at RT, are mainly caused by the heat dissipation of the internal power generated.

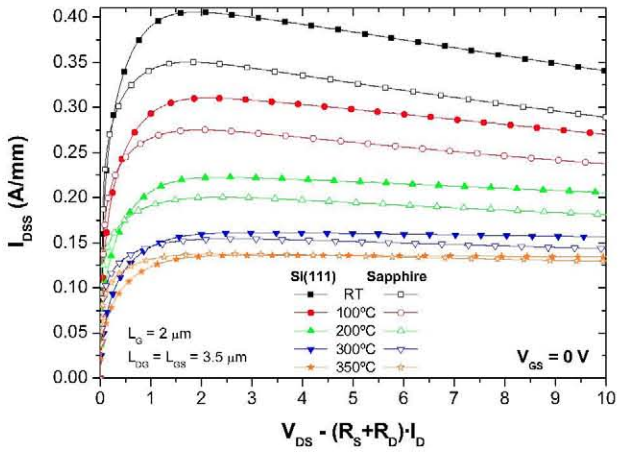

Figure 2 I_{DSS} as a function of the real voltage applied in the intrinsic transistor for HEMTs on Si and sapphire (the effect of R_S and R_D has been removed to obtain a more reliable comparison between HEMTs on both substrates).

Similar results can be clearly observed in Fig. 3 for any pair of devices with the same geometry and different substrates. At RT, HEMTs on Si show better DC performance than sapphire ones, specially for shorter L_G where the I_D and the self-heating are higher; but as temperature increases, I_D values converge.

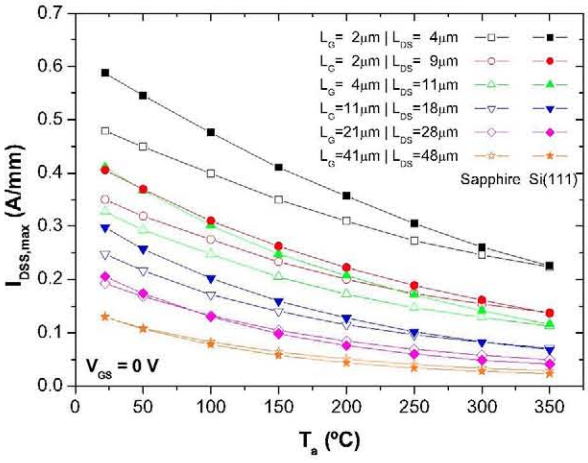

Figure 3 Maximum of I_{DSS} for HEMTs on Si(111) and sapphire with different geometries. All devices have L_{DG} = L_{GS} = 3.5 µm, except HEMTs with results shown by squares, for which L_{DG} = L_{GS} = 1 µm. Reduced distances between gate and ohmic contacts means lower R_S and R_D and higher electric fields on the gate, so their effect is like having a shorter L_G.

The thermal conductivity of the substrate has less importance as devices are heated since the power dissipated is lower and the difference between the channel temperature and T_a decreases. Thus, for HT applications above 300 ºC, it seems that the substrate is not relevant in the DC performance of the devices. On the other hand, the relative reduction of I_D and g_m values from RT up to 350 ºC is higher in HEMTs on Si (around 67% vs 61% for L_G = 2 μm and $L_{DG} = L_{GS}$ = 3.5 μm), issue that should be taken into account for the design of applications working at a wide temperature range.

The geometry of the transistors is another important factor for their HT performance. As L_G increases, the reduction of I_D and g_m is higher, and relative values approaches the drift mobility behaviour, as shown in Fig. 4 for devices on Si(111) and sapphire. For example, the reduction of I_D from RT to 350 ºC for transistors on Si(111) with L_G = 21 μm and 41 μm reach 80% and 82% respectively, close to the 84% reduction observed in the drift electron mobility extracted by TLM measurements. HEMTs on sapphire show a similar dependence than Si ones, but with a lower reduction (between 5-6%) in their DC parameters, close related with their higher self-heating at RT.

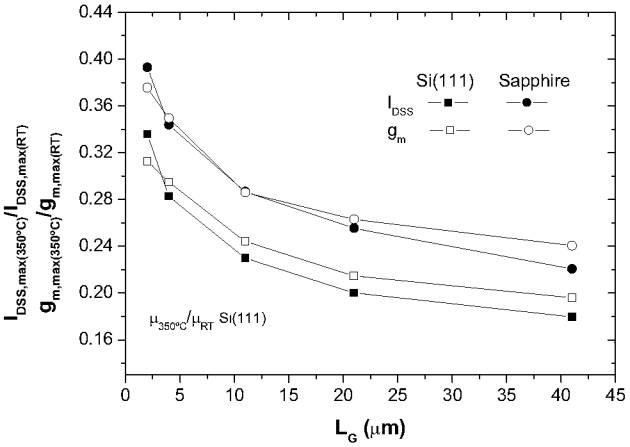

Figure 4 I_{DSS} and g_m at 350 ºC normalized by their values at RT as a function of L_G. For g_m, the V_{DS} chosen corresponds with the maximum of I_{DSS}, i.e V_{DS} = 4 V for HEMTs on Si and V_{DS} = 6 V for HEMTs on sapphire.

A tentative explanation for the dependency of DC parameters with L_G lies in the different magnitude of the effective electric fields in the intrinsic device. Longer L_G means lower fields under the gate for a constant V_{DS}, so devices work at the "low field regime" of drift velocity (v_d) vs electric field curves , where the temperature dependence of v_d is stronger. On the other hand, fields increase as L_G becomes shorter and v_d tends to the saturation region where it is less affected by the temperature. In fact, the relation v_d(350 ºC)/v_d(RT), extracted from Benbakhti et al. simulations is close to 0.35 for an electric field of 25 kV/cm, but for fields 20 times higher is only ~0.95.

Other way to evaluate the effect of the gate length is expressing the thermal evolution of the DC parameters as a power law (I_D, g_m α $T^{-\beta}$). For example, HEMTs on Si(111) with L_G = 41 μm and $L_{DG} = L_{GS}$ =3.5 μm, have a $I_{DSS,max}$ α $T^{-2.3}$, whereas for L_G = 2 μm $I_{DSS,max}$ α $T^{-1.37}$. Following this tendency, submicron gates should have even lower temperature dependence ($T^{-\beta}$, with β between 0.5-0.7), as reported by Tan

4 Conclusion HEMTs on Si(111) show a higher reduction of I_D and g_m with temperature (≈ 67% for L_G = 2 μm from RT up to 350ºC) than HEMTs on sapphire (≈ 61%), although they present better performance at RT due to heat dissipation. Thus, the effect of the substrate on the DC performance diminishes for high temperatures.

Regarding the geometry, compact devices with short L_G and L_{DS} distances are advantageous for HT operation: they reach high I_D and g_m values with a weaker thermal dependence than larger devices. This behaviour is probably related with the thermal evolution of the drift velocity for different electric fields, since as temperature increases v_d decreases in a higher rate for low fields. On this way, as L_G is increased, fields under the gate becomes weaker, and relative reduction of I_D and g_m from RT to 350 ºC approaches the drift mobility behaviour (reduction of 84%).

Acknowledgements Thanks to D. López Romero and M. Pérez de La Lama for their help in the bonding process of the devices. This work has been supported by the European KORRIGAN project (EUROPA MOU 04/102.052/032) and by the Spanish Comunidad de Madrid project (FUTURSEN, S-0505/AMB/0374).

References

U. K. Mishra, P. Parikh, and Y. F. Wu, Proc. IEEE **90**, 1022 (2002).

T. Palacios, A. Chakraborty, S. Rajan, C. Poblenz, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, IEEE Electron Device Lett. **26**, 781 (2005).

R. Cuerdo, J. Pedrós, A. Navarro, A. F. Braña, J. L. Pau, E. Muñoz, and F. Calle, J. Mater. Sci.: Mater. Electron. **18**, (2007) (online).

J. Kuzmík, P. Javorka, A. Alam, M. Marso, M. Heuken, and P. Kordos, IEEE Trans. Electron Dev. **49**, 1496 (2002).

A. M. Darwish, A. J. Bayba, and H. A. Hung, IEEE Trans. Microwave Theory Tech. **52**, 2611 (2004).

B. Benbakhti, M. Rousseau, A. Soltani, and J. C. De Jaeger, IEEE Trans. Electron Dev. **53**, 2237 (2006).

W. S. Tan, M. J. Uren, P. W. Fry, P. A. Houston, R. S. Balmer, and T. Martin, Solid-State Electron. **50**, 511 (2006).