Design of an Intelligent Front-End Signal Conditioning Circuit for IR Sensors

G. de Arcas, M. Ruiz, J. M. López, R. Gutierrez, V. Villamayor, L. Gómez, and Mª. T. Montojo

***Abstract*—This paper presents the design of an intelligent front-end signal conditioning system for IR sensors. The system has been developed as an interface between a PbSe IR sensor matrix and a TMS320C67x digital signal processor. The system architecture ensures its scalability so it can be used for sensors with different matrix sizes. It includes an integrator based signal conditioning circuit, a data acquisition converter block, and a FPGA based advanced control block that permits including high level image preprocessing routines such as faulty pixel detection and sensor calibration in the signal conditioning front-end. During the design phase virtual instrumentation technologies proved to be a very valuable tool for prototyping when choosing the best A/D converter type for the application. Development time was significantly reduced due to the use of this technology.**

***Index Terms*—Data acquisition, digital signal processors, FPGA, signal conditioning, virtual instrumentation.**

I. Introduction

THE use of PbSe infrared (IR) sensors for developing advanced IR vision systems requires designing high performance advanced signal conditioning front-ends due to the peculiar characteristics of this type of sensors. Although from a signal conditioning point of view they appear to be simple sensors, because they are resistive, their particular design and the poor tolerances that appear in their manufacturing process obliges to take into account additional considerations: their matrix-stile design, the high variability of the dark resistance between different elements of the same matrix, the need of high gains due to the large value of their resistance, and the need of scalable signal conditioning modules to easily adapt the design of the system for sensors with different matrix dimensions. Some of these problems and others that appear in the process are traditionally solved by the digital signal processor of the system once the sensor signals have been acquired.

This paper presents an alternative solution that consists of moving some of these functions to the signal conditioning front-end in order to reduce the CPU overload in the digital signal processor so its processing power can be used for the higher level application tasks. In order to do so, FPGA and microcontrollers are used to include processing capabilities (intelligence) in the signal conditioning front end. In particular this paper presents the design of a scalable signal conditioning and conversion module for IR sensors (CADVIR) that permits to connect PbSe sensors of different matrix dimensions to a digital signal processor to develop IR vision systems as shown in Fig. 1.

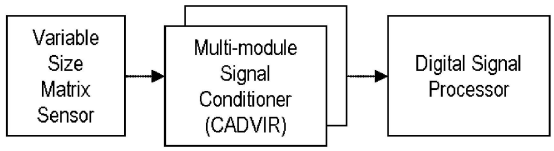

Fig. 1. Block diagram of the final architecture.

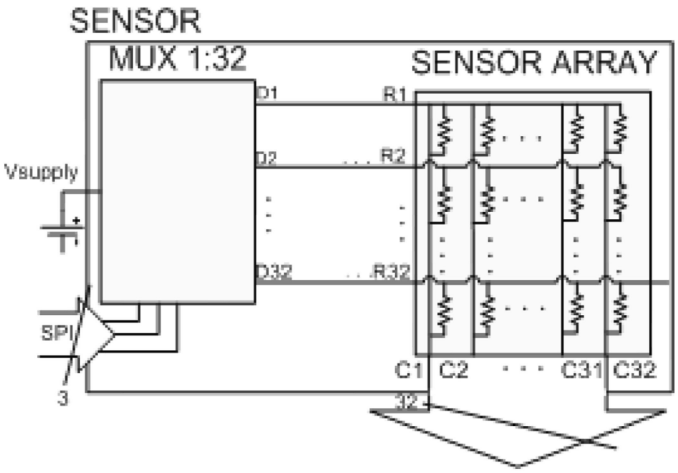

Fig. 2. Internal structure of a 32 × 32 matrix sensor.

The module has been designed to be used with PbSe sensors manufactured by the Centro de Investigación y Desarrollo de la Armada (CIDA), *Research and Development Centre of the Spanish Army* [1]–[3]. The signal conditioning block conditions and converts the signal coming from the sensor into a digital format and transfers it to the digital signal processor. This block can be made of one or several CADVIR modules depending on the dimensions of the sensor matrix.

II. Sensor Characteristics

Fig. 2 shows the internal structure of a 32 × 32 matrix sensor, which is based on a matrix of PbSe photoconductive detectors. The nominal value of the dark resistance of each detector is around 2 MΩ. One of the problems of the sensor is that due to the manufacturing process this value has a poor tolerance. So the actual dark resistance value of the detectors of a matrix sensor can range from 500 kΩ to 5 MΩ.

When infrared radiation reaches a detector, its resistance varies proportionally. The typical signal range observed in

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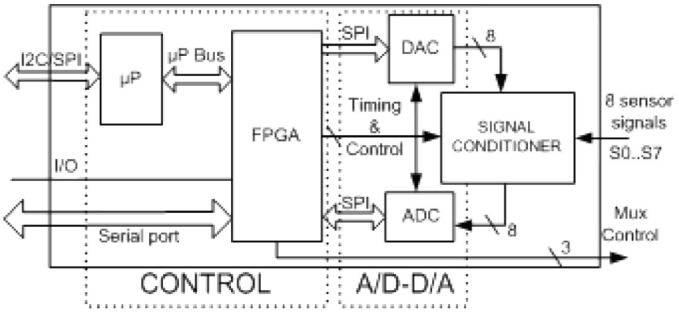

Fig. 3. Block diagram of a CADVIR module.

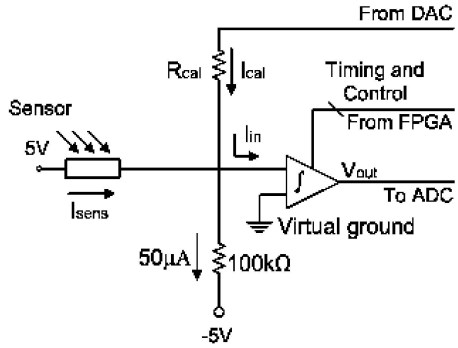

Fig. 4. Simplified schematic of a single channel of the signal conditioner.

these sensors is very small, around 1000 ppm. These two characteristics are the main key points to have in mind during the design of the signal conditioning circuits.

As it can be seen in Fig. 2 one set of terminals (R1 to R32) connects the detectors in each row to form row input of the sensor array. Other terminals connect the detectors belonging to the same column (C1 to C32). The column terminals form the output of the sensor, while the row terminals are connected to an analog multiplexer that is used during signal conditioning to polarize the matrix detectors. This multiplexer is included during manufacturing to facilitate addressing the sensor detectors by rows. The row of detectors to be processed is selected through the serial interface (SPI) of the multiplexer, which connects the supply voltage at the input of the multiplexer to the selected row of detectors. If the signal conditioning circuit to be used has a virtual ground at the input, then a current will flow through each sensor output, whose value will be proportional to the resistance of the selected detector in each column. These are the signals that the CADVIR module has to convert into a digital value corresponding to each pixel of each column.

This scheme permits simultaneous conversion of the pixel values in one row if a simultaneous multi-channel sampling converter is used that has the same number of inputs as the sensor columns.

III. CADVIR Architecture and Description

The CADVIR module has eight inputs, so it can process the current signals coming from eight detectors simultaneously. If the sensor has more than eight columns, several CADVIR modules can be used in parallel to adapt to the desired dimensions as is explained in chapter III.D. For example four modules would be necessary to process the signals from a 32×32 matrix sensor.

Fig. 3 shows the block diagram of a single CADVIR module. It is consists of the following blocks:

1) *Signal conditioner:* converts the small current signals coming from the eight detectors connected to the module's input into a voltage, and adapts them to the analog to digital converter (ADC) dynamic range.
2) *A/D-D/A:* converts the voltage output signals from the signal conditioning block into digital form, and generates the calibration voltages for each detector.
3) *Control:* generates the timing and control signals for the other blocks and pre-processes the data samples before sending them to the digital signal processor.

A. Signal Conditioner Block

This block has eight identical channels connected in parallel. Each of them converts the small current signal coming from a sensor detector ($\mathrm{I_{sens}}$) into a voltage ($\mathrm{V_{out}}$), and amplifies it to adapt it to the dynamic range of the ADC that will be use to digitize it. In order to do this, it uses the output voltage of a digital to analog converter as it is explained below.

The structure of one of these channels is shown in Fig. 4. The current coming from any sensor detector has two components: a constant one, called the dark current, which is caused by the dark resistance of the detector; and, a variable one, the signal current, which is proportional to the received radiation. As the dark current is much higher than the signal current, the signal conditioner must remove the dark current before amplification in order to avoid saturation of the amplifier.

Taking advantage of the virtual ground that appears at the input of the integrating amplifier a constant current is removed from the detector current by connecting a 100 kΩ resistance between the amplifier input and a -5 V reference voltage. This produces a constant 50 μA that would remove the dark current for detectors having a 100 kΩ dark resistance.

This is not enough to remove the effect of the dark resistance of any detector, because as it was mentioned before the dark resistance value can range up to 5 MΩ due to its poor tolerance. Therefore another current is added to the input of the amplifier, whose value can be controlled digitally. In order to do so, a resistance ($\mathrm{R_{cal}}$) is connected between the amplifier input and the output of a digital to analog converter from the A/D-D/A block. With this last modification, depending on the value written in the DAC, the circuit can remove the undesired effect for detectors with dark resistance values from 100 kΩ up to infinity.

Taking into account the virtual ground that appears at the input of the amplifier the input amplifier node equation can be written as follows:

$$I_{in} = I_{\mathrm{sens}} + I_{\mathrm{cal}} - I_{\mathrm{cte}}. \tag{1}$$

A precision switched integrator based on a transimpedance amplifier was chosen to amplify this current due to the extremely high gain value needed in the application. The low pass effect of this type of amplifiers was also considered an advantage for the application as it helps to lower the effect of the sensor noise. In particular, this is the case for Texas Instrument's IVC102 amplifier, which was used in this design. Its gain is obtained from

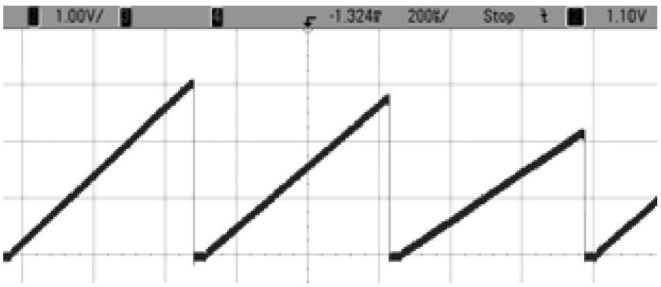

Fig. 5. Measured waveform at the integrator output.

(2), that show the relation between the output voltage (V_{out}), the input current (I_{in}) and the two integrator parameters: the integrating period (T_{int}) and the capacitance (C_{int}). For this application a value of 10 picofarads was chosen for C_{int}, and T_{int} was left as an adjustable parameter in the system that can be changed from the control block. This value can be set between 100 μs and 2 ms, obtaining gains from 10 to 200 millions V/A.

$$V_{out} = -\frac{I_{in} T_{int}}{C_{int}}. \quad (2)$$

The use of this type of amplifiers has some disadvantages. First an integrating period (T_{int}) is needed to amplify the input signal, whose value is proportional to the desired gain value. This has two effects: it introduces a delay in the signal acquisition process, and requires synchronizing the analog to digital converter with the amplifier in order to convert every input sample using the same gain value. On top of that a reset period must be included between samples to reset the integrator capacitor in order to avoid a cumulative offset error. The reset period was chosen to be 10 μs.

Fig. 5 shows the voltage waveform measured with an oscilloscope at the output of one of the integrators of a CADVIR module while it was being used to digitalize an image obtained with a 32 × 32 matrix sensor. The slope of each ramp is proportional to the value of one of the pixels of the sensor. Only the signal of the detectors from the first 3 rows is displayed. The 10 μs reset period at the beginning of each pixel interval can be seen. The final voltage value reached at the end of each integrating interval is proportional to the input radiation; the voltage has been compensated by a variable current (I_{cal}) and a constant current (I_{ctc}) and thus not proportional. Therefore this is the value that will have to be converted with the ADC to obtain the digital pixel value.

B. A/D – D/A Block

The poor tolerance value of the dark resistance of the sensor detectors, together with its low sensitivity, forces the use of a high resolution analog to digital converter, in order to be able to detect small signal variations in a wide dynamic range. Therefore the first idea was to use a Delta-Sigma converter.

The design of the signal conditioner imposed a second constraint when choosing the ADC type: it had to be possible to synchronize the analog to digital converter with the amplifier. This seemed to be against the use of the Delta-Sigma converter due to the uncertainty about the exact moment of the start of conversion in this type of ADC, [4] and suggested to use a sampling ADC such as a classic successive approximation register (SAR) ADC.

From the point of view of the design time it was not possible to validate the best option by developing a prototype for each converter type. Even the use of an evaluation module had to be discarded due to the long delivery times of the distributors. Therefore the use of data acquisition boards that would have the same type of converters was seen as the best option in order to be able to make real measurements in a short period of time.

The boards chosen were the NI-PXI 6122 and NI-PXI 4472 from National Instruments. The first one has a 16 bits SAR type A/D converter, while the second one has a 24 bits Delta-Sigma converter. In order to improve even more the development time of the test system LabVIEW was chosen as the development tool to write the program to automate the measurement and analysis process.

Fig. 6 shows the code of the program. In order to synchronize the acquisition of both boards the program configures both boards to use the same clock and trigger signals, in particular those of the NI-PXI 4472 board. The appropriate signal connections were made between both boards, and their inputs were connected to the output of one of the signal conditioner channels.

The availability of the boards and the use of LabVIEW as the software development tool permitted to setup a test system to evaluate the best type of converter for the application in an extremely short period of time, around two days. In addition to this the test system permitted to easily analyze the acquired data in a personal computer using LabVIEW.

Measurement results showed that the waveform acquired with the Delta-Sigma converter were always delayed with respect to that of the SAR converter due to the delay introduced by the digital filter of the former [4]. In order to be able to compare both waveforms the program included an alignment algorithm. As it can be seen in the lower part of Fig. 6 the cross correlation of both signals was used to estimate the delay between them, and then the NI-PXI 6621 waveform was delayed accordingly.

Fig. 7 shows the measured waveforms obtained at the output of one of the integrators of a CADVIR module while it was being used to digitalize an image obtained with a 32 × 32 matrix sensor.

The measurement results showed another problem of the use of the Delta-Sigma converter in this application: the appearance of a ripple signal at the beginning and the end of each ramp due to the effect of the high frequency components of the transitions in the digital filter of the converter. This along with the uncertainty about the start of conversion instant discarded the use of Delta-Sigma converters for this application. Also, it was considered that 24 bit resolution was not essential for the application.

The maximum resolution found in commercially available sampling ADC was 16 bits, that was considered to be enough. The other requisites that were taken into account in order to choose the A/D converter were: the need to have eight simultaneous sampling input channels; and, the interest of having a serial control interface in order to simplify its interconnection with the rest of the modules, and to simplify and reduce the PCB layout. Following these criteria Analog Devices AD7656 was chosen. It's a SAR type ADC with 16 bits resolution, 6 simultaneous sampling input channels per chip, a maximum sampling frequency

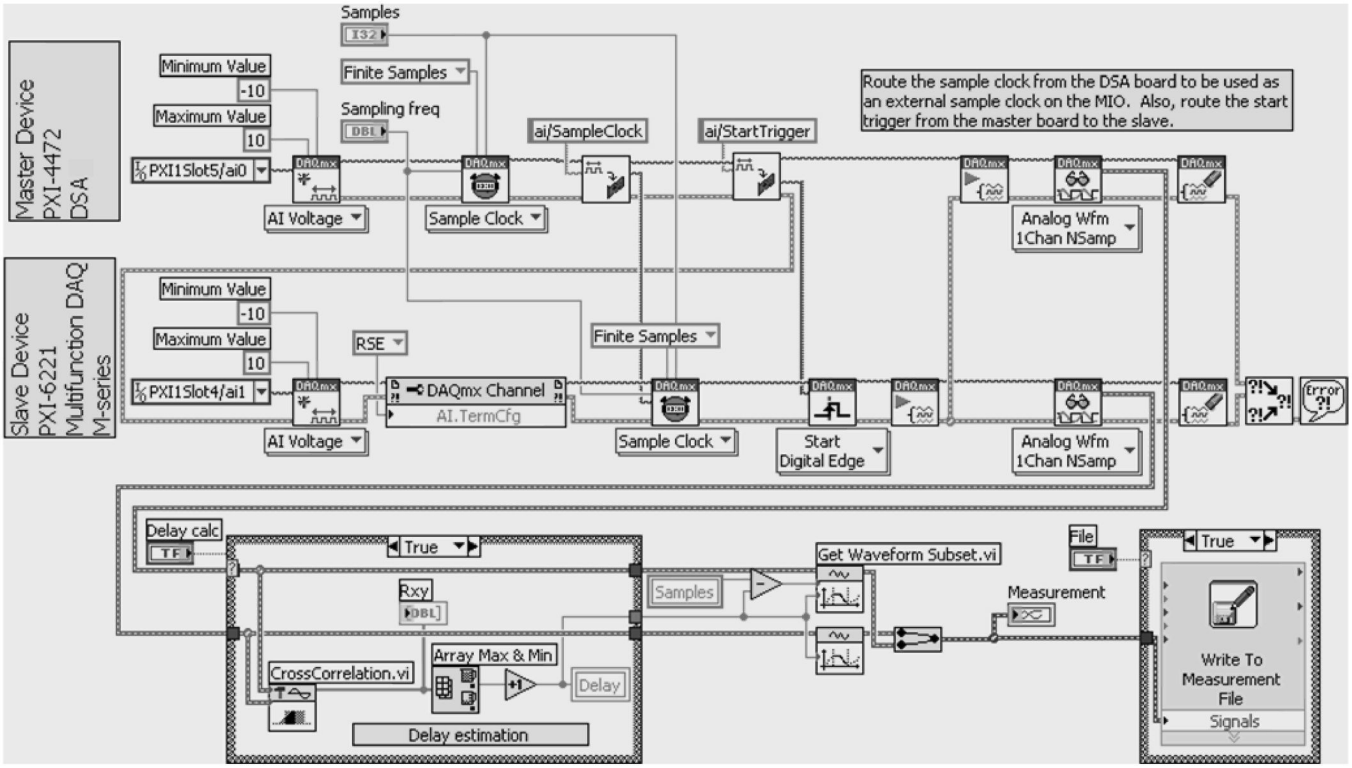

Fig. 6. LabVIEW program used to automate simultaneous measurement and data analysis with two data acquisition boards.

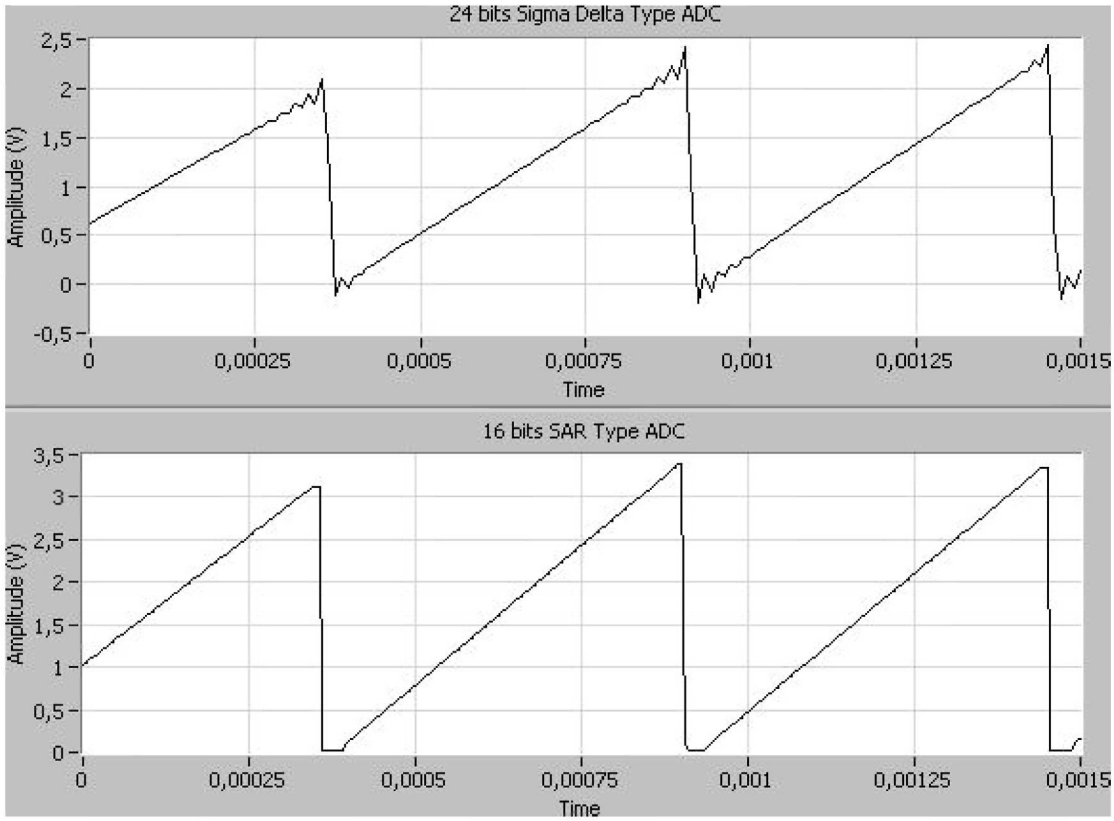

Fig. 7. Integrator output signal waveform acquired with a 24 bits delta-sigma ADC based data acquisition board (top) and with a SAR ADC based board (bottom).

of 250 kHz and an SPI serial interface. Although the number of input channels was not enough, this was not a problem as several converters can be connected in cascade to increase the number of channels. Therefore each CADVIR module has two ICs like this.

Choosing the digital to analog converter was much easier, as there were only two requisites to be observed. First the resolution had to be enough to be able to remove the dark current of any sensor during the calibration phase. Second, it had to be possible to update and stabilize the output of eight channels during the reset period of the integrator, which is less than 10 μs. Texas Instruments TLV5630 converter was chosen as it has eight simultaneous output channels, with 12 bits resolution and an update and settling time of 7 μs for the eight channels.

C. Control Block

This block deals with three main functions: it generates timing and control signals for the rest of the CADVIR blocks (signal conditioner, ADC and DAC); manages the calibration process to find the DAC value needed to compensate the dark current for each detector; and, in case that the CADVIR module is connected to a digital signal processor and to the other modules it is responsible for interfacing.

The block consists of a field programmable gate array (FPGA) and a microcontroller. The FPGA is a EP1C6T144CSN from Altera's Cyclone FPGA family, that has 6000 LE's, 92 Kbytes RAM memory and 185 I/O pins. The microcontroller is a C8051F340 from Silicon Laboratories. It is an 8 bits microcontroller that can handle up to 25 MIPS.

Communication between the FPGA and the microcontroller is done through the external memory interface (EMIF) of the microcontroller. This is connected to one port of a double port memory that is implemented inside the FPGA. The other port is connected to the hardware implemented in the FPGA. This design scheme provides the CADVIR module with two operation modes: stand-alone, and master-slave.

The master-slave mode provides the highest performance. It is intended for applications where the CADVIR module is connected to a digital signal processor. In this operation mode the CADVIR module deals with the signal conditioning, acquisition and pre-processing of the image information, consuming the least possible resources and CPU load of the DSP so it can be fully devoted to the higher level application processing. This mode supports the connection of several CADVIR modules in parallel to adapt the system to sensors with different matrix dimensions. For example, four CADVIR modules would have to be used for a 32×32 matrix sensor.

In this mode the I2C and SPI ports of the microcontroller, and the two UART that it includes are used for high level communication and interfacing tasks with other CADVIR modules and with the DSP. But the heart of the system is the hardware programmed in the FPGA. It is responsible for three tasks: CADVIR subsystems control, communication and high level operations.

The first task that the FPGA deals with consists of generating the timing and control signals needed for the operation of the integrator amplifier, the ADCs and the DACs. The communication task is responsible for transmitting the acquired data stream to the DSP through a high speed serial interface compatible with a multichannel buffered serial port (McBSP).

In addition to this communication, timing and control functions the FPGA performs the following high level operations

1) Faulty Pixel Detection: detectors in a matrix sensor can suffer from faulty behaviour, such as short-circuits. This is an especially problematic case, as a short-circuit in one detector will interfere with the behaviour of the rest of the detectors in the same row. A sensor detector is considered faulty if its dark resistance is less than 100 kΩ. Detection is done by injecting the minimum possible current with the D/A converters and checking if any detectors in the same row produce a negative voltage at the A/D converter inputs. The process is repeated for all sensor rows, thus checking all detectors in the sensor matrix. The faulty detectors positions are saved in an internal memory in the FPGA. When the module goes into measurement mode and is going to address a faulty detector of the sensor matrix, the input of the corresponding integrator amplifier is open-circuit. This forces a constant current to flow through the detector, thus avoiding interference with other detectors of the same row.

2) Sensor Calibration: it is the process of determining the value that has to be written in each DAC to remove the dark resistance effect of every detector. The goal is to obtain the smallest voltage, ideally zero, at the integrator output for every sensor detector when there is no radiation applied to it. Although it seems a simple task, from a practical point of view it presents the following problems:

- —*Amplifier saturation.* If a transimpedance amplifier goes into saturation its input virtual ground no longer exists. This produces a mix between the currents of the same row detectors as they flow through adjacent detectors, making it impossible to measure any detector in that row. The calibration algorithm must take this situation into account in order to avoid oscillatory states.
- —*Calibration interval.* This is a critical parameter of the system. It has to be noted that each time a value is written to the DAC to try to remove the dark current of the detector an ADC conversion must be done. Each conversion has to be preceded by an integration period, which means it will take at least 100 μs. Therefore to test all the possible codes of a 12 bits DAC it will take nearly 30 seconds. A successive approximation algorithm cannot be used because of the amplifier saturation and nonlinearity problems. To solve this problems an array of comparators is included in the FPGA. While the output voltage of the amplifier is saturated the calibration current is varied in steps corresponding to the ADC's dynamic range. Once it comes into range the comparators reach the correct value in a single cycle. Simulation results of this algorithm point to a 10 ms calibration period for the worst case.

When the CADVIR module is used in stand-alone mode it behaves as an independent unit for signal conditioning, acquisition and processing for IR sensors with eight input channels. In this mode all data processing capabilities that must be included in the application are performed in the CADVIR microcontroller, limiting the overall system performance to that of the microcontroller.

In this operation mode the FPGA implements the same timing, control and high level tasks as described above. The communication task is not implemented as there is no need to interface with any external subsystem.

The microcontroller obtains the acquired data stream from the FPGA and runs the data processing algorithms needed for the final application.

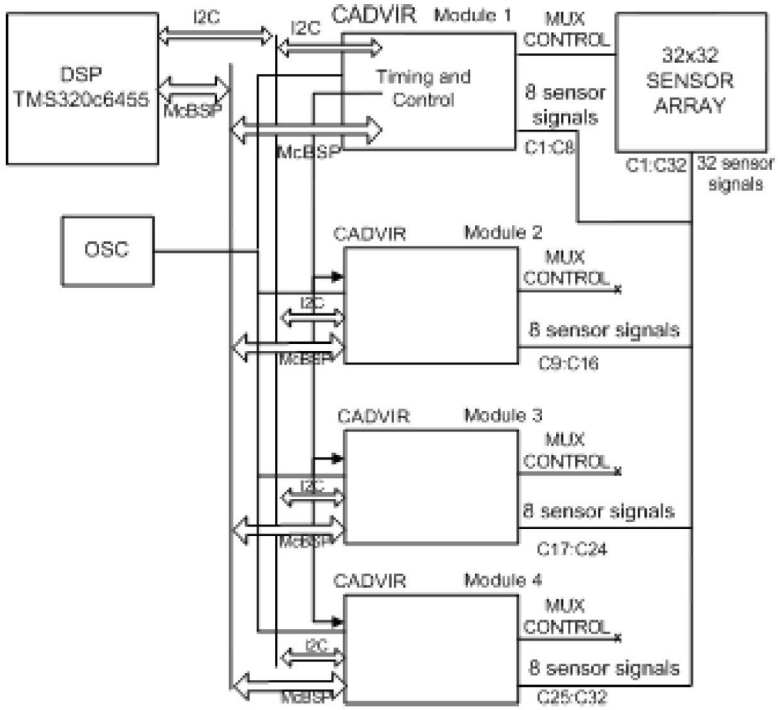

Fig. 8. Interconnection scheme of several CADVIR modules.

D. Multi-Module Interconnection

The current work is focused on the interconnection of several CADVIR modules. The most important issue to be considered when connecting several CADVIR modules together is synchronization. In order to guarantee that the same gain value is used in every signal conditioner module to condition the signal of all detectors, all modules must use the same integration periods. This is achieved by forcing the FPGA of the first CADVIR module to generate the timing signals for all modules as it can be seen in Fig. 8.

All modules will share the same McBSP bus to transmit their data stream to the DSP. The first module will generate the control signals needed to share the bus following a scheduling algorithm based on tokens.

An I2C interface has been included in the CADVIR module so it can be used to transmit higher level, lower priority, information between the DSP and the CADVIR module microprocessors without affecting data stream transfers.

IV. Results

As a result an intelligent front-end signal conditioning circuit for IR sensors has been developed as it can be seen in Fig. 9. The module can be used alone, or it can be connected to a digital signal processor and to the other modules to develop high performance vision systems for different matrix dimensions.

In stand alone mode it is an independent unit for signal conditioning, acquisition and processing for IR sensors with eight input channels.

In master-slave mode it is used to acquire and transmit and image from a sensor matrix to an external digital signal processor consuming the least possible amount of resources and CPU load of the DSP. CADVIR modules include signal conditioning, acquisition and data preprocessing in a signal conditioning scalable front-end. This means that when they are used

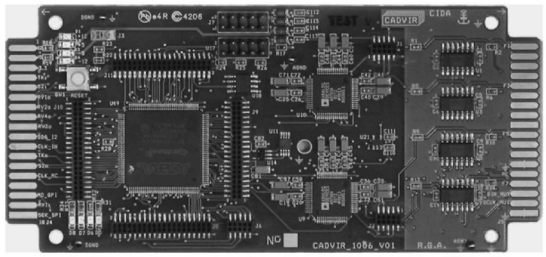

Figura 1

Fig. 9. Top view of the final CADVIR module.

in applications where there is a need for a system processor, the later does not have to take care of image acquisition problems, thus increasing its available processing capabilities for the final application.

For example, in one application four CADVIR modules are connected in parallel to acquire an image from a 32×32 matrix sensor in 4 ms, thus providing an image acquisition speed up to 250 frames per second. This requires a data transmission bandwidth to the DSP of approximately 4 Mbps, which is only a 0,3% of its CPU load when the transmission is controlled with the EDMA interface. Therefore almost all the processing capability of the DSP is available for the system's final application.

Due to its versatile architecture the module can also be used as a hardware platform in any other signal acquisition applications where there is a need to free the main system processor from data preprocessing tasks. The analog input capabilities include eight input channels, that can be configured as current input, with a programmable gain between 10 to 200 millions V/A, or as bipolar voltage input with a dynamic range between -10 V to $+10$ V and 16 bits resolution. It also has eight independent output voltage channels with 12 bits resolution.

From the point of view of its processing capabilities it includes a 25 MIPS 16 bits microcontroller, with I2C, SPI and UART interfaces and a FPGA that can support a maximum clock frequency up to 125 MHz with 6000 LE's, 92 Kbytes RAM memory and 185 I/O pins. After programming the full functionalities mentioned above in the FPGA, 70% of its resources and 50 I/O pins remain at disposal to be tailored for the final application.

Finally it must be mentioned that the use of virtual instrumentation technologies has proved to be a very valuable tool for prototyping during the design phase of this project in order to choose the best A/D converter type for the application. Development time was significantly reduced due to the use of this technology.

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