$1/f$ Electrical Noise in Planar Resistors: The Joint Effect of a Backgating Noise and an Instrumental Disturbance

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Abstract—**Any planar resistor (channel) close to a conducting layer left floating (gate) forms a capacitor C whose thermal voltage noise (kT/C noise) has a backgating effect on the sheet resistance of the channel that is a powerful source of $1/f$ resistance noise in planar resistors and, hence, in planar devices. This $1/f$ spectrum is created by the bias voltage V_{DS} applied to the resistor, which is a disturbance that takes it out of thermal equilibrium and changes the resistance noise that existed in the unbiased device. This theory, which gives the first electrical explanation for $1/f$ electrical noise, not only gives a theoretical basis for the Hooge's formula but also allows the design of proper shields to reduce $1/f$ noise.**

Index Terms—**Backgating effect, distributed bias, excess noise, kT/C noise, noise measurement, parasitic FET, RC cell, $1/f$ electrical noise.**

I. INTRODUCTION

THE HIGH GAIN of GaAs photoconductors at low illumination levels was explained recently by a new gain mechanism [1], [2] based on the variation of conductive volume that occurs in epitaxial layers due to transversal photovoltages developed at boundary space charge regions (BSCRs) cladding them. Thus, this gain is a photo-backgating effect in conductors coming from their BSCRs, and to evaluate the signal-to-noise ratio of this gain, the corresponding noise mechanism must be known. For GaAs thin films, two BSCRs contributed to the aforementioned gain: one in the bottom interface between the GaAs film and the substrate and the second one in the surface BSCR on top [2], thus giving both photo-backgating and photo-topgating contributions to such gain.

For this photo-topgating gain, a $1/f$ noise predicted some time ago [3] has been shown recently in GaAs photoconductors [4] by optically induced fluctuations of their surface BSCR. These fluctuations, which are randomly created in a small region of the sample surface, diffuse over the surface until they reach the ends of the sample. This produces a set of random modulations in the channel, each having a $1/f$ spectrum that

gives a $1/f$ resistance noise in the channel. This field-effect modulation shown in [4] creates a $1/f$ resistance noise in the bulk reflecting a surface effect without contradicting the title of a well-known paper by Hooge [5]. Although the small surface charge disturbances used in [4] are much higher than the thermal ones on average, they unambiguously show that their field-effect action on the underlying channel is a $1/f$ resistance noise due to the surface BSCR. A direct application of this result for GaAs devices is that any ionizing radiation creating a burst of carriers near their surface will produce the same kind of $1/f$ resistance noise shown in [4]. From time to time, cosmic radiation or particles, which are very difficult to be shielded, can produce such bursts within the device whose low-frequency noise is being measured, which are added to the random thermal BSCR charge disturbances.

Although the aforementioned effect from the surface SCR or double layer of many planar detectors would be a reason to find (measure) some $1/f$ resistance noise in such devices, a more powerful source of $1/f$ resistance noise appears when one considers the bottom interface between the thin film and the substrate, as we announced in [4]. In this case, there is an interaction of the BSCR with the external voltage applied to the sample, which leads to a $1/f$ noise synthesized by a set of Lorentzian terms detuned and weighted in the required way to generate this $1/f$ spectrum. It is worth noting that this synthesized $1/f$ noise is ingenuously created by the researcher himself, and the way this happens (a nice example of disturbance due to the measurement action) is the subject of this paper.

II. THEORETICAL BACKGROUND ON RESISTANCE NOISE

To simplify reasoning, let us consider a thin-film channel of n-GaAs clad by two p^+-GaAs layers, the first one being a p^+-GaAs substrate, for example, and the second a p^+-GaAs layer grown on the n-channel as the gate of a junction field-effect transistor (JFET). The use of GaAs comes from our wider experience on this material system, but the present theory also applies to other material systems. Now, let us consider that we have fabricated a true GaAs JFET by making two ohmic contacts at both ends of the n-GaAs channel. Although the p^+-GaAs substrate is a true gate for the n-GaAs channel, we will oversee this detail as it is done in the literature. A clear example of a floating-gate JFET inadvertently used in electrical noise characterization can be seen in [6], but the aforementioned oblivion is particularly frequent with semi-insulating

(SI) GaAs substrates, in spite of their true gate action on the conducting channels they have on top [2], [7]. Therefore, we will use the aforementioned n-GaAs channel as a thin-film resistor (TFR) with the top gate and the bottom p$^+$-GaAs substrate gate both left floating (thus, not connected to the TFR).

This "floating-gate planar resistor" is irritating for people who have handled FETs properly, due to the high impedance of its floating-gate circuit, which is prone to pick up several kinds of noise without a proper shielding. However, let us do this action because even the most experienced people handle inadvertently these floating-gate FET devices, e.g., each time they use a thin-film device grown or placed onto an insulating substrate to have some rigidity in the sample. This is so because a BSCR or double layer at the thin-film/substrate heterojunction is unavoidable to equalize Fermi levels and because the underlying substrate is never a perfect insulator. With the aforementioned two gates left floating, our TFR has two equal cladding BSCRs. From a device viewpoint, it is a JFET with two floating gates, and it is the common plate of two p$^+$-n junction capacitors.

As is well known, a capacitor of capacitance C under open-circuit conditions has a thermal voltage fluctuation $v_n(t)$ known as its kT/C noise [8], whose squared mean value at a temperature T is $\langle v_n^2(t)\rangle = kT/C$ (V^2), with k being the Boltzmann constant. This noise means a root mean squared voltage $v_{\rm rms} = 64$ μV in $C = 1$ pF, which is a true problem in a fast sample-and-hold circuit holding a dc voltage sample of 20 μV in such a small capacitor. Although this 20-μV dc voltage is actually stored as the mean voltage of such a capacitor, the voltage read after the sampling action will be any value around 20 μV with a variance of 64 μV. This kT/C noise will also exist in the two cladding capacitors of our TFR under an open-circuit condition, thus leading to a very interesting situation coming from the fact that each cladding capacitor is not made of fixed metallic plates but of (settled in) a BSCR whose width will vary tracking the voltage fluctuations of its own kT/C noise. Thus, our TFR will not have a strictly constant resistance but a mean value $R_{\rm ch}$, together with a resistance noise, whose magnitude will be evaluated.

By using a doping level of $N_D = 10^{17}$ cm^{-3} for the n-GaAs film and the expression for the width of the SCR of a one-sided p$^+$-n GaAs junction [9], whose built-in voltage will be close to $V_{\rm bi} = 1.42$ V, the thickness of each BSCR in the n-GaAs film is $d = 0.14$ μm. For a 0.5-μm-thick n-GaAs layer ($H_{\rm tech} = 0.5$ μm), the mean thickness $H = H_{\rm tech} - 2d$ for electrical conduction will be $H = 0.22$ μm. The capacitance $C = (\varepsilon \times A_G)/d$ of each cladding capacitor will be proportional to the gate area $A_G = W \times L$, where L is the length of our resistor, and W is its width. To have $C = 1$ pF, $A_G \approx 1.2 \times 10^{-5}$ cm^2 is needed, which is a value that appears for a squared resistor with $W = L = 35$ μm, whose resistance along L is the same as that of a squared resistor with $W = L = 1$ μm and, thus, with a 1225 times lower area. This "small-area" TFR will have the same resistance as the 35×35 μm^2 one, but the kT/C noise of its cladding capacitors will be 1225 times higher in power or 35 times higher in voltage (2.2 mV$_{\rm rms}$) due to its 1225 times lower capacitance: 0.8 fF. This is a resistance noise that scales inversely with the device
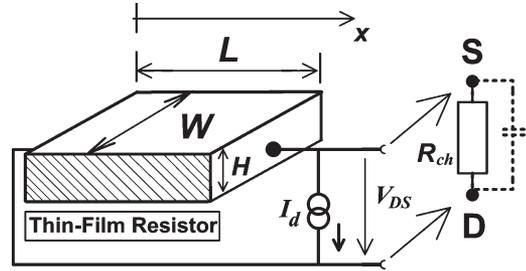

Fig. 1. Simplified view of a planar resistor with "nonplanar" ohmic contacts of area $W \times H$ at both ends.

area, which is a striking property of the so-called "excess noise" in semiconductor devices. Now, let us consider our TFR as a GaAs conducting slab of mean volume $L \times W \times H$ (remember that $H(t)$ fluctuates with time t), which is accessed as it appears in Fig. 1. Its mean resistance $R_{\rm ch}$ will be

$$R_{\rm ch} = \rho \times \frac{L}{W \times H} \Rightarrow \left|\frac{\partial R_{\rm ch}}{R_{\rm ch}}\right| = \left|\frac{\partial H}{H}\right| \Rightarrow \frac{\langle \Delta R_{\rm ch}^2\rangle}{R_{\rm ch}^2} = \frac{\langle \Delta H^2\rangle}{H^2}. \tag{1}$$

The derivative $\partial R_{\rm ch}/\partial H$ leads to the second form of (1), stating that relative fluctuations in resistance $\Delta R_{\rm ch}/R_{\rm ch}$ and relative fluctuations in thickness $\Delta H/H$ of the TFR are equal. This leads to the third term for the normalized mean squared values of resistance and thickness fluctuations, which will be true, provided that the shortest period $T_{\rm sh}$ of the fluctuations in $H(t)$ is much longer than the dielectric relaxation time $\tau_d = \varepsilon/\sigma$ of the material in the TFR. This requirement is met in our case because the spectral components of the low-frequency noise we are going to deal with are below megahertz in general ($T_{\rm sh} \leq 1$ μs), and τ_d is below picoseconds. By using the resistivity given in [9] for this GaAs and doping level ($\rho \approx 0.02$ Ω·cm), the $\tau_d = \varepsilon \times \rho \approx 0.02$ ps thus obtained validates (1) up to modulation frequencies of $H(t)$ in the terahertz range, which is well above the frequencies where low-frequency electrical noise appears. This low τ_d allows n-GaAs FETs to work well in the microwave region.

Therefore, our TFR of mean effective thickness $H = (H_{\rm tech} - 2d) = 0.22$ μm is clad by two trembling boundaries: the two depletion SCR edges associated to two JFET gates left floating. The kT/C noise of their corresponding capacitors will be transferred to the TFR by field effect as a resistance noise, and since the aforementioned kT/C noise is the thermal fluctuation of the energy stored in those cladding capacitors, we must consider first their capacitance per unit area C_Θ (in farads per square centimeter). To simplify reasoning, we will focus on just one p$^+$-n junction or interface, and the noise thus obtained will be just half the resistance noise of our TFR. This interface-induced thermal noise (IIT noise shortly) is thus a thermo-backgating resistance noise whose power spectral density will have units of Ω^2/Hz, or simply Hz^{-1}, if it is normalized by the mean resistance $R_{\rm ch}$.

Fig. 2 shows one of the p$^+$-n junctions that is viewed as a junction capacitor formed by two plates at distance d. One of these plates is the floating gate or p$^+$ GaAs cladding layer,
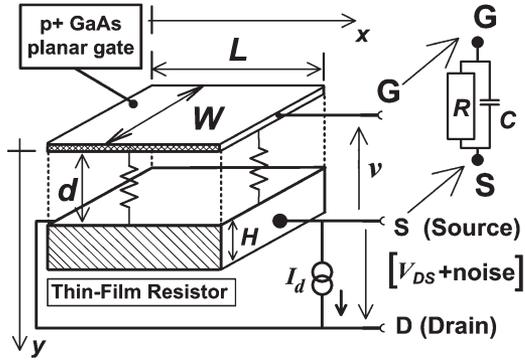
Fig. 2. Simplified view of a planar resistor with a parasitic gate left floating.

and the other plate is the TFR conducting body. For a depletion $d = 0.14$ μm, the transversal capacitance per unit area $C_\Theta = \varepsilon/d$ (in farads per square centimeter) between the floating gate and the TFR is $C_\Theta = 0.83 \times 10^{-7}$ F/cm^2. From N_D donors per cubic centimeter, with all of them ionized for simplicity, the sheet charge density of free carriers in the "channel plate" or TFR is $N_{ch} = q \times N_D \times H$ (C/cm^2), whereas $N_{ch} = 3.5 \times 10^{-7}$ C/cm^2 in our case. To show that the fluctuations in H of thermal origin (relative root mean squared values $\Delta H/H$) are in the parts per million (ppm) range, we need to consider a key device parameter $A_G = (W \times L)$, which is the transversal area for the disturbing capacitance C whose mean squared voltage noise $\langle v_n^2(t) \rangle = kT/C$ (in square voltage) modulates the BSCR width d and, hence, H ($\Delta d = -\Delta H$). We have

$$C = \varepsilon \times \frac{(W \times L)}{d} = C_\Theta \times (W \times L) \quad (2)$$

where ε is the dielectric permittivity of the TFR material. A thermal fluctuation of the energy stored by C requires a variation $\Delta d = -\Delta H$ to allow for the required change in the stored charge per unit area of the junction: $\Delta Q_s = q \times N_D \times \Delta d$. From the noise viewpoint, the sign does not matter, and we have $|\Delta Q_s| = |\Delta N_{ch}| = q \times N_D \times \Delta H$. From this and the definition of $C_\Theta = \Delta Q_s/\Delta v$ (where Δv is the voltage fluctuation in the junction barrier), the mean squared modulation $\langle \Delta H^2 \rangle$ in the slab in Fig. 2 and the mean squared noise voltage in C, $\langle v_n^2(t) \rangle = kT/C$ are related by

$$\langle \Delta H^2 \rangle = \left(\frac{C_\Theta}{q \times N_D} \right)^2 \langle \Delta v^2 \rangle = \left(\frac{C_\Theta}{q \times N_D} \right)^2 \times \frac{kT}{C}. \quad (3)$$

The small value of the $\Delta H/H$ fluctuations due to the IIT noise of our TFR can be obtained from (3) with some typical values for L and W. Taking $L = 50$ μm and $W = 5$ μm, with $H = 0.22$ μm and $\rho \approx 0.02$ $\Omega \cdot$ cm [9], (1) gives $R_{ch} = 9.1$ kΩ for our TFR, disturbed by a capacitor $C = C_\Theta \times W \times L = 0.21$ pF, whose mean squared voltage noise $kT/C = 1.97 \times 10^{-8}$ V^2 is a self-generated voltage noise of 140 μV$_{rms}$. From (3), the root mean squared modulation in the channel will be $\Delta H = 7.28 \times 10^{-10}$ cm$_{rms}$; thus, 33 ppm of its mean value $H = 0.22$ μm, which gives an IIT noise of 0.3 Ω_{rms}.

III. SPECTRUM OF IIT NOISE IN TFRS UNDER THERMAL EQUILIBRIUM (TE)

From (1) and taking the whole free charge in the resistor $Q = qN_D LWH$, we can obtain an equivalent form of (3), i.e.,

$$\begin{aligned} \frac{\langle \Delta R_{ch}^2 \rangle}{R_{ch}^2} &= \frac{\langle \Delta H^2 \rangle}{H^2} \\ &= \frac{\langle \Delta Q^2 \rangle}{Q^2} \\ &= \frac{kTC}{[q \times N_D \times (L \times W \times H)]^2} \end{aligned} \quad (4)$$

where $\langle \Delta Q^2 \rangle$ is the mean squared fluctuation of free charge in the resistor (or in the cladding capacitor). The new term involving Q and its fluctuations comes from Fig. 1, where relative fluctuations in H, in conducting volume and in the whole free charge Q, are equal ($\Delta W/W$ and $\Delta L/L$ are negligible). The charge noise of C of mean squared value $\langle \Delta Q^2 \rangle = kTC$ (in square centimeter) [8] enters the scene, and after some manipulation, we have

$$\frac{\langle \Delta R_{ch}^2 \rangle}{R_{ch}^2} = \frac{kT}{q} \times \frac{C_\Theta}{N_{ch}} \times \frac{1}{N} = V_T \times \frac{C_\Theta}{N_{ch}} \times \frac{1}{N} \quad (5)$$

which is an expression where N is the number of carriers involved in the conductive process, and V_T is the thermal voltage ($V_T \approx 25.9$ mV at room T).

Equation (5) gives the power of normalized resistance fluctuations $\langle \Delta R_{ch}^2 \rangle/R_{ch}^2$ of the IIT noise due to the noise power kT/C of the cladding capacitor, whose spectrum is a Lorentzian one with a cutoff frequency $f_0 = 1/(2\pi RC)$. This is so because such a spectrum is the thermal noise of the capacitor C having some resistance R in parallel [10]. Since the power kT/C (V^2) comes from the integral (from $f = 0$ to $f = \infty$) of this Lorentzian power density, the flat part of this power density below f_0 will be the above power divided by its equivalent noise bandwidth $B_N = (\pi/2)f_0$ [10] set by the parallel R–C cell in Fig. 2. Then, the power density of the normalized resistance fluctuations (S_R/R_{ch}^2) in the flat part of this IIT Lorentzian spectrum (thus for $f \ll f_0$) will be

$$\frac{S_R(f \ll f_0)}{R_{ch}^2} = \frac{2V_T}{\pi} \times \frac{C_\Theta}{N_{ch}} \times \frac{1}{N} \times \frac{1}{f_0} = \frac{\alpha_{TE}}{N \times f_0} \quad (6)$$

which is an expression that we will compare with Hooge's formula [5], [11] for the power density of normalized resistance fluctuations that is

$$\frac{S_R(f)}{R^2} = \frac{S_G(f)}{G^2} = \alpha \times \frac{1}{N} \times \frac{1}{f} = \frac{\alpha}{N \times f} \quad (7)$$

where N is the number of carriers involved in the conductive process, f is the frequency, and α is "not a constant but a volume and device-length independent $1/f$ noise parameter between 10^{-7} and 10^{-3}" [12].

The Bode plots in Fig. 3 compare the IIT noise spectrum (thick solid line) of our TFR under TE to the highest $1/f$ noise given by Hooge's formula for $\alpha_{max} = 10^{-3}$, and the IIT noise power density at its cutoff frequency f_0 surpasses
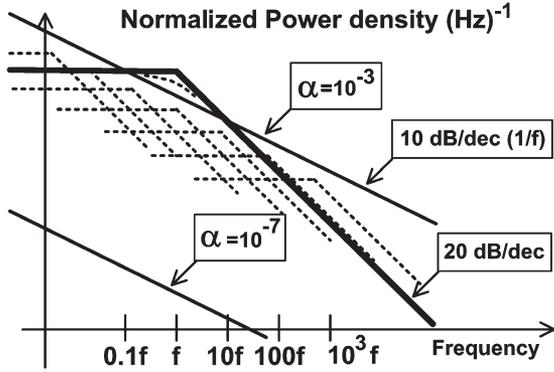
Fig. 3. Bode plot (modulus) of the Lorentzian voltage noise spectrum expected to be found in the TFR with $I_d = 200$ μA, provided that it was unaffected by the bias used in the measurement (see the text). Dashed lines represent several Lorentzian terms coming from different parts of the TFR under the above bias.

the aforementioned $1/f$ noise. This comes from $\alpha_{TE} = 3.9 \times 10^{-3}$ of (6) that only gives the effect of one of the two capacitors cladding the TFR. For this $\alpha_{TE} = 3.9 \times \alpha_{max}$, the corner of the asymptotic IIT noise Bode plot will be 5.9 dB over the $1/f$ line at f_0 for $\alpha_{max} = 10^{-3}$, and hence, the true round corner (dashed line) of this IIT Lorentzian noise at f_0 will also be over (2.9 dB) the aforementioned $1/f$ noise. Adding 3 dB more to this noise power due to the other p^+-n junction left floating, one would say that the low-frequency noise predicted by our electrical theory is a strong Lorentzian IIT noise emerging over the "universal" $1/f$ noise given by Hooge's empirical formula. Nevertheless, the aforementioned comparison is a misleading one because we have compared the IIT noise of our TFR under TE to the $1/f$ noise of samples measured out of TE. This situation must properly be considered, and to prepare the way, let us write the spectrum of the IIT noise that exists under TE. It is

$$\frac{S_R}{R_{ch}^2} = \frac{2V_T}{\pi} \times \frac{C_\Theta}{N_{ch}} \times \frac{1}{N} \times \frac{\left(\frac{1}{f_0}\right)}{1 + \left(\frac{f}{f_0}\right)^2} \qquad (8)$$

where it is quite apparent that the tg^{-1} function will appear if we perform an integration in f to recover the power of the normalized resistance noise in the resistor, which is the opposite process to the one we did to go from (5) to (6) by means of the equivalent noise bandwidth $B_N = (\pi/2)f_0$ of the Lorentzian spectrum of IIT noise under TE.

IV. CONSIDERATIONS ABOUT THE MEASUREMENT OF THE IIT NOISE IN TE

The existence of the IIT noise in our TFR under TE means that its thermal noise power is not strictly constant. By using Nyquist's result for the available thermal power of a constant resistance [13], the power density of our TFR becomes $S_v(f, t) = 4kTR_{ch}(t)$. This is so because $T_{sh} = 1$ μs is also much longer than the mean collision time of the free-carrier gas that allows thermal energy exchanges in the TFR. The measurement of $S_v(f, t)$, however, is difficult due to the statistical nature of

the noise signal that requires some time averaging to have an acceptable "signal-to-noise" ratio (trace roughness) in the obtained spectra. This averaging tends to give the Johnson noise of the mean resistance R_{ch} around which the varying resistance $R_{ch}(t)$ fluctuates, and thus, the small IIT noise attenuated by the averaging process is lost in the aforementioned roughness.

Thus, the IIT noise exists in resistors under TE and has a Lorentzian spectrum, which is quite difficult to measure. Since this is quite disappointing, we will try to convert it into a voltage noise with enough amplitude to surpass $S_v(f) = 4kTR_{ch}$, which is the Johnson noise power density. An innocent attempt to do this is by means of a dc current I_d through our TFR, trying to convert its 0.3-Ω_{rms} IIT noise into an ac voltage noise power that is able to excite a spectrum analyzer, which is an action that a resistance noise, such as IIT noise, cannot do. An injected dc current $I_d = 200$ μA, as it shown in Fig. 2, would convert the aforementioned resistance noise into a 60-μV$_{rms}$ voltage fluctuation that is added to the dc term V_{DS} of our TFR. The Johnson noise density of our TFR is $S_v(f) = 1.5 \times 10^{-16}$ V^2/Hz, which is a flat floor that must be surpassed by the converted noise of 60 μV$_{rms}$ to be observed, and this depends on the bandwidth, from dc to $f_0 = 1/(2\pi RC)$, where the converted noise is expected to appear. As shown in [2], the R value that gives the cutoff frequency f_0 of the R–C cell made from the p^+-n junction in Fig. 2 is the dynamical resistance $R = r_d(v)$ of the planar diode, i.e., an exponential function of its bias voltage v. This bias voltage can be a photovoltage, such as those in [2], but it can also be an overseen voltage due to an innocent conversion method.

Taking f_0 in the hertz range for this p^+-n GaAs junction of quite-high $V_{bi} \approx 1.4$ V [2], the power of the converted noise will be concentrated in a frequency band from dc $(f \to 0)$ to a few hertz. By using $f_0 = 1$ Hz and the $B_N = (\pi f_0)/2$ for this presumable Lorentzian spectrum, the power density of its flat part will be $(60 \mu V_{rms})^2/B_N = 2.26 \times 10^{-9}$ V^2/Hz; thus, it is well over $S_v(f) = 1.5 \times 10^{-16}$ V^2/Hz, even for 10^6 times higher f_0 values $(f_0 \leq 10$ MHz). Then, why not use $I_d = 200$ μA to measure the IIT noise of our TFR through its converted voltage noise? The answer that introduces the main contribution of this paper is because the converted noise thus obtained (out of TE) will not be a pure Lorentzian noise as the IIT noise was in TE. The reason is the dc voltage drop along the TFR that will appear in Fig. 2 for $I_d = 200$ μA, which is $V_{DS} = R_{ch} \times I_d = 1.82$ V. This V_{DS} will bias the floating-gate FET that our TFR is, and hence, the highly conducting p^+ floating gates will acquire (after a quite long waiting time for f_0 in the hertz range) a floating voltage between zero and V_{DS} (see the Appendix). As shown in Fig. 4, part of the planar junction, next to the source terminal, becomes forward-biased, whereas the remaining junction becomes reverse-biased in such a way that the opposed injection and extraction currents flowing through each region of the junction cancel each other. This makes the net charge transfer from the TFR channel to the p^+ gate null, but the bias voltage v of the planar junction at the ends of the TFR differs by $V_{DS} = 1.82$ V (70 times the thermal voltage V_T). From the exponential dependence of $r_d(v)$ shown in [2] for GaAs planar diodes, which has also
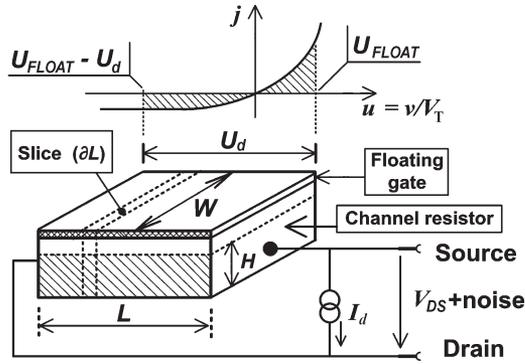
Fig. 4. Simplified view of a planar resistor with a parasitic floating gate that acquires a floating voltage due to the injected current I_d.

been confirmed recently in Si Schottky diodes [14], we must consider that the planar junction is very differently "tuned" in Fig. 2, going from source to drain. This would give a range of cutoff frequencies $f_0(v)$ close to $\exp(70) = 2.5 \times 10^{30}$, and moreover, the aforementioned $R_{ch} = 9.1$ kΩ would not be true because the thickness $H(x)$ of the TFR would vary along the x-axis due to the well-known "pinch-off" effect in a JFET, next to its drain terminal.

Once the effects of the V_{DS} used in the measurement have been emphasized, they can be alleviated, but not removed, by using a lower I_d to have a smaller departure from TE conditions. For ten times lower I_d, the new $V_{DS} = 182$ mV would only be 7 V_T, but the power of the converted voltage noise would be 100 times lower. For $f_0 = 100$ kHz, the power density of the converted voltage noise below f_0 would be 2.26×10^{-16} V^2/Hz, which is very close to the thermal floor $(1.5 \times 10^{-16}$ V^2/Hz), giving some hope of seeing a small "step" in the noise spectrum around $f_0 = 100$ kHz due to the sum of the power of thermal and converted IIT noises and a bigger step for $f_0 < 100$ kHz. However, this hope vanishes as soon as we consider that $V_{DS} = 7\,V_T$ along the TFR gives rise to very different $r_d(v)$ for the planar junction at each position x along the TFR, thus giving a continuous distribution of cutoff frequencies over three decades: $\exp(7) = 1096$. Taking our TFR as the series connection of differential JFETs (one at each x position in Fig. 2), a continuous set of Lorentzian noise terms appears in the TFR channel (one at each position x), whose cutoff frequencies will cover three decades. Applying (8) to this situation, we obtain the set of dashed Lorentzian spectra shown in Fig. 3, each having a flat part that is inversely proportional to its f_0, which is a condition that is required to obtain a $1/f$ noise from a set of Lorentzian terms (see [15, Fig. 1]). This fact leaves out our last hope of observing a Lorentzian noise step around f_0 for $I_d = 20$ μA (a $1/f$ noise is obtained instead), thus revealing the ingenuous character of the method that is used to convert IIT noise into a voltage noise image "proportional" to the IIT noise that existed under TE ($I_d = 0$). In addition, this gives a reason why a $1/f$ electrical noise is found by most researchers: The ingenuousness of the conversion method they use synthesizes the $1/f$ electrical noise in each measurement. The mathematical work supporting this has been done in the Appendix.
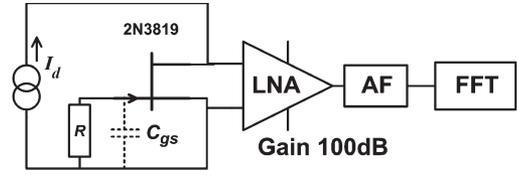

Fig. 5. Noise-measuring setup used to measure resistance noise in a 2N3819 JFET (see the text).
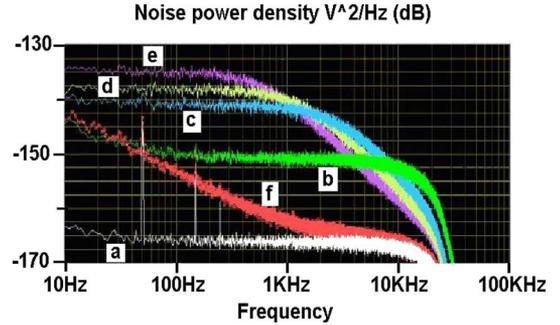

Fig. 6. Voltage noise spectra in the channel of a 2N3819 JFET due to the kT/C noise present at the input capacitor C_{gs} for different R values shunting it.

V. EXPERIMENTAL RESULTS

The predictions made for our TFR with two floating gates suggest that the low-frequency noise of commercial n-channel JFETs in their ohmic region (low V_{DS}) could give some experimental support to our theory. This is so because these devices also used to have a channel clad by two gates, the upper one being accessible through a metallic gate wire. There is a second gate under the channel (a planar junction to set the channel thickness) that is left floating and inaccessible, thus being the kind of $1/f$ noise source revealed by our theory. This is why we have measured the channel noise of a 2N3819 n-channel JFET (a silicon counterpart of our GaAs TFR) whose n-type channel will have a p-type region on top connected to its gate wire, and there will be another p-type region under the channel to limit its thickness in order to have an appropriate pinch-off voltage. Fig. 5 shows the arrangement used to measure noise in the channel resistance of a 2N3819 JFET under two bias conditions: $I_d = 0$ (thus $V_{DS} = 0$ V) and $I_d = 622$ μA dc, leading to $V_{DS} = 155$ mV when I_d was injected into the JFET through a 20-kΩ resistor in series with a 12.6-V battery shunted by a 10-μF high-quality capacitor. The 20-kΩ resistor appearing in parallel with $R_{ch} = V_{DS}/I_d = 250$ Ω with this setup barely modifies the noise coming from R_{ch}. The spectrum analyzer in Fig. 5, which was recently used in [4], has a 25-kHz cutoff frequency, fourth-order Butterworth filter [antialiasing filter (AF)], and a PC-based sampler (16 bits) programmed to take sets of 2.4×10^5 samples at a rate of 2.0×10^5 samples/s, whose power spectrum was obtained by fast Fourier transform. Each curve shown in Fig. 6 is the average of 64 of the aforementioned spectra, whereas 128 averaged spectra were used in Fig. 7.

The low thermal noise power density $S_v(f) = 4kTR_{ch} \approx 4$ (nV)^2/Hz of this channel or its spot noise $v_{dT} = 2$ nV/$\sqrt{\text{Hz}}$ falls below the input spot noise ($e_n \approx 4$ nV/$\sqrt{\text{Hz}}$) of the
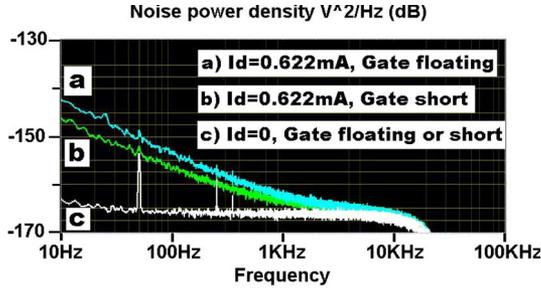
Fig. 7. $1/f$ noise increase in the channel of a 2N3819 JFET due to its wired gate left floating (see the text).

low-noise amplifier (LNA), but this is not a serious drawback because we are not interested in the Johnson noise of the JFET channel but in its IIT noise. The aforementioned values, however, will set the lowest noise at the output of our system because the current noise $i_n \approx 5$ fA/$\sqrt{\text{Hz}}$ of the LNA leads to a product $(R_{\text{ch}} \times i_n)$ well below e_n. This can be seen in Fig. 6, which shows the noise power densities measured for $I_d = 0$ and for $I_d = 622$ μA. As expected, no excess noise appears for $I_d = 0$ because the flat spectrum at -167 dB V^2/Hz) ($e_{\text{ntot}} \approx 4.5$ nV/$\sqrt{\text{Hz}}$, curve a) comes from the addition in power of $(e_n)^2 \approx 16$ nV^2/Hz and $(v_{\text{dT}})^2 \approx 4$ nV^2/Hz. Lines at 50, 150, and 250 Hz are interferences from the main power line. Thus, the thermal noise of the JFET channel is one fourth the noise of the LNA (1/4 power ratio), but we are more interested in the noise power density due to the resistance noise ΔR_{ch} that will emerge well over the aforementioned $(e_{\text{ntot}})^2$ if we use enough I_d (traditional approach). With $I_d = 622$ μA, the resistance noise clearly emerges, and curves b, c, d, and e in Fig. 6 correspond to the R values of 1, 10, 20, and 40 MΩ. They show the Lorentzian or GR-like resistance noise expected for R_{ch} as a mirror of the kT/C_{gs} noise of C_{gs} shunted by different R values. Taking $f_c \approx 650$ Hz from curve e, for example, $C_{\text{gs}} \approx 6$ pF is obtained, which matches the C_{gs} of the 2N3819 datasheets in parallel with ≈ 2 pF of parasitic capacitance of the shielded noise test fixture used.

An interesting effect observed in curves c to e is the conservation of their noise power kT/C_{gs} as R is changed. This corresponds to the same $(v_{\text{rms}})^2 = kT/C$ value that is obtained in a linear R–C parallel circuit, no matter what R value is used [10]. As can be observed, the rounded corners of curves c, d, and e appear to be aligned along a straight line with a $1/f$ slope due to their kT/C_{gs} noise power being equal, and due to the logarithmic spacing of the resistances put in parallel with C_{gs} (10, 20, and 40 MΩ), they form a kind of constant-step ladder that is similar to that in Fig. 3 for Lorentzian noises (dashed lines) of different slices of channel having similar capacitances being shunted by logarithmically spaced $r_d(v)$ values produced by the linear distribution of V_{DS} along the channel that is one of the plates of its own disturbing capacitor.

This JFET with its gate–source junction shunted by a linear j–v characteristic (the resistor R in Fig. 5) overriding its exponentially dependent dynamical resistance $r_d(v)$ allows the observation of the Lorentzian spectra in Fig. 6, which are similar to those that will appear for planar junctions having an $r_d(v)$ that is independent of the junction voltage v. Nev-

ertheless, as $R \to \infty$ (curve f in Fig. 5), the tunable $r_d(v)$ of the junction synthesizes the $1/f$ noise in the way sketched in Fig. 3, and this leads to an interesting test on this 2N3819 JFET to check our model about the $1/f$ noise in planar resistors. Making $R \to 0$ in Fig. 5, the noise spectrum obtained for $I_d = 622$ μA is similar to the curve f in Fig. 6 but with its $1/f$ part attenuated by ≈ 3 dB (half noise power). This means that with $R = 0$, we have silenced one of the two floating gates cladding the channel (the top one connected to the gate wire), but, at least, a similar gate still remains floating under the channel. This backgate and its effects in noise measurements are the oblivion that this paper reveals for the first time. Fig. 7 shows these measurements for $I_d = 622$ μA. Curve a shows the noise spectrum (thermal+converted IIT noise) of the JFET channel with its gate wire left "on the air," and curve b shows the channel noise spectrum of the JFET with this gate wire shorted to the source. The $1/f$ noise reduction by a factor of two (≈ 3 dB) for all those frequencies giving a $1/f$ noise (two decades) strongly suggests the simple explanation given previously that backs our theory about the electrical origin of $1/f$ excess noise in planar resistors. The nonperfect parallelism at 3 dB of the $1/f$ lines as we approach the thermal floor is due to the effect of such a floor added in power to the $1/f$ converted noise, thus reducing the 3-dB separation as we approach this floor.

VI. DISCUSSION

The field effect causing a $1/f$ resistance noise in conductors allows having both the $1/f$ IIT noise related with a distributed RC line in the surface [4] (equivalent to a diffusion process [16]) and the $1/f$ IIT noise synthesized by the applied bias, thus being a unifying feature leading to a $1/f$ noise that scales inversely with the area A_G and fits in Hooge's formula. The shot noise of transversal currents (both forward and reverse ones) induced in planar junctions by the applied V_{DS} will add to the kT/C noise of the disturbing capacitor having the very same Lorentzian spectrum. This increases the IIT noise in the channel, thus giving a first explanation for the high $1/f$ noise found in GaAs FET devices fabricated on SI GaAs substrates, whose $1/f$ corner frequency is well above 100 kHz [17]. The low built-in voltage of the n-channel/SI-GaAs junction diode leads to high transversal currents and, hence, to a high shot noise in the disturbing capacitor. This suggested a way to reduce the $1/f$ noise in these devices [18], which is useful to reduce noise upconversion effects in GaAs microwave oscillators, for example.

To end this reflection on devices often overseen in "simple" resistors, a dashed capacitor placed in parallel with R_{ch} in Fig. 1 is the required device $(C_d = \tau_d/R_{\text{ch}})$ to account for a property of the material in the resistor: its dielectric relaxation time τ_d that will give a drop of the $S_v(f) = 4kTR_{\text{ch}}$ power density at a frequency $f_d = 1/(2\pi\tau_d)$. This f_d can fall below the frequency for which quantum effects cause $S_v(f)$ to drop [13]. This would happen in our TFR having $N_d = 10^{16}$ cm^{-3}, for example, and then, many textbooks and review papers (see [19, Fig. 1], for example) could be improved by this remark about τ_d, which also reveals a difficult matching of transmission lines

in millimetrics (e.g., at 150 GHz) with a pure resistance slab $R_{\text{end}} = Z_0 = 50\ \Omega$ made from a material with $\tau_d = 1$ ps. Considering the excellent work of Nyquist [13] for "conductors of pure resistance R," this paper only adds the remark that actual resistors are not such hypothetical devices, but only approach them, because devices offering a pure resistance R, which are constant at all frequencies, simply do not exist because any material used to fabricate them will have a non-null τ_d. Going back to an old report showing a $1/f$ electrical noise in vacuum tubes written by Johnson in 1925 (see [20, Fig. 7]), our electrical theory for $1/f$ noise applies quite straightforwardly [21], [22]. In this case, the voltage drop along the filament to heat it would play the role of V_{DS} to modify the cathode-grid potential barrier for electron emission along the cathode of the vacuum tubes (audions) used by Johnson in [20]. The plate of each tube, summing currents coming from each cathode position (and their fluctuations), would synthesize the $1/f$ noise in the plate current. The planar geometry of these "standard Western Electric 102-D audions with plane-parallel plates and grids" described in [20] and the field effect they had in common with today's field-effect devices to control carriers is worth noting.

VII. CONCLUSION

Planar photoconductors in the dark are resistors having an electrostatic coupling with their underlying substrate or layer that has been overlooked in noise studies. This coupling leads to parasitic gates in the vicinity of such devices that make them true FET devices with one or more floating gates, thus having a mean resistance R_{ch} together with a resistance noise that reflects the kT/C noise of boundary capacitors. This model gives a pure electrical explanation for the excess noise of planar devices based on a field effect and on the thermal noise of boundary capacitors.

Another important issue also overseen over the course of time is that the bias voltage used to convert resistance noise into voltage noise takes the devices under test out of TE, thus modifying the IIT noise that existed without bias. The higher the V_{DS} used, the greater the disturbance is on the sample: a disturbance leading in general to a set of Lorentzian noise terms often viewed as synthesized $1/f$ noise.

Finally, the field effect that produces IIT noise in thin-film devices fits well in Hooge's formula. In this way, two old mathematical models for $1/f$ noise (e.g., those based on diffusion processes and those synthesizing $1/f$ noise from Lorentzian terms) are possible under a unifying feature: the backgating effect in conducting channels from neighbor interfaces. A careful removal of this IIT noise will allow the proper evaluation of other theories on low-frequency noise like those (theories) which handle conductivity fluctuations taking place in rigid geometries, which is an approach that we have not considered here.

APPENDIX

When a current I_d is injected (Figs. 2 and 4), a linear voltage drop V_{DS} appears along x in the TFR, and the floating gate has to acquire a floating voltage V_{float} between zero and V_{DS} in order to balance two opposed currents crossing the junction: a reverse current from the channel to the gate in the drain side and a forward current from the gate to the channel in the source side. An exponential j–v characteristic (j is current density) for the gate-channel junction has been shown in Fig. 4 to calculate V_{float}. This is done by allowing the same positive and negative area under the j–v curve for the segment of length $U_d = V_{\text{DS}}/V_T$ that appears along L using V_T units for the voltage drop along the channel. The j–v function used is

$$j(v) = j_{\text{sat}} \times [\exp(v/V_T) - 1] = j_{\text{sat}} \times [\exp(u) - 1] \quad (9)$$

whose integral from $U_{\text{float}} = V_{\text{float}}/V_T$ (forward bias of the junction in the source) to $(U_{\text{float}} - U_d)$ (reverse bias in the drain) must be zero. This gives

$$U_{\text{float}} = \text{Ln}\left[U_d/(1 - \exp(-U_d))\right] \approx \text{Ln}(U_d), \quad \text{for } U_d \geq 3 \tag{10}$$

which is a logarithmic converter that gives this result: For V_{DS} values surpassing few V_T units, most of the floating gate is reverse-biased. This is so because the fraction of junction under forward bias L_F/L is

$$L_F/L = U_{\text{float}}/U_d = (1/U_d) \times \text{Ln}\left[U_d/(1 - \exp(-U_d))\right]$$
$$\approx \left[\text{Ln}(U_d)\right]/U_d, \quad \text{for } U_d \geq 3 \quad (11)$$

which is a useful equation to estimate the shot noise of the planar junction that, added to its kT/C noise, will be transferred to the channel as IIT noise. Ideality factors other than unity in (9) lead to similar results, but we have avoided them for clarity purposes.

Due to the weak dependence of the junction capacitance C with its bias voltage v (particularly for V_{DS} values of few V_T), Fig. 4 can be seen as a capacitor C, setting the total noise power kT/C, whose spectral distribution (spectrum) will be different at each position, depending on the allowed paths (dynamic resistances) for energy relaxation at each position x. Considering TFR slices of thickness ∂L as that shown in Fig. 4, we can say that for $V_{\text{DS}} = 0$ (thus in TE), the power relaxed by such a slice is a fraction $\partial L/L$ of the total noise power kT/C due to energy relaxations taking place in C. This way, two slices of the same thickness ΔL dissipate the same mean power $(kT/C) \times (\partial L/L)$ by conduction currents orthogonal to the equipotential plates. This must be so to make null the mean current of thermal origin flowing along the resistor or along the p^+ plate.

To know what happens when I_d (and, thus, some V_{DS}) is applied along the resistor slab to convert its resistance noise, we have to consider the inner geometry of the electric fields within the device. In planar junctions, the electric field due to the junction itself ($E = V_{\text{bi}}/d \approx 10^5$ V/cm typically) is much higher than the disturbing field due to V_{DS} in Fig. 4 (e.g., 1 V in an $L = 100\ \mu$m typically; thus, $E_L = 10^2$ V/cm), although both fields, at right angles, will add vectorially. Hence, the first term dominates, and any thermal charge fluctuation existing in C will relax through conduction currents that are

very orthogonal to the p$^+$ and TFR plates. This means that the electric-field structure of the sample in the TE is roughly kept under the small disturbance due to V_{DS}, and this requires keeping C as the energy-storing element that sets the whole thermal power kT/C.

Since the channel "plate" of this capacitor is not equipotential, as is the p$^+$ gate, the dynamical resistance per unit area of the junction $R_\Theta(x) = r_d(v) \times A_G$ ($\Omega \cdot \mathrm{cm}^2$) in each slice will vary along x. Considering that the time constant $\tau = R_\Theta \times C_\Theta = R \times C$ sets the rate at which the energy stored transversally in the junction relaxes at each individual slice, we can advance that the rate $\tau(x)$ of these energy relaxations will be different as we move along the channel (Condition I). However, this set of relaxation dynamics cannot give rise to a net energy transfer along x from thermal origin (otherwise, one side of the TFR would be heated, while the other would be cooled). Therefore, no matter how the relaxation dynamics exist at each slice, the mean power relaxed by each slice under $V_{\mathrm{DS}} \neq 0$ must be $(kT/C) \times (\partial L/L)$, which is the same as it was for $V_{\mathrm{DS}} = 0$ (Condition II). However, a striking property of the electrical noise of an R–C parallel circuit is that its noise power is always kT/C, no matter how the R value shunts C [10], which is a feature that allows the same power dissipation by slice in Fig. 4, having the same $\partial C = (C/L) \times \partial x$ but very different $\partial r_d(v)$, thus fulfilling Conditions I and II. Therefore, the bias voltage V_{DS} creates both the floating-gate voltage V_{float} and the voltage drop along the channel that bias the planar junction at each position x differently. This will set a different time constant $\tau(x) = R_\Theta(v) \times C_\Theta$ for the planar junction at each position x, or, in other words, the gate-channel capacitor ∂C of each slice will have its own kT/C-like noise power that will be a fraction $\partial L/L$ of the total noise power in the gate-channel capacitor but "tuned" by its own ∂R–∂C parallel circuit that will have its own cutoff frequency $f_0(x) = 1/[2\pi\tau(x)]$. By using the time constant of the planar junction in TE $\tau_0 = 1/[2\pi f_0]$, the time constant of such junction under a bias voltage v (positive if forward) becomes [2]

$$\tau(v) = \tau_0/\left[\exp(v/V_T)\right] = \tau_0 \times \exp(-u)$$
$$\Rightarrow 1/f_0(u) = [1/f_0] \times \exp(-u). \quad (12)$$

The "tuned fraction" of kT/C noise existing in the differential junction of each slab will transfer an IIT noise to the differential portion of channel of such a slab in the same way it would do if the slab was embedded in the structure of Fig. 4, making $I_d = 0$ but uniformly biased with v volts applied vertically between the p$^+$ gate and the channel (e.g., by using a metallic contact of area $(W \times L)$ placed under the TFR slab). Particularizing (8) for the junction under this uniform bias by $v = u \times V_T$, the normalized IIT noise spectrum (Hz^{-1}) in the TFR channel becomes

$$\frac{\langle S_R \rangle}{R_{\mathrm{ch}}^2} = \frac{2V_T}{\pi} \times \frac{C_\Theta}{N_{\mathrm{ch}}} \times \frac{1}{N} \times \frac{\left(\frac{1}{f_0}\right)\exp(-u)}{1 + \left(\left(\frac{f}{f_0}\right)\exp(-u)\right)^2} \quad (13)$$

and thus, the IIT resistance noise spectrum (Ω^2/Hz) of a slab of thickness ∂L will be

$$\langle S_{\mathrm{Rslab}} \rangle = R_{\mathrm{ch}}^2 \times \frac{2V_T}{\pi} \times \frac{C_\Theta}{N_{\mathrm{ch}}} \times \frac{1}{N}$$
$$\times \frac{\left(\frac{1}{f_0}\right)\exp(-u)}{1 + \left(\left(\frac{f}{f_0}\right)\exp(-u)\right)^2} \times \frac{\partial x}{L} \quad (14)$$

where it is quite apparent that an integral over x summing the resistance noise of all the slices connected in series recovers (13).

From the linear drop of V_{DS} (and, hence, of $U_d = V_{\mathrm{DS}}/V_T$) along the channel length L, we have $\partial x/L = \partial u/U_d$, and (14) becomes

$$\langle S_{\mathrm{Rslab}} \rangle = R_{\mathrm{ch}}^2 \times \frac{2V_T}{\pi} \times \frac{C_\Theta}{N_{\mathrm{ch}}} \times \frac{1}{N}$$
$$\times \frac{\left(\frac{1}{f_0}\right)\exp(-u)}{1 + \left(\left(\frac{f}{f_0}\right)\exp(-u)\right)^2} \times \frac{\partial u}{U_d} \quad (15)$$

which gives the IIT noise spectrum in the differential channel of a slice whose junction bias voltage is $v = u \times V_T$. Therefore, $V_{\mathrm{DS}} = I_d \times R_{\mathrm{ch}} \neq 0$ leads to a set of slabs connected in series, continuously tuned from $u = U_{\mathrm{float}}$ to $u = (U_{\mathrm{float}} - U_d)$, all having I_d to convert their resistance noise into an ac voltage noise superimposed to the dc one V_{DS}.

Integrating (15) from $u = (U_{\mathrm{float}} - U_d)$ to $u = U_{\mathrm{float}}$, we will collect the IIT resistance noise of all the slices (a continuous set of Lorentzian terms) that will give the IIT noise spectrum of the channel observed as a whole, because the IIT noise at each position is a different Lorentzian term. It is worth noting that this is equivalent to the integration in x mentioned below (14) to recover (13). We have

$$\frac{\langle S_R \rangle}{R_{\mathrm{ch}}^2} = \frac{2V_T}{\pi} \times \frac{C_\Theta}{N_{\mathrm{ch}}} \times \frac{1}{U_d} \times \frac{1}{N} \times \frac{\partial f}{f} \times \int_{\Theta_1}^{\Theta_2} \frac{\partial \Theta}{1 + \Theta^2} \quad (16)$$

where the variable Θ and the limits Θ_1 and Θ_2 are

$$\Theta = \frac{f}{f_0} \times \exp(-u) \Rightarrow \frac{\partial \Theta}{\partial u} = -\Theta \quad (17)$$

$$\Theta_1 = \frac{f}{f_0 \times \exp(U_{\mathrm{float}})} \quad \text{and} \quad \Theta_2 = \Theta_1 \times \exp(U_d). \quad (18)$$

For frequencies f making $\Theta_1 \ll 1$ and $\Theta_2 \gg 1$, the tg^{-1} function resulting from the integral in (16) gives a $\pi/2$ factor that converts (16) into

$$\frac{\langle S_R \rangle}{R_{\mathrm{ch}}^2} = \frac{V_T \times C_\Theta}{N_{\mathrm{ch}} \times U_d} \times \frac{1}{N} \times \frac{1}{f} = \frac{\alpha_{\mathrm{IIT}}}{N \times f} \quad (19)$$

which is Hooge's formula with an α_{IIT} parameter, including the number of thermal voltage units used as V_{DS}. This helps

in explaining the dispersion in α given in [12] ($10^{-7} \leq \alpha \leq 10^{-3}$) as due to the different V_{DS}, C_{Θ}, N_{ch}, and V_T values used by each author. Moreover, this can be worse for careless measurements done in channels under pinch-off conditions. Doubling the value $\alpha_{\mathrm{TE}} = 3.9 \times 10^{-3}$ obtained for our GaAs TFR (to consider its two floating gates), we can predict that, for a $V_{\mathrm{DS}} = 155$ mV ≈ 6 V_T applied to observe its IIT resistance noise as we did in the JFET in Section VI, we would have $\alpha_{\mathrm{IIT}} = 2 \times 10^{-3}$, which is equal to the empirical $\alpha = 2 \times 10^{-3}$ given by Hooge [5] as an average 37 years ago. A remark concerning α_{IIT}, which refers to its simple formula involving V_T, C_{Θ}, N_{ch}, and U_d, is given next. This formula gives the lowest α value that will be found in actual samples because the shot noise in the planar junction must also be considered, particularly for low-V_{bi} junctions where it is very likely to surpass the kT/C noise. This neutralizes the $1/U_d$ term that suggests a $1/f$ noise proportional to V_{DS} rather than to $(V_{\mathrm{DS}})^2$, which is not observed empirically, as a referee argued against a paper on the subject of this Appendix. This referee, however, did not consider the increase (proportional to U_d) of the currents across the junction that appears from (11) for $U_d \geq 3$. The corresponding increase of shot noise in the junction compensates the $1/U_d$ factor for any empirical α coming from a junction where shot noise dominates. Finally, the $1/f$ noise power predicted by our theory is finite, as is its origin: the noise in the planar junction diode. This follows from the flat power density predicted for $f \ll f_0 / \exp(U_d - U_{\mathrm{float}})$ and from its drop as $1/f^2$ for $f \gg f_0 \times \exp(U_{\mathrm{float}})$; thus, it does not have the problems about divergent $1/f$ noises studied in [16].

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