Effects of N_2 Plasma Pretreatment on the SiN Passivation of AlGaN/GaN HEMT

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***Abstract*—The impact of *in situ* low-power N_2 plasma pretreatment, prior to silicon-nitride (SiN) deposition, was investigated in AlGaN/GaN high-electron mobility transistors (HEMTs). These studies reveal that the use of N_2 plasma in HEMT passivation reduces current-collapse and gate-lag effects. Such treatment is also beneficial to improve gate leakage, and from RF measurements, no degradation of $f_{\max}$ was observed. These beneficial effects of the N_2 plasma pretreatment seem to be due to a significant reduction in interface charge density, as shown in this letter using GaN MIS devices, where a decrease of 60% was observed.**

***Index Terms*—AlGaN/GaN high-electron mobility transistors (HEMTs), current collapse, GaN MIS, passivation, silicon nitride (SiN).**

I. INTRODUCTION

FOR HIGH-TEMPERATURE/high-power microwave and industrial electronic applications, AlGaN/GaN high-electron mobility-transistor (HEMT) devices are very promising [1]. Although significant progresses have been made, additional efforts are required in relation to current-collapse effects and reliability issues [2]. It has been shown that the current-collapse effects can be minimized by proper device surface passivation when the dominant mechanism is related to trapping/detrapping surface states [3], [4]. Although different dielectric films have been deposited on the AlGaN/GaN HEMT for this objective, the most widely used passivating layer is silicon nitride (SiN) [3]. However, the passivation mechanisms and the properties of the insulator–AlGaN interface are not fully understood, and a successful passivation is not always achieved.

There are few available reports that are related to the effects of specific surface cleanings and treatments, before SiN passivation layer, on AlGaN/GaN structures. The most commonly used step is wet chemical cleaning (organic solvents and NH_4OH [5]), although several plasma pretreatments have been recently reported showing that the use of NH_3 [6], $O_2 + CF_4$ [4], and O_2/SF_6 [7] plasma pretreatments prior to passivation could improve device performance. The effect of the N_2 plasma pretreatment prior to SiN deposition in the AlGaN/GaN HEMTs is still under discussion due to the different plasma treatments [5], [7], [8]. MIS studies are also scarce in this type of studies, making comparisons even more difficult. In this sense, this letter focuses on the use of low-power N_2 plasma-treatment effects just before the SiN deposition on both AlGaN/GaN HEMTs and GaN MIS structures.

II. EXPERIMENTAL SETUP

AlGaN/GaN heterostructures with 20–30-nm-thick undoped AlGaN barriers (28%–36% Al), on a high-resistivity GaN buffer layer, and grown by metal–organic chemical vapor deposition (CVD) on 4H-SiC or sapphire substrates were used. Ti/Al/Ti/Au (20/100/40/55 nm) provided source and drain ohmic contacts ($R_c = 0.5{-}0.8\ \Omega \cdot \mathrm{mm}$ and $R_{\mathrm{sheet}} = 480\ \Omega/\square$). By optical lithography, Pt/Ti/Au Schottky gates of 1.5–2 μm in length and 75–150 μm in width were fabricated. Mesa isolation was obtained by reactive ion etching using SiCl4/Ar/SF_6. In the standard passivation processing, the SiN was deposited at 300 °C in a conventional RF plasma-enhanced CVD system, and no previous *in situ* cleaning or plasma treatment was applied. SiH_4 and NH_3 were used as precursors, obtaining a slightly N-rich SiN layer with $n = 1.83$ and $\varepsilon_r = 7.0$, as determined by ellipsometry. The treatment investigated was an *in situ* N_2 plasma prior to the SiN deposition, at 200 °C for 1 min at low power (60 W), after a wet cleaning with NH_4OH at 50 °C. MIS structures were also fabricated on an n-type GaN ($N_D = 3 \times 10^{18}\ \mathrm{cm}^{-3}$), with and without the N_2 plasma pretreatment (N_2PP) before the SiN deposition.

The effect of N_2PP was studied in the AlGaN/GaN HEMTs. As a set of first experiments, the standard SiN passivation layer in the already processed HEMT was removed using buffer-oxide-etching (BOE). Afterwards, the sample was divided into two pieces. One piece (P1) was repassivated using the standard passivation step (without N_2PP), and the other one (P2) was repassivated using the N_2PP described previously. This approach tried to minimize processing and sample inhomogeneity effects.

In a second set of experiments, samples P3 and P4, from a wafer with the same nominal structure than P1 and P2, were used to fabricate the AlGaN/GaN HEMT in a continuous processing flow. Transistors in P3 were passivated without N_2PP, whereas transistors in P4 were SiN-passivated using now the N_2PP.

Manuscript received October 26, 2007; revised December 12, 2007. This work was supported in part by the FPU research grant from the Ministry of Education and Science (MEC), Spain, and in part by the KORRIGAN project (EDA—04/102.052/032 CA 2157v7). The review of this letter was arranged by Editor J. del Alamo.

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Digital Object Identifier 10.1109/LED.2008.915568

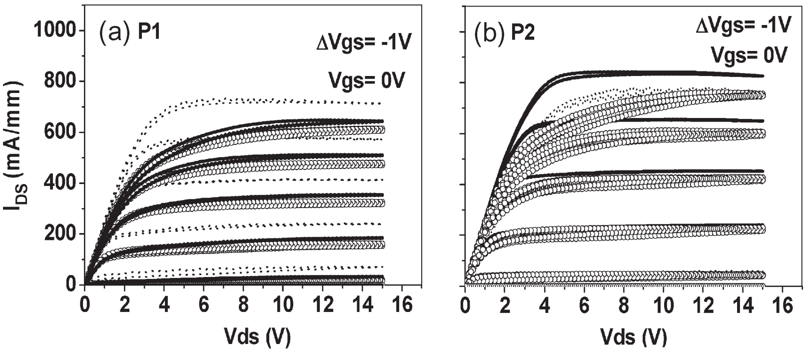

Fig. 1. Pulsed $I_{\mathrm{DS}}-V_{\mathrm{DS}}-V_{\mathrm{GS}}$ characteristics of AlGaN/GaN HEMT with the initial SiN passivation (dot lines), after removing the SiN layer (hollow-circle lines), and the SiN repassivation (solid lines), (a) without and (b) with N_2 plasma pre-treatment ($V_{\mathrm{GS}} = -5$ V to 0 V), $\Delta V_{\mathrm{GS}} = 1$ V. The pulses have a width of 500 μs and a period of 10 ms. Quiescent bias point is $(V_{\mathrm{DS}}, V_{\mathrm{GS}}) = (0\ \mathrm{V}, -6\ \mathrm{V})$.

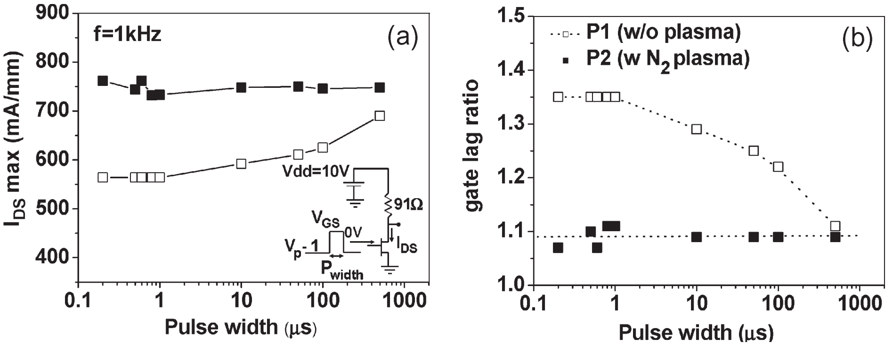

Fig. 2. Evolution of (a) $I_{\mathrm{DS}}^{\mathrm{max}}$ and (b) gate-lag ratio as a function of gate pulsewidth, with a constant frequency (1 kHz) and a V_{DD} (10 V). White and black squares correspond to P1 and P2, respectively. Solid and dot lines are guides to the eye.

The HEMT devices were characterized by dc and pulsed I–V measurements (gate pulsewidth from 200 ns to 500 μs and a period of 10 ms) from -6 V (1 V lower than the pinch-off condition) to 0 V (open channel) [9]. Moreover, after the HEMT repassivation, gate-lag measurements were performed, fixing V_{DD} at 10 V and applying pulsed V_{GS} excitation from OFF- to ON-state.

III. RESULTS AND DISCUSSION

The pulsed output characteristics in P1 and P2 samples are shown in Fig. 1. The I–V characteristics of devices having the original SiN passivation step are shown in dotted lines in Fig. 1. After removing their SiN passivation layer, current-collapse phenomena were noticeable, leading to a reduction in $I_{\mathrm{DS\,max}}$ and to an increase in hysteresis effects and knee voltage. After repassivation, in P1 HEMT (no N_2PP), $I_{\mathrm{DS\,max}}$ was almost recovered (Fig. 1(a), solid lines). However, by using N_2PP, P2 devices showed that I_{DS} is increasing about 10% from the initial situation (passivated), and the knee voltage was reduced (Fig. 1(b), solid lines). These results demonstrate a significant reversibility of the standard SiN passivation process and even an improvement using N_2PP, despite the adverse situation of removing SiN with BOE, which could have slightly modified the AlGaN surface, as the results in Fig. 1(a) seem to indicate. To further quantify the effect of the N_2PP, the ratio of I_{DS} for dc and pulsed V_{GS} at $V_{\mathrm{DS}} = 5$ V (current-collapse ratio r^{cc}) was determined at each step. The current collapse was similar $(r^{\mathrm{cc}} \sim 1.2)$ in P1 and P2 transistors having their original standard passivation, increasing this ratio $(r^{\mathrm{cc}} \sim 1.4)$ after removing the SiN. After repassivation with N_2PP, the current collapse in P2 decreased drastically to 29% with respect to the last step, leading to $r^{\mathrm{cc}} = 1.0$, in contrast to the case without it (P1) with a decrease of only 7% $(r^{\mathrm{cc}} \sim 1.3)$.

In addition, the I_{DS} time response in P1 and P2 devices, for gate pulses of various widths and repetition rates, was analyzed. Fig. 2(a) shows the evolution of the steady-state current $(I_{\mathrm{DS}}^{\mathrm{SS}})$ as a function of gate pulsewidth. Pulses from 200 ns caused negligible $I_{\mathrm{DS}}^{\mathrm{SS}}$ changes in P2 (repass with N_2PP). However, in P1 devices (without N_2PP), a significant variation of $I_{\mathrm{DS}}^{\mathrm{SS}}$, around a 22% decrease for 500 μs to narrower pulses, was found. Both results were independent of the V_{DD} bias (6, 10, and 15 V were used). This reduction in $I_{\mathrm{DS}}^{\mathrm{SS}}$ for narrow gate pulses is attributed to the presence of slow traps at the SiN–AlGaN interface, which leads to the observed "gate-lag" and hysteresis effects. The gate-lag ratio, which is defined as the ratio of the maximum pulsed I_{DS} value in steady state to the dc I_{DS} value at $V_{\mathrm{DS}} = 5$ V $(V_{\mathrm{DD}} = 10$ V$)$, is shown in Fig. 2(b) as a function of the pulsewidth. The gate-lag ratio in P1 (without N_2PP) decreases with the pulsewidth from 1 μs, which suggests that charge emission from these traps occurs with time constants above 1 μs. P2 devices (with N_2PP) show constant and much lower gate-lag ratio values, pointing to the presence of a much smaller density of these "slow" traps. Additional transient measurement was made using longer pulsewidths (1 s), showing a time response on the order of 10^2 ms in P1 HEMT.

To compare the presence of traps in samples P1 and P2, the I–V output characteristics were also measured under different

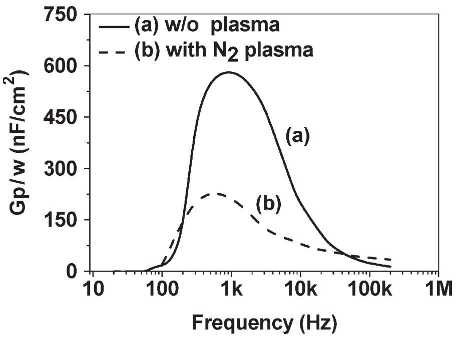

Fig. 3. n-GaN/SiN MIS parallel conductance G_p/w versus frequency (0 V bias) (a) without and (b) with the N_2 plasma pretreatment.

light excitation intensities. In P1 devices, a strong increase of $I_{\rm DS}$ (12%) was observed when light was raised from darkness to full illumination, whereas almost no significant $I_{\rm DS}$ variation in P2 devices was observed. This fact points again to a lower trapped charge density when using the N_2PP.

Comparing the transistors in P3 and P4 samples, results were the same than those from the repassivation study. Transistors passivated using the N_2PP (P4) showed significant improvements in dc, current-collapse behavior, and illumination effects, as compared with the P3 devices (no N_2PP), following the behavior shown in both Figs. 1 and 2.

The effect of the N_2PP seemed not to affect the device isolation, which turned out to be dominated by the passivation layer itself. Moreover, gate-leakage measurements revealed that N_2PP can reduce the gate-leakage current by about two to three orders of magnitude with respect to the standard passivation step (from 7.7 to 2.3×10^{-2} A/cm^2 at $V_{\rm GD} = -20$ V). This positive behavior was observed both in HEMT and in Schottky test diodes (from 8×10^{-3} to 5×10^{-4} A/cm^2 at $V = -20$ V). This seems to indicate that one of the dominant mechanisms in gate current leakage involves surface traps in the gate-drain area, which the N_2PP is able to reduce, in agreement with [10]. Preliminary HEMT RF characterization indicated that no degradation in f_T and $f_{\max}$ (typically, 7 and 22 GHz, respectively) was shown by using the N_2PP, and a small ($\sim$5%) increase in $f_{\max}$ was found.

The GaN MIS structures were electrically characterized by capacitance–voltage (C–V) and conductance–frequency ($G-f$) measurements in order to estimate the influence of N_2PP on the interface charge density. Fig. 3 compares the parallel conductance at $V_G = 0$ V with and without N_2PP. The response time of the traps was around 1 ms, confirming the aforementioned results in HEMT. Additionally, from peak heights, a 65% reduction in interface state density down to 2×10^{12} cm$^{-2} \cdot$ eV^{-1} was observed when the N_2PP is used. These results in the MIS structures are in agreement with those obtained in the AlGaN/GaN HEMT, indicating that low-power N_2PP is able to improve the SiN passivation to further minimize the current-collapse and frequency-dispersion effects, due to the strong reduction of a high native density of trapped charges at the insulator/semiconductor interface.

IV. CONCLUSION

The beneficial effects of *in situ* short-time low-power N_2PP prior to passivating the SiN deposition have been studied in the AlGaN/GaN HEMTs. From their output electrical characteristics, a significant enhancement with respect to not using N_2PP is observed. Pulsed measurements led to a reduction of the current-collapse and gate-lag effects, suggesting that N_2PP was able to reduce the density of slow traps ($\tau \geq 1$ μs) in the active area of the device, which are, at least partially, responsible for the current-collapse effects. This hypothesis was confirmed by illumination measurements and by conductance versus frequency characterization in GaN MIS, where a 65% reduction in interface state density was obtained in the case of using N_2PP. Such a reduction in surface traps by N_2PP would allow an improved HEMT $1/f$ noise performance, with benefits in RF broadband LNA and oscillator performance. Therefore, we deduce that the use of this plasma is able to further mitigate the current-collapse effects, and it is suggested to be included as a complementary step in the passivation process with SiN. XPS—UPS surface-spectroscopy analyses are in progress to clarify the physical–chemical role of this plasma pretreatment.

ACKNOWLEDGMENT

The authors would like to thank M. Pérez and D. López-Romero for their technical assistance and Dr. A. del Prado for valuable comments.

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