Control of D-STATCOM During Unbalanced Grid Faults Based on DC Voltage Oscillations and Peak Current Limitations

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***Abstract*— The safe operation of grid connected power converters during abnormal condition is a key issue in order to guarantee its operation and to avoid undesired trips. In this paper different control strategies for the operation of a D-STATCOM are introduced, where the reference currents are determined in such a way that not only none of the phase currents goes over the limits, but also the DC voltage fluctuations remain in safe operation limit. Fluctuating active power interchange, during unbalanced condition leads to DC voltage oscillation. Severe unbalanced condition and small DC capacitor selection (to meet the size and cost constraints) intensify the DC voltage oscillation. Therefore, the contribution of this paper lays on the combination of the DC voltage oscillations and the current limit control. The effectiveness of three proposed control strategies are verified by simulating a D-STATCOM tied to an industrial distribution network. Moreover a scaled scenario has been reproduced experimentally which shows that the results cope well with the analytical equations and the simulation results.**

Index Terms*— Current control; DC voltage oscillations; D-STATCOM; negative sequence; reactive power; safe operation.

I. INTRODUCTION

Grid codes worldwide are becoming more restrictive day by day [1]. The increasing installation of Distributed Generation Power Supplies (DGPS), based on power converters brings the opportunity of utilizing their unique features. Grid supporting functionalities, even under severe transient conditions, such as grid faults is an outstanding capability of DPGS. Nowadays, when a grid fault occurs, grid connected power converters are required not only to remain connected to the grid but also they must reduce their active power delivery and increase the reactive power injection for supporting the grid [2]. Numerous research works have reported different power control strategies for DGPS or shunt connected power electronics converters, like D-STATCOMs, for operating under abnormal grid conditions[3]-[5]. Since most of the grid faults are unbalanced faults, several research works have done for voltage profile regulation by injecting unbalanced reactive currents to boost the positive sequence voltage as well as minimizing the negative sequence component. Considering the impedance of the Point of Common Coupling (PCC), a control algorithm is proposed for PCC voltage regulation in [6]. The effectiveness of STATCOMs to enhance the stability margin of a fixed speed wind power plants under unbalanced faults is presented in [7]. Three reactive current injection strategies to influence on positive and negative voltage sequences at terminal of wind power plants have developed in [8]. Different strategies for injecting a coordinated combination of positive and negative sequence currents in D-STATCOMs are introduced in [9]-[11]. In a fault condition, the PCC voltage and injected currents are unbalanced. Therefore, the interaction between positive and negative sequences in the voltage and their counterparts in the injected current results in active power fluctuations and consequently DC link voltage oscillations. Regardless of the control strategy objective, a safe operation of the converter from the perspective of maximum instantaneous phase currents, as well as the maximum instantaneous over voltage of DC bus because of fluctuations is critically important. Surpassing either of the aforementioned limits would give rise to an undesired converter tripping. Controlling the maximum phase current of a STATCOM encountering an unbalanced grid faults was introduced in [12]. Respecting the maximum phase current criterion, [13] has studied the maximum active and reactive power delivery of a DGPS. Maximum phase current constraint in low voltage ride through of a DGPS and reactive current injection are respectively presented in [14] and [15]. DC voltage oscillation issue is not addressed in the above mentioned research works.

In association with DC voltage oscillations, the effects of unbalanced supplying voltage on a conventional controlled D-STATCOM and its effects on DC voltage oscillations is discussed in [16]. For a 48 pulse STATCOM responsible for the regulation of positive and negative sequence voltages, [17] proposes to use a single phase inverter, in series with the DC link capacitor for eliminating the DC voltage oscillations during the fault period. Elimination of DC voltage oscillations in a transmission level STATCOM [18] is tackled by introducing a second order term to the angle controller of the converter. DC voltage oscillation reduction in a HVDC system is discussed in [19].

On the other hand, DC link capacitors play an important role

in size, cost and failure rate of the converter. With the industry trend to use high reliable as well as cost effective DC link capacitors, high reliable film capacitors are used extensively [20]. However, for an affordable price, their energy density is low. Optimal DC side capacitor design which copes with stringent reliability and cost constraints moves toward minimization of the capacitor size [21]. In a converter with a reduced size DC link capacitor, the amount of DC voltage oscillations in fault condition is quite high.

Moreover, in a voltage source converter with a fixed modulation algorithm, high amount of oscillations superimposed on the DC voltage, introduce non-characteristics harmonics in the output voltage spectrum [22].

Therefore, it is necessary to involve the DC voltage oscillation constraint in accompany with peak current limitation in calculation of reference current. A control algorithm which considers both criteria, DC bus voltage oscillations limit as well as phase current limitation, has not been studied in deep. Moreover, up to now little work has been done on the limitation of DC voltage of D-STATCOMs facing severe unbalanced situations. In this research, three strategies of reactive power injection are introduced which fulfill not only the phase current limitation but also DC voltage oscillation constraint, to ensure a secure operation of D-STATCOM while riding through the fault.

This work is an extended version of [23] with further simulations and more discussion.

This three reactive power injection strategies are named: Average Active Reactive Control(AARC), Balanced Positive Sequence Control (BPSC) and Positive Negative Sequence Control (PNSC).

For each strategy, a couple of reactive power reference values are calculated which satisfy the peak current limitation and maximum DC voltage oscillations criteria respectively. By comparing this reference values, the final reactive power reference is chosen, which will respect both the DC voltage oscillation and peak current limitation.

The organization of the paper is as follows. Section II discusses the basics of the three different reactive power control strategies. The derivation of active power fluctuations and consequence DC voltage oscillations are presented in section III. Section IV is devoted to calculation of maximum phase currents. The overall control system is discussed in section V and the performance of a D-STATCOM, connected to a weak industrial network experiencing fault condition is analyzed in section VI. Finally the experimental evaluation of a laboratory scaled D-STATCOM considering both limiting criteria is shown in section VII, just before the conclusions.

II. Different Reactive Power Control Strategies

In an arbitrary three phase network with unbalanced variables $f \in \{v, i\}$ and supposing a three wire system as well as the availability of a Δ connection in one of the windings of interfacing transformer, as shown in Fig. 1, the zero sequence voltages and currents at the point of

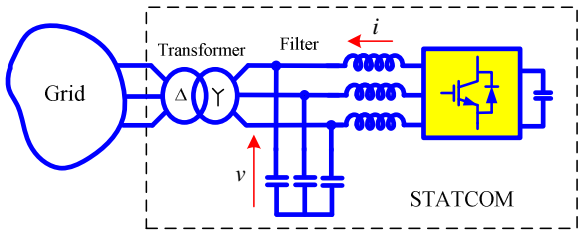

Fig. 1. Structure of a D-STATCOM connected to the grid

connection of the converter to the grid will be eliminated. Therefore, by using a constant amplitude Clark Transformation, we can write:

$$\begin{bmatrix} f_\alpha(t) \\ f_\beta(t) \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ 0 & 1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix} \begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} \quad (1)$$

where $f_i(t), i \in \{a, b, c\}$ are phase variables (voltages and currents), furthermore each variable in stationary reference frame can be decomposed into a couple of balanced sets of positive(+) and negative($-$) variables as shown below:

$$f_\alpha(t) = f_\alpha^+(t) + f_\alpha^-(t) \quad (2)$$

$$f_\beta(t) = f_\beta^+(t) + f_\beta^-(t) \quad (3)$$

In fact, it is very common to use a couple of in-quadrature 90^o shifted vectors to develop the reactive power definition:

$$f_{\perp\alpha}(t) = f_{\perp\alpha}^+(t) - f_{\perp\alpha}^-(t) \quad (4)$$

$$f_{\perp\beta}(t) = f_{\perp\beta}^+(t) - f_{\perp\beta}^-(t) \quad (5)$$

Fig. 2 represents system variables in the stationary reference frame. $\boldsymbol{F}$ is the rotating space vector and $\boldsymbol{F}_\perp$ is its in-quadrature counterpart. $\boldsymbol{F}^+$ and $\boldsymbol{F}^-$ are the positive and negative sequence components respectively.

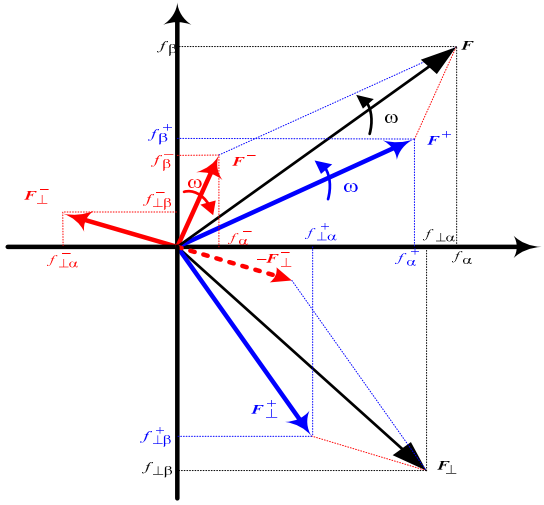

Fig. 2. Vector representation in stationary reference frame

According to Fig. 2, the time expressions for the positive and the negative sequences for both the real and in-quadrature vectors can be written as:

$$\begin{bmatrix} \boldsymbol{F}^{+}(t) \\ \boldsymbol{F}^{-}(t) \\ \boldsymbol{F}_{\perp}^{+}(t) \\ \boldsymbol{F}_{\perp}^{-}(t) \end{bmatrix} = \begin{bmatrix} f_{\alpha}^{+}(t) \\ f_{\alpha}^{-}(t) \\ f_{\perp\alpha}^{+}(t) \\ f_{\perp\alpha}^{-}(t) \end{bmatrix} + j. \begin{bmatrix} f_{\beta}^{+}(t) \\ f_{\beta}^{-}(t) \\ f_{\perp\beta}^{+}(t) \\ f_{\perp\beta}^{-}(t) \end{bmatrix} = \begin{bmatrix} F^{+}.\cos(\omega t + \theta_f^{+}) \\ F^{-}.\cos(-\omega t + \theta_f^{-}) \\ F^{+}.\cos(\omega t + \theta_f^{+} - \frac{\pi}{2}) \\ F^{-}.\cos(-\omega t + \theta_f^{-} - \frac{\pi}{2}) \end{bmatrix} + j. \begin{bmatrix} F^{+}.\cos(\omega t + \theta_f^{+} - \frac{\pi}{2}) \\ F^{-}.\cos(-\omega t + \theta_f^{-} - \frac{\pi}{2}) \\ F^{+}.\cos(\omega t + \theta_f^{+} - \pi) \\ F^{-}.\cos(-\omega t + \theta_f^{-} - \pi) \end{bmatrix} \quad (6)$$

In case of using constant amplitude Clark Transformation, active and reactive powers can be written as:

$$p = (\frac{3}{2})\mathbf{v}.\mathbf{i} \quad (7)$$

$$q = (\frac{3}{2})\mathbf{v}_{\perp}.\mathbf{i} \quad (8)$$

where $\mathbf{v}$, $\mathbf{v}_{\perp}$ and $\mathbf{i}$ are voltage , in-quadrature voltage and current vectors respectively.

In Average Active Reactive Control (AARC) strategy, active and reactive current components are oriented across the voltage space vector and its in-quadrature vector respectively. The modulus of $\mathbf{v}$ and $\mathbf{v}_{\perp}$ remain constant throughout grid period. Orientation of reference current across the positive sequence voltage leads to a balanced current injection in Balanced Positive Sequence Control (BPSC). A set of unbalanced currents are injected to the grid in Positive Negative Sequence Control (PNSC). The reference current vector is directed in a way that cancel out the oscillations in the instantaneous powers injected into the grid. Details of AARC, BPSC and PNCS schemes and their characteristics are given in [24] and the reference currents are shown in Table I. P^{*} and Q^{*} are active and reactive power set points and V^{+} and V^{-} are the voltage positive and negative sequence amplitudes respectively.

Table I. Reference current vectors for different power injection schemes

Scheme	Reference Current Vector
AARC	$\mathbf{i}^{*} = \frac{(2/3)P^{*}}{(V^{+})^{2} + (V^{-})^{2}}\mathbf{v} + \frac{(2/3)Q^{*}}{(V^{+})^{2} + (V^{-})^{2}}\mathbf{v}_{\perp}$ (9)
BPSC	$\mathbf{i}^{*} = \frac{(2/3)P^{*}}{(V^{+})^{2}}\mathbf{v}^{+} + \frac{(2/3)Q^{*}}{(V^{+})^{2}}\mathbf{v}_{\perp}^{+}$ (10)
PNSC	$\mathbf{i}^{*} = \frac{(2/3)}{(V^{+})^{2} - (V^{-})^{2}}[P^{*}(\mathbf{v}^{+} - \mathbf{v}^{-}) + Q^{*}(\mathbf{v}_{\perp}^{+} + \mathbf{v}_{\perp}^{-})]$ (11)

III. Effect of Different Reactive Power Control Strategies on DC Bus Voltage Oscillations

This section is devoted to the calculation of active power fluctuations in the three aforementioned reactive power control strategies considering unbalanced voltage condition. Furthermore, a step by step derivation of the DC voltage oscillations, based on the principle of energy conservation is presented. Finally, some hints for proper DC capacitor selection are presented.

A. Active Power Fluctuations

According to the instantaneous power theory [25], the active power fluctuations at the terminal of a power converter could be written as:

$$\tilde{p}(t) = (3/2)(v_{\alpha}^{+}i_{\alpha}^{-} + v_{\alpha}^{-}i_{\alpha}^{+} + v_{\beta}^{+}i_{\beta}^{-} + v_{\beta}^{-}i_{\beta}^{+}) \quad (12)$$

For extracting the voltage sequence components used in (12), the main principles of several research works, such as [26] is considered.

It could be inferred from (12) that the active power fluctuation is a consequence of the different sequence voltages and currents interaction. In other words, for a balanced voltage and pure balanced positive sequence current injection, there is no power fluctuation. At the other extreme, when the voltage is balanced and the converter only injects a negative sequence current to the grid, the amplitude of the power fluctuations reaches its maximum value. The major part of converter current is allocated to negative sequence current. Hence, the 2nd and 4th terms in (12) are negligible. In contrast, 1st and 3rd terms are significant and the power fluctuation reaches its maximum. This condition is very probable when the D-STATCOM works in a load current balancing mode. Under unbalanced grid fault conditions, when the D-STATCOM works in grid voltage supporting mode, positive sequence voltage is always higher than the negative sequence voltage, therefore, the strategies which inject more negative sequence current, produces higher active power fluctuations.

In (12) the current components are generated by the control block with respect to the reactive power injection scheme. Reference currents for each aforementioned strategy could be achieved by inserting the arbitrary voltages of (6) into (9)-(11). The D-STATCOM ohmic losses compared with its rated V.A is insignificant so the reference active power is almost zero ($P^{*} \approx 0$). Inserting the calculated reference currents as well as the voltage components in (12), the active power fluctuations for different schemes are introduced in Table II, where λ is the Voltage Unbalance Factor (VUF) as a measure of severity of voltage imbalance which is defined as:

$$\lambda = V^{-}/V^{+} \quad (13)$$

Regardless of the AARC that presents no fluctuations in active power, two later schemes experience a 2nd order component fluctuations with the amplitudes influenced from reactive power set points and the voltage unbalance factor.

Table II. Active power fluctuations for different schemes

Scheme	Active Power Fluctuations	
AARC	$\tilde{p}(t)=0$	(14)
BPSC	$\tilde{p}(t)=\lambda.Q^{*}\sin(2\omega t+\theta_v^{+}-\theta_v^{-})$	(15)
PNSC	$\tilde{p}(t)=\frac{2Q^{*}.\lambda}{1-\lambda^{2}}\sin(2\omega t+\theta_v^{+}-\theta_v^{-})$	(16)

B. DC Capacitor Voltage Oscillations

Neglecting the converter losses and according to the energy conservation theory, the DC link power absorption ($p_c(t)$) is the same as the input power, therefore:

$$p_c(t)=\tilde{p}(t) \tag{17}$$

The DC link capacitor voltage is:

$$v_c(t)=\overline{V}_c+\tilde{v}_c(t) \tag{18}$$

where this voltage is a composition of a constant component ($\overline{V}_c$) and a fluctuating component($\tilde{v}_c(t)$), as a result:

$$p_c(t)=v_c(t).i_c(t)=v_c(t).C\frac{dv_c(t)}{dt} \tag{19}$$

by substituting (18) in (19) :

$$p_c(t)=C(\overline{V}_c.\frac{d\tilde{v}_c(t)}{dt}+\tilde{v}_c(t).\frac{d\tilde{v}_c(t)}{dt})\approx C.\overline{V}_c.\frac{d\tilde{v}_c(t)}{dt} \tag{20}$$

in the above equation, the second term in comparison to the first one is negligible therefore, by integrating (20) an equation for the DC voltage oscillations is attained:

$$\tilde{v}_c(t)=\frac{1}{C.\overline{V}_c}\int p_c(t)dt=\frac{1}{C.\overline{V}_c}\int\tilde{p}(t)dt \tag{21}$$

DC voltage oscillations, proportionally relate to the active power fluctuations. In contrast, higher the DC voltage value or capacitance, lower is the DC voltage oscillations.

Using (14)-(16) in (21), a superimposed second order oscillations on the average DC value for all the aforementioned control schemes are listed in Table III.

It is clear that the higher voltage unbalance factor, the higher is the DC voltage deviation. The deviation above the average value is more important than the undergoing voltage. Overvoltage has detrimental effects on the semiconductor switches and the DC link capacitor, might actuate the DC over voltage protection unit.

Table III. DC voltage oscillations for different schemes

Scheme	DC Voltage Oscillations	
AARC	$\tilde{v}_c(t)=0$	(22)
BPSC	$\tilde{v}_c(t)=\frac{-Q^{*}.\lambda}{2\omega.C\overline{V}_c}\cos(2\omega t+\theta_v^{+}-\theta_v^{-})$	(23)
PNSC	$\tilde{v}_c(t)=\frac{-Q^{*}.\lambda}{\omega.C\overline{V}_c(1-\lambda^{2})}\cos(2\omega t+\theta_v^{+}-\theta_v^{-})$	(24)

For a specified permissible DC overvoltage, the maximum reactive power can be determined. DC voltage oscillations amplitude for a typical 4MVA D-STATCOM, delivering rated and 50% of rated V.A, with respect to the voltage unbalanced factor is presented in Fig. 3. It is vividly shown that if the reactive power reference is not reduced the DC voltage deviation would not be tolerated. Beside, the active power fluctuations is not occurred in AARC strategy and it is the finest strategy for preventing the DC voltage oscillations. On the other hand, PNSC strategy suffers from high DC voltage deviation in large VUFs and if the reactive power set-point is not reduced properly it might result in converter tripping.

C. DC Capacitor Selection to Meet the Criteria

The main criteria for DC capacitor sizing is to be sure about the D-STATCOM capability in the regulation of voltage during transients. Different research works have presented different methods for sizing the capacitor with regards to transient performance requirements [27]-[28]. However, fault ride through performance of the D-STATCOM and the effect of capacitor size on the DC voltage oscillations is not considered in previous works. The main principle for all the methods used

for capacitor sizing lays on the fact that the change in the capacitor's stored energy should be equal to a multiplication of the D-STATCOM rated power (S_{rated}) by a specified period of time, e.g. 0.5-1 cycle. A typical relation is :

$$\frac{1}{2}C(\overline{V}_{c,\max}^{2}-\overline{V}_{c,\min}^{2})=k_s.S_{rated}.T_{tran} \tag{25}$$

where $\overline{V}_{c,\max}$ and $\overline{V}_{c,\min}$ are the maximum and the minimum permissible values for DC voltage. k_s is a coefficient that determines the share of D-STATCOM contribution for a specific transient time, T_{tran} .

For limiting the amplitude of the DC voltage oscillations, a level of immunity could be defined like:

$$\left|\tilde{v}_c(t)\right|\le k.\overline{V}_c \tag{26}$$

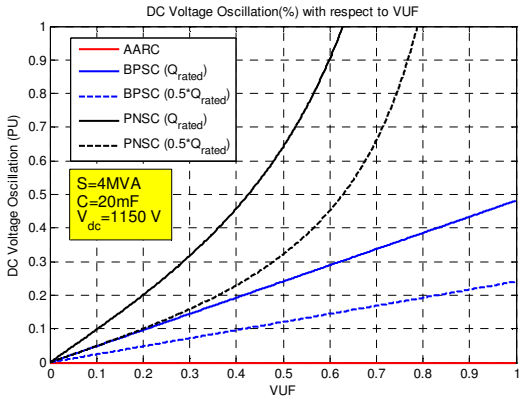

Fig. 3. DC voltage oscillations of a typical 4MVA D-STATCOM

where $\left|\tilde{v}_c(t)\right|$ is the amplitude of DC voltage oscillations and k is the allowed percentage of nominal DC voltage.
In the AARC strategy, DC voltage oscillations are zero and the value of capacitance is derived from (25). By inserting the oscillations amplitude from (23) in (26), the minimum capacitance to meet DC voltage oscillations for BPSC is:

$$C \geq \frac{Q^*.\lambda}{2\omega.k.\overline{V}_c^2} \tag{27}$$

In the same way by combining (24) and (26) for PNSC, the minimum capacitance value is calculated as:

$$C \geq \frac{Q^*.\lambda}{\omega.k.\overline{V}_c^2(1-\lambda^2)} \tag{28}$$

It is evident that the capacitance value inversely relate to square value of the DC voltage. Furthermore, the capacitance is a function of voltage unbalanced factor (λ). The maximum value of the calculated capacitance among (25) and (27)-(28), meets both the transient response requirement as well as limitation of DC voltage oscillations. Considering size and cost constraints, selecting a capacitor that maintains the amplitude of 2nd order oscillations below the level of immunity for all values of λ is not sensible. Therefore, in the design stage, the capacitor is sized for an assumed maximum value of λ . If in practice an unbalanced condition with larger λ appears, the controller calculates the reference reactive power in a way that DC voltage oscillation does not surpass the immune value.

IV. Maximum Phase Current in Different Reactive Power Control Strategies

Considering an unbalanced voltage condition, if the reactive power set point is not reduced, it is likely that currents in one or more phases pass over their nominal values and the over current protection of the converter would be activated. This section concentrates on the derivation of new reactive power set point for each strategy in which the maximum of phases currents kept in a safe region according to the nominal current.
Assuming a set of arbitrary equation for phase currents in natural (abc) frame as:

$$\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} = \begin{bmatrix} I_a\cos(\omega t+\varphi_a) \\ I_b\cos(\omega t+\varphi_b) \\ I_c\cos(\omega t+\varphi_c) \end{bmatrix} \tag{29}$$

for each strategy the magnitude of maximum phase current according to the positive and negative sequence voltage components are extracted and then the permissible amount of reference reactive power is calculated.

A. Maximum Phase Current for AARC Strategy

Considering (9), the reference current for AARC is:

$$\mathbf{i}^* = \begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = b_1.\begin{bmatrix} v_{\perp\alpha} \\ v_{\perp\beta} \end{bmatrix} = b_1.\begin{bmatrix} v_\beta \\ -v_\alpha \end{bmatrix} = b_1.\begin{bmatrix} v_\beta^+ + v_\beta^- \\ -v_\alpha^+ - v_\alpha^- \end{bmatrix} \tag{30}$$

where b_1 is an instantaneous susceptance and defined as:

$$b_1 = \frac{(2/3)Q^*}{(V^+)^2+(V^-)^2} \tag{31}$$

putting the time domain positive and negative voltage components from (6) in (30), magnitude of maximum phase current are calculated as:

$$I_a = b_1\sqrt{(V^+)^2+(V^-)^2+2V^+V^-\cos(\delta+\pi)} \tag{32}$$

$$I_b = b_1\sqrt{(V^+)^2+(V^-)^2+2V^+V^-\cos(\delta-\pi/3)} \tag{33}$$

$$I_c = b_1\sqrt{(V^+)^2+(V^-)^2+2V^+V^-\cos(\delta+\pi/3)} \tag{34}$$

where $\delta = \theta_v^+ + \theta_v^-$ which is available at the output of sequence extraction block. The maximum safe amplitude of the phase currents is the nominal one. For a specific unbalanced condition the maximum permissible reactive power in which none of the phase currents surpass the limitation could be determined. By inserting (13) and (31) in (32) to (34), the maximum allowed reactive power as a function of positive sequence voltage and VUF could be obtained. This relation is presented in Fig. 4 for $\delta = 0$. It is clear that in case of faulty condition the reactive power set point must be decreased to maintain the phase current less than the rated values. It is worth mentioning that some of the point in this graph are not achievable in practice.

B. Maximum Phase Current for BPSC Strategy

The reference current for BPSC strategy is inspired from (10) and is expressed as:

$$\mathbf{i}^* = \begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = b_2.\begin{bmatrix} v_{\perp\alpha}^+ \\ v_{\perp\beta}^+ \end{bmatrix} = b_2.\begin{bmatrix} v_\beta^+ \\ -v_\alpha^+ \end{bmatrix} \tag{35}$$

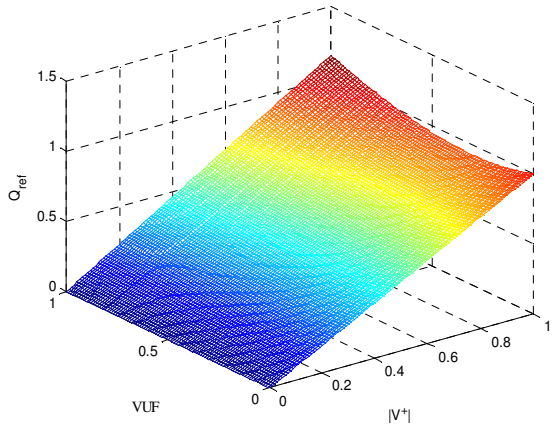

Fig. 4. Maximum permissible reactive current set point in AARC strategy

where b_2 is defined as:

$$b_2 = \frac{(2/3)Q^*}{(V^+)^2} \tag{36}$$

In this strategy all the phases have same amplitude which is calculated as:

$$I_a = I_b = I_c = \frac{(2/3)Q^*}{V^+} \tag{37}$$

From (37) it could be inspired that for keeping the phase currents safely to rated value, the maximum reference reactive power must be reduced in proportion of V^+.

C. Maximum Phase Current for PNSC Strategy

According to (11), in PNSC strategy the current controller must track the following reference current:

$$\mathrm{i}^* = \begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = b_3 . \begin{bmatrix} v_{\perp\alpha}^+ + v_{\perp\alpha}^- \\ v_{\perp\beta}^+ + v_{\perp\beta}^- \end{bmatrix} = b_3 . \begin{bmatrix} v_\beta^+ + v_\beta^- \\ -v_\alpha^+ - v_\alpha^- \end{bmatrix} \tag{38}$$

where b_3 is defined as:

$$b_3 = \frac{(2/3)Q^*}{(V^+)^2 - (V^-)^2} \tag{39}$$

By applying components of (6) in (38) and applying reverse Clark transformation, the phase current amplitudes are obtained as:

$$I_a = b_3\sqrt{(V^+)^2 + (V^-)^2 + 2V^+.V^- \cos(\delta)} \tag{40}$$

$$I_b = b_3\sqrt{(V^+)^2 + (V^-)^2 + 2V^+.V^- \cos(\delta + 2\pi/3)} \tag{41}$$

$$I_c = b_3\sqrt{(V^+)^2 + (V^-)^2 + 2V^+.V^- \cos(\delta - 2\pi/3)} \tag{42}$$

Assuming $\delta = 0$ and combining (13) with (40)-(41) results in Fig. 5 which presents the drop of reference reactive power as a function of voltage unbalanced condition for PNSC strategy.

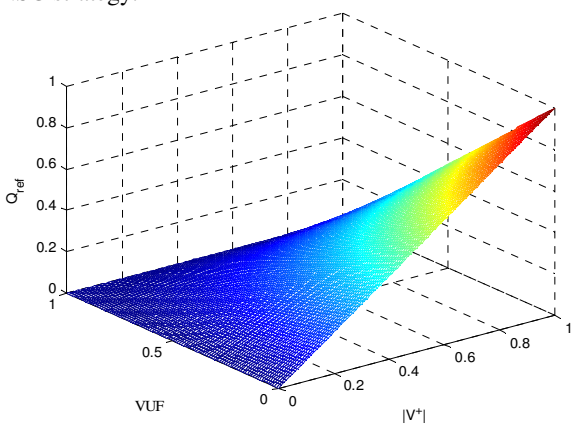

Fig. 5. Maximum permissible reactive current set point in PNSC strategy

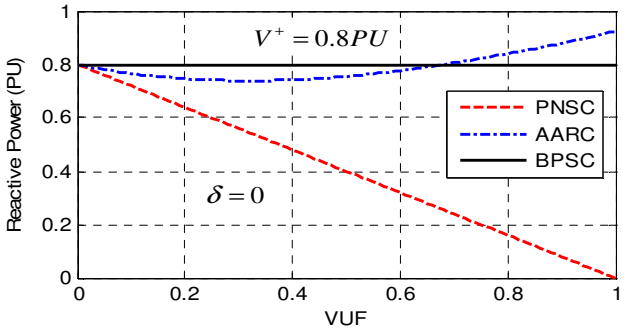

Fig. 6. Permissible safe operating reactive power reference comparison

For a similar amount of voltage dip ($V^+ = 0.8\ PU$), Fig. 6 visually has compared the maximum permissible reactive power for aforementioned three strategies.

It is clear that in case of PNSC strategy, as the VUF increases, the average reactive power descends in order to keep the phase current in a safe band. In contrast, as BPSC strategy does not care about VUF, it decreases the reactive power proportional to the positive sequence voltage. In case of AARC the drop of reference power is more than BPSC in low VUFs but for severe VUFs the average reference reactive power is higher for AARC. It should be mentioned that for different values of δ, the pattern of the reactive power remains approximately the same for different strategies, similar to Fig. 6.

V. Overall Control Scheme

The overall control system is built up with the aggregation of voltage limitation and safe current injection limitation as a unified controller that not only cares about peak current limitation but also DC voltage oscillations as well.

A simplified block diagram of the proposed control strategy is shown in Fig. 7. A voltage sequence extraction block based on Double Second Order Generalized Integrator (DSOGI) accompanied by a Frequency Locked Loop (FLL) presented in [29] is responsible for the positive and negative sequence voltage extraction in stationary reference frame.

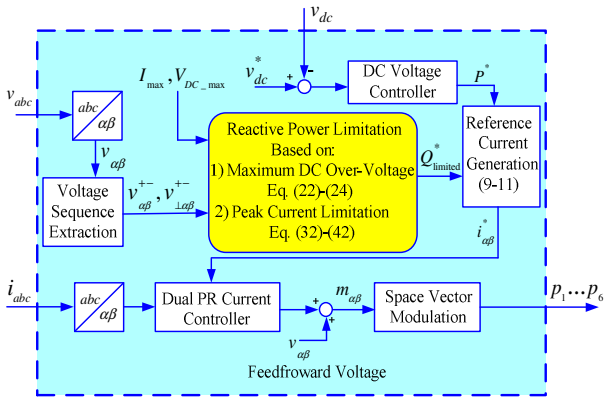

Fig. 7. Block diagram of the D-STATCOM control

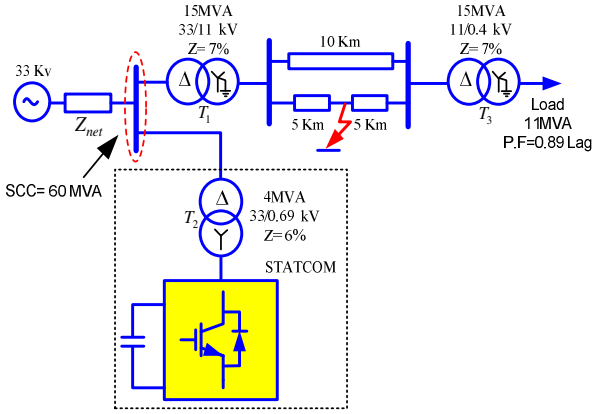

Fig. 8. Connection of a D-STATCOM to a distribution grid

The DC voltage of the capacitor is kept on its nominal average value via a DC voltage control loop. For a fast and accurate tracking of the generated reference currents a couple of Proportional-Resonant (PR) controllers as well as a feed-forward voltage from the point of common coupling (PCC) is embedded in the controller. Space Vector Modulation (SVM) is utilized to generate the gating pulses of the switches in a two level inverter.

VI. Performance Simulation of D-STATCOM in a Weak Distribution Grid

To validate the behavior of the proposed control strategy, the operation of a 4MVA D-STATCOM in a weak distribution grid which is shown in Fig. 8, is analyzed.

The DC link nominal voltage and capacitance are 1150V and 20mF respectively. In this study case, when the converter is supplying a 0.17 PU reactive power, a Single Line to Ground (SLG) fault happens in the middle of one of the parallel lines. The behavior of DC voltage, active and reactive powers and their maximum deviations for all the three aforementioned control strategies are presented in Fig. 9. As it can be seen, there is a good matching between the analytical calculations shown in Table IV and the oscillations captured in Fig. 9.

Maintaining the peak current and the DC voltage in their secure operation regions is introduced in Fig. 10.

It can be seen that in this fault scenario the current limit criterion reach faster than the overvoltage limit in the DC bus. The type of fault as well as its location leads to different unbalance characteristics.

Based on unbalance characteristics, either of maximum phase current limitation or DC voltage limitation criteria could arise first.

Table IV. Analytical expectation for amplitude of active power fluctuations and DC voltage oscillations

	AARC	BPSC	PNSC
$\lvert \tilde{p}(t) \rvert$	$\simeq 0$	0.64 MW	1.142 MW
$\lvert \tilde{v}_c(t) \rvert$	$\simeq 0$	44.4 V	79.4 V

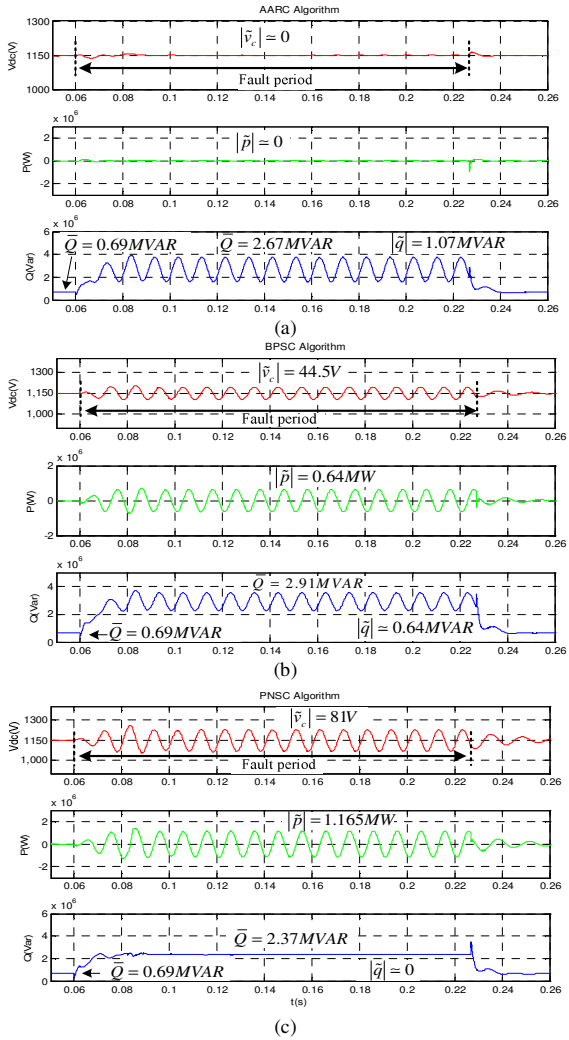

Fig. 9. DC voltage oscillations and active /reactive powers for a) AARC, b) BPSC, c)PNSC strategies

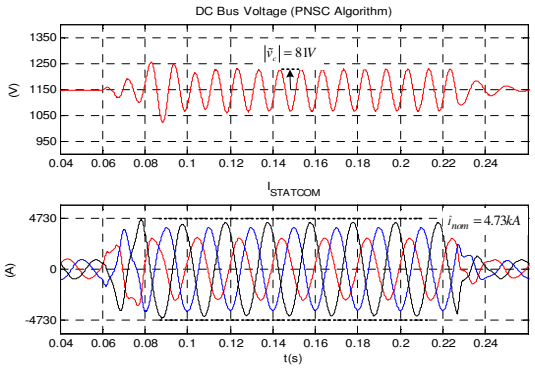

Fig. 10. DC voltage and phase currents are kept in a secure range

Fig. 11 presents the results of happening a SLG fault at the sending end of parallel lines. In this unbalanced scenario, the reactive power set point is dominated by DC voltage limiting sub-algorithm. The maximum permissible DC

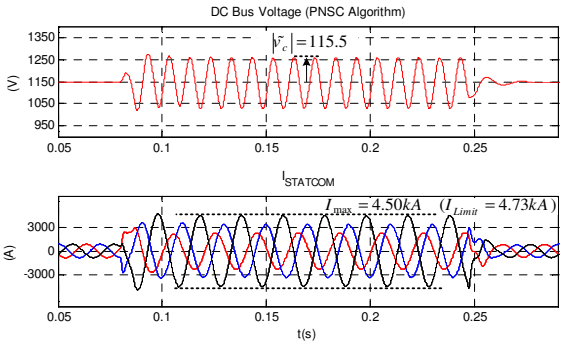

Fig. 11. DC voltage limitation reach faster than phase currents limitation. SLG fault happens at the sending end of the lines

voltage oscillation (k=10% and $|\tilde{v}_c| = 115.5$) is reached but, the maximum of phase current(4.5kA) is less than the limiting value (4.73kA).

VII. Experimental Results

The proposed control strategies are implemented in dSPACE DS1103 platform and applied to a 5KVA ,400V inverter with a 700V DC bus and DC capacitance of 4.7mF. The switching frequency is chosen to be 10kHz. The experimental platform is demonstrated in Fig. 12.

The performance of the control strategies, considering the DC voltage and phase current limitations, are evaluated facing a D type voltage sag. Utilizing a power amplifier commanded from OPAL-RT real time simulator a D-type voltage sag with a characteristics of $0.3\angle -35°$ is applied to the terminal of the converter. The voltage sag occurred when the converter was delivering 3KVAR (7A peak current) to the grid.

Fig. 13 shows the unbalanced voltage and the injected currents when using the AARC strategy and Fig. 14 is presenting the active power, reactive power as well as DC voltage oscillations in this strategy. During the fault, the phase which experiences more dip has the maximum current and current peaks do not surpass the maximum set point (7A here).

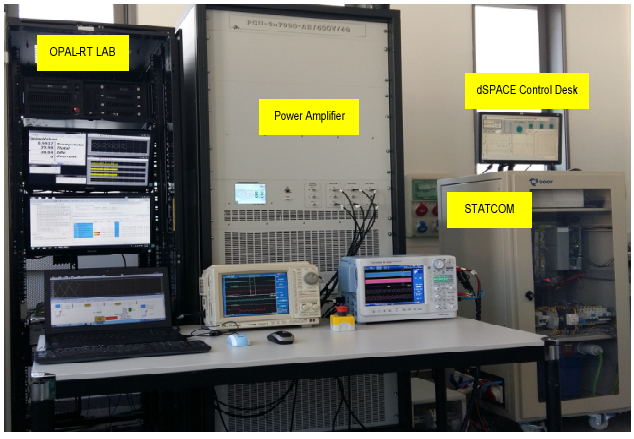

Fig. 12. Experimental platform

There is no fluctuation in active power and no oscillation in DC voltage either. The reference reactive power decreased from 3KVA to 1.7KVA which is superimposed by a 100Hz oscillations. Fig. 15 and Fig. 16 are belonging to BPSC strategy.

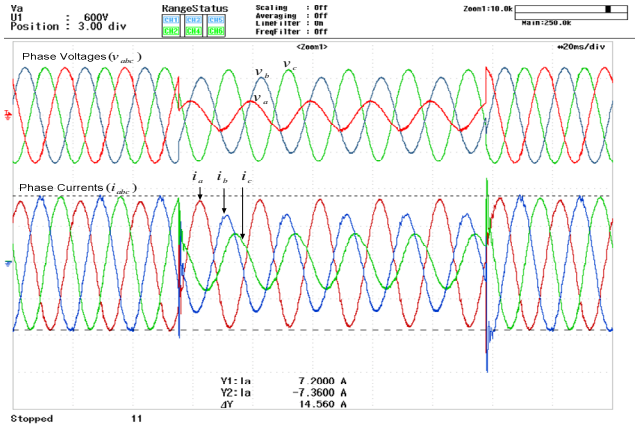

Fig. 13. PCC voltage and injected currents in AARC strategy

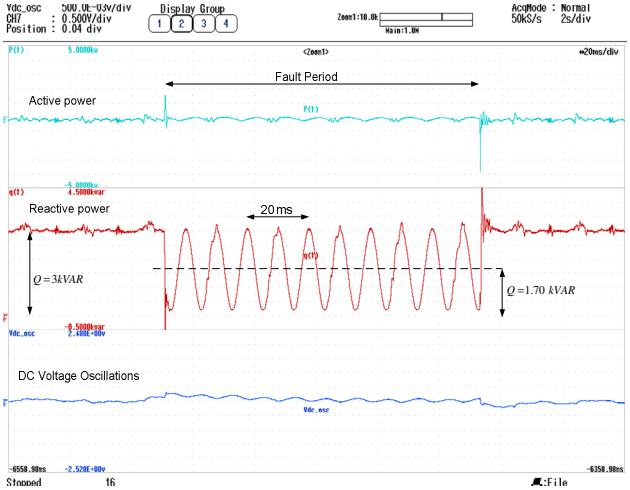

Fig. 14. Active / Reactive power and DC voltage oscillations in AARC

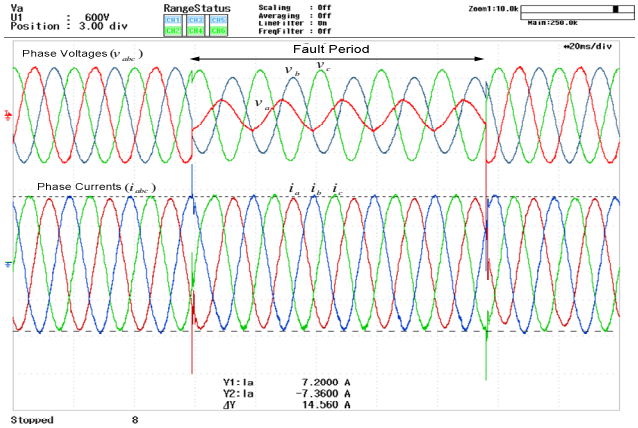

Fig. 15. PCC voltage and injected currents in BPSC strategy

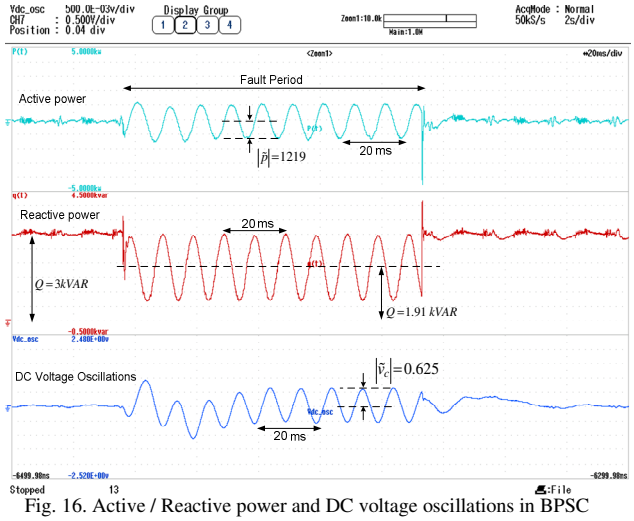

Fig. 16. Active / Reactive power and DC voltage oscillations in BPSC

During the unbalanced voltage condition, phase currents are balanced and are limited to the rated current but as a consequence double frequency oscillations appeared in both active and reactive powers. The behavior of PNSC strategy is shown in Fig. 17 and Fig. 18. As it can be seen, again currents are bounded in a safe region. In this strategy for the sake of oscillation cancellation in the reactive power, the reference currents are determined in such a way that the phase with lowest voltage dip sinks the most current.

Analyzing the DC voltage oscillations for all three strategies, it can be seen that they meet the expectations inspired by Fig. 3. DC voltage oscillations are almost eliminated in AARC and are the most significant in PNSC.

Converter loss influence on the analytical expectation for DC voltage oscillations amplitude is evaluated in Table V.

The mismatch between analytical expectation and experimental results is originated from the converter loss. In BPSC, all the phases carry the rated current but it is not the case for PNSC. Therefore, converter loss in PNSC is less than BPSC and the mismatch is very small.

In contrast to a laboratory scaled converter, a real high power D-STATCOM has higher efficiency and with a good accuracy the losses can be ignored and thus the mismatch is even smaller.

On the other side, the values of reactive power reference in Fig. 14, Fig. 16 and Fig. 18 are in good agreement with Fig. 6. It could be deduced that among these three reviewed strategies, BPSC is the best in keeping the reference power as higher as possible. From this insight, AARC treats very close to BPSC but the reference reactive power in PNSC descends drastically as an unbalanced voltage condition occurs.

Table V. Amplitude of DC voltage oscillation in analytical and experimental study

	AARC	BPSC	PNSC
Analytical Expectation (mV)	0	590	751
Experimental Results (mV)	≃ 0	625	770
Mismatch (%)	≃ 0	5.9	2.6

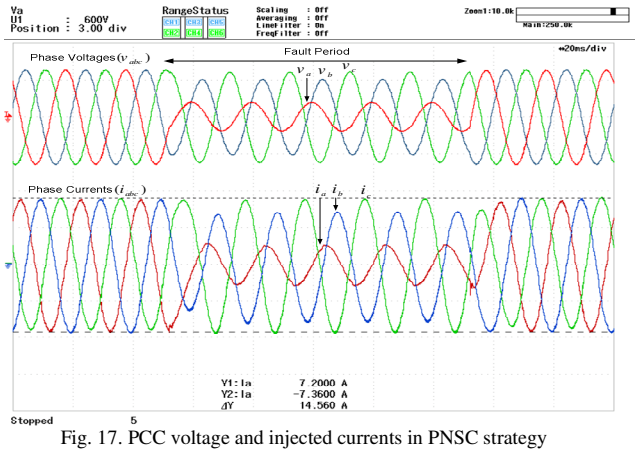

Fig. 17. PCC voltage and injected currents in PNSC strategy

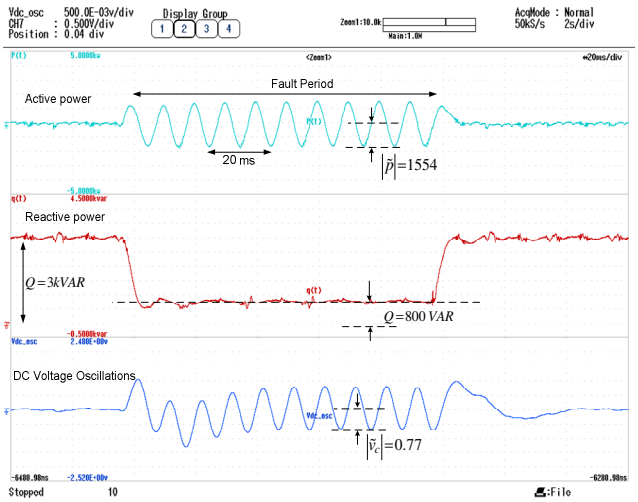

Fig. 18. Active / Reactive powers and DC voltage oscillations in PNSC

Moreover, according to (9) the reference current vector in AARC is oriented in a way that consequences in negative sequence voltage reduction. On the other hand, the injected current in PNSC strengthen the negative sequence voltage.

Table VI gives a comparison between three introduced strategies and depicts their capabilities.

Table VI. Comparison of the proposed strategies

strategy	Reactive Power Injection	DC Voltage Oscillation Limitation	Negative Sequence Voltage Reduction
AARC	Intermediate	Superior	Superior
BPSC	Superior	Intermediate	Intermediate
PNSC	Inferior	Intermediate	Inferior

Considering all the objectives of minimum DC voltage oscillations, maximum reactive power delivery as well as negative sequence voltage reduction, AARC is recognized as the best.

VIII. CONCLUSION

In this work, safe operation of grid connected converters with regards to peak current limitation as well as maximum permissible DC voltage oscillations is discussed. The main effort is concentrated on analyzing of the DC voltage oscillations.

Toward this goal, a set of mathematical expressions is developed which prepares a good insight to active power fluctuations (which results in the DC voltage oscillations) as well as maximum current limitation for three different strategies. Deduced analytical expressions are validate by simulations as well as experimental tests and there is a good agreement between them.

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