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DESIGN OF A CONDITIONING CIRCUIT FOR MAGNETIC CMOS-MEMS SENSORS

A Master's Thesis

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by

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Abstract

This thesis report describes the design process of two different analog circuits required to perform the readout of a CMOS-MEMS Magnetometer based on the Lorentz Force Effect.

The designed circuits are the Low Noise Amplifier (LNA) that performs the conditioning of the sensor response and the Programmable Floating Current Source needed to induce the Lorentz Force in the sensor. Both circuits are meant to be integrated on-chip with the magnetometer and fabricated with a 180 nm CMOS technology provided by Taiwan Semiconductor Manufacturing Company (TSMC).

The result of the design is a Fully Differential Operational Transconductance Amplifier based on a Folded Cascode Topology with 10 nV/$\sqrt{\text{Hz}}$ of input referred noise and a Floating Current Source with a 3-bit programmability which allows different current values from 8 µA to 1 mA. In the case of the LNA, the design is made at both schematic and layout level with a final area of 368 µm x 136 µm, which represents a 44% of the sensor's surface (615 µm x 182 µm).

As for the Programmable Current Source, the design was made at schematic level and its estimated area is 103 µm x 103 µm, a 9.5% of the sensor's.

Furthermore, during the design of the differential LNA, a low consumption alternative to enhance the linearity of the Common Mode Feedback (CMFB) loop was found. With this approach, based on a source degeneration of the differential pair, an error amplifier with low consumption, 53.3 µA, was achieved.

Finally, an optimal value for the degeneration resistor was found when linearizing the CMFB loop. As a result, a SFDR of 80dB was obtained.

Acknowledgements

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1. Introduction

1.1. Current State of CMOS MEMS

During the last years, the use of MEMS for micro-scale sensors and actuators has grown up to a point in which they are now prevalent in our daily life [1]. Smart phones, automobiles, inkjet printers, planes, video consoles are just a few examples of common commercial application that include MEMS. Moreover, its market value is expected to reach 18.880 million U.S. dollars by 2022 [2].

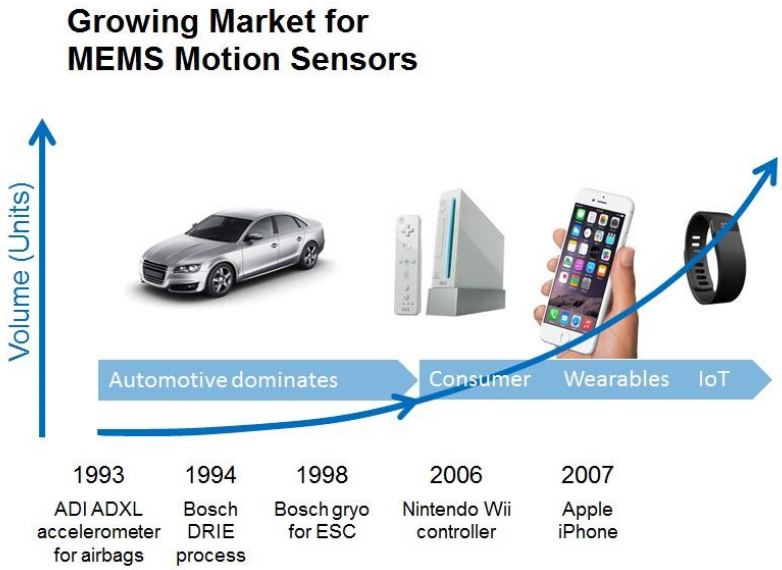


Figure 1.1: Market Growth of MEMS over the years expanding from the automotive industry to wearables like smartphones [3]

Micro-Electro-Mechanical Systems (MEMS) are micrometer-scale systems with both mechanical and electrical devices. Due to their reduced size and their electrical behaviour, one actual approach to fabricate them is using CMOS (Complementary Metal Oxide Semiconductor).

About CMOS, it is a mainstream technology since it is the predominant process used to fabricate integrated circuits (IC). Some advantages that MEMS could take from this technology are:

- The improvements in terms of yield and reliability that CMOS has acquired over the years.
- The possibility of integrating additional on-chip circuitry near the MEMS device too [4].

When both MEMS and the electronics are fabricated with CMOS technology and are included inside the same chip, the term CMOS MEMS is often used to describe them [4].

Some examples of typical CMOS MEMS sensors are pressure sensors, inertial sensors, frequency reference devices [1] and magnetometers, which are the ones that we are considering for the design of our conditioning circuit.

The tradeoff in CMOS-MEMS is that in general it is not possible to modify the materials since manufacturers' purpose is to implement the electronic devices, not the micromechanical ones.

1.2. Description of the Magnetometer

The magnetometer considered in this thesis can be regarded as a parallel-plate capacitor where one of the plates is fixed and the other is movable (Figure 1.2). Equation (1.1) shows the dependency with the distance between plates and their capacitance.

$$C = \frac{\varepsilon A}{z} \tag{1.1}$$

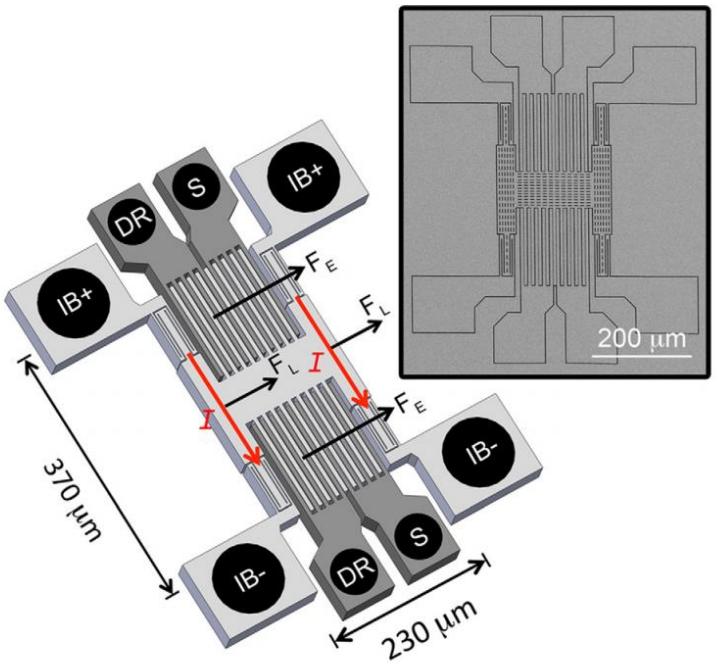


Figure 1.2: Example of a CMOS MEMS Lorentz Force Magnetometer [5].

The Lorentz Force states that a charged particle moving at a given velocity in the presence of a magnetic field B experiences a force F. In our case, the moving particles are the electrons of the current flowing along the sensor's movable plate I, with length L. The resulting force is perpendicular to both the current and magnetic field.

$$\vec{F} = L\vec{I}_{Lorentz} x \vec{B} \tag{1.2}$$

When the Lorentz Force deforms the movable plate springs, the distance between plates changes, which at the same time causes a variation in the capacitance (as stated in equation (1.1)). Those variations can provide information about the applied magnetic field B.

Furthermore, if the current that causes the Lorentz Force is applied periodically the movable plate acts as a mechanical resonator. For our application, this fact was interesting

because if the frequency of the Lorentz Force is similar to the natural frequency of the resonator, the changes in capacitance in front of the magnetic field are maximum.

In consequence we could say that at the resonance frequency, the sensor offers the maximum sensitivity in front of a magnetic field (behaviour similar to Figure 1.3).

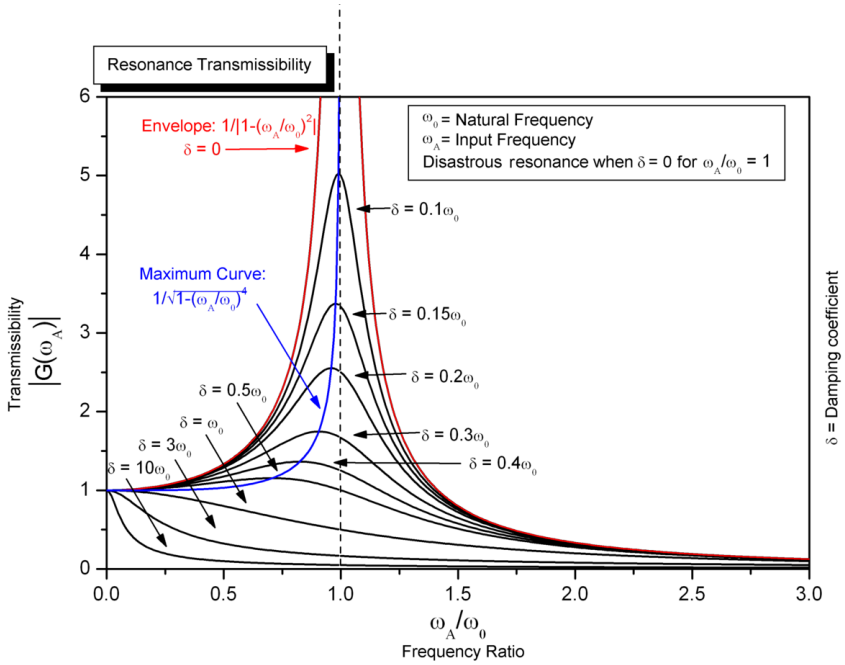


Figure 1.3: Frequency response of a Resonant System [6]

From these assumptions, in order to work with the maximum possible sensitivity:

- The measurement of the capacitance variation is made in the AC domain.
- To tune the frequency of the Lorentz Force, the current that causes the Lorentz-Effect ($I_{LORENTZ}$) should be AC and its frequency adjustable.

1.3. Objectives of this Thesis

The objective of this thesis is to design the electronics required by the sensor to:

- Perform the capacitive read-out.
- Provide the necessary current to cause the Lorentz-Effect.

For the read-out, a Low Noise Amplifier is used whereas a programmable floating source will provide the current for the Lorentz-Effect.

Both blocks are mostly analog and will be integrated on-chip along the sensor. Therefore the design will be made at transistor level and the results of this design will be the schematics and layout of both the LNA and the floating current source.

2. Readout Circuit

2.1. LNA Topology

This block is the responsible of reading the response of the CMOS-MEMS magnetometer and condition it to convert it in a signal more suitable for posterior processing systems.

To condition the sensor's response, a half Wheatstone bridge circuit and an amplifier are integrated on chip along with the sensor, as shown in Figure 2.1. The purpose consists in achieving a signal with better Signal to Noise Ratio (SNR) due to reduced parasitic capacitances at the interface nodes between the sensor and the LNA than in the case of using discrete components outside the chip. Hence, the noise is an important issue to consider in the design.

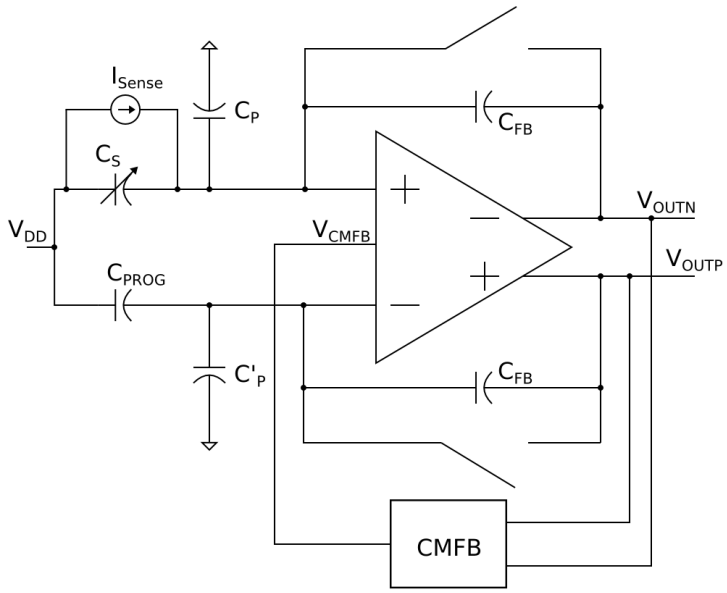


Figure 2.1: Half Bridge and Amplifier's configuration used to condition the magnetometer

Magnetometer Modelling

The amplifier is designed specifically for this application. To determine the required specifications, a provided electric model of the sensor was used. Regarding this model, three main parameters are taken into account:

- The injected noise.
- The parasitic capacitance due to the plates that form the sensor.
- The current variation generated because of the magnetic field.

When the DC voltage across the sensor is kept constant, variations of the sensor capacitance are translated into a movement of charges that generates a current. This current is then measured by the LNA.

$$I_{Sense}(t) = \frac{dq_C(t)}{dt} = C(z)\frac{dU_C(t)}{dt} + U_C\frac{dC(t)}{dt} = V_{DC}\frac{dC(t)}{dt} \quad (2.1)$$

Thereby, it can be modelled as a fixed capacitance, an alternating current source to consider the charge variation and an additional RLC branch that represents the resonant behaviour of the sensor (see Figure 2.2). The current's amplitude depends on:

- The magnetic field measured at that moment, B.
- The amplitude of the current used to generate the Lorentz Force ($I_{Lorentz}$).
- The DC voltage between the sensor plates.

$$I_{Sense}(t) = V_{DC} \cdot B \cdot I_{Lorentz} \cdot S \quad (2.2)$$

Where S is the sensor sensitivity, which depends on mechanical characteristics of the sensor.

Moreover, the sensor is a resonant one and its sensitivity turns out to be maximum at the resonant frequency. For our design, this resonant frequency is already characterized as 130 kHz. In consequence, we take this value as a constant when modelling the sensor.

In consequence, the output of the LNA should be a sinusoidal signal that behaves as indicated in equation (2.3), where C_f is the feedback capacitor.

$$V_{Out}(s) = \frac{I_{Sense}(s)}{sC_f} \quad (2.3)$$

	Sense C [pF]	Parasitic C [pF]	Brownian Noise [nV/$\sqrt{Hz}$]	Current Sensitivity [pA/(μT·mA·V)]	Output Ref Noise [nV/$\sqrt{Hz}$]	Conditions
X/Y axis	1.4	1.2	77	28.88	942.7	V_{dc} = 1 V C_{fb} = 100 fF F_r = 130 kHz
Z Axis	2	1.2	332	72.7	4054.5	V_{dc} = 1V C_{fb} = 100 fF F_r = 130 kHz

Table 2.1: Sensor's parameters obtained from previously manufactured versions

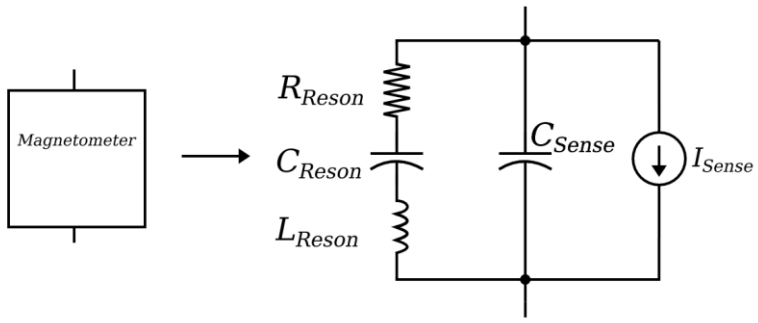


Figure 2.2: Electric model of the magnetometer for the OTA design

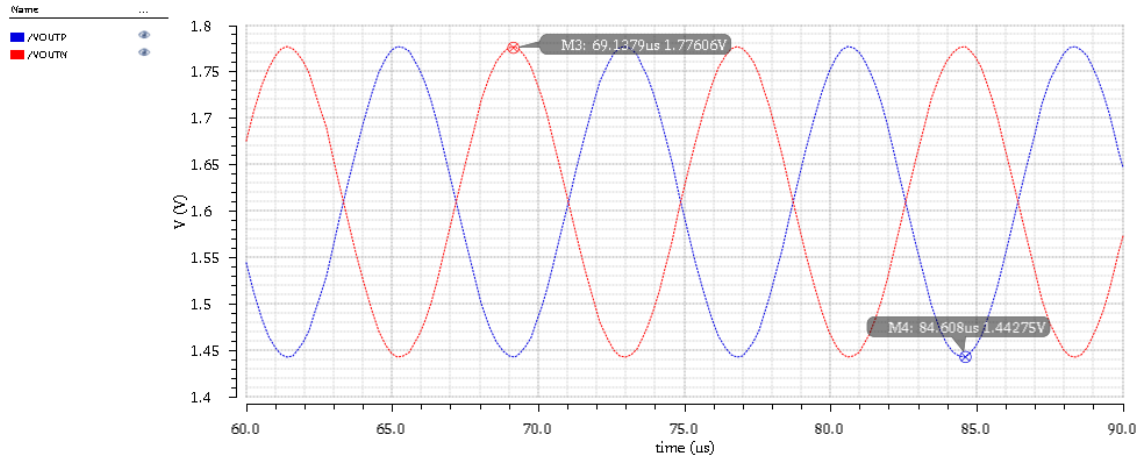


Figure 2.3: Response of the LNA when sensing a magnetic field of B = 1mT with $I_{LORENTZ}$ = 1mA and V_{DC} = 1.65V

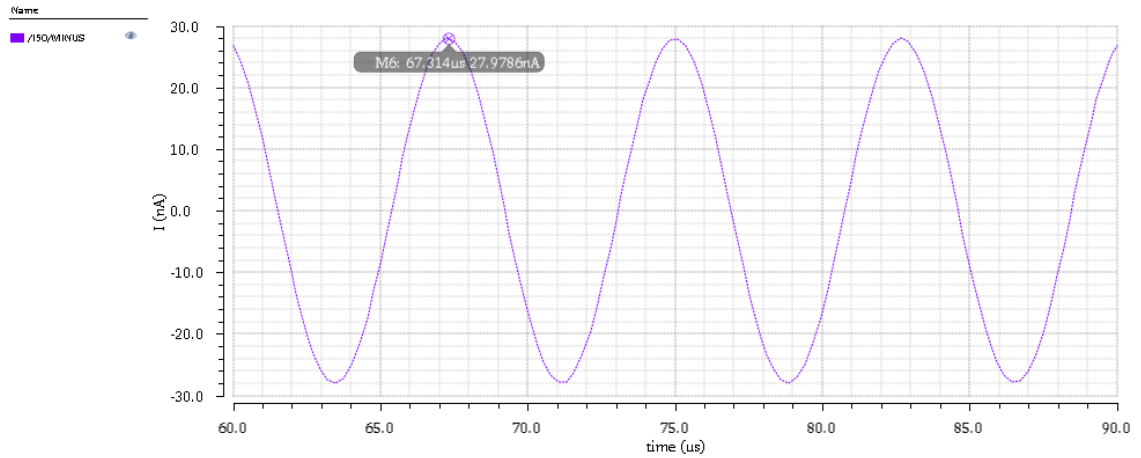


Figure 2.4: Current provided the sensor due to charge variation when applying the Lorentz Current

Required Specifications

Taking into account the noise levels of the sensor, its operation frequency and the capacitances appearing in the circuit, the LNA specifications are detailed in Table 2.2.

Specifications	**Min**	**Nom**	**Max**	**Units**
Voltage Supply (V_{DD})	*-*	*3.3*	*-*	*V*
Common-Mode Voltage	*-*	*1.65*	*-*	*V*
Current Consumption	*-*	*200*	*-*	*uA*
Open-Loop Gain (130 kHz)	*59*	*67*	*-*	*dB*
Phase Margin	*60*	*65*	*-*	*Degrees*
Unity Gain Bandwidth (GBW)	*120*	*-*	*-*	*MHz*
Opamp Load Capacitance	*-*	*0.8*		*pF*
Output PSRR+ (300 kHz and below)	*-43*	*-65*	*-*	*dB*
Output PSRR- (300 kHz and below)	*-43*	*-65*	*-*	*dB*
Output CMRR (300 kHz and below)	*-76*	*-86*	*-*	*dB*
Output Swing	*-*	*1.05*	*-*	*Vpp*
Opamp input referred noise	*-*	*-*	*45*	*$nV/\sqrt{Hz}$*
Slew Rate (300 kHz and below)	*1.96*	*20.75*	*-*	*V/µs*

Table 2.2: Table of Specs derived from the Sensor characteristics

2.2. OTA Topology

2.2.1. Folded cascode topology

An Operational Transconductance Amplifier based on a folded cascode topology with fully differential input and output is chosen to amplify the response of the magnetometer.

The reasons are mainly the high gain that this topology can offer with a single stage, which reduces the compensation issues present in multi-stages topologies [7]. In addition, the folded cascode topology combined with the use of wide swing cascode current mirrors allows to have a high dynamic range at the output.

Apart of these aspects, the OTA has been designed to offer low noise and a wide GBW response with a reasonable current consumption. In order to reach the specifications, we need to understand which parameters can affect our stability, gain or unity gain bandwidth. For this reason, some expressions obtained from the Small Signal Analysis have been considered to design properly this OTA.

This topology includes a differential pair, two cascode pairs and two pairs of current sources as illustrated in Figure 2.5.

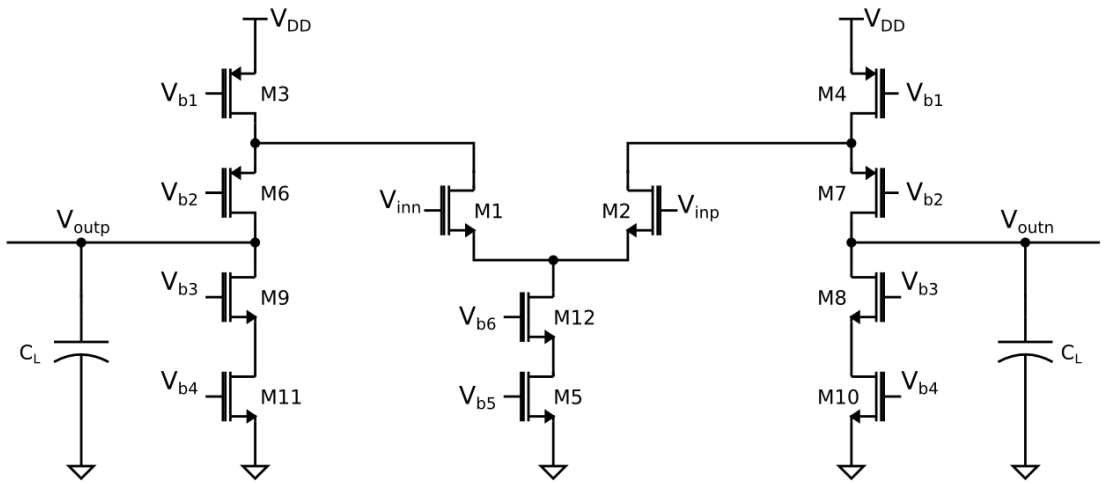


Figure 2.5: Folded Cascode Amplifier Used in the Design

Differential Folded Cascode Amplifier					
Instance	***Type***	***Width[µm]***	***Length[µm]***	***Multiplier***	***Aspect Ratio***
M1	***Native NMOS 3V***	*3*	*1.2*	*32*	*80*
M2	***Native NMOS 3V***	*3*	*1.2*	*32*	*80*
M5	***NMOS 3V***	*3*	*3*	*120*	*120*
M10	***NMOS 3V***	*3*	*3*	*96*	*96*
M11	***NMOS 3V***	*3*	*3*	*96*	*96*
M8	***NMOS 3V***	*3*	*3*	*24*	*24*
M9	***NMOS 3V***	*3*	*3*	*24*	*24*
M3	***PMOS 3V***	*2.2*	*0.8*	*156*	*429*
M4	***PMOS 3V***	*2.2*	*0.8*	*156*	*429*
M6	***PMOS 3V***	*2.2*	*0.8*	*24*	*66*
M7	***PMOS 3V***	*2.2*	*0.8*	*24*	*66*

Table 2.3: Transistor sizes for Folded Cascode Amplifier

2.2.2. Gain and Unity Gain Frequency

As in any differential amplifier, the differential pair acts as a transconductor, converting a voltage difference at the input in a difference of currents between both branches.

However, since it is desired to have the output as a differential voltage and at the same time high gain, both currents are passed through a device which behaves as an active load (high resistance) AC [8]. This device is the cascoded current source.

$$A_V = g_{m1} \cdot R_{OUT} \tag{2.4}$$

$$R_{OUT} \approx ((r_{DS1} || r_{DS3}) \cdot r_{DS6} \cdot g_{m6}) || (r_{DS11} \cdot g_{m9} \cdot r_{DS9}) \tag{2.5}$$

Where g_{m1} and g_{m6} are the transconductances of the differential pair and the cascode stages and r_{DS1} and r_{DS6} the resistances offered by the differential pair and the cascode respectively [9]. R_{DS9} and r_{DS11} are the resistances of the NMOS current source and cascode respectively and g_{m6} is the transconductance of the PMOS cascode stage.

As the cascode results in a large gain, when combined with the load capacitor C_L it limits the bandwidth of our amplifier and defines the dominant pole of the system.

$$BW = \frac{1}{2\pi R_{OUT} C_L} \tag{2.6}$$

Combining both expressions, and assuming that the non-dominant pole is far enough to be neglected, the Unity Gain Frequency can be obtained [10]:

$$GBW \approx \frac{g_{m1}}{2\pi C_L} \tag{2.7}$$

The conclusion that we could obtain from this expression is that the GBW is set mainly by the load capacitance and the differential pair. Therefore, the sizes of the differential pair and its biasing current will be determinant for the amplifier's GBW and should be the first part to set in the design.

Since the load capacitance will be caused by a buffer stage of 800 fF that drives the chip pads and the desired GBW is 120 MHz, the minimum transconductance offered by the differential pair should be at least g_{m1}=603.19 µA/V.

However, to guarantee this condition even for the worst case corner, a higher transconductance was targeted when sizing the differential pair for the nominal case. Therefore, the final transconductance is set to 708.52 µA/V which leads to a GBW of 136 MHz. The sizes and resulting parameters are indicated in Table 2.4 and Table 2.6, respectively.

Differential Pair Parameter	***Value***	***Unit***
g_{m1}	*708.52*	*µA/V*
Width	*96*	*µm*
Length	*1.2*	*µm*
W/L	*80*	*-*
Diff. Pair Current (I_{SS})	*100*	*µA*

Table 2.4: Size parameters and current required by the differential pair

Finally, to size the folded cascode branches, it was intended that the PMOS cascode was as wide as possible in order to have a greater g_{m6} without increasing the current consumption too much.

When designing a folded cascode with NMOS transistors in the differential pair, it is recommended to set the current sources taking into account the extreme case where the differential pair consumes I_{SS} completely from one of the branches.

To leave current still flowing through the folded cascode in this situation, the PMOS are designed to conduct 1.3 times I_{SS} which leaves $0.8 \cdot I_{SS}$ for the NMOS current source when the differential pair is equilibrated (see Figure 2.6).

On the opposite situation, if the differential pair has I_{SS} flowing completely at one side, the remaining current would be $0.3 \cdot I_{SS}$. Greater current factors could be chosen, however this option also leads to great consumptions.

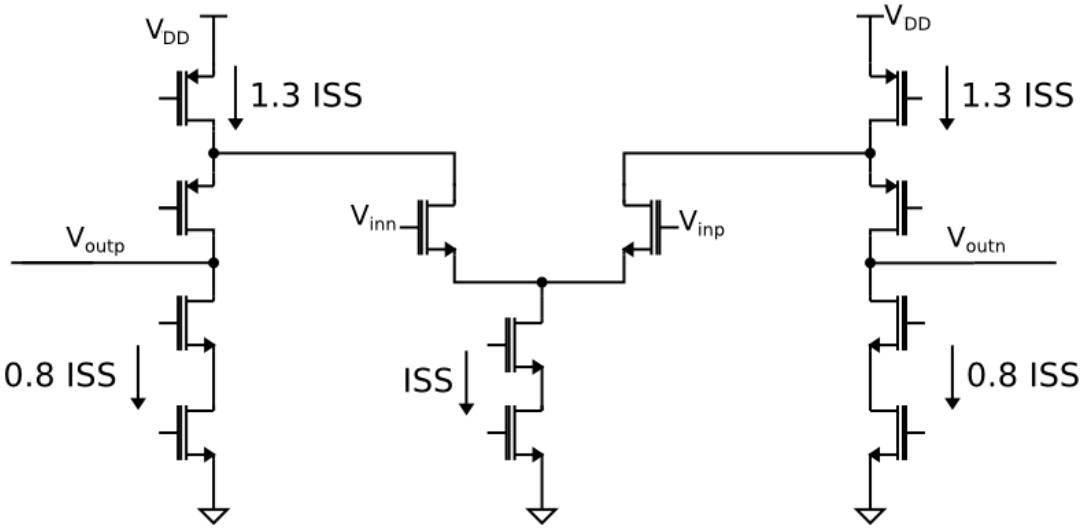


Figure 2.6: DC current consumption at different parts of the OTA

By setting I_{SS} = 100 µA, the cascode width at 52.8 µm at its length at 0.8 µm (aspect ratio 66), a g_{m6} = 543.4µA/V was achieved. With this value, the resulting gain is 74.83dB and the BW turns out to be 25.74 kHz.

Furthermore, g_{m6} is not only important for the gain. In section 2.2.3, it is explained how g_{m6} should be also as large as possible in order to enhance the stability of our amplifier. Therefore, increasing g_{m6} helps the design to reach both the gain and the Phase Margin specifications.

OTA Parameter	*Value*	*Unit*
I_{SS}	*100*	*µA*
I (PMOS Current Source)	*130*	*µA*
I (NMOS Current Source)	*80*	*µA*
g_{m6}	*543.4*	*µA/V*
Width	*52.8*	*µm*
Length	*0.8*	*µm*
W/L	*66*	*-*

Table 2.5: PMOS cascode parameters after setting current

OTA Parameter	*Value*	*Unit*
Gain at low f	*74.83*	*dB*
Bandwidth	*25.74*	*kHz*
GBW	*136*	*MHz*

Table 2.6: OTA parameters after sizing the differential pair and the cascodes

Regarding the rest of the parts of the amplifier, since a specific current mirror topology is being used (more details in section 2.2.5), a fixed relation between the PMOS cascode and its current source should be accomplished, so determining the size of the current source is immediate.

Finally, the NMOS branch of the folded cascode was the last part to size in the design. Since it does not take part in the signal path, its size should not be critical for the final GBW or PM. Therefore, only noise considerations have been applied when sizing this part.

2.2.3. Stability Analysis

Regarding the stability of our amplifier, a Phase Margin in open loop of at least 60º is required. Assuming that our amplifier is a system with only 2 poles, an approximate expression for the Phase Margin can be obtained (see expression (2.8)).

$$PM = 180º - arctg\left(\frac{f_u}{f_{p1}}\right) - arctg\left(\frac{f_u}{f_{p2}}\right) \approx 90º - arctg\left(\frac{f_u}{f_{p2}}\right) \qquad (2.8)$$

The stability gets better when the distance between the dominant pole and the nearest non dominant one is greater. In our case, the non-dominant pole is located at the drain of the transistors belonging to the differential pair, as shown in expression (2.9).

$$f_{p2} = \frac{g_{m6}}{2\pi C_X} \qquad (2.9)$$

Where g_{m6} is the transconductance of the PMOS cascode, and C_X is the addition of the parasitic capacitance of the differential pair and the transistors of the PMOS current source and its cascode.

$$C_X = C_{GD1} + C_{GD3} + C_{GS6} \tag{2.10}$$

The non-dominant pole should be located as far as possible from the dominant one to have a better stability. In consequence, g_{m6} should be large and C_X as small as possible.

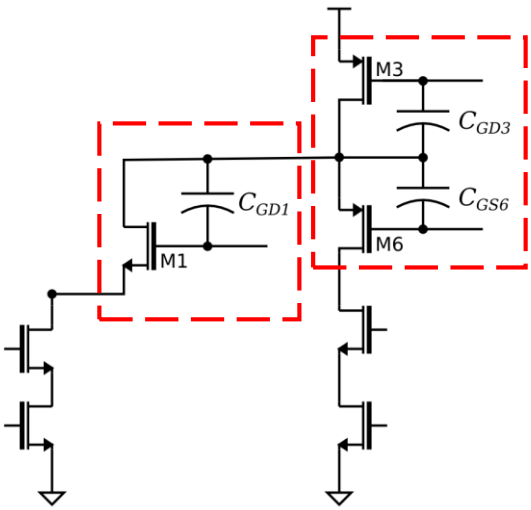


Figure 2.7: Half circuit, with capacitances contributing to the non-dominant pole

Concerning the sizes of the differential pair and the current source, they should be as small as possible to have good stability. In principle, this requirement presents a conflict with the GBW (differential pairs tend to have large widths) and with the noise. As we will see in future chapters, low-noise transistors tend to have large sizes.

In consequence, a trade-off between all 3 specifications should be considered when sizing the differential pair, the PMOS current source and the PMOS cascode.

By fulfilling this trade-off and using the load capacitance to set the dominant pole, the required Phase Margin (PM) is achieved as shown in Table 2.7.

OTA Parameter	***Value***	***Unit***
g_{m6}	*543.4*	*µA/V*
C_{GD1}	*36.51*	*fF*
C_{GD3}	*137.6*	*fF*
C_{GS6}	*151*	*fF*
Expected f_{nd}	*266.43*	*MHz*
PM	*62*	*Degrees*

Table 2.7: Capacitances considered in the non-dominant pole and PM of the OTA

2.2.4. Noise

For the purpose of avoiding a SNR degradation of the signal provided by our sensor, having a low noise at the output was an essential feature to take into account in the design.

Since our amplifier works at 130 kHz, the criteria to minimize the electronic noise was achieving a level below the Brownian noise, which is the thermal contribution introduced by the capacitive sensor.

After setting the limit, which is 40 nV/$\sqrt{\text{Hz}}$, the next steps consisted in identifying:

- The transistors of the design that have the largest noise contribution.
- Which types of noise present those transistors and how to minimize it.

Generally in folded cascode topologies, the output noise is mostly delivered by the transistors placed in current mirrors and differential pair. The contribution of transistors acting as cascodes is practically negligible [11].

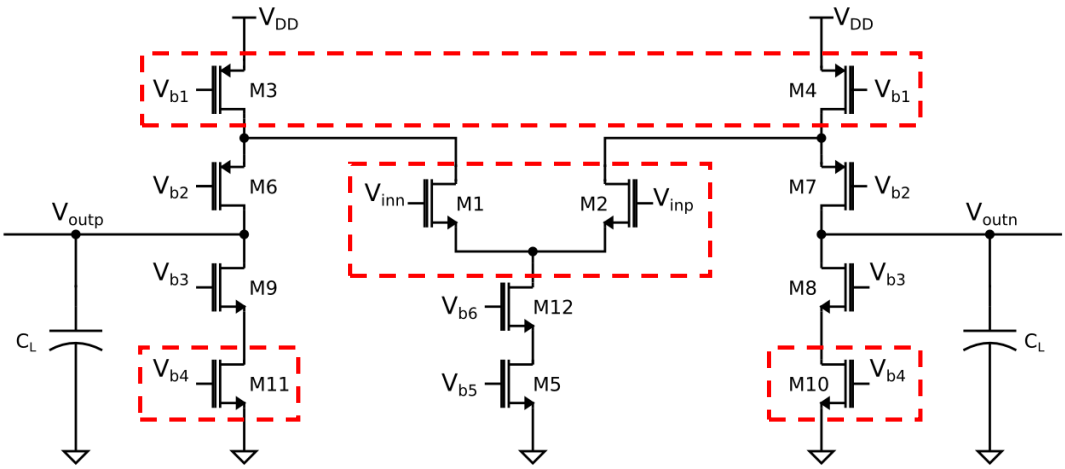


Figure 2.8: Schematic highlighting the main noise contributors

Concerning the amplifier's noise, the most important contributions at 130 kHz are:

- Flicker Noise.
- Thermal Noise.

In the case of flicker noise, enlarging the area of the transistor is enough to reduce it. Increasing either the width or the length is a valid option for any case, as shown in equation (2.11).

$$\overline{V_{N,Out}^2} = \frac{K}{C_{OX}WL}\frac{1}{f} \tag{2.11}$$

Where C_{OX} is the gate oxide capacitance of the transistor and K is a constant dependent on device properties [7].

Regarding the thermal contribution, first we should consider the function performed by the transistor. If it is used as an active load (current mirror), it is interesting to have a low transconductance by using a low aspect ratio [10] (see equation (2.12)).

$$\overline{V_{N,Out}^2} = 4kT\gamma g_m r_O^2 \tag{2.12}$$

Where k is the Boltzmann constant, T is the temperature, γ is a parameter that depends on the region of the transistor (2/3 if saturation) and r_O is the output resistance of the transistor.

On the other hand, for transistors used in differential pairs normally it is intended to achieve high transconductance to obtain larger gain. The reason is to minimize the input referred noise of the whole amplifier.

Despite all these considerations were taken into account, some trade-offs had to be reached in order to fulfil other specifications too:

- PMOS size had a critical impact in the stability of the amplifier and sizing them with low aspect ratios caused a worse performance from the stability point of view.
- In the NMOS case, since they are present in the signal path, their influence in the stability was not so important so it was possible to reduce the aspect ratio and setting large sizes.
- Finally, for the differential pair, native transistors were used since they offered a lower noise level than the normal NMOS counterpart. They were sized as wide as possible but excessive widths led to an increase of the parasitic capacitance in the non-dominant pole, which resulted in a worse stability performance too.

Instance	***Output noise level [$nV/\sqrt{Hz}$]***	***Contribution of total [%]***
M3	*12.88*	*26.27*
M4	*12.88*	*26.27*
M10	*5.11*	*4.15*
M11	*5.06*	*4.05*
M1	*6.4*	*6.46*
M2	*6.4*	*6.46*

Table 2.8: Flicker and Thermal contribution to the output referred noise of the most important transistors at 130 kHz

From the final sizes of the design, it is expected to have the PMOS current sources as the largest contributors of noise inside our design. When obtaining the noise report of the design (provided in Table 2.8), this suspicion is confirmed indeed. Despite this fact, an input referred noise much lower than the specified one is achieved, as indicated in Table 2.9.

Noise Parameter	***Value***	***Unit***
Input Referred Noise	*9.55*	$nV/\sqrt{Hz}$

Table 2.9: Noise level achieved in the design

The result is 4 times lower than the one specified. Apparently one could assume that this OTA is overdesigned from the noise point of view. However, the resulting transistors are sized considering other parameters like stability, gain, unity gain frequency that have resulted in a very low noise level at the end.

2.2.5. Low-voltage current mirror

As large output dynamic range was targeted for this application while having at the same time large output resistance in AC, a cascoded current source topology capable of working at low voltages of the output node was required.

Hence, all current sources of the design have been implemented with the low-voltage topology depicted in the following schematic.

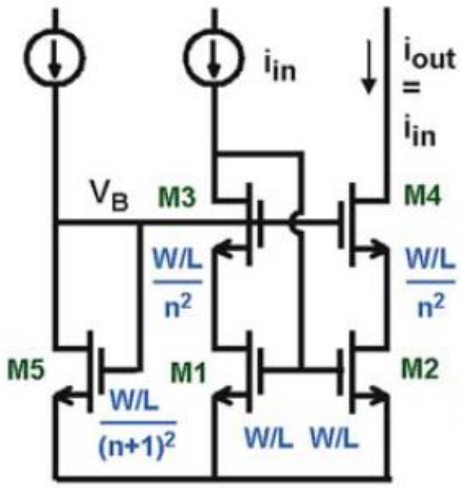


Figure 2.9: Low-Voltage Current Mirror Topology [10].

If proper biasing is applied to the cascode transistors, both M2 and M4 are in saturation only requiring a $V_{OUT} > V_{OD}|_{M4} + V_{OD}|_{M2}$, which is good enough for the desired 1 V_{pp} at the output [10] for the 3.3V power supply.

The main drawback of this topology is that the biasing of the cascodes should be generated by another branch, which adds an extra current consumption. Moreover, a relationship between the cascode and the current source should be fulfilled in order to behave as a current mirror [10]:

$$\left|\frac{W}{L}\right|_{Cascode} = \frac{\left|\frac{W}{L}\right|_{CS}}{n^2} \qquad \left|\frac{W}{L}\right|_{Reference} = \frac{\left|\frac{W}{L}\right|_{CS}}{(n+1)^2} \tag{2.13}$$

In our case, n is 2. Therefore the aspect ratio of the cascodes are:

$$\left|\frac{W}{L}\right|_{Cascode} = \frac{\left|\frac{W}{L}\right|_{CS}}{4} \tag{2.14}$$

About the biasing voltage, it should be high enough to guarantee that the voltage drop across the cascode does not force the current mirror to enter into ohmic region. Therefore, the transistor generating the bias will have a smaller aspect ratio than the cascodes.

Making the same reasoning for the reference cascode, it should be 9 times larger than the transistors present in the current source. Even though this ratio should ensure that both transistors are in saturation, in our case the reference has an aspect ratio 12 times smaller to guarantee this saturation for variability that may occur in the circuit.

$$\left|\frac{W}{L}\right|_{Cascode} = \frac{\left|\frac{W}{L}\right|_{CS}}{12} \tag{2.15}$$

In addition, the biasing transistor was implemented by placing several transistors in series instead of shortening the width. This approach was taken in order to consider the body effect of the cascodes and achieve a better matching of the threshold voltage between the reference and the rest of cascodes.

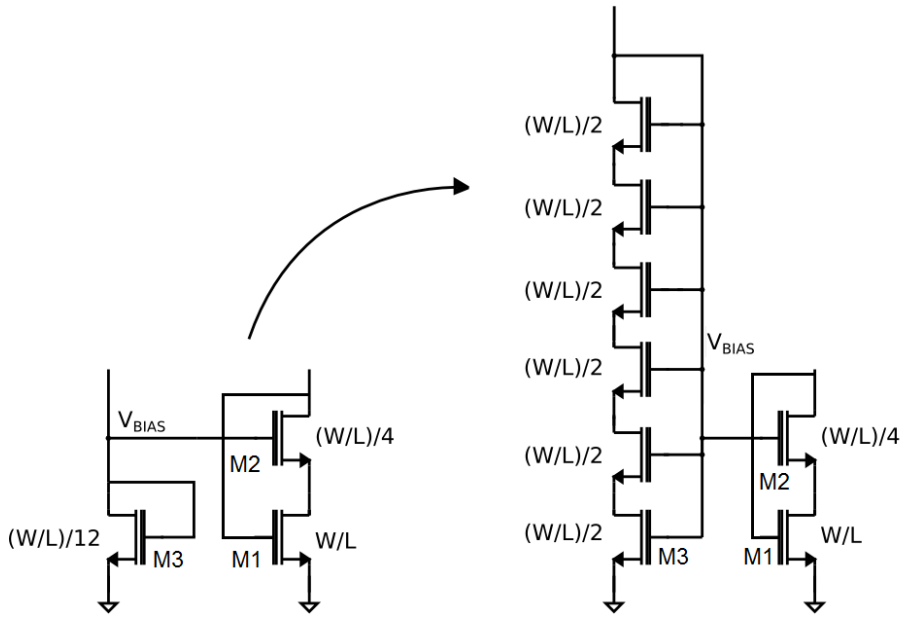


Figure 2.10: Current mirror and reference for cascode transistors. Instead of lowering the aspect ratio by using narrower transistors, several transistors in series generate the cascode bias.

Biasing circuit for Current Mirrors and Cascodes					
Instance	***Type***	***Width[µm]***	***Length µm]***	***Multiplier***	***Aspect Ratio***
Biasing for Current Mirror (M1)	*NMOS3V*	*3*	*3*	*12*	*12*
Cascode (M2)	*NMOS3V*	*3*	*3*	*3*	*3*
Biasing for Cascodes (M3)	*NMOS3V*	*3*	*3*	*6*	*1(6parallel/6 series)*

Table 2.10: Sizes for the transistors of the biasing circuit for all NMOS current mirrors

Regarding the PMOS transistors, the biasing voltage is generated in a similar way. The ratio between the cascodes and the current sources is the same. The biasing voltage of the current mirrors is provided by the CMFB.

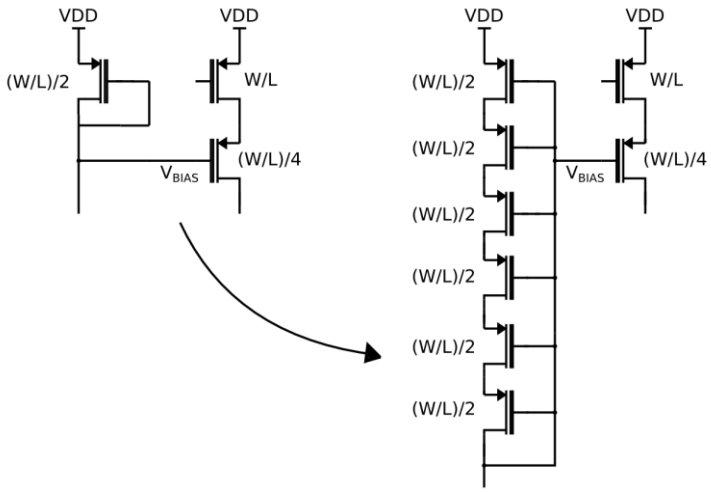


Figure 2.11: PMOS transistors in series generating Vbias for all PMOS cascodes

Biasing circuit for Current Mirrors and Cascodes					
Instance	***Type***	***Width[μm]***	***Length[μm]***	***Multiplier***	***Aspect Ratio***
Biasing for Cascodes	*PMOS3V*	*2.2*	*0.8*	*4*	*0.6(4parallel/6series)*

Table 2.11: Sizes for the transistors of the biasing circuit for all PMOS cascodes

2.3. Common Mode Feedback

Since the output of the LNA is differential, a Common Mode Feedback Amplifier is required in order to fix the DC voltage at both outputs.

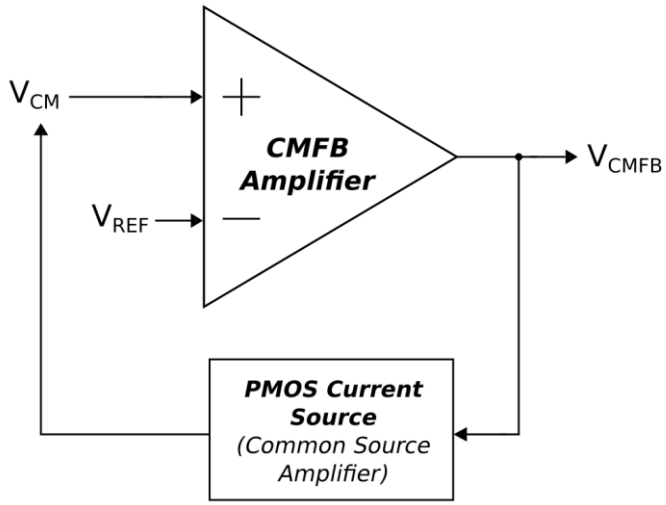


Figure 2.12: Block Diagram of a CMFB

Usually, the common mode of the output voltage is controlled using a negative feedback system that:

- Compares the common mode voltage of the outputs V_{CM} with a reference value V_{REF}.
- The difference generates a voltage, V_{CMFB}, which is returned to the main differential amplifier in order to adjust V_{CM} and make it equal to V_{REF} [12].

When returning V_{CMFB}, it is usually applied to an element of the biasing network in the main amplifier. In our case, the PMOS current sources, which act like a common source amplifier.

Both the CMFB amplifier and the common source provide gain to the negative feedback. The total gain of the loop is known as the open loop gain β and the higher it is, the lesser the error we have between V_{CM} and V_{REF}.

$$\beta = A_{DiffAmp}A_{CommonSource} \tag{2.16}$$

For our purposes, common mode regulation is required in order to have the amplifier working properly, but it is not necessary to achieve a very low error level since the measurement is made at AC to avoid the effects of offset and flicker noise.

2.3.1. Differential Amplifier

For our design, a Differential Amplifier is chosen to generate V_{CMFB} from the outputs of the main amplifier [12]. About this topology:

- The differential pairs perform the comparison between the reference voltage and the average of the outputs.
- The PMOS current mirrors convert the difference of currents in V_{CMFB}.
- Source degeneration has been applied to the differential pairs.

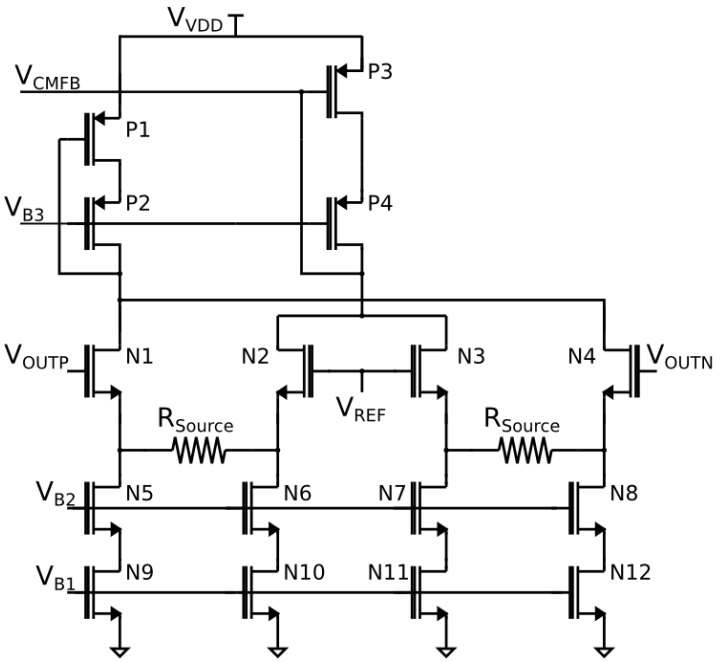


Figure 2.13: CMFB implemented with a Differential Amplifier

CMFB's Differential Amplifier					
Instance	***Type***	***Width[µm]***	***Length[µm]***	***Multiplier***	***Aspect Ratio***
M1	***Native NMOS 3V***	*2*	*1.2*	*4*	*6.66*
M2	***Native NMOS 3V***	*2*	*1.2*	*4*	*6.66*
M3	***Native NMOS 3V***	*2*	*1.2*	*4*	*6.66*
M4	***Native NMOS 3V***	*2*	*1.2*	*4*	*6.66*
M5	***NMOS 3V***	*3*	*3*	*4*	*4*
M6	***NMOS 3V***	*3*	*3*	*4*	*4*
M7	***NMOS 3V***	*3*	*3*	*4*	*4*
M8	***NMOS 3V***	*3*	*3*	*4*	*4*
M9	***NMOS 3V***	*3*	*3*	*16*	*16*
M10	***NMOS 3V***	*3*	*3*	*16*	*16*
M11	***NMOS 3V***	*3*	*3*	*16*	*16*
M12	***NMOS 3V***	*3*	*3*	*16*	*16*
P2	***PMOS 3V***	*2.2*	*1*	*8*	*17.6*
P4	***PMOS 3V***	*2.2*	*1*	*8*	*17.6*
P1	***PMOS 3V***	*2.2*	*1*	*32*	*70.4*
P3	***PMOS 3V***	*2.2*	*1*	*32*	*70.4*

Table 2.12: Transistor sizes for Differential Amplifier used in CMFB

The main advantage of this topology is that large resistors, used sometimes to obtain the common-mode voltage, are avoided, since the differential pair is able to provide a measure for the average voltage and at the same time it provides a satisfactory accuracy depending on the gain of the Common Mode Loop.

On the other hand, the limited input range and nonlinearity of the differential pairs makes this topology suitable only for circuits with small voltage swing [12].

Because of the design's requirement of output dynamic range around 1 V_{pp} and avoiding large resistors was a desirable feature, solving this range limitation was necessary. The techniques applied to enhance both characteristics will be explained in detail in section 2.3.4.

2.3.2. CMFB Loop Response

As shown in equation (2.16), the loop gain is provided by the CMFB amplifier and the PMOS current sources.

Therefore, the total open loop gain can be obtained by analysing each stage individually. Concerning the CMFB amplifier, its response can be approximated as a single pole system produced by the gate source capacitance of the PMOS current sources.

$$A_{CMFBAmp} = \frac{1}{2}\frac{g_{mPair}}{g_{mp}}\frac{1}{(1+\frac{s}{g_{mp}/(2C_{GS})})} \tag{2.17}$$

Whereas in the common source amplifier, we should take into account 2 poles, one caused by the load capacitance and the other caused by the parasitic capacitances of the differential pair, the current source and the cascode of the main amplifier.

$$A_{CommonSource} = g_{CS}R_{OUT}\frac{1}{\left(1+\frac{s}{1/(R_{OUT}C_L)}\right)\left(1+\frac{s}{g_{m6}/C_X}\right)} \tag{2.18}$$

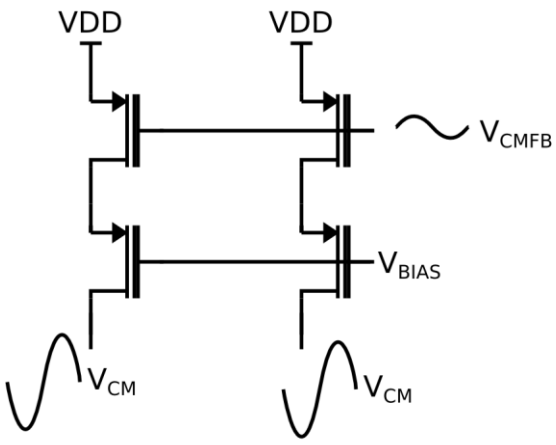


Figure 2.14: Current Sources acting as a Common Source Amplifier for V_{CMFB}

Joining both expressions the loop gain would result in a function with 3 poles as in equation (2.19).

$$\beta = \frac{\frac{1}{2} g_{mPair} N R_{OUT}}{\left(1 + \frac{s}{1/(R_{OUT} C_L)}\right)\left(1 + \frac{s}{g_{mp}/(2C_{GS})}\right)\left(1 + \frac{s}{g_{m6}/C_X}\right)} \tag{2.19}$$

Where N is the relationship between the aspect ratios in the PMOS transistors of the main amplifier and the PMOS of the CMFB amplifier and g_{mpair} is the transconductance of the differential pair used in the CMFB amplifier.

From here, the gain, GBW and the poles to consider for the stability of the feedback can be obtained.

$$Gain_\beta = \left(\frac{g_{mPair}}{g_{mp}}\right)(g_{mCS} R_{OUT}) = \frac{1}{2} g_{mPair} N R_{OUT} \tag{2.20}$$

$$GBW_\beta = \frac{1}{2\pi R_{OUT} C_L}\left(\frac{1}{2} g_{mPair} N R_{OUT}\right) = \frac{g_{mPair} N}{2\pi C_L} \tag{2.21}$$

$$f_{p1} = \frac{1}{2\pi R_{OUT} C_L} \qquad f_{p2} = \frac{g_{mp}}{4\pi C_{GS}} \qquad f_{p3} = \frac{g_{m6}}{2\pi C_X} \tag{2.22}$$

Loop Parameter	***Value***	***Unit***
g_{mp}	*301*	*µA/V*
C_{GS}	*860.7*	*fF*
f_{p2}	*27.83*	*MHz*
g_{m6}	*501*	*µA/V*
C_X	*325.1*	*fF*
f_{p3}	*264*	*MHz*

Table 2.13: Expected locations of the second and third pole and parameters values used to estimate them

Loop Parameter	***Value***	***Unit***
β Gain at low f	*58.42*	*dB*
β GBW	*18.26*	*MHz*
f_{p1}	*21.90*	*kHz*

Table 2.14: Expected parameters of β

The dominant pole turns out to be the one caused by the load capacitor as in the main amplifier. However, due to the presence of 3 poles, it is possible to have an unstable loop. Hence a compensation network may be required to deal with them.

Apart from the stability issues, due to both the large C_L and the use of linearization techniques (explained in chapter 2.3.3), the GBW of the common mode loop is reduced drastically. Therefore, it is expected to have a GBW_{CM} below the differential GBW_{Diff}. Despite having $GBW_{CM} > GBW_{Diff}$ is usually a requirement for CMFB circuits, depending on the application it is possible to keep it below. Indeed, if it is not expected to have fast variations of the common mode voltage, this specification can be relaxed [10].

2.3.3. Feed Forward Stabilization (Nulling Resistor)

To ensure stability for the Loop Response, a compensation network has been added to the CMFB amplifier (see Figure 2.15). The main reason to use the feed forward compensation is that allows to enhance the stability of the loop without reducing the unity gain bandwidth drastically [13].

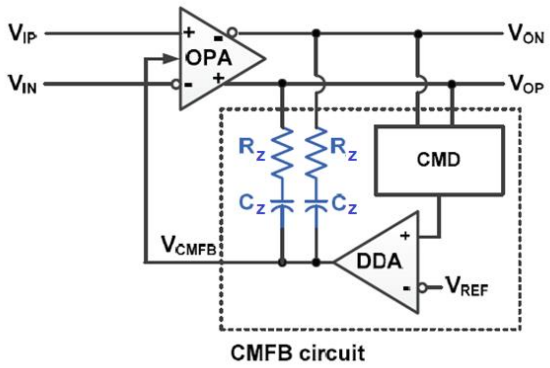


Figure 2.15: Block Diagram of a CMFB using feed forward stabilization [13].

Before using this compensation technique, the stability enhancement was only possible by reducing the GBW either by increasing C_L or using a bigger degeneration resistor R_S. With C_L=0.8 pF and R_S=57 kΩ a PM = 48º and a GBW around 12.5 MHz was achieved whereas using the feed forward stabilization allowed us to get a much better Phase Margin and Gain Bandwidth (PM = 84.54º, GBW = 22 MHz) with the same load and degeneration.

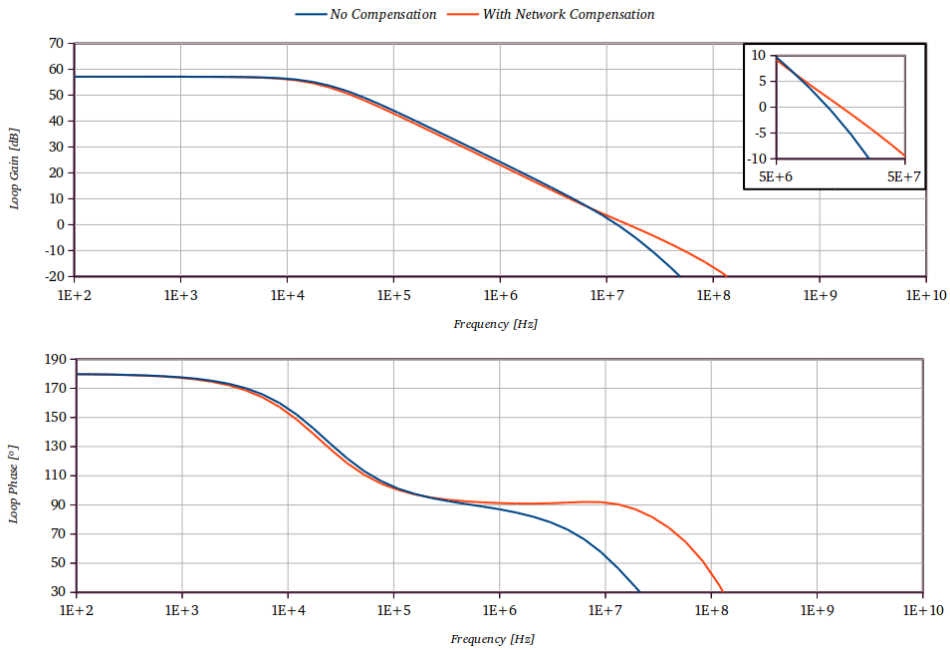


Figure 2.16: Bode plot of the CMFB Loop before (blue) and after using compensation (orange)

As depicted in Figure 2.16, the network causes a noticeable stability improvement with the PM going from 48º to 85º.

The network consists of a capacitor C_Z, which moves the dominant pole at a lower frequency and migrates the second pole at a higher frequency [13], and a Nulling Resistor R_Z, that includes an additional zero at higher frequencies, reducing the effect of the non-dominant pole and allowing an improvement of the Phase Margin of the Loop.

In our case, the second pole that affects our loop stability is the pole caused by the gate of the PMOS current sources. Therefore, the zero should be near this pole, which was located around 27 MHz.

When applied to the CMFB, its response can be approximated with expression (2.23).

$$\frac{v_{cmfb}}{v_{cm}} \approx \frac{1}{2}\frac{g_{mn}}{g_{mp}}\frac{1+\left(R_Z+\frac{1}{g_{mn}}\right)C_z s}{\left(1+\frac{s}{g_{mp}/(2C_{GS}+2C_X)}\right)\left(1+\frac{s}{1/(R_Z C_z)}\right)} \tag{2.23}$$

Regarding the case without compensation, the network introduces an additional zero and a pole. Their locations can be estimated with equations (2.24) and (2.25). Their derivation is explained in section 5.

$$f_{Zero} = \frac{1}{2\pi\left(R_Z+\frac{1}{g_{mn}}\right)C_Z} \tag{2.24}$$

$$f_{Pole} = \frac{1}{2\pi R_Z C_Z} \tag{2.25}$$

Where g_{mn} is the transconductance of the differential pair used to compare the common mode voltage with the reference.

The final network characteristics are provided in table Table 2.15 as well as the final specifications for the CMFB loop after compensation.

Network Element	***Value***	***Units***
Network Capacitance C_Z	*200*	*fF*
Nulling Resistor R_Z	*5.36*	*kΩ*
Effective g_{mn}	*29.85*	*µA/V*
Expected Zero Location	*20.19*	*MHz*
Expected Pole Location	*148.46*	*MHz*

Table 2.15: Characteristics of the compensation network

CMFB Parameter	***Value***	***Unit***
Loop Gain at (130 kHz)	*42.95*	*dB*
Loop GBW	*22.24*	*MHz*
Loop PM	*84.54*	*Degrees*
Consumption	*53.3*	*µA*

Table 2.16: Main Parameters of the CMFB Response in the Nominal Corner after compensation

2.3.4. Source Degeneration (CMFB dynamic range enhancement)

As mentioned in previous sections, this topology has a problem with the input dynamic range and the linearity offered by the differential pair when applying large voltage swings.

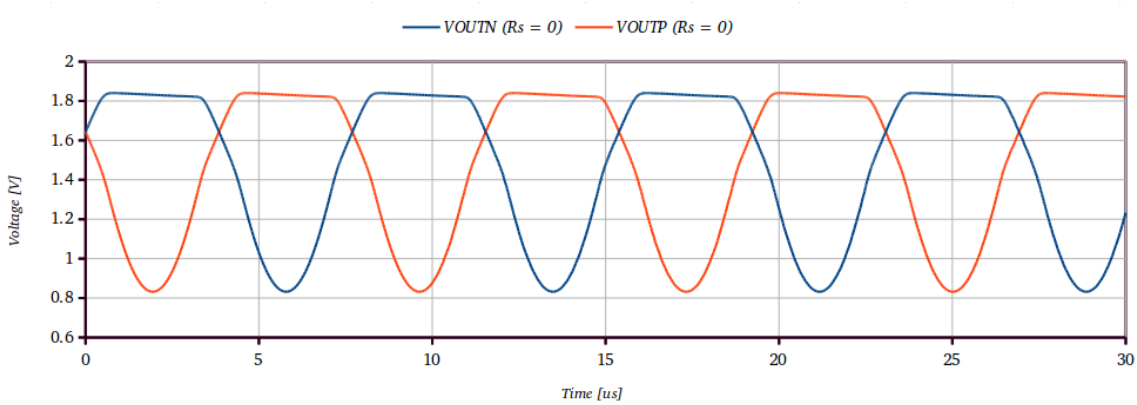


Figure 2.17: CMFB distorts the Output Waveform

Both problems can be minimized:

- By reducing the aspect ratios (W/L) of the differential pair, which reduces the amplifier's gain.
- Increasing the current flowing through them [12], which causes a large consumption of the circuit.

The input range extension caused by the previous options can be calculated with equation (2.26) [8]. As long as the differential peak to peak voltage of the output is inside this range, the behaviour of the differential pair can be considered linear and the CMFB loop controls properly the common mode.

$$\Delta V_{INmax} = \sqrt{\frac{2I_{SS}}{\mu_n C_{OX}(W/L)}} \qquad (2.26)$$

In our design an alternative approach was taken to resolve this issue without increasing the current consumption of the amplifier. This alternative consists in using a source degeneration in the amplifier (see Figure 2.18).

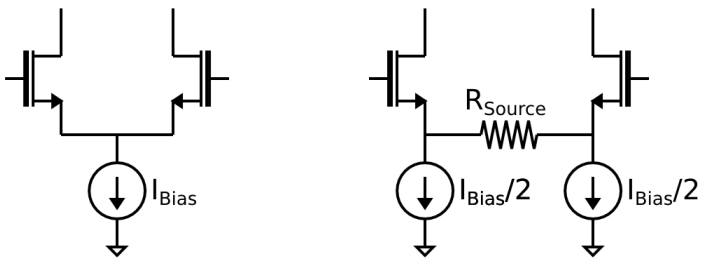


Figure 2.18: A conventional NMOS differential pair and the one with source degeneration

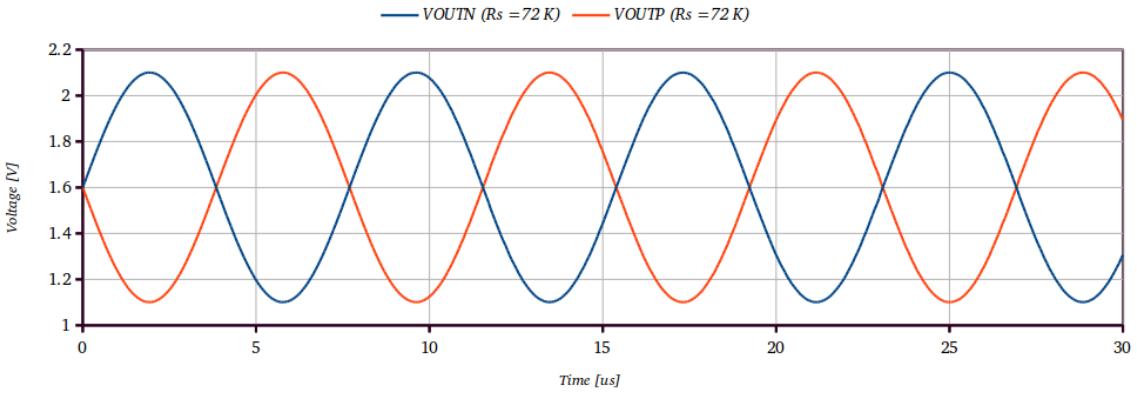


Figure 2.19: Output Waveform after adding source degeneration

Adding a source degeneration degrades the gain of the amplifier and the GBW of the CMFB loop, but provides extra linearization in case that the previous approaches are not enough [14]. This gain degradation occurs due to the loss of transconductance in the differential pair introduced by the resistor, which can be modelled with the expression provided in equation (2.27). In consequence, a trade-off when choosing the resistor value should be reached.

$$G_{m\,Effective} = \frac{g_m}{1 + g_m \cdot R/2} \tag{2.27}$$

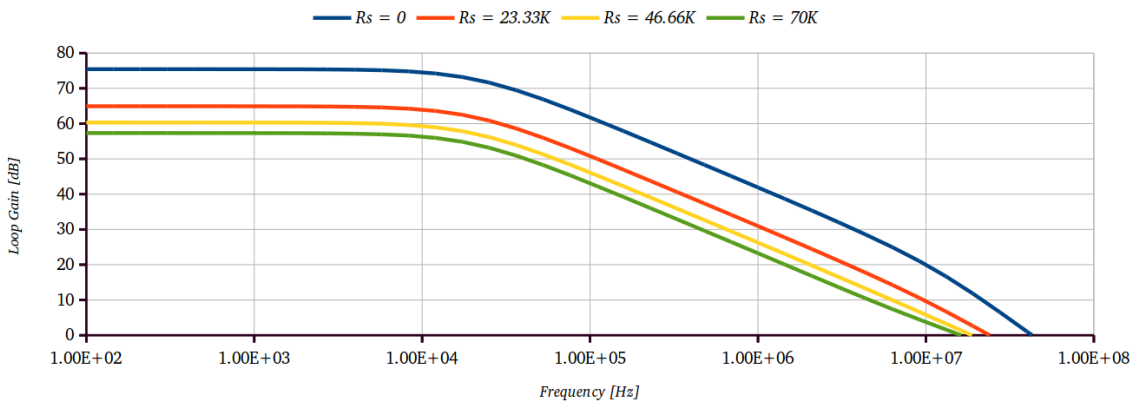


Figure 2.20: Degradation of both Gain and GBW of the CMFB Loop when the source resistor is higher. The resistance value was swept from 10k to 100k

When including the source degeneration, the maximum input range to work inside the linear region can be estimated from equation (2.28). The steps to obtain it are explained in chapter 6.

$$\Delta V_{INmax} = \sqrt{\frac{2I_{SS}}{\beta}} + \frac{R_S I_{SS}}{2} \tag{2.28}$$

From the equation, one can conclude with that the source degeneration, both the resistance and the bias current have a greater impact in the improvement of the input range than in the previous case.

Network Element	Value	Units
Resistor	*57*	*kΩ*
Expected Gm Effective	*29.85*	*µA/V*

Table 2.17: Resistor value to implement source degeneration

The effect over the currents in the differential pair is depicted in Figure 2.21. The larger the degenerating resistance, the wider the linear region of the differential pair.

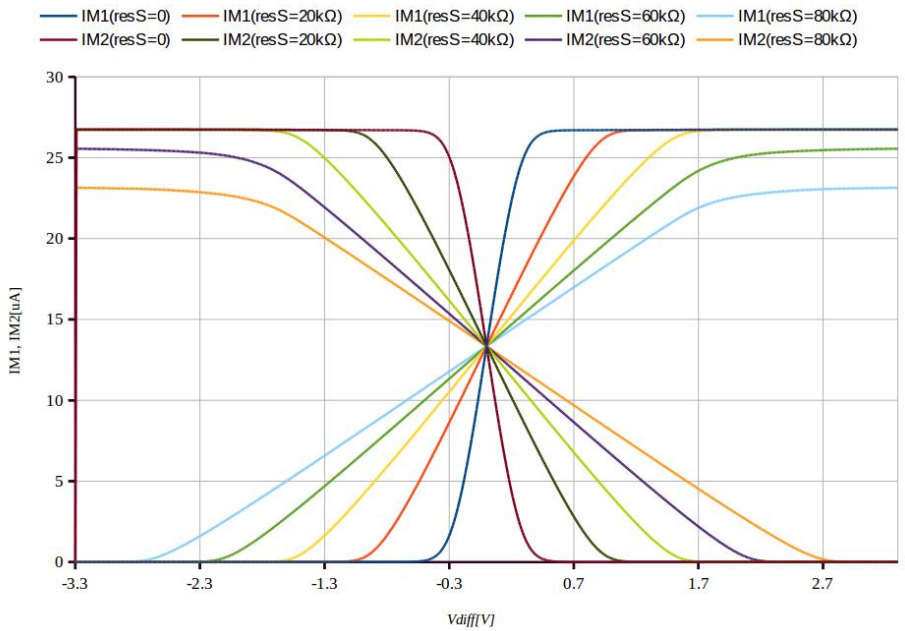


Figure 2.21: Differential Pair Current with linearized response due to degeneration

To characterize better the linearity improvement, a DFT of the amplifier output working as a feedback amplifier with gain 1 was made. At the input, a pure tone of 1 V_{pp} at 130 kHz was set.

Despite the amplifier is working with differential signals, from the DFT point of view the signals are evaluated as single ended, due to the distortion caused by the CMFB loop is only noticeable if the output is evaluated single ended or from the common mode perspective.

Figure 2.22 shows the DFT of the input signal, which a single tone at 130 kHz (our fundamental frequency).

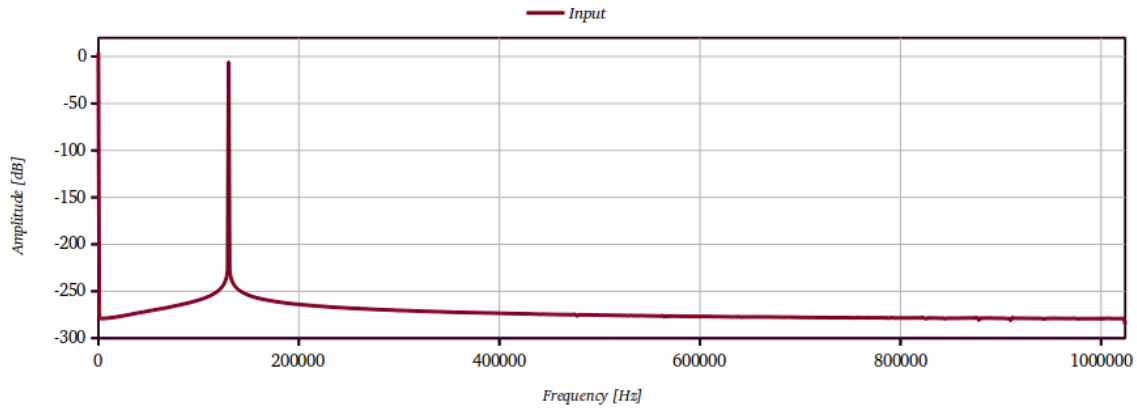


Figure 2.22: FFT of Input Signal (Single Ended Component). Fundamental tone at 130 kHz

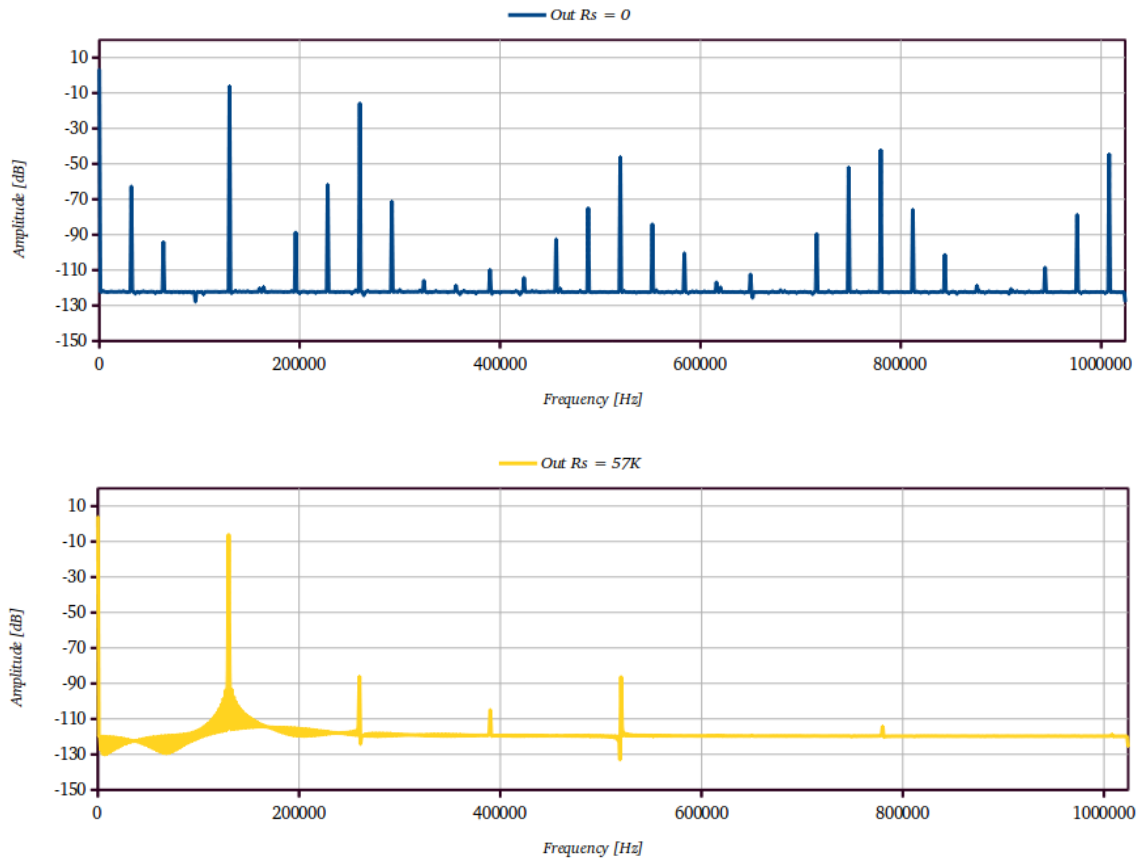


Figure 2.23: FFT of the amplifier output (single ended) for values of R_{Source} 0 kΩ and 57 kΩ

As it can be seen from the result, some harmonic tones appear (Figure 2.23) and when the resistor value is increased both the number of harmonic components and their amplitudes are reduced.

To quantify the improvement in linearity, the Spurious Free Dynamic Range was measured. Its definition is provided in equation (2.29).

$$SFDR = Amplitude_{Fundamental}(dB) - Amplitude_{Largest\ Spur}(dB) \qquad (2.29)$$

When calculating for different values of the source degeneration, an optimal SFDR of 80dB is found when R_S = 57 kΩ. For upper values no further linearity improvement is obtained. For this reason this value is chosen to implement the source degeneration.

Source Res [kΩ]	SFDR [dB]
$R_S = 0$	9.68
$R_S = 35k\Omega$	50.05
$R_S = 57k\Omega$	79.79

Table 2.18: SFDR achieved with different R_{Source}

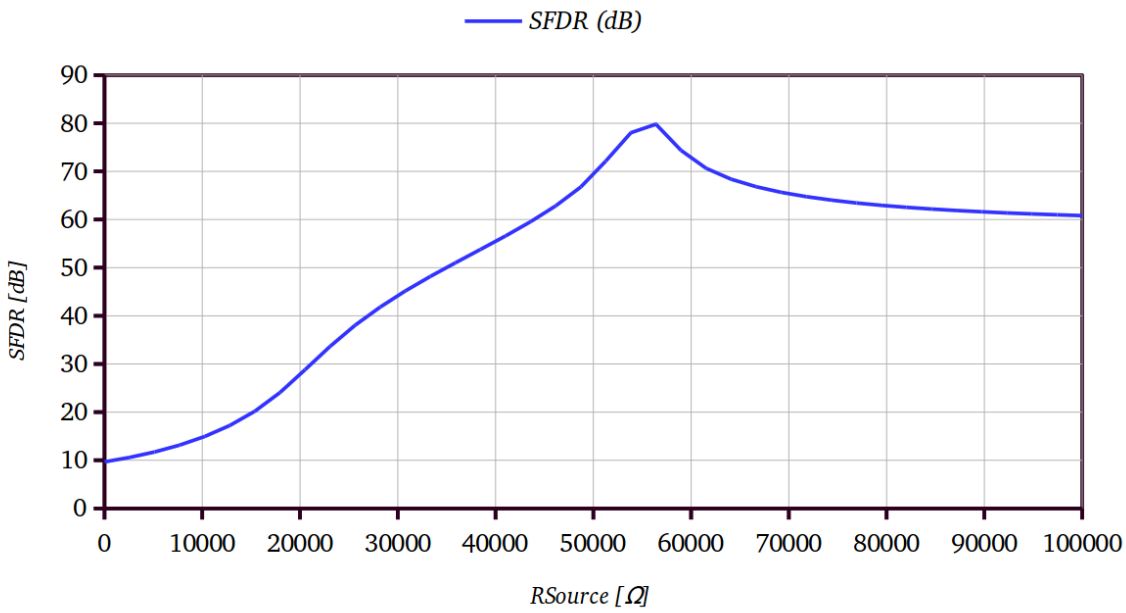


Figure 2.24: SFDR obtained as a function of the R_{Source}

2.4. OTA Characteristics after Design

After the design, some of the general features are:

- Input referred noise below 11 nV/Hz.
- GBW larger than 120 MHz.
- Phase Margin of 62º.
- DC Open Loop Gain of 74.83 dB (60 dB at 130 kHz).
- Consumption of 320 µA when operating.
- Output Dynamic Range of 1.05 V_{pp}.
- IP activation controlled by an Enable Pin.

General Enable Pin

The designed OTA includes the possibility of disabling the amplifier. To do so, an Enable Pin E is provided. If E = '1', the OTA is operating whereas in the opposite case, the amplifier is shutoff.

When the amplifier is disabled, all the nodes of the circuit are driven to a fixed voltage (V_{DD} or GND). Therefore the current consumption of the circuit when disabled is practically null. However, it is not zero due to leakage and subthreshold currents that transistors offer even when they are supposed to be shutoff.

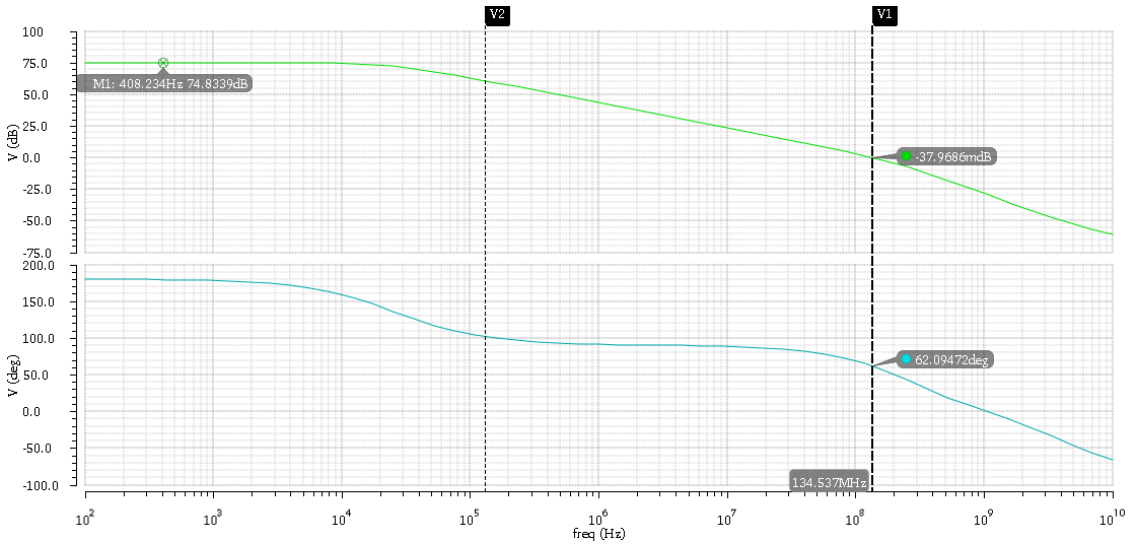


Figure 2.25: Amplifier's gain and phase response vs frequency

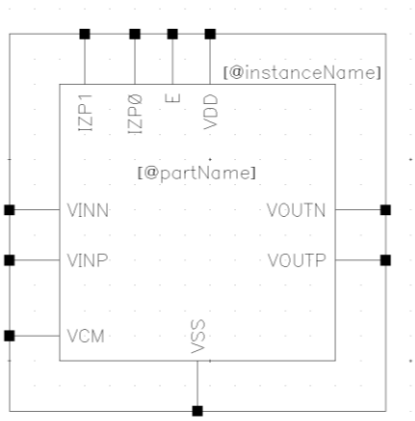
PIN	DESCRIPTION	Expected Range Value	SYMBOL
VDD	*Supply Voltage*	*3.3V*	
VSS	*Ground*	*0V*	
E	*General Enable*	*0V – 3.3V*	
VINP	*Positive Input*	*1.55V – 1.75V*	
VINN	*Negative Input*	*1.55V – 1.75V*	
IZP1	*Current Reference 1*	*10uA*	
IZP0	*Current Reference 0*	*10uA*	
VREF	*Ref Voltage for CMFB*	*1.65V*	
VOUTP	*Positive Output*	*1.15V – 2.15V*	
VOUTN	*Positive Output*	*1.15V – 2.15V*	

Table 2.19: Pinnout of the OTA

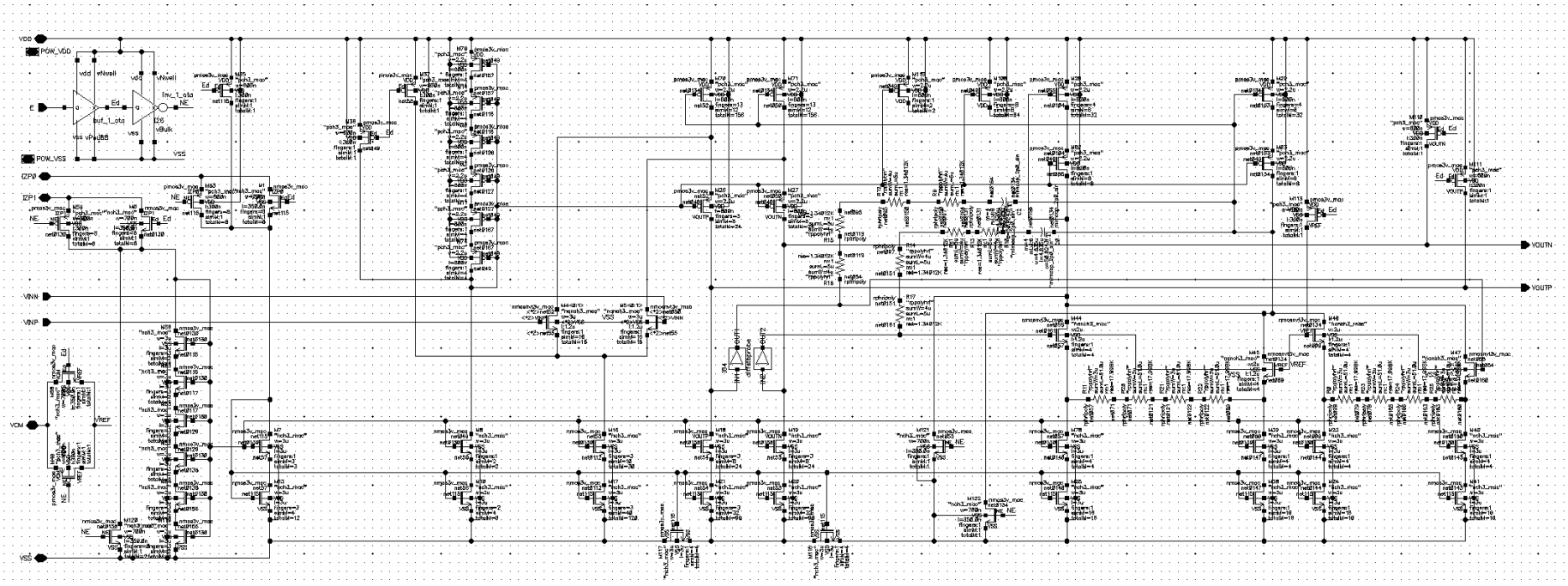


Figure 2.26: Complete schematic of the OTA

PARAMETER	CONDITIONS	UNITS	MIN	TYP	MAX	COMMENTS
Voltage Supply		*V*		*3.3*		
Ref Bias Current		*uA*		*10,00*		
Current Consumption	*E = '1', OTA Enabled*	*uA*	*299*	*307*	*315.7*	*Simulated at T=[-25ºC, 27ºC, 75ºC] for corners ff, ss, fs, sf and 100 Montecarlo Iterations.*
	E = '0', OTA Disabled	*pA*	*128.3*	*136*	*154.8*	*Simulated at T=[-25ºC, 27ºC, 75ºC] for corners ff, ss, fs, sf and 100 Montecarlo Iterations.*
Load Capacitor		*pF*		*0.8*		
GBW		*MHz*	*119.6*	*135.5*	*150.8*	*Simulated at T=[-25ºC, 27ºC, 75ºC] for corners ff, ss, fs, sf and 100 Montecarlo Iterations.*
Gain_130k		*dB*	*59.77*	*60.76*	*61.78*	*Simulated at T=[-25ºC, 27ºC, 75ºC] for corners ff, ss, fs, sf and 100 Montecarlo Iterations.*
PM		*Degrees*	*61.73*	*62.75*	*63.65*	*Simulated at T=[-25ºC, 27ºC, 75ºC] for corners ff, ss, fs, sf and 100 Montecarlo Iterations.*
InputNoise130k		*nV√Hz*	*8.572*	*9.652*	*10.87*	*Simulated at T=[-25ºC, 27ºC, 75ºC] for corners ff, ss, fs, sf and 100 Montecarlo Iterations.*
CMRR_300K		*dB*	*101.5*	*113.7*	*135.2*	*Simulated at T=[-25ºC, 27ºC, 75ºC] for corners ff, ss, fs, sf and 100 Montecarlo Iterations.*
PSRR+out_300K		*dB*	*-26.09*	*-28.69*	*-32.9*	*Simulated at T=[-25ºC, 27ºC, 75ºC] for corners ff, ss, fs, sf and 100 Montecarlo Iterations.*
PSRR-out_300K		*dB*	*-47.07*	*-58.79*	*-80.12*	*Simulated at T=[-25ºC, 27ºC, 75ºC] for corners ff, ss, fs, sf and 100 Montecarlo Iterations.*
Offset		*mV*	*15.16E-3*	*1.041*	*4.494*	*Simulated at T=[-25ºC, 27ºC, 75ºC] for corners ff, ss, fs, sf and 100 Montecarlo Iterations.*
CMFB_GBW		*MHz*	*19.72*	*21.48*	*23.25*	*Simulated at T=[-25ºC, 27ºC, 75ºC] for corners ff, ss, fs, sf and 100 Montecarlo Iterations.*
CMFB_PM		*Degrees*	*87.36*	*88.1*	*88.82*	*Simulated at T=[-25ºC, 27ºC, 75ºC] for corners ff, ss, fs, sf and 100 Montecarlo Iterations.*
VCM		*V*	*1.572*	*1.624*	*1.594*	*Simulated at T=[-25ºC, 27ºC, 75ºC] for corners ff, ss, fs, sf and 100 Montecarlo Iterations.*

Table 2.20: Specifications of the Folded Cascode OTA

2.5. Layout

2.5.1. Design Flow

The Layout is full-custom made considering the design rules of TSMC018 technology. This CMOS technology has a feature size of 180nm, is provided by the company Taiwan Semiconductor Manufacturing Company (TSMC) and supports analog, mixed-signal and digital. The process includes up to 6 different types of metals and allows different supply voltage for analog (3.3 V) or digital (1.8 V) circuits.

In order to validate that the design is valid for fabrication, the layout must pass successfully the following steps (see Figure 2.27):

- Design Rule Check (DRC) and Electrical Rule Check (ERC).
- Layout versus Schematic (LVS).
- Post-Extraction Simulation.

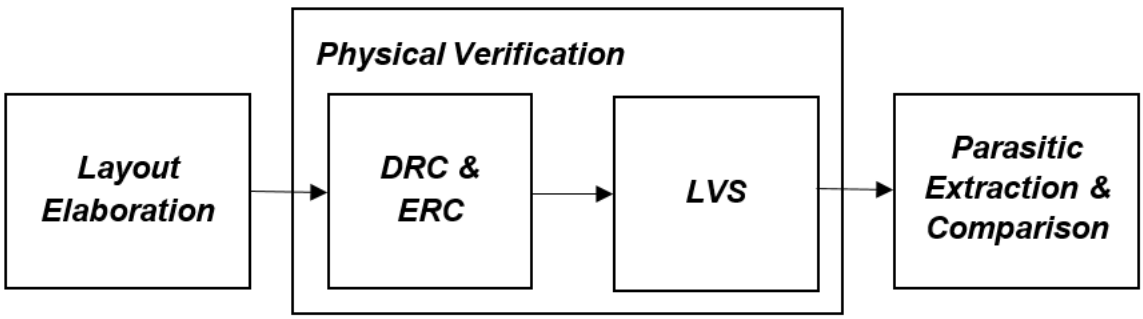


Figure 2.27: Design Flow of a full custom Analog Layout

Both DRC and LVS validations and the parasitic extraction are performed with Calibre tools (from Mentor Graphics), available in the design kit.

With regard to each one of the steps, the first one DRC checks if the layout passes all the design rules indicated by the manufacturer as minimum distance between layers, minimum width, minimum percentage of metal coverage, etc.

Secondly, the electrical rule check (ERC) is a set of rules that verifies the robustness of a design against situations of electrical stress like floating gates or interconnections, no substrate or well connection or spots likely to suffer latch up.

Furthermore, an additional verification that should be passed is the antenna check, whose objective is to avoid the antenna effects, as known as Plasma Induced Damage. This effect consists in charge accumulation in isolated nodes of an integrated circuit during its manufacturing process [8] [15].

About LVS, basically it checks that the layout implementation exactly matches the schematic.

Finally, the parasitic extractor is the tool that generates a netlist with all the devices found in the layout including parasitic resistances and capacitances. This netlist can be simulated and if the final behaviour fits the one expected from the first design, the final result is considered ready for fabrication.

2.5.2. Mismatch Effects

Mismatch is the process that causes random variations in physical quantities of identically designed devices [16]. Its effects normally cause variability in the final specification of a design and in the case of amplifiers it is the direct cause of a very famous non-ideality, the offset as well as CMRR and PSRR.

Despite the impossibility of avoiding those variations, their effects can be reduced in analog layouts:

- Using devices with large sizes.
- Using matching techniques at important parts of the circuit.

To identify which transistors caused more variability due to mismatch, Montecarlo simulations were done with the OTA. During this simulations, it was found that matching was important between transistors forming part of the differential pair and the current sources. In the case of cascode transistors, mismatch effects were not critical.

Thereby, the design was divided in several groups in order to apply the matching techniques between the devices.

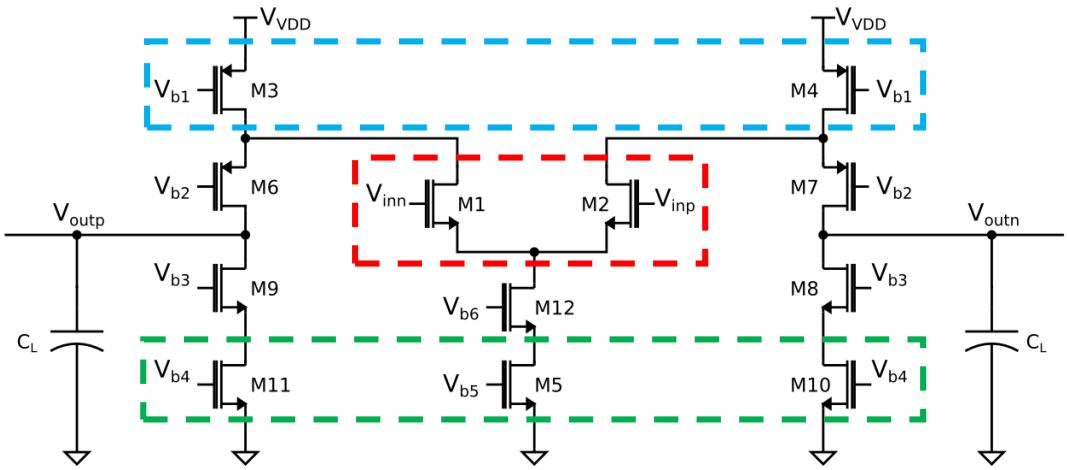


Figure 2.28: Group considered to apply matching techniques between transistors

For the differential amplifier the groups for matching are:

- The differential pair.
- The PMOS current sources.
- The NMOS current sources.

In the case of the cascode transistors, whose matching is not so critical, it was intended to imbricate them inside the matching pattern of the nearest current source when possible. In some cases, they were separated and placed in independent groups.

As for the CMFB, similar groups were made. However, additional groups were added too:

- Source degeneration resistors.
- Resistors from the compensation network.
- Capacitors from the compensation network.

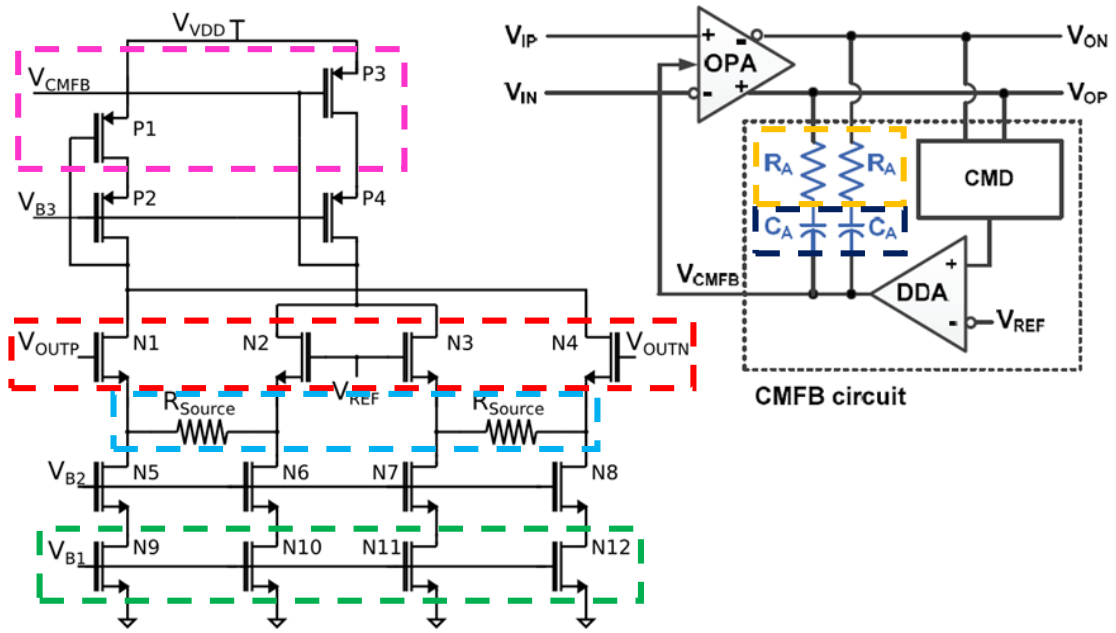


Figure 2.29: Matching Groups for the CMFB Amplifier

2.5.3. Matching Techniques

When good matching between devices is desired, the techniques to achieve it imply interdigitation and the use of common centroid patterns [15].

Interdigitation means to split the devices to match into smaller ones and array them along one dimension.

When placed, they normally follow a pattern to ensure that any kind of variations is suffered equally by the devices. To do so, matched devices share the same centroid and the same symmetry axis.

The rules to have proper matching between devices can be summarized in the following points [15]:

- **Coincidence**. The centroids of the matched devices should coincide.
- **Symmetry**. The array should be symmetric around both the X and Y axes.
- **Dispersion**. The array should exhibit the highest possible degree of dispersion.
- **Compactness**. The array should be as compact as possible.
- **Orientation.** Each matched device should consist of an equal number of segments oriented in either direction.

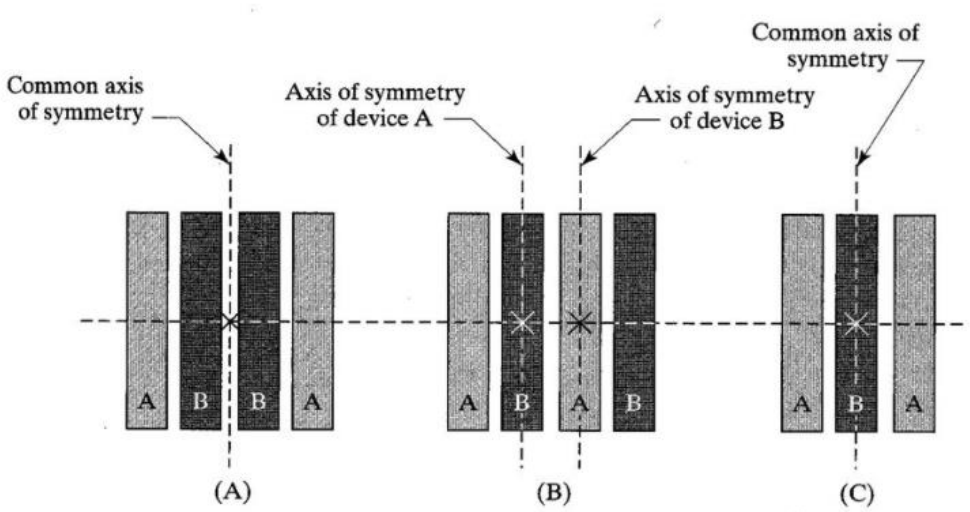


Figure 2.30: Example of interdigitated transistors A and B. Cases A and C show an interdigitation with common centroid whereas case B is an example of interdigitation without common centroid [15]

As for the techniques used in our design, the interdigitation and general patterns used to place the fingers are depicted in Table 2.21, Table 2.22 and Table 2.23 as well as some captures of the layout showing the result after applying those techniques in figures Figure 2.31 and Figure 2.32.

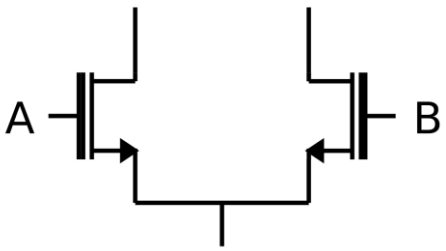
DIFFERENTIAL PAIR	***PATTERN***
	*…ABBA ABBA | ABBA ABBA…* *…BAAB BAAB | BAAB BAAB…* *…BAAB BAAB | BAAB BAAB…* *…ABBA ABBA | ABBA ABBA…*

Table 2.21: Matching pattern for differential pairs

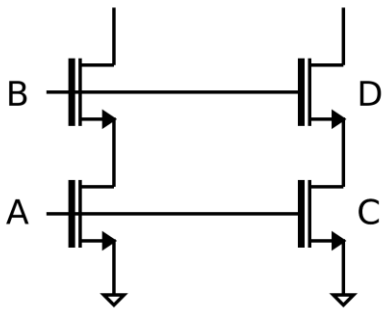
CASCODED CURRENT SOURCE	***PATTERN***
	*…DC ABBA CDDC AB | BA CDDC ABBA CD…* *…BA CDDC ABBA CD | DC ABBA CDDC BA…* *…BA CDDC ABBA CD | DC ABBA CDDC BA…* *…DC ABBA CDDC AB | BA CDDC ABBA CD…*

Table 2.22: Matching pattern for current sources with their cascodes included inside the pattern

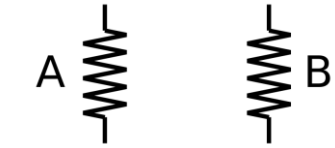
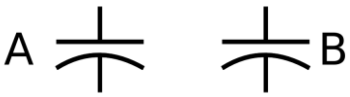
RESISTORS & CAPACITORS	*PATTERN*
	*…ABBA | ABBA…* *…BAAB | BAAB…*
	

Table 2.23: Matching pattern used for resistors and capacitors

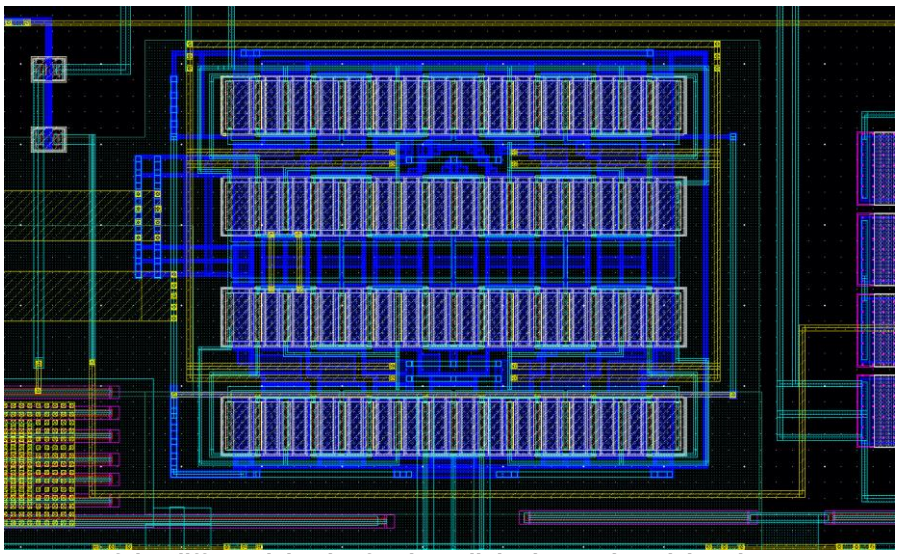


Figure 2.31: Layout of the differential pair after interdigitation and applying the correspondent pattern to have common centroid

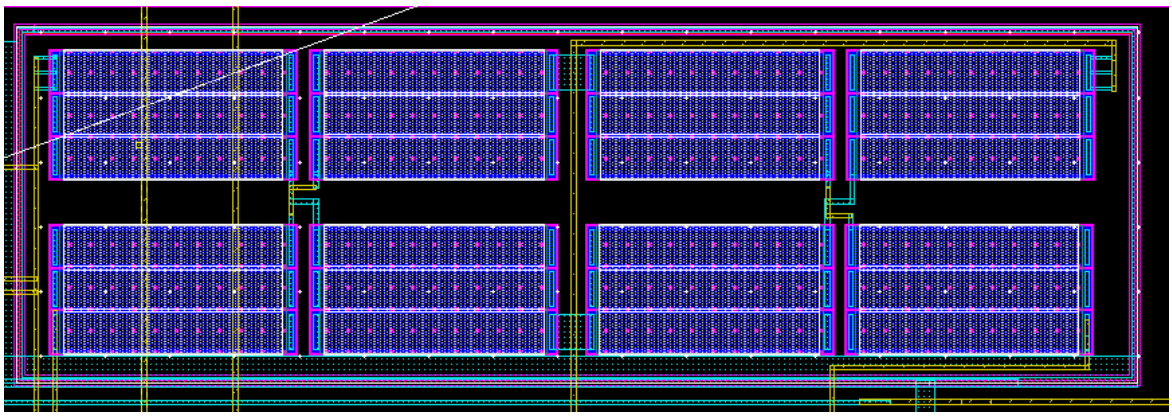


Figure 2.32: Layout of the source degeneration applying the interdigitation and matching pattern

2.5.4. Layout Result

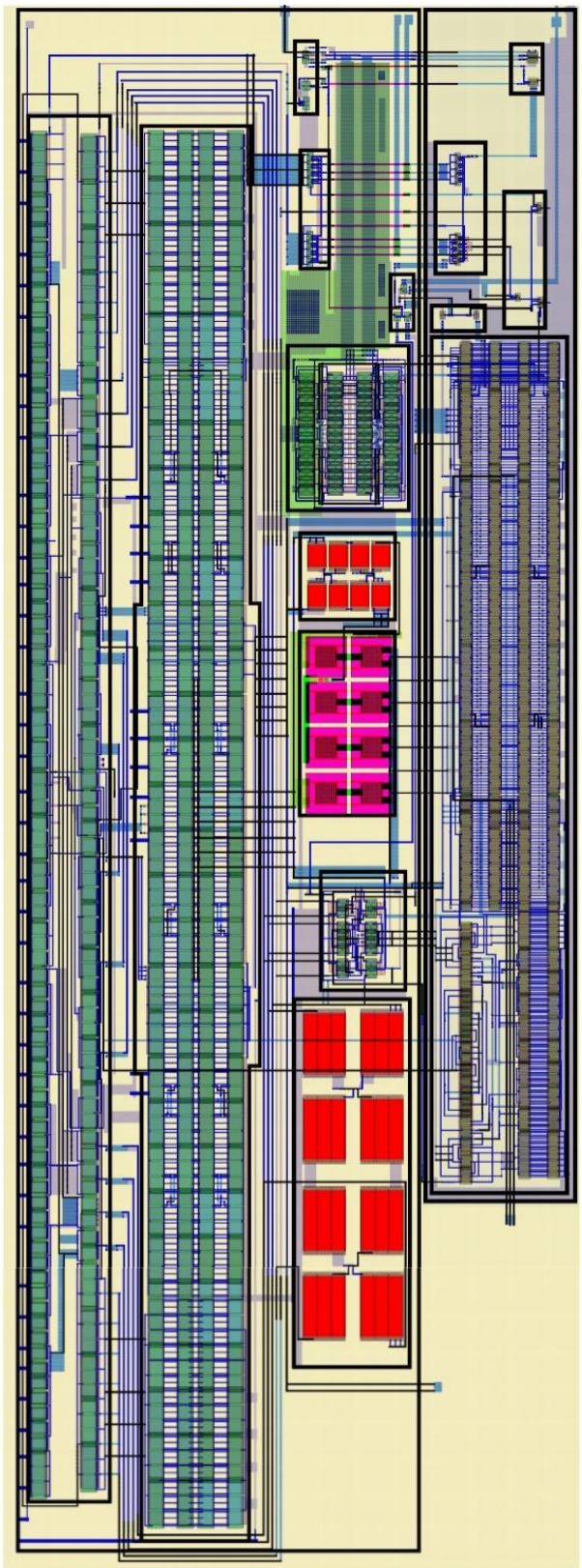


Figure 2.33: Final Layout

As mentioned in section 2.5.4, the design was divided in several groups taking into account matching considerations, and when placing them it was intended to have a routing as simple as possible.

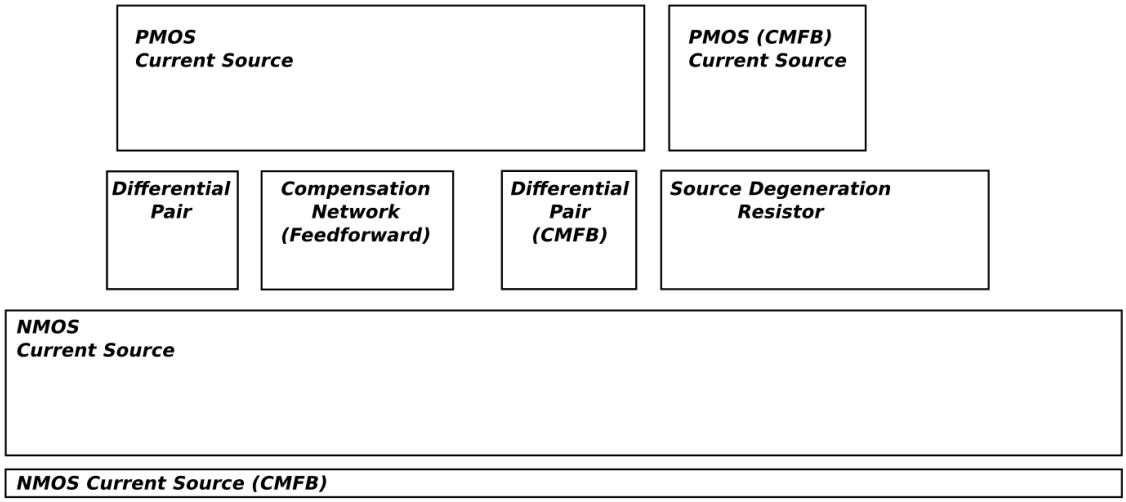


Figure 2.34: Implemented floorplan when elaborating the layout

Concerning the final area occupied, it turns out to be 367.5 µm x 135.46 µm, which represents a 44% of the area occupied by the smallest magnetometer.

Because of the large area occupied by the sensors, the layout size was not a critical issue since it was already expected to have a chip with large area due to the magnetometers. Therefore, the actual area of the OTA can be accepted.

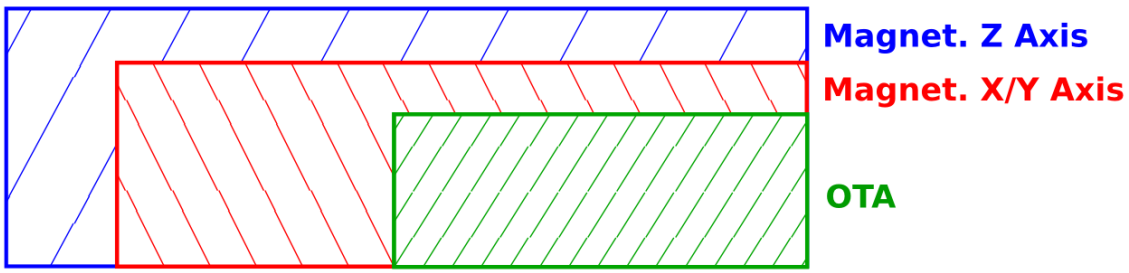


Figure 2.35: OTA Layout area compared with the area occupied by the sensors

Cell	*Dimensions*	*$Area_{OTA}/Area_{Sensor}$*
OTA	*367.5 µm x 135.46 µm*	*-*
Magnet. X/Y Axis	*615 µm x 182 µm*	*44%*
Magnet. Z Axis	*714 µm x 230 µm*	*30%*

Table 2.24: Dimensions of the designed OTA and the magnetometers

2.5.5. Post Layout Simulation

Once the layout had passed DRC and LVS, a post-extraction simulation of our layout was performed to compare the behaviour with the original design. From the extracted netlist it is expected a slight reduction of the specs, since the previous design did not consider any parasitic element.

When comparing the simulation results with the original design, the only remarkable differences are a slight reduction in:

- The Unity Gain Frequency from 136 MHz to 126.44 MHz.
- The Phase Margin from 62º to 61º.

PARAMETER	UNITS	TYP	COMMENTS
Voltage Supply	*V*	*3.3*	
GBW	*MHz*	*126.44*	*Simulation at T=27 ºC*
Gain_130k	*dB*	*60.24*	*Simulation at T=27 ºC*
PM	*Degrees*	*61.75*	*Simulation at T=27 ºC*
InputNoise130k	$nV/\sqrt{Hz}$	*9.65*	*Simulation at T=27 ºC*
CMRR_300K	*dB*	*94.67*	*Simulation at T=27 ºC*
PSRR+out_300K	*dB*	*-24.31*	*Simulation at T=27 ºC*
PSRR-out_300K	*dB*	*-31.73*	*Simulation at T=27 ºC*
VCM	*V*	*1.62*	*Simulation at T=27 ºC*

Table 2.25: Simulation results from post-extracted version of the OTA

Apart from these differences, the OTA works as expected. Hence, the layout can be considered finished.

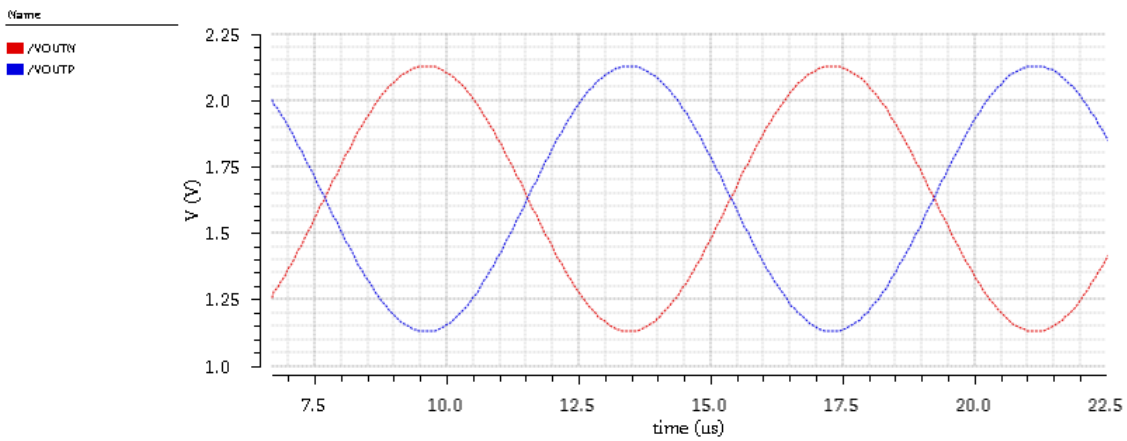


Figure 2.36: Output of the amplifier delivering 1 V_{pp} of output at 130 kΩ after post extraction simulation

3. Programmable Floating Current Source

3.1. Current Source Description

In order to implement the current source that provide $I_{LORENTZ}$, the designed circuit includes a floating current source with cascoded current mirrors, switches in bridge topology and a CMFB regulator to control the DC operation point as depicted in Figure 3.1.

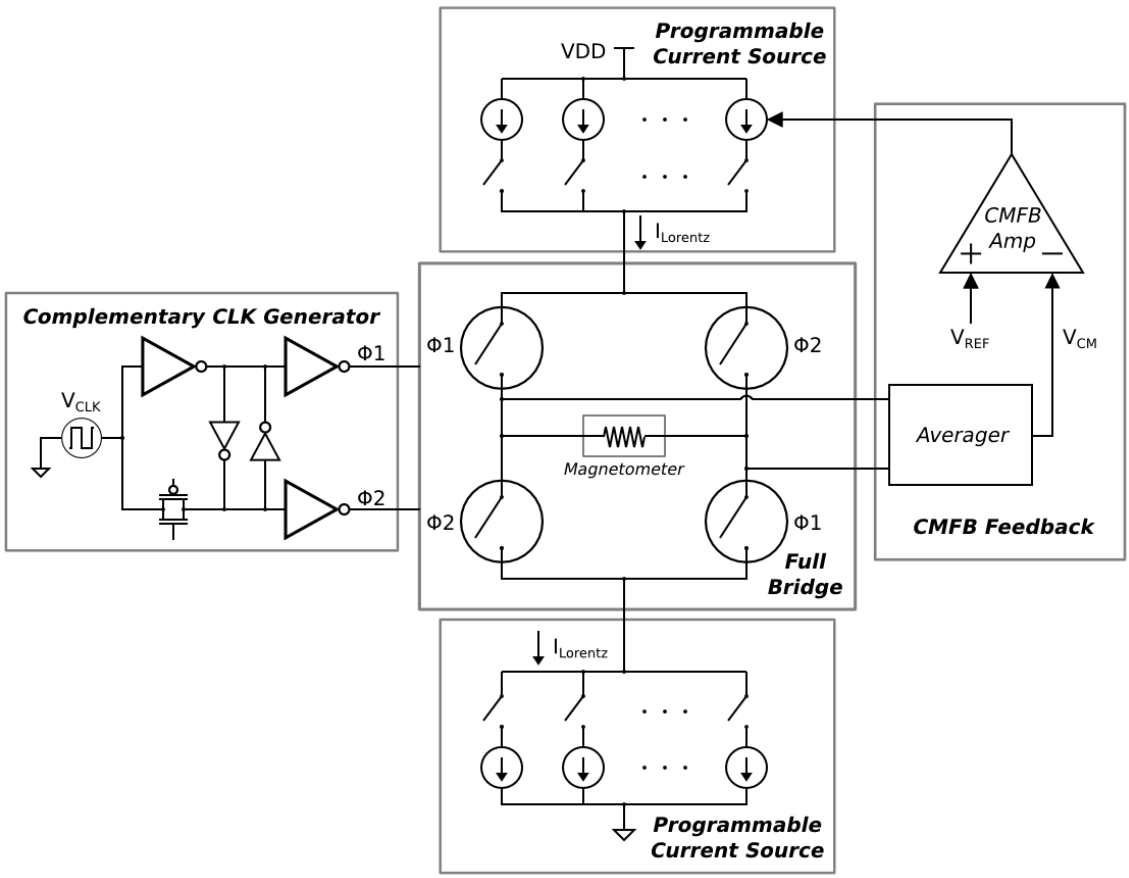


Figure 3.1: Block diagram implemented to design the Programmable Floating Current Source

Required Specifications

To provide proper excitation of the magnetometer, the specifications provided in Table 3.1 are set for the design of the current source.

Specifications	Min	Nom	Max	Units
Voltage Supply (V_{DD})	-	*3.3*	-	*V*
Reference Bias Current	-	*10*	-	*µA*
Lorentz Current	*8*	-	*1000*	*µA*
Output Load Resistance	*1.3*	-	*1.6*	*kΩ*
Parasitic Capacitance	*2*	-	*10*	*pF*
Rise/Fall Time	-	*150*	-	*ns*
Switching Peaking	-	*10*	-	*%*
Programmability	-	*8*	-	*Bits*
Gain Error	-	*1*	-	*% FSR*

Table 3.1: Table of Specs for the Current Source

3.1.1. Magnetometer Model

From the electrical point of view, the magnetometer is expected to offer some electrical resistance and capacitance. For simulation purposes, the magnetometer has been modelled as depicted in the schematic of Figure 3.2.

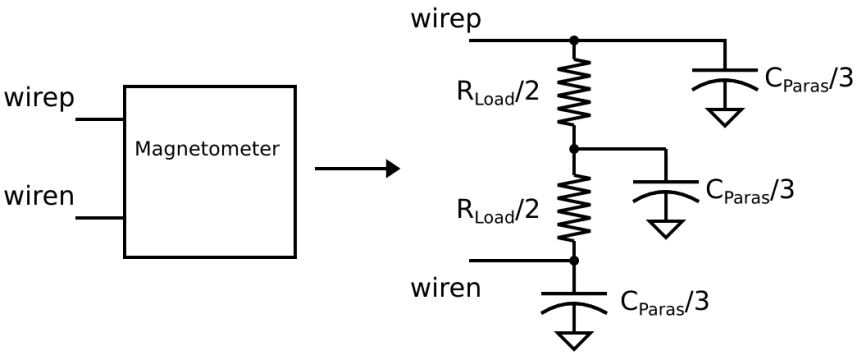


Figure 3.2: Schematic used to model the magnetometer

The expected values of the resistance and the capacitance of the whole sensor appear in Table 3.2. These values are shared between the 2 resistances and the 3 capacitors of the model.

Parameter	***Minimum Value***	***Maximum Value***
Resistance (R_{Load})	1.3 kΩ	1.6 kΩ
Capacitance (C_{Paras})	2 pF	10 pF

Table 3.2: Electrical characteristics of the sensor used for simulation

3.2. Current Mirror Topology

3.2.1. Low-voltage topology

As in the OTA, a cascoded current mirror with improved dynamic range is used to implement the current sources. Similar to the amplifier case, the cascode biasing with several transistors in series. Here cascodes and current mirrors have identical aspect ratios.

$$\left|\frac{W}{L}\right|_{Cascode} = \left|\frac{W}{L}\right|_{CS} \tag{3.1}$$

About the biasing voltage for cascodes, it is generated with a MOS transistor in diode configuration. Its aspect ratio is 5 times lower than the cascode in order to guarantee that both transistors are in saturation.

$$\left|\frac{W}{L}\right|_{BiasCascode} = \frac{\left|\frac{W}{L}\right|_{CS}}{5} \tag{3.2}$$

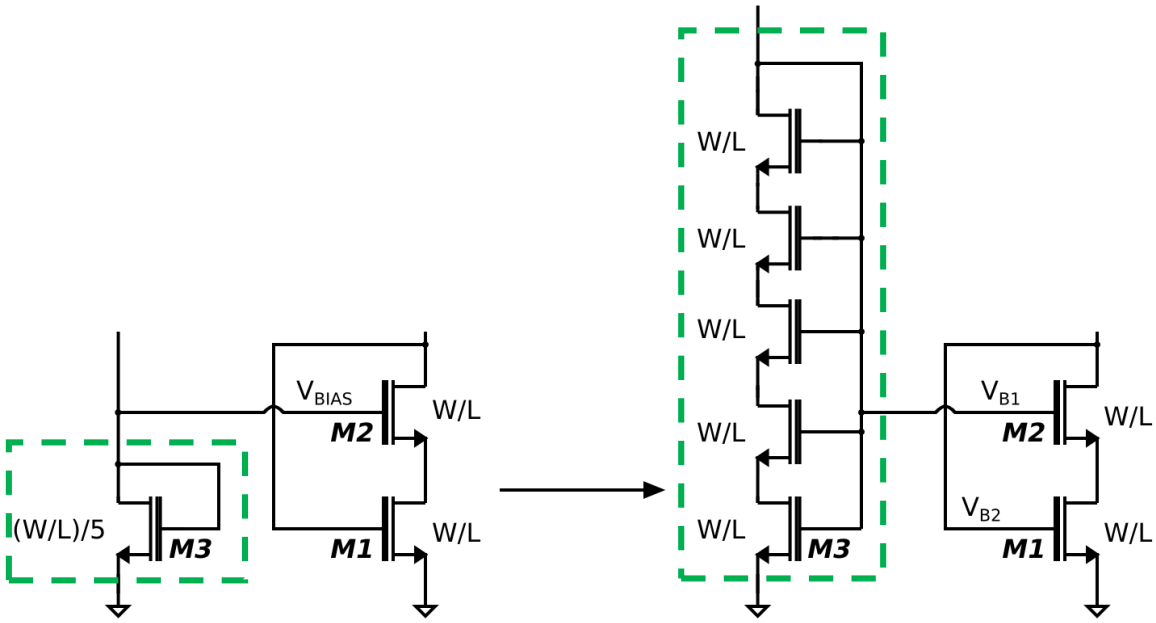


Figure 3.3: Schematic to generate biasing for the NMOS current sources (VB2) and their cascodes (VB2)

Biasing circuit for Current Mirrors and Cascodes					
Instance	***Type***	***Width [µm]***	***Length [µm]***	***Multiplier***	***Aspect Ratio***
(M1) Biasing for Current Mirror	*NMOS3V*	*2*	*1*	*5*	*10*
(M2) Current Mirror Cascode	*NMOS3V*	*2*	*1*	*5*	*10*
(M3) Biasing for Cascodes	*NMOS3V*	*2*	*1*	*5*	*1 (5parallel/5series)*
Biasing for Current Mirror	*PMOS3V*	*2.5*	*1*	*4*	*10*
Current Mirror Cascode	*PMOS3V*	*2.5*	*1*	*4*	*10*
Biasing for Current Mirror	*PMOS3V*	*2.5*	*1*	*4*	*4/5 (4parallel/5series)*

Table 3.3: Sizes for the transistors of the biasing circuit for all NMOS current mirrors

3.2.2. Programmability

The design includes 2 sources whose current is adjustable by using 3 bits allowing 8 possible current values.

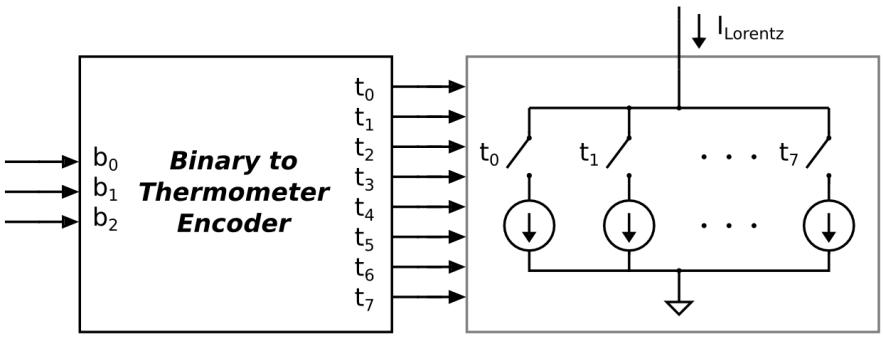


Figure 3.4: Approach used to implement the programmable current source

To control the current, externally an unsigned binary value should be provided. After that, the binary value is converted to thermometer code. Finally, every bit of the thermometer code is used by one of the current sources. The structure resembles to the approach normally used for unary weighted DACs, as shown in Figure 3.4.

This way, we have control over the increase of current injected to the sensor. In our case it was desired that each step of current was the double of the previous one.

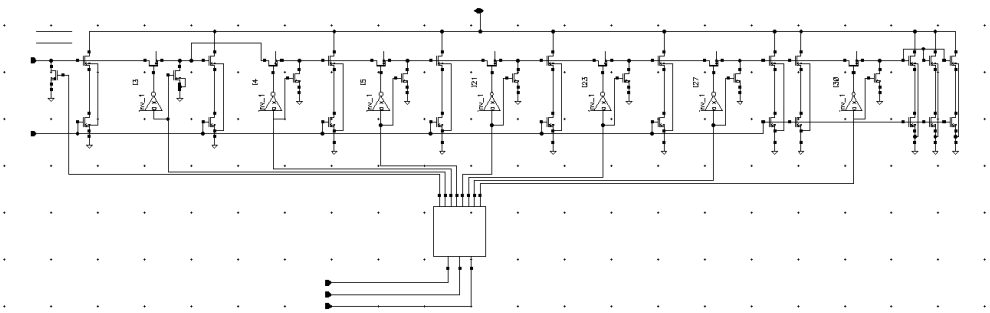


Figure 3.5: Programmable current source with NMOS transistors

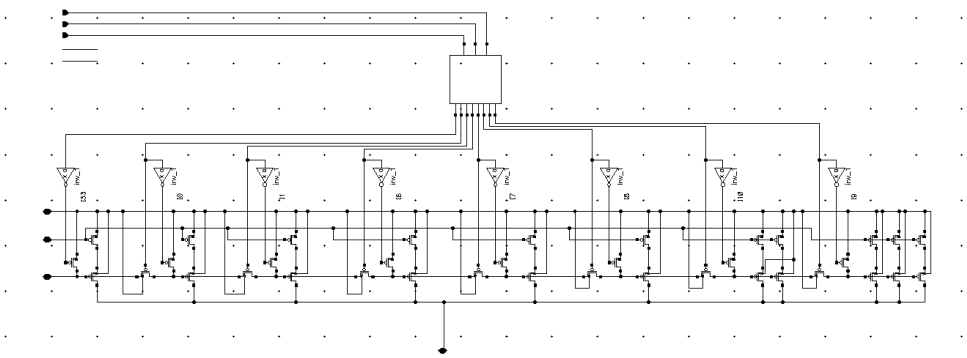


Figure 3.6: Programmable current source with PMOS transistors

Binary Code [b2b1b0]	Thermometer [t6t5t4t3t2t1t0]	Output Current [µA]
000	1111111	8
001	1111110	16
010	1111100	32
011	1111000	64
100	1110000	128
101	1100000	250
110	1000000	500
111	0000000	1000

Table 3.4: Output current depending on the input binary code

As for the binary to thermometer encoder, it's entirely made with combinational logic. The logic gates used are depicted in Figure 3.7.

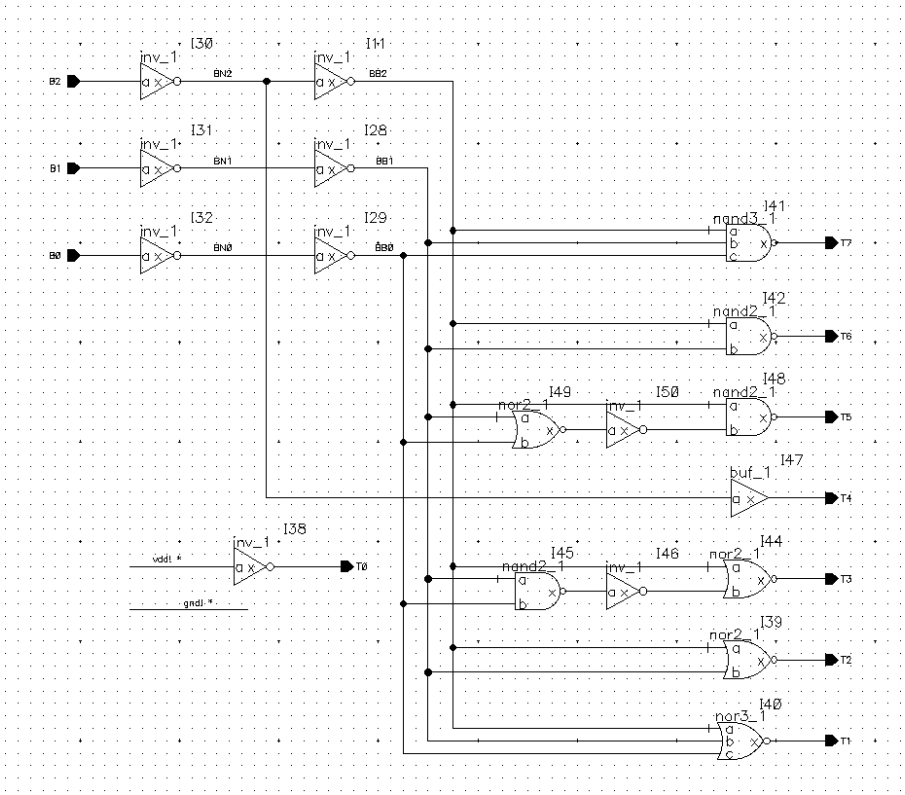


Figure 3.7: Binary to Thermometer encoder

3.3. Common Mode Feedback Amplifier

Similar to the case of the OTA, to control de DC voltage of the magnetometer, a common mode feedback amplifier is used. This topology is chosen to avoid using resistors in parallel to the magnetometer.

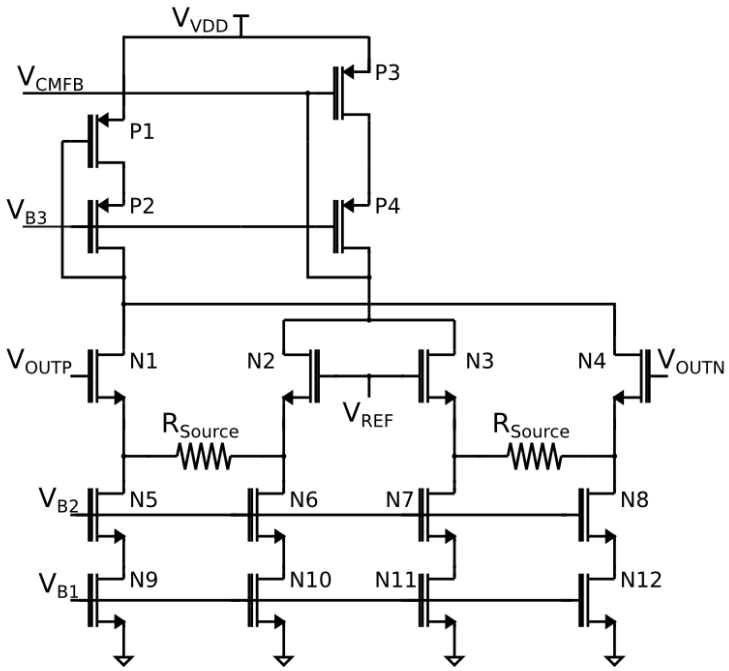


Figure 3.8: CMFB Amplifier

CMFB's Differential Amplifier					
Instance	***Type***	***Width[µm]***	***Length[µm]***	***Multiplier***	***Aspect Ratio***
N1	***NMOS 3V***	*2*	*0.350*	*4*	*22.86*
N2	***NMOS 3V***	*2*	*0.350*	*4*	*22.86*
N3	***NMOS 3V***	*2*	*0.350*	*4*	*22.86*
N4	***NMOS 3V***	*2*	*0.350*	*4*	*22.86*
N5	***NMOS 3V***	*2*	*1*	*4*	*8*
N6	***NMOS 3V***	*2*	*1*	*4*	*8*
N7	***NMOS 3V***	*2*	*1*	*4*	*8*
N8	***NMOS 3V***	*2*	*1*	*4*	*8*
N9	***NMOS 3V***	*2*	*1*	*4*	*8*
N10	***NMOS 3V***	*2*	*1*	*4*	*8*
N11	***NMOS 3V***	*2*	*1*	*4*	*8*
N12	***NMOS 3V***	*2*	*1*	*4*	*8*
P2	***PMOS 3V***	*2.5*	*1*	*8*	*20*
P4	***PMOS 3V***	*2.5*	*1*	*8*	*20*
P1	***PMOS 3V***	*2.5*	*1*	*8*	*20*
P3	***PMOS 3V***	*2.5*	*1*	*8*	*20*

Table 3.5: Transistor Sizes for the CMFB

Like in the Folded Cascode case, source degeneration was introduced to enhance the linearity of the differential pair. It proved to be useful for the cases where voltage drop along the sensor was maximum ($I_{LORENTZ}$=1 mA) where the loop is still able to fix the output DC voltage at 1.65 V.

To determine which percentage of current should be controlled by the CMFB, a Montecarlo simulation has been performed on the current sources. The results of the simulation are shown in Table 3.6.

Bin Code	*Current Source*	*Min [µA]*	*Mean [µA]*	*Max [µA]*	*σ [µA]*
000	***NMOS Source***	7,554	8,18	8,88	0,2128
	PMOS Source	7,355	8,126	8,774	0,2697
001	***NMOS Source***	15,43	16,37	17,34	0,3761
	PMOS Source	14,86	16,26	17,66	0,5088
010	***NMOS Source***	30,91	32,72	34,29	0,6448
	PMOS Source	29,86	32,55	35,48	0,981
011	***NMOS Source***	62,24	65,42	68,12	1,268
	PMOS Source	59,68	65,07	70,88	1,948
100	***NMOS Source***	125,1	130,9	136,2	2,467
	PMOS Source	119,7	130,1	141,1	3,866
101	***NMOS Source***	250	261,7	272,4	4,88
	PMOS Source	239,5	260,2	281,5	7,764
110	***NMOS Source***	487,8	511,59	511,1	10,36
	PMOS Source	464	508,34	507,7	16,12
111	***NMOS Source***	977,7	1023	1065	19,04
	PMOS Source	934,1	1017	1101	30,25

Table 3.6: Results of Montecarlo for different current values

From the results, our criteria is that our CMFB should be able to control an amount of current equivalent to 5σ. This represents approximately a 15% of the current driven in each step.

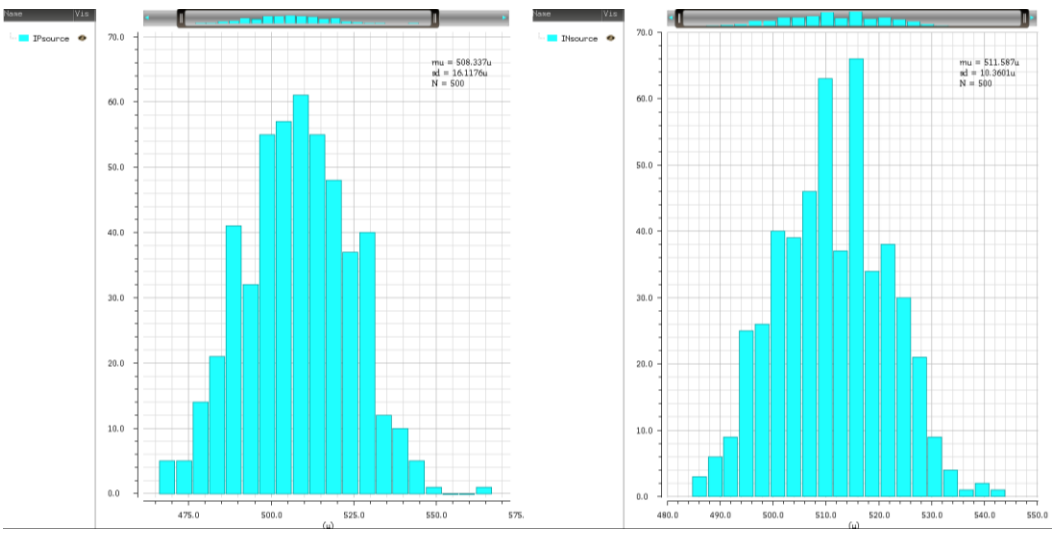


Figure 3.9: Montecarlo Simulation considering only the programmable Current Sources without CMFB control at 500 uA. 5σ represents almost a 15% of the current driven by the programmable source

Finally, the current source has been included in the design and with the CMFB connected, the sensitivity against mismatch has been checked again. This time, the mean was 499.21 µA and the sigma 9.66 µA for a Montecarlo Simulation of 200 samples.

3.4. Switch Sizing

The switches of the full bridge are implemented with MOSFETs. When using them as switches, 2 important attributes should be considered:

- The voltage drop due to the resistance offered by the transistor.
- The charge injection caused by the intrinsic capacitance of the MOS transistor.

The voltage drop should be minimized in order to have enough margin for the current sources to work in saturation. To do so, transistors operating as switches should have an aspect ratio as high as possible to offer low resistance in ohmic mode.

$$R_{MOS} = \frac{1}{K\frac{W}{L}(V_{GS} - V_{th})} \tag{3.3}$$

About the charge injection, this effect of the MOS transistor causes peaking at the output current waveform. Each time a digital signal drives the gate of a MOS transistor, the gate oxide capacitance injects a charge Q_I to the channel of the transistor [17] and the amount is proportional to the area of the transistors. To minimize it, the switch's area should be as small as possible.

$$Q_I = C'_{OX} \cdot W \cdot L \cdot (V_{DD} - V_S - V_{THN}) \tag{3.4}$$

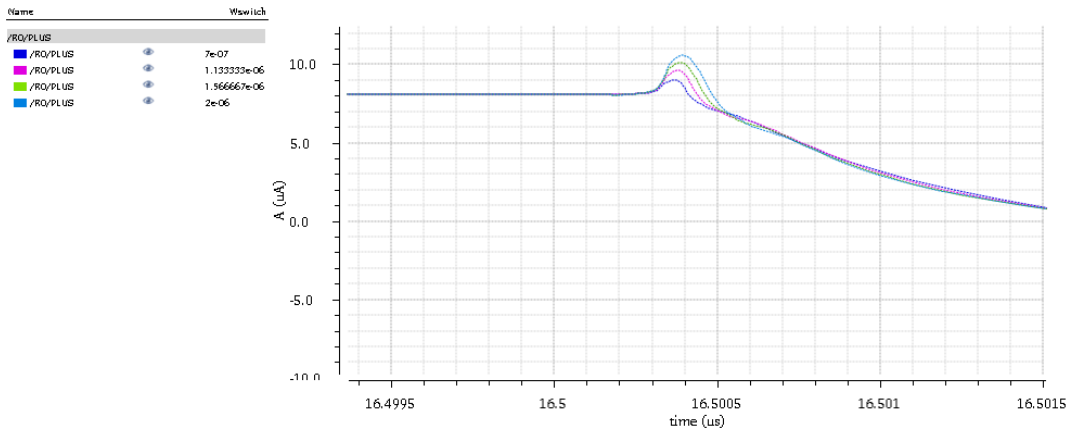


Figure 3.10: Peaking reduction when reducing the area to implement switches

From here, it is easy to recognize a trade-off between reducing charge injection and having a lower voltage drop. To deal with it, lowering the resistance was priorized when sizing and then, peaking was coped with alternative techniques like dummy half sized switches or synchronization stages for the control signals. The implemented sizes appear in Table 3.7.

	Size Width / Length	Multiplier	V_{DS} Drop [mV]
PMOS Switches	1.2µ / 0.3µ	16	263.2
NMOS Switches	0.6µ / 0.35µ	16	169.1

Table 3.7: Switch Parameters and Voltage drop when delivering 1mA

A total voltage drop of 432.3mV when Iout = 1 mA appears at the switches. Considering that the voltage drop at the magnetometer in the worst case is 1.6V, a supply voltage of 3.3 V leaves a margin of 1.27 V which is good enough to have both NMOS and PMOS current sources in saturation.

Dummy Switch

One of the most widely used solutions to deal with charge injection is the dummy switch [17]. This method basically consists in placing a transistor with drain and source shorted between the main switch and the node where we want to avoid charge injection as depicted in Figure 3.11.

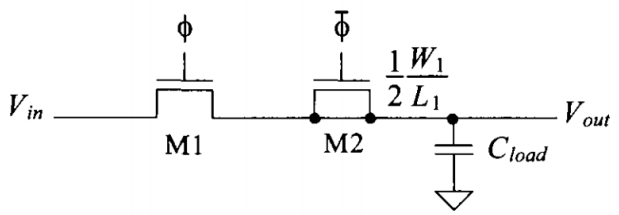


Figure 3.11: Dummy switch M2 used to minimize charge injection at Vout [17]

The idea is to use the dummy switch to compensate the charge injected or absorbed by M1 to C_{LOAD}: In consequence, the dummy switch M2 should:

- Work with the complementary signal that drives M1.
- Have half the aspect ratio of M1.

Figure 3.12 shows the reduction in the current peak when using this technique.

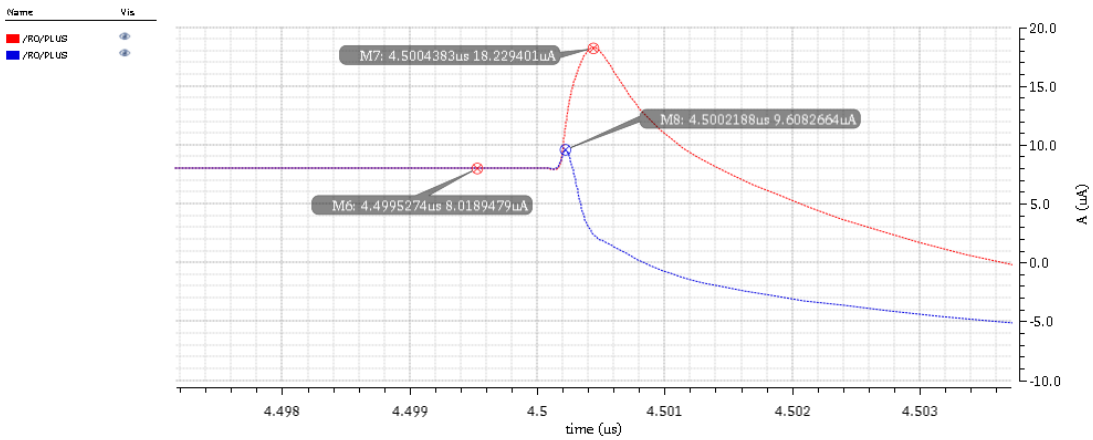


Figure 3.12: Difference in behaviour before and after using dummy switches

3.5. Timing Block

Finally, the last block of the design is the Timing Block to control the phases of the switching. Basically, the phases are controlled by 2 signals, Φ_1 and Φ_2, complementary between them and with no skew between them, running at 300 kHz. They are generated from a CLK signal at the same frequency. In spite of being 130 kHz the expected resonance frequency of the sensor, the design is simulated at 300 kHz to make sure that the block works at twice the resonance frequency. The purpose is to make possible the use of other modulations in order to read the response of the sensor.

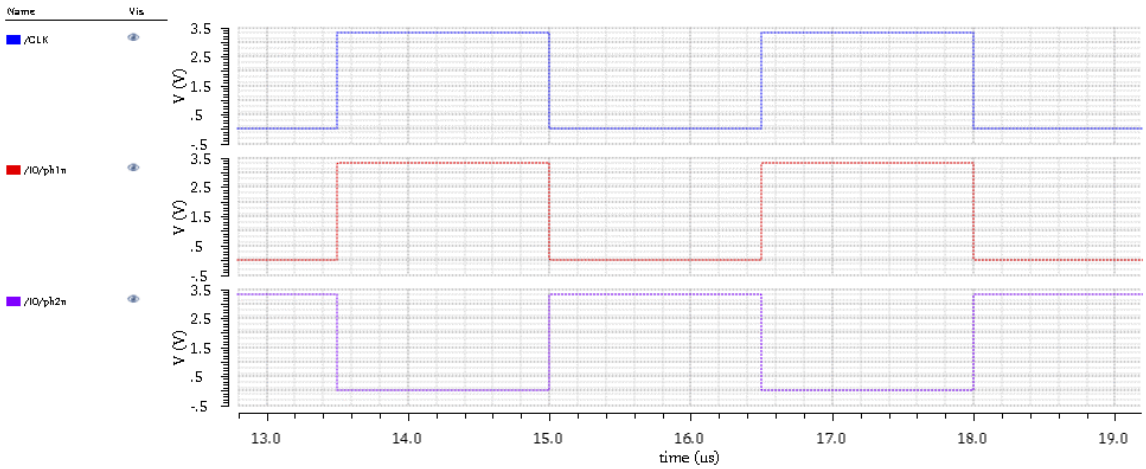


Figure 3.13: Expected phases ph1 and ph2 obtained from the CLK signal

When applying the control signals to the switches, the 2 possible states for the bridge are depicted in Figure 3.14. Basically, the bridge changes the direction of the current which results in a squared waveform for the Lorentz Current.

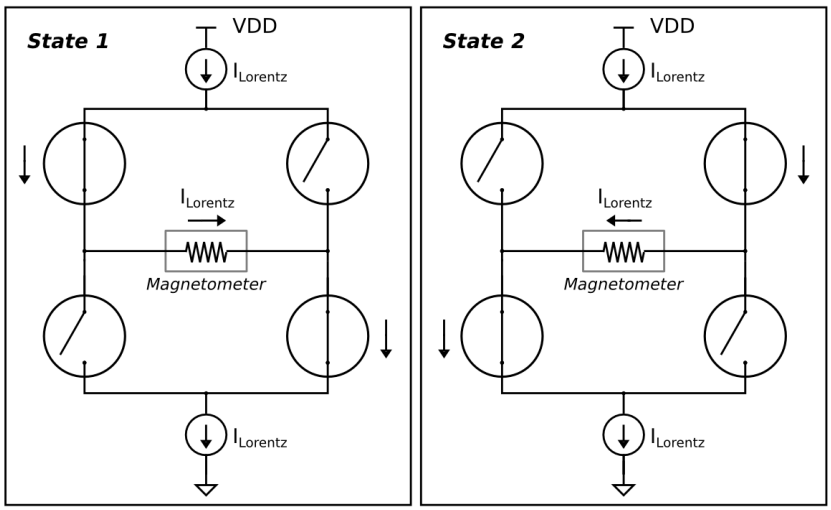


Figure 3.14: Possible States for the Full Bridge when delivering a square current waveform

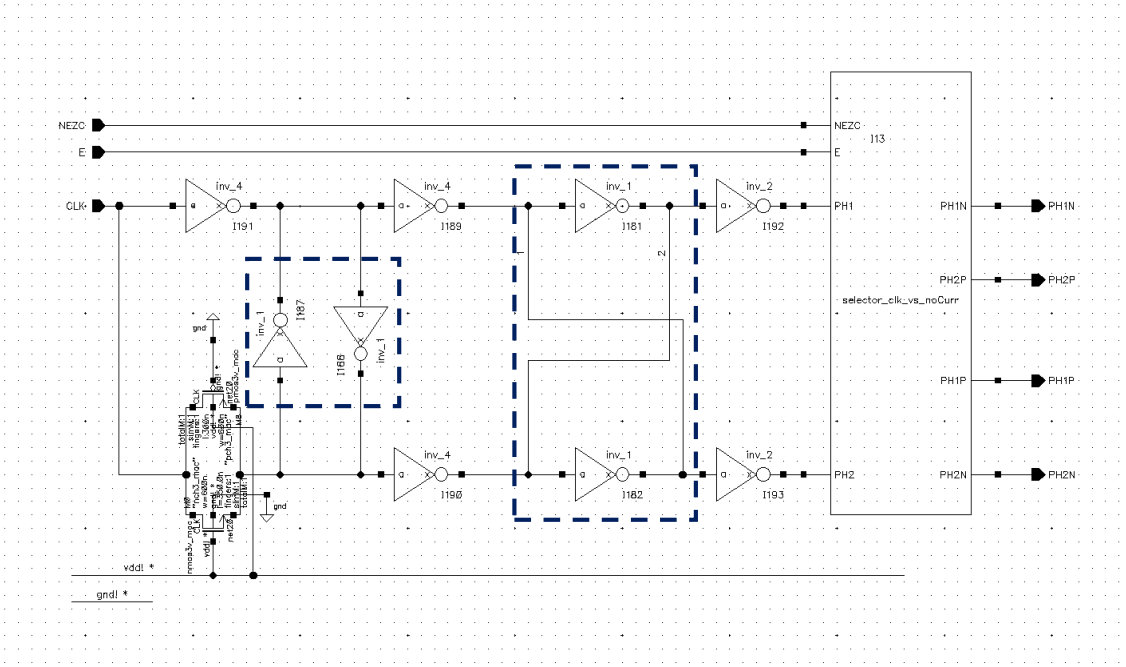


Figure 3.15: Timing Block Schematic

Despite only requiring 2 signals to control the bridge, the timing block has 4 outputs. The reason is to take into account the disable (E='0') and the zero current mode (NEZC='1'). Depending on the operating mode, the timing block will deliver the complementary clock to the switches or proper logic values to disable them. To do so, a selector is placed inside the timing block just before the outputs.

The logic gates inside the selector are shown in Figure 3.16 and the expected values for the output depending on the mode are indicated in Table 3.8.

Outputs	***E = '1'***	***E = '0' or NEZC = '1'***
ph1p	Φ_1	*'0' (Disabled)*
ph1n	Φ_1	*'1' (Disabled)*
ph2p	Φ_2	*'0' (Disabled)*
ph2n	Φ_2	*'1' (Disabled)*

Table 3.8: Expected outputs of the timing block depending on the mode

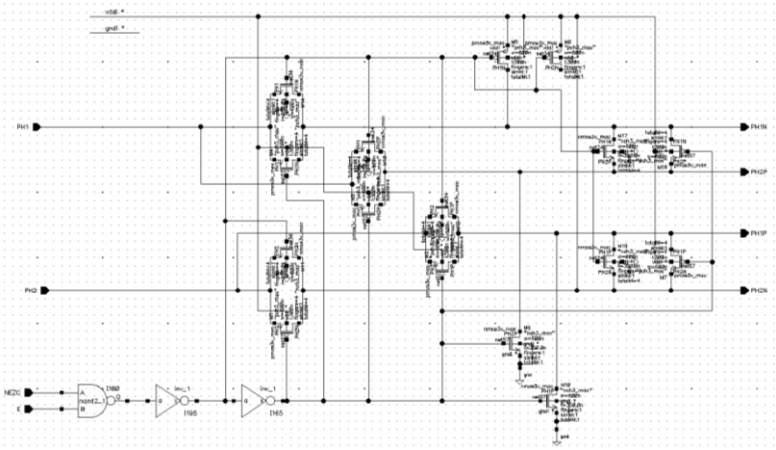


Figure 3.16: Schematic of the selector

3.5.1. Phase alignment between complementary signals

When generating the phase signals, having no skew between them is a desirable feature since it contributes to minimize the output current peaks.

To force phase alignment, some latches are placed between Φ_1 and Φ_2 path as depicted in Figure 3.15. Their positive feedback forces their output to change the output level at the same time. This is the effect that causes both signals to be much more complementary.

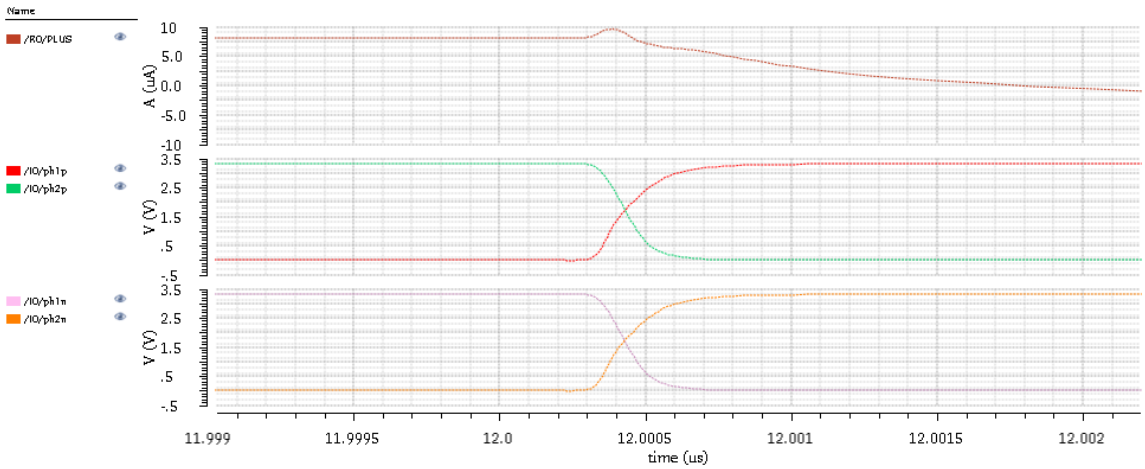


Figure 3.17: Timing block output signals with aligned edges

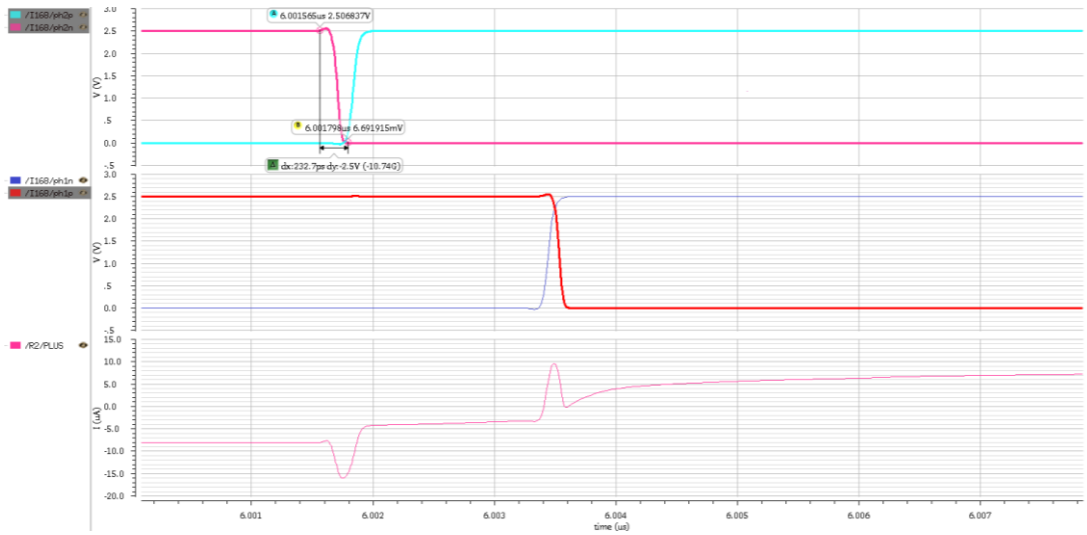


Figure 3.18: Timing of the switches without edge alignment

Figure 3.18 shows clearly that the control signals of the switches are the ones responsible for the peaking behaviour. However, this compensation is not perfect since any variation in the characteristics of the transistors can cause a slight difference between the edges and the glitches can be seen again.

3.5.2. Zero Current

The block is supposed to implement an AC current source. However, it is possible to have no current through the load by enabling the pin NEZC (Not Enable Zero Current). With this feature, we obtain a waveform with steps through zero.

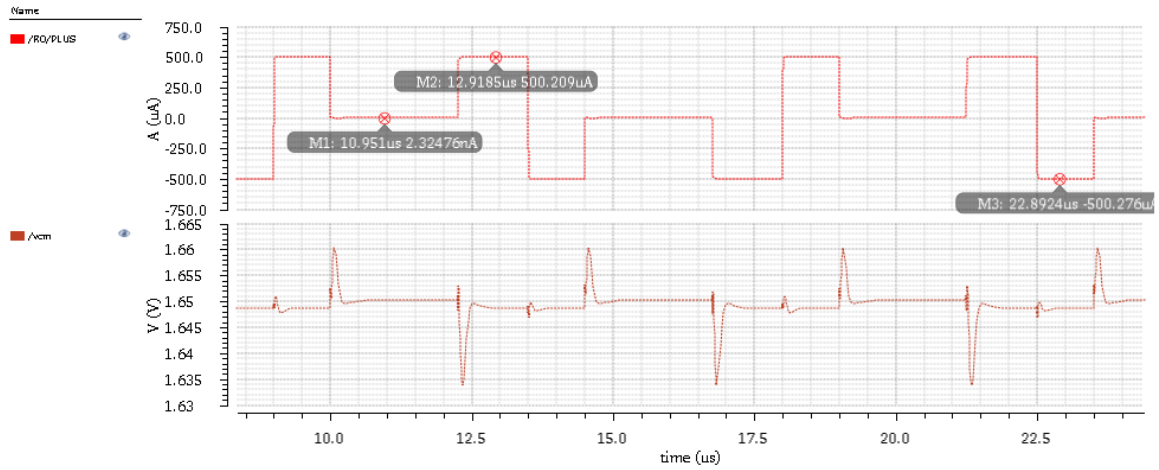


Figure 3.19: Lorentz current at 500 µA and zero current mode enabled. The current has intermediate steps by 0. Output DC voltage is still adjusted at 1.65 V.

The feature is enabled when NEZC is set to '0'. Despite having no current through the magnetometer, the block still has a current consumption equivalent to the typical working condition. This happens because to avoid current through the sensor, all the Lorentz current is being diverted to the switches and the whole bridge is conducting (see Figure 3.20).

This could have been implemented in an alternative way where the current provided by the programmable sources was shutoff. However, it was impossible to achieve fast rise and fall times of the current waveform as well as a lot of charge injection was introduced, which affected to the peaks of the current source. This mode is not related at all with the disable mode of the whole floating current source.

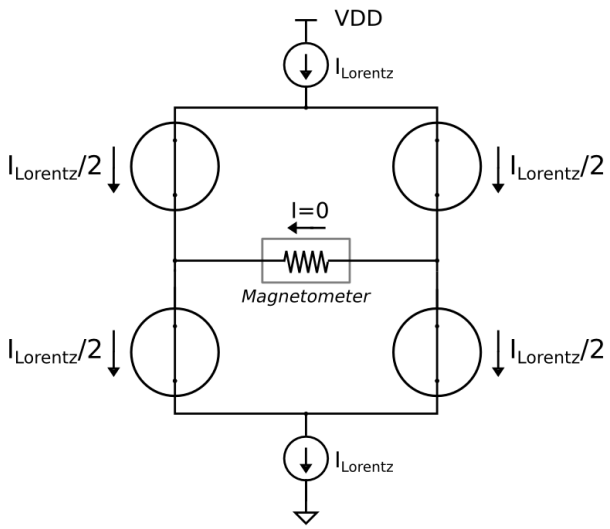


Figure 3.20: Implemented approach to have Zero current in the waveform

3.6. Programmable Floating CS's Characteristics after Design

Some Features of the final design are:

- Programmable I_{OUT} current from 8 µA to 1 mA.
- Control of the common mode voltage of the load at $V_{DD}/2$.
- Zero consumption when the block is disabled.
- Fast enabling and disabling of the current when supplying the load.
- General Enable to disable the IP and offer 0 current consumption.

General Enable Pin

As in the case of the OTA, the Current Source can be disabled too. An Enable pin E is available. If E = '1', the OTA is operating whereas in the opposite case, the amplifier is shutoff. Like in the previous block, all the nodes of the circuit are driven to a fixed voltage (V_{DD} or GND) when disabled.

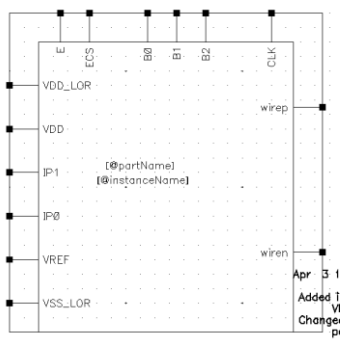
PIN	DESCRIPTION	Expected Range Value	SYMBOL
VDD	*Supply Voltage*	*3.3V*	
VDD_LOR	*Supply for Lorentz Curr*	*3.3.V*	
VSS_LOR	*Ground for Lorentz Curr*	*0V*	
E	*Enable General Block*	*3.3V*	
NEZC	*Not Enable Zero Current*	*0V – 3.3V*	
CLK	*Clock Signal*	*0V – 3.3V*	
IP1	*Current Reference 1*	*10uA*	
IP0	*Current Reference 0*	*10uA*	
VREF	*Reference Voltage for CMFB*	*1.65V*	
B[2:0]	*Bits to select $I_{LORENTZ}$*	*"000" – "111"*	
wirep	*Positive pin to connect the sensor*	*0V – 2.45V*	
wiren	*Negative pin to connect the sensor*	*0V – 0.85V*	

Table 3.9: Pinnout of the Lorentz Current Source

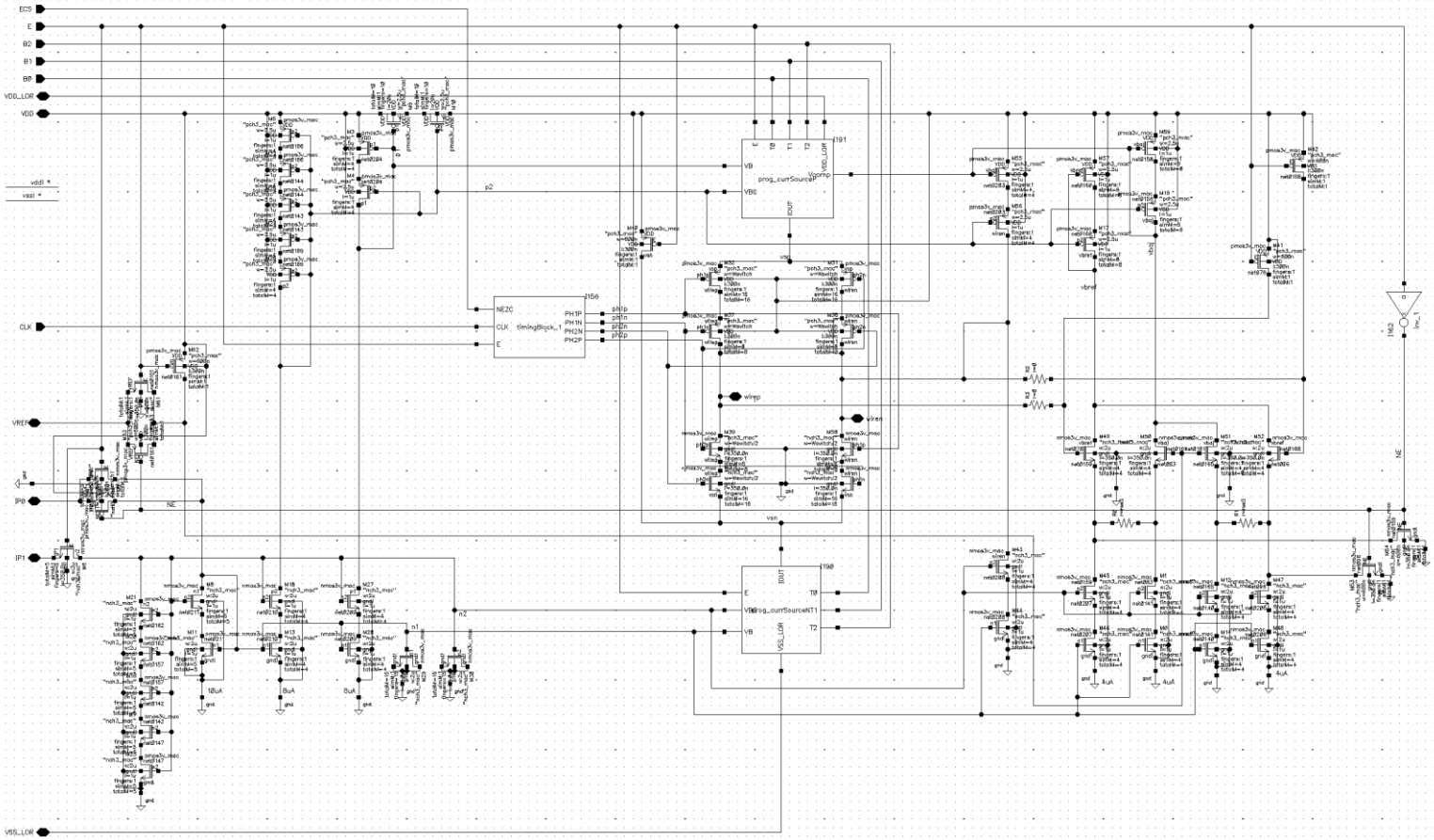


Figure 3.21: Current Source Schematic

PARAMETER	CONDITIONS	UNITS	MIN	TYP	MAX	COMMENTS
Voltage Supply		V		3,30		
Ref Bias Current		µA		10,00		
Current Consumption		µA	25,35	26	27,06	Without the Lorentz Current. Simulated at T =[-30 ºC, 27 ºC, 100 ºC] for corners ff, ss, fs, sf and 20 Montecarlo Iterations.
Lorentz Current	B2B1B0 = "111"	µA	959,2	992,20	1025	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100 ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = "110"	µA	478,9	497	516,7	R=1.6 kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100 ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = "101"	µA	252,90	257,34	265,90	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = "100"	µA	123,30	127,10	132,30	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = "011"	µA	61,94	63,51	66,11	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = "010"	µA	30,48	32,23	33,37	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = "001"	µA	15,51	16,12	16,13	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = "000"	µA	7,627	7,93	8,468	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
Load Resistance		kΩ	1,30		1,60	Expected load for the block. If Rload = 0, the block works but the provided specs are no longer guaranteed.
Parasitic Capacitance		pF	2,00		10,00	Expected parasitic capacitances of the load.
Current Rise/Fall Time	B2B1B0 = "111"	Ns	5,90	6,04	6,11	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC] for corners ff, ss, fs, sf. Average value of the corners
	B2B1B0 = "000"	Ns	5,95	6,32	6,63	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC] for corners ff, ss, fs, sf. Average value of the corners
Current Ena/Dis Time	B2B1B0 = "111"	Ns	105,38	109,90	114,00	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC] for corners ff, ss, fs, sf. Average value of the corners
	B2B1B0 = "000"	Ns	8,41	8,73	9,12	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC] for corners ff, ss, fs, sf. Average value of the corners
Switching Peaking [111]	B2B1B0 = "111"	%	0,01	0,08	0,18	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = "110"	%	0,06	0,16	0,27	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = "101"	%	0,06	0,33	0,82	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = "100"	%	0,07	0,75	1,67	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = "011"	%	0,20	1,76	3,41	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = "010"	%	0,98	3,94	7,47	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = "001"	%	4,92	8,57	12,32	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations

	B2B1B0 = “000”	%	10,89	19,71	27,19	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
Peaking Energy	B2B1B0 = “111”	fJ	0,026	0,37	0,063	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = “110”	fJ	0,031	0,38	0,062	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = “101”	fJ	0,027	0,04	0,062	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = “100”	fJ	0,029	0,049	0,079	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = “011”	fJ	0,037	0,075	0,12	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = “010”	fJ	0,067	0,13	0,19	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = “001”	fJ	0,15	0,193	0,25	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = “000”	fJ	0,222	0,244	0,27	R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
Programmability		Bit		3,00		Unsigned binary code
Gain Error	B2B1B0 = “111”	%			**4,08**	Expected value 1000uA. R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = “110”	%			**4,22**	Expected value 500uA. R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = “101”	%			**3,87**	Expected value 256uA. R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = “100”	%			**3,67**	Expected value 128uA. R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = “011”	%			**3,30**	Expected value 64uA. R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = “010”	%			**4,75**	Expected value 32uA. R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = “001”	%			**3,06**	Expected value 16uA. R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
	B2B1B0 = “000”	%			**5,85**	Expected value 8uA. R=1.6kΩ, Cp=10pF. Simulated at T=[-30ºC, 27ºC, 100ºC]; Corners ff, ss, fs, sf; Montecarlo 20 iterations
Temperature Sensitivity	B2B1B0 = “111”	nA/ºC		9,55		Obtained when ILorentz = 1mA

Table 3.10: Specifications of the Lorentz Current Source

3.7. Area estimation

Note: To make the area estimation, 2 assumptions have been made:

- All the transistors of the analog part will be interdigitated to get a better matching. Therefore, drain and source terminals will be shared.
- The drain and source contacts will occupy 600nm, twice the minimum length of the technology (for transistors with 3.3 V supply).

$$\text{Total Length} = \text{N}_{\text{Fingers}} \cdot \text{N}_{\text{Instances}} \cdot (\text{Length} + 0.6\mu) \tag{3.5}$$

$$\text{Area} = \text{Total Length} \cdot \text{Width} \tag{3.6}$$

Finally all the Areas have been added and the square root performed to provide an equivalent Square Length. This measurement would be the equivalent length of a squared layout that would occupy the same area than our layout.

CURRENT SOURCE							
PMOS	**Instances**	**Length [µm]**	**Width [µm]**	**Fingers**	**Total Length [µm]**	**Width [µm]**	**Area [µm^2]**
Ref Current	2	1	2,5	4	11,84	2,5	29,6
Ref Cascode	4	1	2,5	4	23,68	2,5	59,2
ThermSwitch	8	0,3	0,6	1	6,24	0,6	3,74
CurrSourceProg	1	1	2,5	500	740	2,5	1850
CurrSourceCascode	1	1	2,5	500	740	2,5	1850
CMFBCurrentSource	2	1	2,5	2	5,92	2,5	14,8
Switches	2	0,3	1	16	24,96	1	24,96
Dummy Switches	2	0,3	1	8	12,48	1	12,48
NMOS	**Instances**	**Length [µm]**	**Width [µm]**	**Fingers**	**Total Length [µm]**	**Width [µm]**	**Area [µm^2]**
Ref Current	2	1	2	5	14,8	2	29,6
Ref Cascode	4	1	2	5	29,6	2	59,2
Current Source	2	1	2	4	11,84	2	23,68
Cascode	2	1	2	4	11,84	2	23,68
ThermSwitch	8	0,35	0,7	1	6,64	0,7	4,648
CurrSourceProg	1	1	2	500	740	2	1480
CurrSourceCascode	1	1	2	500	740	2	1480
Switches	2	0,35	0,5	16	26,56	0,5	13,28
Dummy Switches	2	0,35	0,5	8	13,28	0,5	6,64

CMFB							
PMOS	**Instances**	**Length [µm]**	**Width [µm]**	**Fingers**	**Total Length [µm]**	**Width [µm]**	**Area [µm^2]**
CurrentSource	2	1	2,5	2	5,92	2,5	14,8
Cascode	2	1	2,5	2	5,92	2,5	14,8
NMOS							
CurrentSource	2	1	2	2	5,92	2	11,84
Cascode	2	1	2	2	5,92	2	11,84
Differential Pair	4	0,35	2	4	13,28	2	26,56

CAPS							
PCAP	2	30	30	1	60,96	30	1828,8
NCAP	2	30	30	1	60,96	30	1828,8

Total Area [µm2]	10702,952
Square Lenght [µm]	103,455

Table 3.11: Data obtained from the area estimation

4. Conclusions and future development

4.1. Conclusion

An Integrated Circuit design to perform an AC read-out of a CMOS-MEMS magnetometer at its resonance frequency (130 kHz) is presented in this master thesis.

The electronics include the Low Noise Amplifier with input referred noise below 10 $nV/\sqrt{Hz}$ to condition the sensor response as well as the 3-bit Floating Programmable Current Source to induce the Lorentz Force in the sensor and modulate its frequency. Up to 8 different current values from 8 µA to 1 mA are supported in order to control the magnetometer's sensitivity.

Both blocks are designed to be integrated on-chip with the sensor for a CMOS 180nm technology and in the case of the LNA, the design is made at both schematic and layout level with a final area of 368 µm x 136 µm, which represents a 44% of the sensor's surface (615 µm x 182 µm).

As for the Programmable Current Source, the design was made at schematic level and its estimated area is 103 µm x 103 µm, a 9.5% of the sensor's.

Furthermore, during the design of the differential LNA, a low consumption alternative to enhance linearity of the Common Mode Feedback (CMFB) loop was found. With this approach, based on a source degeneration of the differential pair, an error amplifier with low consumption, 53.3 µA, was achieved.

Finally, an optimal value for the degeneration resistor was found when linearizing the CMFB loop. As a result, a SFDR of 80dB was obtained.

4.2. Future Work

Due to time constraints in the framework of this master thesis, one of the main objectives was unfinished, the layout of the floating current source. It is important to notice that a technology migration (from IHP 240 nm to TSMC 480 nm) during the design development was produced, in order to be able to manufacture the MEMS devices. For future works related with the thesis, the remaining tasks pending are:

- Complete Layout Design of the Floating Current Source and the posterior verifications like DRC, LVS and post-layout simulation.
- Layout Design of the whole chip integrating both blocks with the magnetometers.
- Characterization of the system after manufacturing.

Bibliography

[1] H. Qu, «CMOS MEMS Fabrication Technologies and Devices,» *Micromachines,* 2016.

[2] «Markets and Markets,» May 2017. [En línea]. Available: http://www.marketsandmarkets.com/Market-Reports/mems-market-13689179.html.

[3] «Semiconductor Engineering,» [En línea]. Available: http://semiengineering.com/the-future-of-mems-sensor-design-and-manufacturing.

[4] O. B. H. Baltes, «CMOS-based Microsensors,» *Eurosensors XIV,* 2000.

[5] E. V. C. Y. e. a. M.Li, «Lorentz force magnetometer using a micromechanical oscillator,» *Applied Physics Letters,* 2013.

[6] K. Ogata, System Dynamics, Pearson Prentic Hall.

[7] K. M. David A. Johns, Analog Integrated Circuit Design, John Wiley & Sons, Inc..

[8] B. Razavi, Design of Analog CMOS Integrated Circuits, New York: McGraw-Hill, 2001.

[9] D. R. H. Phillip E. Allen, CMOS Analog Circuit Design, Oxford University Press, 2002.

[10] W. Sansen, Analog Design Essentials, Springer, 2006.

[11] P. M. Jack Ou, "A gm/ID Based Noise Optimization for CMOS Folded-Cascode Operational Amplifier," *IEEE Transactions On Circuits And Systems,* 2014.

[12] J. C. J. J. D. Louis Luh, «A Continuous-Time Common-Mode Feedback Circuit (CMFB) for High-Impedance Current Mode Application,» *IEEE,* pp. 347-350, 1998.

[13] Y.-K. C. a. B. H. Park, «Loop Stability Compensation Technique for Continuous-Time Common-Mode Feedback Circuits,» *ISOCC (IEEE),* pp. 241, 242, 2015.

[14] M. M. Zhang, «Effect of Nonlinearity in the CMFB Circuit that Uses the Differential-Difference Amplifier,» 2006.

[15] A. Hastings, The Art of Analog Layout, 2006.

[16] A. C. D. A. P. W. Marcel J.M. Pelgrom, «Matching properties of MOS Transistors,» *IEEE Journal Of Solid-State Circuits,* 1989.

[17] R. J. Baker, CMOS Circuit Design, Layout, and Simulation, Wiley.

Appendices

5. Derivation of expression for the CMFB's compensation network

Assumptions:

- The differential pair is simplified as 2 transistors, 1 with V_{REF} and the other with V_{CM} directly.
- Instead of V_{CM}, we are compensating a differential signal $V_{ERR} = V_{CM} - V_{REF}$. This assumption allows us to have virtual ground in the differential pair.

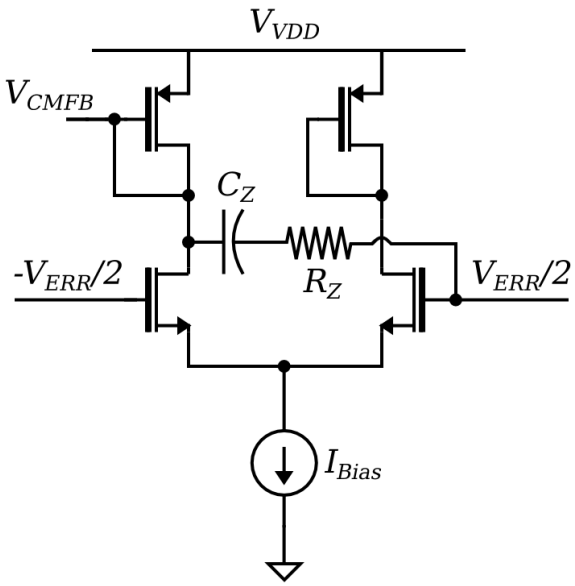


Figure 5.1: Simplified version of the CMFB amplifier used to obtain the equations

The initial equation relating the error voltage with V_{CMFB}, the biasing voltage applied to compensate V_{CM} would be the one indicated in equation (5.1).

$$\frac{v_{err}}{2}\left(g_{mn} + \frac{1}{Z_Z}\right) = \frac{1}{Z_{Pole}} v_{cmfb} \tag{5.1}$$

Considering Z_Z the impedance of the compensation network (equation (5.2)) and Z_{Pole} the impedance of the pole in node V_{CMFB} (equation (5.3)).

$$Z_Z = R_Z + \frac{1}{sC_Z} \tag{5.2}$$

$$Z_{Pole} = \frac{1}{g_{mp}} || \frac{1}{sC_X} \tag{5.3}$$

The following development leads to an expression for the frequency response of the CMFB circuit with the compensation network (see equation (5.4)).

$$\frac{v_{cmfb}}{\left(\frac{v_{err}}{2}\right)} = \frac{g_{mn} + \frac{sC_Z}{1+sRC_Z}}{g_{mp}(1 + \frac{s}{g_{mp}/(2C_X)}) + \frac{sC_Z}{1+sRC_Z}} = \frac{g_{mn}(1+sRC_z) + sC_z}{g_{mp}(1 + \frac{s}{g_{mp}/(2C_X)})(1+sRC_z) + sC_z}$$

$$= \frac{g_{mn} + g_{mn}RC_z s + sC_z}{g_{mp}\left(1 + \frac{s}{g_{mp}/(2C_X + C_Z)} + \frac{s}{1/(R_Z C_Z)}\right) + \frac{s^2}{g_{mp}/(R2C_X C_Z)}}$$

$$\frac{v_{cmfb}}{v_{err}} = \frac{1}{2}\frac{g_{mn}}{g_{mp}} \frac{1 + \left(R_Z + \frac{1}{g_{mn}}\right)C_z s}{1 + \left(\frac{1}{g_{mp}/(2C_X + C_Z)} + \frac{1}{1/(R_Z C_Z)}\right)s + \frac{s^2}{g_{mp}/(R_Z C_X C_Z)}} \tag{5.4}$$

Since $2C_X = 2 \cdot 830fF = 1.6$ pF and $C_Z = 200fF$. Assuming $C_X >> C_Z$, the response can be approximated as indicated in the expression (5.5).

$$\frac{v_{out}}{v_{err}} \approx \frac{1}{2}\frac{g_{mn}}{g_{mp}} \frac{1 + \left(R_Z + \frac{1}{g_{mn}}\right)C_z s}{\left(1 + \frac{s}{g_{mp}/(2C_X)}\right)\left(1 + \frac{s}{1/(R_Z C_Z)}\right)} \tag{5.5}$$

Zeroes:

$$z1 = -\frac{1}{\left(R + \frac{1}{g_{mn}}\right)C_Z}$$

Poles:

$$p1 = \frac{1}{2\pi R_Z C_Z} \qquad p2 = \frac{g_{mp}}{2\pi C_X}$$

6. Derivation of the maximum differential amplitude for lineal behaviour of differential pair in CMFB

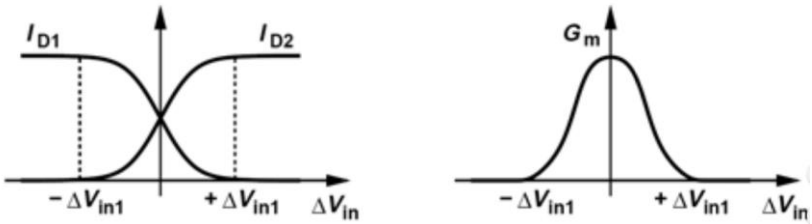


Figure 6.1: Linear characteristic of a differential pair [8]

The equation for the V_{GS} drop of a NMOS transistors is indicated in equation (6.1) [8]:

$$V_{GS} = \sqrt{\frac{2I_{DS}}{\beta}} + V_T \tag{6.1}$$

If the differential pair is completely unbalanced and the maximum differential input voltage is being applied, the maximum gate voltage at one side and the minimum at the other can be estimated from expressions (6.2) and (6.3).

$$V_{Gmax} = \sqrt{\frac{2I_{SS}}{\beta}} + V_T + V_{S1} \tag{6.2}$$

$$V_{Gmin} \approx V_T + V_{S2} \tag{6.3}$$

When no source degeneration is applied, $V_{S1} = V_{S2}$ and in consequence, expression (6.4) is obtained.

$$\Delta V_{INmax} = \sqrt{\frac{2I_{SS}}{\beta}} + V_T + V_{S1} - (V_T + V_{S2}) = \sqrt{\frac{2I_{SS}}{\beta}} \tag{6.4}$$

If source degeneration is used the assumption $V_{S1} = V_{S2}+R_S \cdot I_{SS}/2$ can be made and the result would be equation (6.5).

$$\Delta V_{INmax} = \sqrt{\frac{2I_{SS}}{\beta}} + V_T + (V_{S2} + \frac{R_S I_{SS}}{2}) - (V_T + V_{S2}) = \sqrt{\frac{2I_{SS}}{\beta}} + \frac{R_S I_{SS}}{2} \tag{6.5}$$

Glossary

AC	Alternating Current
BW	Bandwidth
CLK	Clock
CMFB	Common-Mode FeedBack
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common-Mode Rejection Ratio
CS	Current Source
DAC	Digital to Analog Converter
DC	Direct Current
DFT	Discrete Fourier Transform
DRC	Design Rule Check
ERC	Electrical Rule Check
GBW	Gain Bandwidth
IC	Integrated Circuit
LNA	Low Noise Amplifier
LVS	Layout Versus Schematic
MEMS	Micro Electro Mechanical System
NEZC	Not Enable Zero Current
NMOS	N-type Metal Oxide Semiconductor
OTA	Operational Transconductance Amplifier
PM	Phase Margin
PMOS	P-type Metal Oxide Semiconductor
PSRR	Power Supply Rejection Ratio
SFDR	Spurious Free Dynamic Range
SNR	Signal To Noise Ratio
TSMC	Taiwan Semiconductors
VPP	Peak to Peak Voltage