Faculdade de Engenharia da Universidade do Porto

Mixed-signal Test and Measurement Framework for Wearable Monitoring System

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Resumo

Circuitos de sinais analógicos e mistos proliferam em todas as áreas da eletrónica e, apesar de os sistemas digitais beneficiarem de soluções e estratégias de teste bem estabelecidas, o mesmo não pode ser dito para os sistemas analógicos, de radiofrequência e baseados em sensores. Os custos e o tempo de desenvolvimento e de realização do teste dos elementos analógicos são contribuintes maioritários para o custo total de projeto e produção, bem como o tempo de entrada no mercado, devido à sua complexidade, situação agravada quando se consideram cenários multi-sensor heterogéneos. Este é o caso da tecnologia de monitorização vestível, que rapidamente se está a tornar uma alternativa reconhecida na medicina, na reabilitação e no desporto. A transição da observação qualitativa para a monitorização quantitativa, que atualmente extravasa os ambientes controlados para incluir os espaços e contextos do dia-a-dia, deve ser acompanhado por estratégias contínuas *in-situ* de verificação do estado dos sensores, de modo a assegurar a fiabilidade dos dados. Em particular, os sensores passivos tendem a manifestar alterações de comportamento devido ao esforço induzido, forças externas, uso contínuo e desgaste geral. Estas alterações paramétricas progressivas dos sensores necessitam de ser acompanhadas por estratégias que considerem ocorrências de acessibilidade flexíveis a múltiplos níveis (i.e. considerando séries de sensores ou arranjos distribuídos de sensores), em particular para a tecnologia de monitorização vestível que apresenta condições dinâmicas em permanente modificação. O trabalho aqui apresentado propõe uma infraestrutura e uma metodologia para medição e teste que responde às necessidades atuais de sistemas baseados em sensores – um mecanismo de acesso in-situ, primordialmente direcionado para sensores passivos, gestão de recursos, sincronização de medições e controlo de estratégias de grupo, designado por SCPS - Setup, Capture, Process and Scan (Configuração, Aquisição, Processamento e Rastreio). A degradação dos sensores e o diagnóstico de falhas baseado em limiares foram considerados como cenários de teste. Uma implementação modular baseada num circuito digital reprogramável (FPGA – Field Programmable Gate Array) foi desenvolvida tendo em consideração DOIs casos de estudo: sensores resistivos de força (FSR – Force Sensing Resistors) e elétrodos de superfície descartáveis de prata e cloreto de prata, Ag-AgCl. A estratégia de medição e teste proposta foi implementada com recurso ao protocolo de barramento I2C – Inter-Integrated Circuit, enquanto um controlador I2C independente foi utilizado para execução de instruções na perspetiva de uma prova de conceito. Além disso, o acesso externo ao barramento de transporte de dados, utilizado para efeitos de depuração e teste, foi realizado por acesso direto aos registos dos módulos implementados na FPGA por uma ligação USB – Universal Serial Bus gerida por uma interface gráfica codificada em linguagem Python. A impedância dos sensores alvo foi caracterizada em vários cenários de degradação comuns por forma a estabelecer modelos base e respetivos desvios.

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Abstract

Analogue and mixed-signal circuits are proliferating in all areas, and although digital systems benefit from well-established testing solutions and strategies, the same cannot be said for analogue, RF and sensor based systems. Testing costs for the analogue elements drive the overall design and production cost and time to market, due to their complexity, which are aggravated when considering heterogeneous multi-sensor scenarios. Such is the case for wearable monitoring technology (WMT), which is rapidly becoming a recognized alternative in medicine, rehabilitation and sports. Such transition from qualitative to quantitative based monitoring, which now transcends controlled environments to include every-day settings, must be accompanied by continuous *in-situ* sensor status monitoring strategies, in order to insure data reliability. In particular, passive sensors tend to undergo behavioural modifications due to induced stress, external forces, continuous usage and general wear and tear. Such progressive parametric alterations of the sensors need to be addressed through strategies which consider flexible accessibility occurrences at multiple levels (i.e., considering sensor arrays or distributed sensor arrangements), in particular for WMT which present ever-changing dynamic conditions. The work hereby presented seeks the design of a measurement and testing framework that responds to the present needs of sensor based systems --- an *in-situ* access mechanism, initially intended for passive sensors, resource management, measurement synchronization, an group strategies control; named SCPS (Setup, Capture, Process and Scan). Sensor degradation and fault diagnostics based on threshold were considered as testing scenarios. A field programmable gate array (FPGA) based modular implementation was developed considering two case-studies: force sensing resistors (FSR) and disposable surface Ag-AgCl electrodes. The proposed test and measurement strategy was implemented using the inter-integrated circuit (I2C) bus protocol, while an independent I2C controller for instruction handling was utilized as a proof of concept scenario. Additionally, external access to the data transport bus, utilized for debugging and testing purposes, was achieved at the present stage through direct access to the implemented FPGA modules registers through an USB connection managed by a Python based graphical user interface. The impedance of the targeted sensors was characterized in a number of common degradation scenarios in order to ascertain base models as to establish deviations.

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To my wife, my never-ending guiding light…
To my daughter for the pure joy she brings
To my father, wish he could have stayed to see this
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Pero Dios no dio ninguna respuesta, y se desvaneció como una poderosa tempestad.

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Acronyms and Abbreviations

List of acronyms, abbreviations and initialisms (ordered alphabetically)

- 10GA: 10-bit group address.
- ABM: analogue boundary module.
- ACK: acknowledge.
- ADC: analogue to digital converter.
- AFE: analogue front end.
- ATB: analogue test bus.
- BAN: body area network.
- BILBO: built-in logic block observer.
- BIST: built-in self-test.
- BISTC: built-in self-test/calibration.
- BSDL: boundary scan description language.
- BSN: body sensor network.
- CAN: controller area network.
- CAPT: capture.
- CFI: cell functional input.
- CFO: cell functional output.
- CIS: capture instruction set.
- CPM: central processing module.
- CTI: cell test input.
- CTL: cell test language.
- CTO: cell test output.
- DARPA: Defence Advanced Research Projects Agency.
- DC: direct current.
- DfT: design for testability.
- DIAMOND: Diagnosis, error-modelling and correction for reliable systems design.
- ECG: electrocardiography.
- EEG: electroencephalography.
- ELESIS: European library-based flow of embedded silicon test Instruments.
- EMBS: Engineering in Medicine and Biology Society.
- EMG: electromyography.
- EOG: electrooculography.
- ESA: embedded system access.
- ESTSP-IPP: Escolar Superior de Tecnologia do Saúde do Porto – Instituto Politécnico do Porto.
- FEUP: Faculdade de Engenharia da Universidade do Porto.
- FPGA: field programmable gate array.
- FSR: force sensing resistor.
- GADDR: group address.
- GNU: GNU's Not UNIX.

- GPS: global positioning system.
- GRP: group register pointer.
- GUI: graphical user interface.
- GWP: group write pointer.
- HBIST: hybrid BIST.
- HTSG: hybrid test signal generators.
- I2C or IIC: inter-integrated circuit.
- IC: integrated circuit.
- IEEE: Institute of Electrical and Electronics Engineers
- IIC or I2C: inter-integrated circuit.
- INSTR: instruction register.
- IR: instruction register.
- LED: light emitting diode.
- LFSR: linear feedback shift register.
- LSB: least significant bit.
- MADDR: member address.
- MEMS: micro-electromechanical systems.
- MISR: multiple input shift register.
- MSB: most significant bit.
- NI: national instrument.
- OBIST: oscillation BIST.
- PCB: printed circuit board.
- PrIS: process instruction set.
- PROC: processing.
- PSET: pre-setting configuration.
- PXI: peripheral component interconnect) eXtensions for instrumentation.
- RQST: request.
- RRP: read register pointer.
- RTL: register-transfer level.
- RX: receive, receiver or reception.
- ScIS: scan instruction set.
- SCL: I2C serial clock line.
- SCPS: Setup Capture Process Scan.
- SDA: I2C serial data line.
- SGT: SCPS global transaction.
- SIB: segment insertion bit.
- SiP: system in package.
- SIS: setup instruction set.
- SMBUS: system management bus.
- SNR: signal to noise ratio.
- SoC: system on chip.
- SPI: serial peripheral interface.
- Sr: I2C re-start.

- SRT: SCPS read transaction.
- STATU: SCPS status register.
- STBY: SCPS stand-by register.
- STIL: standard test information language.
- STT: SCPS transfer transaction.
- SWT: SCPS write transaction.
- TAM: test access mechanism.
- TAP: test access port.
- TBIC: test bus interface circuit.
- TCK: test clock.
- TDO: test data out.
- TDI: test data in.
- TDR: test data register.
- TKR: SCPS token register.
- TMS: test mode select.
- TOETS: Towards One European Test Standard.
- TRST: test reset.
- TX: transmit, transmitter or transmission.
- UDP: user defined parameter.
- UDR: user defined register.
- USB: universal serial bus.
- VI: virtual instrument.
- W2M2: wireless wearable monitoring module.
- WBAN: wireless body area network.
- WBC: wrapper boundary cells.
- WBR: wrapper boundary register.
- WBSS: wearable biomedical sensors and systems.
- WBY: wrapper bypass register.
- WIMU: wearable inertial monitoring unit.
- WIR: wrapper instruction register.
- WMT: wearable monitoring technology.
- WPAN: wireless personal area network.
- WPP: wrapper parallel port.
- WRP: SCPS write register pointer.
- WSC: wrapper serial control.
- WSI: wrapper serial input.
- WSN: wireless sensor network.
- WSO: wrapper serial output.
- WSP: wrapper serial port.
- ZRA: zero resistance ammeter.

Chapter 1

Introduction

1.1 Motivation and Problem Definition

Words such as ubiquitous, pervasive, ambient, and seamless are common among most technological research areas of our day. The quest for integrating the individual within areas of technological development never has been more sought after, or among so many and varied fields. With each passing day, commercial products seem to become smaller, more complex, and more importantly, designed to be portable (dare we say wearable); the need for an individual to remain untethered seems to dominate most electronic consumer markets. Advances within technological domains such as, integrated circuits (IC), body/wireless sensor networks (BSN and WSN respectively), smart sensors, and data processing, to name a few, have contributed to the last decade's proliferation of systems designed for monitoring and responding to an individual's actions and reactions. Such human-centric approach has consequently affected the way one has come to think of personal performance and daily activities monitoring, as well as intervention assessment, progress appraisal, biosignals acquisition; and naturally a new array of associated challenges emerges.

Multiple paradigms shifts are taking place, were the snap-shot approach is replaced by continuous prolonged data gathering (e.g., instead of a doctor's consult, a patient's condition can be monitored for days or weeks); the laboratory is replaced by every day settings; and where real-time analysis is becoming a protagonist. Wearable monitoring technology (WMT) introduces a refinement to personal monitoring by allowing a long-term on-person direct-contact approach; thus permitting for a new level of understanding of an individual's interaction with their surrounding environment. Multi-sensor settings, non-standard assembly, heterogeneous components, and unorthodox operating situations are a few of the conditions commonly addressed by WMT; thus a wide variety of systems can be expected. Many examples can be cited when referring to WMT: LifeGuard (Mundt, Montgomery, Udoh, & al., 2005), ClimBSN (Pansiot, ing, Mcllwraith, Lo, & Guang-Zhong, 2008), Ayushman (Venkatasubramanian & Gupta, 2008), BIOTEX (Coyle S. , Lau, Moyna, & al., 2010), SwimMaster (Bächlin, Föster, & Tröster, 2009), to name a few pioneers, designed for numerous purposes, scenarios and environments (an extended examination of the WMT topic will be covered in Chapter 2), and Portugal has actively contributed in this endeavour, including projects from the Faculty of Engineering of the University of Porto (FEUP) such as: WalkinSense (Telgenkamp, 2012) a product from Tomorrow Options (now Kinematics, a start-up commenced within FEUP), the BIOSWIM project which produced the WIMU - wearable

inertial monitoring unit (Silva, Salazar, Borges, & Correia, 2013), W2M2 – wireless wearable monitoring module, produced for the *Escola Superior de Tecnologia de Saúde do Porto* for rehabilitation progress monitoring purposes (Salazar, et al., 2013), and the ProLIMB project (da Silva J. M., 2014).

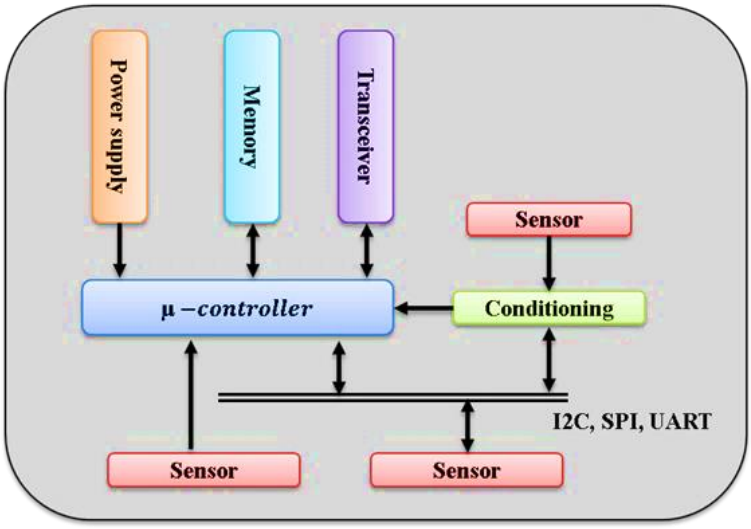


Figure 1-1 — Generalized wearable module architecture.

Wearable monitoring solutions are expected to become commonplace devices within numerous fields such as healthcare, rehabilitation, assistive technology, sports, and even entertainment, driving the need for universal options as opposed to custom designs. The before mentioned expectations require a highly flexible approach, there seems to be some concensus on the general design of a sensor node (Van Laerhoven K. , et al., 2004) (Tufail & Islam, 2009) (Pantelopoulus & Bourbakis, 2010) (Rehman, Mustafa, Javaid, Qasim, & Khan, 2012) (Lara & Labrador, 2013) (Virk, 2013); following the structure presented by the BSN node project (Lo & Yang, 2007), seen in Figure 1-1.

In the case of healthcare and rehabilitation facilities, monitoring systems are expected to be reused by a number of individuals and for changing life-cycles, varying from one-time use to shelve-life measured in years. In spite of the present progress, there are a number of obstacles to overcome for truly achieving seamless WMT, such as: energy availability, data compression, textile integration, feature extraction, pattern/event recognition, and biomechanical models, among many more. Nevertheless, considering that WMT's general purpose is the monitoring of an event, be it a physiological, inertial, or otherwise subject/environment influenced parameter, data reliability becomes of paramount importance; not to mention inter-session and inter-subject data comparability for systems intended for multiple uses and users. How can we insure that the equipment performs the same way between subjects and sessions? Or stated differently, how can we confidently compare the data? A number of factors come into play such as sensor quality (which can affect data resolution and error), positioning (which can vary due to physiology of the

patient, sensor shape and size, not to mention the ability of the physician/subject to place the sensor), degradation, to mention a few. All mentioned factors influence the collected data, which can have a strong effect on the final result if not compensated through calibration, filtering or associated strategies which contribute to final data comparability. Even though some compensation strategies can be applied after the fact, through data processing at software level, or through signal conditioning (e.g., filtering out noise), *in-situ* mechanism are sometimes needed, such as the classic right leg drive circuit for ECG measurements.

Wearable and portable monitoring devices are on the rise; however, modest attention has been paid to supplementary calibration/testing protocols and mechanism, in order to insure the reliability and comparability of the measurements, especially when considering long term scenarios. The concept of reliability itself needs to be adjusted from that of traditional IC and device testing, which considers field failure rate and the balance of manufacturing cost and yield (International Technology Roadmap for Semiconductor, 2011). It is no longer the case that one needs to verify the device (and its subsections) only during production or once post-production (prior to customer shipping); product quality needs to be verified continuously during the active product life, even during usage for some instances, such as the case of WMT. The concern for some WMT is not if the system or its components will fail, instead a certainty that it will fail at different levels at some point during operation. Constantly changing conditions on the sensors could produce sporadic failures (e.g. temporary disconnects of an electrode), measurement condition degradation or even a change in the sensor's transconductance reference scale. A complex problem when considering that analogue and sensor testing are considered to be in their infancy (Azimane, 2012) when compared to the digital arena.

Traditional approaches such as parametric characterization or hardware specific testing apparatus are far from providing the cost stabilizing effects achieved by automatic testing equipment (ATE) and built-in self-testing (BIST) during the last decades of digital technology revolution. This is of particular concern when considering *in-situ* solutions which require external equipment independence; such strategies are not only limited in space, resources and accessibility (the traditional concerns of testing), they also require operation time transparency.

The world of testing seemed to favour embedded system access solutions (ESA) in the past decade (Wenzel & Ehrenberg, 2012). In fact, embedded instruments are making their mark as well, as it is evidenced by the focus of standards such as IEEE STD. 1687 and the efforts being done to develop ESA standard libraries in the "European library-based flow of embedded silicon test Instruments" (ELESIS) project (ENIAC, 2013). Although embedded test instruments can serve to increase the test quality by providing target localized resources, they are not a complete solution. Issues such as accessibility and controllability only exacerbate on WMT, due to the heterogeneous nature of their elements; and although a number of strategies can

be extrapolated from traditional testing (functional and structural alike), BIST, and design for testability (DfT), especially those aimed for system on chip (SoC) and system in package (SiP) (system in package), key differences exists that require a different approach (coverage of current testing strategies are presented of Section 2.2). The issue remains, as most testing strategies and standards were designed with the production line mind frame, as opposed to product active life time.

A number of standards and proposals are currently being used for digital and analogue testing accessibility, where the undebatable golden standard is the IEEE 1149.1. Originally meant as a set of modules and registers for facilitating board level test access through a boundary scan approach, the 1149.1 has proven extremely flexible, supporting a wide array of approaches for testing, debugging, and even in-circuit programming. Among other well-documented standards one finds the: IEEE standards 1149.4, 1149.6 and most recently 1149.7 (a discussion of such standards can be found in Section 2.2.3). The evolution of packaging strategies and increased circuit complexity has demanded the formulation of new standards that address such issues, such as the IEEE 1500 and the IEEE STD. 1687 (expected to reach standard level in short time), which are aimed for different scenarios such as core testing within SoC and for embedded instrumentation, respectively. All these standards aim to facilitate the testing of the different target elements by providing a structured access, while homogenizing the control process, but still more work is needed in order to fill the gaps left by analogue, sensor and mixed-signal testing.

Multi-sensor centric systems present the same accessibility issues found at core or board testing levels. Likewise, they can be composed by a heterogeneous array of packages, joined by innovative non-planar ways (e.g., layered flexible PCB for instance), or include distributed interconnected modules; which only serves to exacerbate the accessibility issue. In addition, if testing (on-line or off-line) during normal operation is required, static specification or fault-models might prove insufficient, and adaptive testing strategies need to be applied while limited to *in-situ* resources. The ideal scenario is to verify functionality of a sensor under known stable conditions as to compare with a well-established reference in order to determine deviations. Nonetheless, that is not possible for operation time testing, so alternative strategies based on context-awareness, sensor redundancy, and multi-modal data fusion are sometimes necessary. Furthermore, references for some sensors are quite sensitive to drift, hysteresis, temperatures and other factors, producing a lack of well-defined fault and behavioural models as norm. The interface of sensors with the physical environment presents an unpredictable state when performing a test during operation (or during controlled conditions for that matter), making functional and structural strategies specifications a moving target. In order to better understand such scenarios let's consider two common WMT passive sensors: electrodes and force sensing resistors (FSR).

A number of biosignals (such as ECG, EMG, EEG, EOG, bioimpedance) can be captured through the use of electrodes (be it disposable, dry, textile, capacitive, etc.), which provide

a wealth of information regarding the subject — cardiac properties, muscle activity, ocular activity, nerve activity are some of the associated measures. Electrodes for biomedical applications are well understood and have been utilized for decades. The problematic influence of the electrode-skin interface in measurements has been subject of different studies. The works presented in (Spach, Barr, Havstad, & Long, 1966) (Rosell, Colominas, Riu, Pallas-Areny, & Webster, 1988) (McAdams, Jossinet, Lackermeier, & Risacher, 1996) (Huigen, Peper, & Grimbergen, 2002) (Kappenman & Luck, 2010) provide a sample of relevant related issues on the subject. The sensor in this case, while basically a piece of metal (or metal bonded material, such as the case for textile electrodes), combines with the subject to form a continuously fluctuating element, dependant on numerous ever changing parameters, such as sweat, temperature, pressure, power-line interference, and motion.

Commonly, a pairing of electrodes is necessary due to their half-cell nature, which complicates any functional or structural approach. In spite of the before mentioned complications, a number of models have been proposed to describe the electrode-skin interface. Swanson and Webster (Swanson & Webster, 1974) proposed a single time-constant linear-component equivalent model of the electrode-skin impedance which, although limited due to the non-linear nature of the interface, is widely utilized and has sprung many variations and alternative models. These models permit the formulation of specification parameters, but are quite dependant on the subject and remain time variant.

In the case of FSR sensors, different challenges are present (Buis & Convery, 1997). For these sensors the issue is not as much a problem of condition variations as FSR do not create an intrinsic relation with the object pressuring them, even though atmospheric pressure, temperature, humidity play a part on its response. FSR can be modelled as a capacitor in the absence of minimal pressure and as a variable resistor when a force is applied. In case a catastrophic failure occurs, such as a sensor connector breakage, its behaviour becomes indistinguishable from a non-pressure condition without the necessary precautions; moreover, the outer membrane's elasticity is well known to cause drift and hysteresis effects. While this might not be crucial for crude measurements or pressure switching scenarios, when utilized for sensitive measurements, wear and tear, bending, constant pressure, could introduce a significant error on the measurements. Fine tuning calibration might not be possible in a runtime scenario due to the lack of a reference pressure stimulus; however, a general idea of the health status might be, thanks to alternative approaches, as one based on the frequency response analysis.

It is not uncommon to find these two sensor cases in the form of arrays or distributed sensors, which in order to reduce wires and consolidate components, benefit of resource sharing such as an analogue bus and/or localized instruments (such as stimuli generators or signal conditioning section for acquisition). Such scenarios require synchronization strategies for routing, activation, etc., in order to avoid elements usage overlapping and even damage

to components. The associated required control and accessibility complexity could combine with design for testability (DfT) strategies to alleviate the matter.

Motivated by the complexity of the issue, consensus exists on the need to invest on testing strategies, in particular for the case of analogue, sensor and mixed-signal scenarios (the case of a significant number of WMT systems), driven by the cost that testing represents on product development and its influence in time to market. Joint industry and academia projects, funded by the international consortiums, such as TOETS - "Towards One European Test Standard" (TOETS), ELESIS (ENIAC, 2013), and DIAMOND (CORDIS, 2010) – "Diagnosis, error-modelling and correction for reliable systems design", are testament to the efforts that have been made in the area.

1.2 Objectives

The present doctoral work focused on the design of a measurement/testing framework that responds to the present and evolving needs of sensor based systems --- an in-situ access mechanism, which provides resource management and synchronization, while considering multi-element accessibility named SCPS (from Setup, Capture, Process and Scan). Fault diagnosis represents a driving motivation of the SCPS framework, providing flexibility for strategies that include fault detection, fault localization and/or fault prediction. That said, the main target testing scenarios considered were sensor degradation and threshold based fault detection schemes; while considering sensors inter-dependence setups. Sensors inter-dependence refers to settings where sensor characterization depends on multiple sensor instances (e.g. the case of electrode pairs for biosignals measurements) or multi-element measurement associations (e.g. context determination through multiple sensor readings combination).

Secondary objectives include a proof-of-concept implementation of the before mentioned framework and a series of experiments focused on wearable monitoring technology familiarization, sensor characterization and protocol development in order to ascertain proper methodological procedures and approaches, such as:

- Wearable monitoring technology research and familiarization, including design and implementation of prototype system for rehabilitation scenarios, patient data acquisition, and data analysis.
- In-vitro and in-vivo electrode-skin impedance characterization experiments with fault monitoring considerations, with corresponding SCPS framework setup formulation and verification.
- Force sensing resistor characterization under controlled pressure with fault monitoring considerations, with corresponding SCPS framework setup formulation and verification.

1.3 Thesis contributions

In reference to the previously stated, there exists a need to address the current gaps in sensor testing within wearable monitoring technology, which have led to the research and development of the present thesis. The particularity of wearable monitoring technology adds complexity to *in-situ* sensor testing, thus complicating data reliability and comparability. Two underlined issues serve as motivation: accessibility and addressability.

Accessibility is a well-known issue of testing in general. Access to specific locations within a board, IC, SoC, SiP, or in this case WMT (which can be a mix of all the previously mentioned with multiple instances), can present a challenge. When considering *in-situ* multi-sensor normal operation scenarios, the issue of access becomes also an issue of mode operation and local resource scheduling. Under such scenario not only mechanisms must exist for routing the corresponding modules in the proper setup (connecting a test instrument to the target), also a methodology for the participating components to synchronize their actions (using multiple operation modes). For instance, when considering an analogue bus shared by multiple sensors (an array or heterogeneous combination), it becomes necessary to schedule the operations as to avoid unwanted connections to occur (and even avoid damaging consequences). Additionally, a holistic approach to sensor testing might be required in order to address physical system state considerations as to determine expected sensor reference/response relation. Parameters such as temperature, orientation, and event detection, could proof necessary as to establish if a test or measurement should proceed a normal sensor response capture operation (e.g., the temperature might vary the transconductance of a particular sensor, then a synchronized reading from a temperature measuring sensor would provide a way to establish the proper response specifications). Consequently, addressability of the involved elements is also an issue.

Current standards address such issues by compartmentalizing the actions of the involved modules (such as IEEE STD. 1687 through communication to the test data registers, TDR or 1500 wrapper strategy) or controlling the actions of all reachable elements (such as 1149.1 and 1149.4) through boundary scan sequences. However, the message generation complexity would hard press an *in-situ* controller; as it stands, 1149.1 test sequence generation are constructed with the boundary scan description language (BSDL) support, and one would seldom expect such capability to be present on automatic local resources. Additionally, the resulting response transport of multiple elements may well be required for decision making or in order to apply adaptive testing strategies, regardless of the specific approach: functional or structural, BIST or DfT, on-line or off-line test mode. Thus, a framework that simplifies communication and considers multiple levels of addressability (unicast, multi-cast and broadcast) presents itself more pliable to WMT scenarios.

The present work aimed to develop an integrated system design for testability data transport mechanism that addresses setups with heterogeneous sensor types and varying testing approaches, while considering test instruments (ATE independent) scenarios. The

structure was organized around a four stage approach, reflective of its inspiration on proven 1149 standards. An overview of the stages follows:

- ***Setup:*** intended for initialization of settings for all stages prior to testing/calibration execution or for modification/adaptation to changing scenarios. Considered actions include, e.g., signal/pattern preloading, sampling settings, grouping of components, and BIST handling procedure.
- ***Capture:*** reminiscent of the EXTEST instruction, this stage manages the signal/pattern loading/generation, data collection and BIST activation.
- ***Process:*** intended for data processing and allocation on decision making registers. This stage seeks to manage the comparison of collected data through updates of registers that can be used to follow sensor history, global reference upkeep or specific reference comparison. Localized algorithm/heuristics such as least mean square strategies, Kalman filters, Markov's chains, etc., can be activated and processed at this stage.
- ***Scan:*** intended for data and instruction distribution. Possibilities of interfacing with external elements for setup and data gathering modes are being considered.

The SCPS modules (as they will be referred from now on) themselves are subdivided in four sections: I2C interpreter, SCPS interpreter, SCPS registers, and SCPS handler. The structure provides implementation flexibility, while permitting compatibility with numerous commercial sensors through the use of I2C as the communication bus. The method also permits the inclusion of these sensors together with test instruments (I2C compatible) within a testing/calibration strategies, by expanding their functionality; consequently offering a structured mixed-signal test infrastructure.

Multi-level addressability is achieved through the SCPS interpreter, considering a group approach mechanism that related multiple modules with a shared 10-bit address. An instruction set, managed internally through registers, flags and associative pointers, permits the synchronization of events, while allowing the sharing of common resources (such as an analogue bus) by token request through broadcast instructions. Although I2C is mostly a master-slave centric protocol ("general call" instructions are also part of the I2C protocol, however seldom utilized), multiple level addressability is not excluded and thus achievable with care in sequencing. Some SCPS introduced capabilities include slave-to-slave data transfer, on-the-fly action setup, and reduced instruction incremental action sequence activation, to name a few. All SCPS based I2C sequences remain transparent to non-addressed I2C elements, preserving I2C compliance. A special case usage of the I2C bus as a test stimuli/response transport was considered for digital stimuli/response utilized for testing analogue elements, such as the bioamplifier conditioning circuit and associated electrodes for the ProLIMB project system; thus, demonstrating the expandability of the SCPS module approach to particular resource re-usage strategies.

The SCPS modules were implemented on a Spartan 6 FPGA (Atlys and Nexys 3 from Digilent Inc.), while the switching segments, which formed the analogue bus interfacing section, were based on Analog Devices' ADG173 single-supply analogue switches (on custom PCBs). The I2C bus was controlled through an USBee ZX controller from CWAV and real-time monitoring was achieved with the Digiview™ DV-100 Portable Logic Analyser. Internal register status was observed through a USB connection between the FPGA and a computer, managed through a custom Python graphical user interface (GUI) based on FPGALink bindings (an open source FPGA connectivity solution). The GUI allows for programming of the FPGA, as well as directly reading/writing to the SCPS modules registers within the FPGA. A National Instrument PXI based impedance analyser with corresponding virtual instrument (VI) was implemented for test stimuli generation and capture, to serve as a conceptual test instrument. A standalone impedance analyser setup is proposed, although not implemented. Two case studies sensors were considered: disposable Ag-AgCl electrodes and FSR.

In collaboration with the *Escola Superior de Technologia da Saúde do Porto* of *the Instituto Politécnico do Porto* (ESTSP-IPP), a methodology was developed for characterization of disposable electrodes exposed to traditional fault scenarios such as wrong positioning, poor skin preparation, improper lead handling and partial detachment. A Gamry G 300 potentiostat/galvanostat/ZRA and a Faraday cage setup were used for the electrode characterization experiments, in combination with a custom current limiter safety circuit developed for this work. The experiments were performed on Agar based gel for observation of a number of parameter effects, such as time, temperature, obstruction, etc. Human trials focused on variation of electrode-skin variation with time and when exposed to physical activity. A corresponding SCPS based setup was confirmed through adaptation of the PXI test instrument based on a current controlled voltage source strategy for injected current limitation, demonstrating a viable mechanism for electrode-skin monitoring. Additionally, a test case was developed for the ProLIMB project system, focused on managing the EMG module's bioamplifier conditioning section and corresponding electrodes.

Force sensing resistors (FSR) are not as well studied as electrodes, probably due to their relatively recent entrance within the personal monitoring field and their previous role mainly as pressure based switches. Moreover, FSR are thought as a variable resistor reactive to pressure, and their complete impedance model is seldom considered within literature or applications. Consultation with a manufacturer (Tekscan Inc.) and preliminary analysis revealed an expected capacitive component present within the FSR that can be useful for presence determination, since their high resistance on rest state makes them a hard target to identify for standard DC (direct current) based setups. A setup was developed for FSR characterization undergoing controlled pressure through the use of the Tira Test 2705 tensile testing machine, intended to establish common sensor behavioural pattern. Friction degradation was achieved through custom pieces specifically designed. The intention of the experiment was to produce controlled dynamic pressure and friction scenarios in order to

generate characterization patterns and degradation profiles, using the PXI based test instrument with an auto balancing bridge strategy. The FSR were later characterized through the SCPS compatible setup.

1.3.1 *Contributions to Projects*

Initial efforts focused on familiarization with wearable monitoring technology through development and implementation of actual wearable designs. An in-depth bibliographical search was performed, focused on wearable monitoring systems for sports, which present more dynamic conditions and sensor arrangement than their healthcare counterparts (restricted by numerous medical standards). Direct experience was gained by working with members of the BIOSWIM project, which focused on the design of a wearable swimming suit for world competition level swimmers monitoring. The WIMU (Wearable Inertial Monitoring Unit) developed for the project was used for swimmer characterization, through acceleration data processing, offering insight on the effects of positioning and data reliability within alternative scenarios (such as water environments for this case). Such efforts resulted in several international conference publications and a journal article.

At the request of the Escola Superior de Tecnologia da Saúde do Porto, a rehabilitation progress inertial monitoring unit was designed and implemented utilizing commercially available components. The W2M2 (Wireless Wearable Monitoring Module) was then used with a number of stroke survivors for upper limb movement characterization. A second prototype was designed and implemented following a modular approach, for multiple type sensor module arrangements. Such efforts resulted in several international conference publications and a journal article.

1.3.2 *Publications and State of the Art Contributions*

The work hereby presented resulted in a number of published contributions, among them twelve (13) peer-reviewed scientific events proceedings, four (4) peer-reviewed journal articles, two (2) international projects reports, (2) patent research process and (2) national project report. Additional publications not included in this section are in the initial stages of the review process or still not submitted. Following is a succinct overview:

- National Projects contributions:
  - BIOSWIM: involvement on experiment setup and undertaking for human trial of the developed wearable inertial monitoring unit, including post-acquisition data processing.
  - W2M2: design and implemented a wireless inertial monitoring unit for rehabilitation progress monitoring, including protocol developed, human trial, and post-acquisition data processing. Strategies for repeatability, stability, event recognition are some of the developed data processing strategies. A second

prototype of a modular re-arrange able version for multiple test adaptability was design and implemented.

- PROLIMB: test strategy for EMG module development and implementation based on SCPS strategy, utilizing the I2C bus for test stimuli/response transport.
- BIAL Project - Human motor re-learning - the use of sensor information fusion: contributed to the project plan development, this resulted on a BIAL grant.

- International Projects contributions:
  - TOETS "Towards One European Test Standard" (TOETS): contributions focused on electrode and FSR alternative characterization.
  - ELESIS "European library-based flow of embedded silicon test Instruments" (ELESIS): contributions included current standards gaps identification for sensor testing, SCPS framework and corresponding demonstrator
- Provisory patent No 106787 titled "Mixed signal test and measurement framework for monitoring systems."
- Provisory patent No 107537 titled "Mixed signal bus module for multiple circuit resources management."
- Journal accepted publications:
  - "Built-In Self-Testing Methodology and Infrastructure for an EMG Monitoring Sensor Module." International Journal on Advances in Systems and Measurements, v 7 n 1&2 2014. Originally accepted with required revisions on May 2nd; received in revised form on May 31st; second round of revisions requested on June 16th; received in revised form on June 21st. The authors in publication order are: Antonio José Salazar Escobar, José Alberto Machado da Silva, Miguel Fernando Velhote Correia, Bruno José Mendes.
  - "Low-cost wearable data acquisition for stroke rehabilitation: a proof of concept study on accelerometry for functional task assessment." Topics in Stroke Rehabilitation, Volume 21, Number 1, Pages 12-22, DOI: 1010.1310/tsr2101-12, online date: February 12, 2014. The authors in publication order are: Antonio J. Salazar, Ana S. Silva, Claudia Silva, Carla M. Borges, Miguel V. Correia, Rubim S. Santos, and Joao P. Vilas-Boas.
  - "Co-activation of upper limb muscles during reaching in post stroke subjects: an analysis of the contralesional and ipsilesional limbs." Journal of Electromyography and Kinesiology, accepted for publication on 15th of April of 2014. Editor in Chief, Moshe Solomonow, PhD, MD (hon). It was originally received on: September 30, 2013; received in revised form: April 1, 2014; Accepted: April 15, 2014; Published Online: May 08, 2014, with DOI: 10.1016/j.jelekin.2014.04.011. The authors in publication order are: Cláudia C. Silva, Augusta Silva, Andreia Sousa, Rita Pinheiro, Catarina Bourlinova, Ana Silva, Antonio Salazar, Carla Borges, Carlos Crasto, Miguel Velhote Correia, João Paulo Vilas-Boas, and Rubim Santos.

- "Wearable monitoring unit for swimming performance analysis." Biomedical Engineering Systems and Technologies, Communications in Computer and Information Science, Volume 273, 2013, pp 80-93, Springer Berlin Heidelberg, DOI 10.1007/978-3-642-29752-6_7. The authors in publication order are: Ana S. Silva, Antonio J. Salazar, Carla M. Borges, and Miguel V. Correia.

- Conferences
  - "An I2C Based Mixed-Signal Test and Measurement Infrastructure," 19th Annual International Mixed-Signals, Sensors, and Systems Test Workshop 2014. Accepted without changes.
  - "Characterization of the Electrode-Skin Impedance of Textile Electrodes," Conference on Design of Circuits and Integrated Systems, DCIS 2014. Accepted with minor changes.
  - "Built-in Self-Testing Infrastructure and Methodology for an EMG Signal Capture Module," 2nd International Conference on Global Health Challenges, GLOBALHEALTH 2013. Oral presentation by author. Best Paper Award.
  - "Análisis de Movimientos Compensatorios del Miembro Superior en Pacientes Post ACV," 8th International Seminar on Medical Information Processing and Analysis, SIPAIM 2012. Oral presentation by co-author.
  - "Experiencias en tecnología portable para comunicación y monitoreo personal de bajo costo," in Proceedings of 4to Congreso Venezolano de Bioingeniería, BIOVEN 2012. Oral presentation by co-author.
  - "Propuesta preliminar de un índice de consistencia para patrones de cinemática de marcha humana," in Proceedings 4to Congreso Venezolano de Bioingeniería, BIOVEN 2012. Poster presentation.
  - "W2M2: Wireless wearable modular monitor: a multifunctional monitoring system for rehabilitation," in Proceedings of International Conference on Biomedical Electronics and Devices, 2012. Oral presentation.
  - "Compensatory movement detection through inertial sensor positioning for post-stroke rehabilitation," in Proceedings of International Conference on Bioinspired Systems and Signal Processing, 2012. Oral presentation by co-author.
  - "Sensor characterization for portable and wearable applications," in Proceedings of 17th Portuguese Conference on Pattern Recognition, 2011. Poster presentation.
  - "Post-stroke patients functional task characterization through accelerometry data for rehabilitation intervention and monitoring," in Proceedings of 17th Portuguese Conference on Pattern Recognition, 2011. Poster presentation.
  - "A Comparison of Look-up Table Based Sine Wave Generation Implementations" VII Jornadas sobre Sistemas Reconfiguráveis, REC2011. Oral presentation.
  - "WIMU: Wearable inertial monitoring unit. A MEMS-based device for swimming performance analysis" 4th International Joint Conference on Biomedical

Engineering Systems and Technologies, BIOSTEC 2011. Oral presentation by co-author.

- "An initial experience in Wearable Monitoring Sport Systems" 10th IEEE International Conference on Information Technology and Applications in Biomedicine, ITAB2010. Oral presentation.

1.3.3 *Chapters Description*

Following is an overview of the thesis organization through a chapter per chapter description:

- Chapter 2 – State of Art: an overview of wearable monitoring technology state of the art and associated elements description; as well as, an overview of mixed-signal, analogue and sensor testing's state of the art, focusing on challenges and current approaches and standards.
- Chapter 3 – The SCPS Framework: the SCPS framework is presented and explained, including the physical, electrical and conceptual aspects. Examples of scenarios are explained in order to gain insight into the framework's proficiencies and extension.
- Chapter 4 - SCPS Framework Implementation: the physical application is presented, specifically its I2C modular implementation within a FPGA, and functional and feature structure. The related hardware elements are also discussed including the switching modules for sensor interface and the USB debugging setup through a Python based graphical user interface.
- Chapter 5 - Case Studies Characterization: Disposable Electrode Ag/AgCl - The disposable electrode case study is discussed, including the particularities of this type of sensor, related models and effects of the electrode-skin impedance. Explanation of the experimental setup, protocols, implemented and utilized hardware is presented, including the data generated from studied scenarios and the extrapolated parameter consideration. Force Sensing Resistor - The force sensing resistor case study is discussed, including the particularities of this type of sensor, related models and affecting degradation factors. The hardware setup for characterization is discussed as well as the collected data and analysed parameters.
- Chapter 6 – Case Studies SCPS Methodologies: the SCPS based strategies and setups for both the disposable electrodes and the FSR sensor are presented. The associated I2C-SCPS sequence and associated hardware elements are presented for both cases based on the PXI impedance analyser and associated single-supply analogue front-end.
- Chapter 7 - Conclusions and Recommendations: the conclusions of the thesis are presented, as well a list of recommendations regarding issues encountered and developmental paths.

Chapter 2

State of Art

2.1 Wearable Monitoring Technology

Although WMT is a relatively old idea (e.g. the bioharness used by astronauts during the 1960's Apollo missions (NASA, 1975)), it is only with recent advances that they have become viable alternatives. It is inferred from the term that it must achieve three specific tasks:

- It must be suitable to wear.
- It must observe/measure/record an action/condition/event, related/produced by the individual or its surroundings.
- It must be composed in part by technological components (currently there exists an inference of electronic components).

From such a definition it is understood that WMT include a growing set of technological products with a wide range of objectives, covering most fields of research. Various research areas can be consider sub-fields of WMT, such as body sensor networks (BSN), body area networks , wireless body area networks, human activity recognition, wearable health monitoring systems, wearable body area networks, bodynets, pervasive sensors, ubiquitous computing, among others. All mentioned areas share commonalities regarding objectives, methods, hardware and approaches, and sometimes their associated projects differentiate only on their philosophical objective. For instance a human activity recognition system with the objective of monitoring daily activities such as walking, running, jogging, etc., aimed for an athlete, can serve equally for health monitoring purposes (for instance by monitoring an elderly subject's actions) allowing it to be referred as a wearable health monitoring systems (just by changing the subject and the data usage intention). Regardless of the focus, one considered within this body of work that all technology designed for wearability with the objective to monitor intra/inter subject parameters as a WMT. Even though wearable solutions are associated with electronics integrated within clothing, a broader functionality based concept is considered, one that includes all solutions designed for omnipresence continuous usage (Lukowicz, 2007). Following (Avci, Bosch, Marin-Perianu, Marin-Perianu, & Havinga, 2010), one could classify WMT through their functional objectives in four broad groups:

- **Medical applications:** for monitoring, diagnosis and rehabilitation purposes.
- **Home monitoring and assisted living**: such as child and elderly care, cognitive or chronic disorder assistance, among others.

- **Sports:** for performance analysis, injury prevention or even event assistance.
- **Leisure, entertainment or personal assistance**: such for control applications, daily activity assistance. A prime example would be the Google Glass project.

Prior to these human-centric focused designs, WSN paved the way (Akyildiz I. F., Su, Sankarasubramaniam, & Cayirci, 2002) with some examples which challenged the creativity and vision of many researchers of the time, such as: SensoNet and Aware home (GeorgiaTech), WINS (UCLA), PicoRadio (U.C. Berkley), PACMAN (USC), COUGAR (Cornell), among others. The Smart Dust project of the University of California Berkley stands out, although initially a Defence Advanced Research Projects Agency (DARPA) funded project, which sparked a number of advances in design, protocols, and integration (Warneke, Last, Liebowitz, & Pister, 2001); setting the tone for smaller, more efficient and less power consuming sensor systems. One could argue that, WMT fast paced evolution was due to advances in several areas, such as electronics, micro-electromechanical systems (MEMS), and smart sensors. Body sensor networks (BSN) in particular have had a great influence. BSN generally refers to wireless networked wearable electronic devices which seek to measure an array of chemical, physiological, movement or position changes of an individual; and efforts in this area have greatly contributed to the current development of WMT in general.

In 2002 the term body sensor network was introduced by Prof. Guang-Zhong Yang of the Imperial College (London, UK) who spearheaded efforts in the area, initially focused on medical applications and more recently in sports and other fields. Prof. Guang-Zhong team's efforts have facilitated the fast paced evolution of BSNs through numerous articles and conferences organization such as the *International Workshop on Wearable and Implantable Body Sensor Networks*. Worth mentioning is the book *Body Sensor Networks* (Yang G.-Z., 2006) (of which Prof. Guang-Zhong is the editor); which provides the newcomer with a complete recompilation of wireless sensor networks (WSN) and BSN early history and applications, as well as a guide for developing BSN applications based on online (publisher website located) complementary material.

In 2004, the Engineering in Medicine and Biology Society (EMBS) established a technical committee on wearable biomedical sensors and systems (WBSS) (Technical Committee on Wearable Biomedical Sensors and Systems: Home, 2008), thus recognizing this field's importance and the need for further research and development. It was such committee which established that a typical architecture of a WBSS should seek (Bonato P. , et al., 2006):

1. To sense biomedical signals or parameters on user and/or environmental conditions.
2. To route signals or data to a processor (worn by the user).
3. To process signals or data to compute medical and/or environmental parameters (e.g., heart rate, CO_2 level).
4. To interpret parameters.
5. To diagnose conditions and determine the necessary response.

6. To transmit signals, parameters, diagnosis and response to remote monitoring site.
7. To provide a user interface that enables interaction.
8. To execute responses on/by the user.
9. To learn from experience.

Commercially available monitoring solutions; referred to as sensor nodes (or *motes* by some researchers), originally the result of past efforts in WSN, provide a stepping stone to researchers seeking to explore wearable monitoring solutions. By the year 2005, a significant number of BSN solutions already existed (Lo & Yang, 2005), including: MITes, CIT sensor node, BSN node, iMote 2, XYZ sensor node, Telos, M1010, Mica-Z, Tmote sky, Pluto EmberNet. All these systems addressed specific design considerations, and while possessing commonalities among their schemes and components, they were far from being mirror copies of one another. Off-the-shelf monitoring solutions benefit researchers without electronic backgrounds or those who prefer to focus on the captured data and processing algorithms, instead of the sometimes slow process of electronics debugging and troubleshooting process.

Table 2-1. Comparison of commercially available sensor nodes.

Mote	Model	Processor	Features	Power
Imote2	IPR2400	Intel PXA271 XScale CPU	I2C, 2 SPI (one dedicated to radio), 3 high speed UARTs, GPIOs, SDIO, USB client and host, AC97 and I2S audio codec interfaces, a fast infrared port, PWM, Camera Interface, high speed bus (Mobile Scaleable Link).	3xAAA batteries, Li-Ion or Li-Poly batteries, USB
IRIS 2.4 GHz	XM2110CA	Atmel ATmega128L	Digital I/O,I2C,SPI, 10 bit A/D 8 channel, 0-3V input, UART 0-3V transmission levels	2xAA batts. External 2.7 V - 3.3 V
MICAz 2.4 GHz	MPR2400	Atmel ATmega128L	Digital I/O,I2C,SPI, 10 bit A/D 8 ch., 0-3V input, Serial Comm. UART 0-3V TX levels	2xAA batts. External 2.7 V - 3.3 V
TelosB	TPR2400	TI MSP430	Digital I/O,I2C,SPI, 12 bit DAC 2 ports, 12 bit A/D 8 ch., 0-3V input, UART 0-3V TX levels	2xAA batteries, USB v1.1 or higher
Shimmer	SH-SHIM-KIT-001	TI MSP430	Digital I/O, I2C, SPI, 8 ch. of 12 bit A/D, 3D MEMS acc., Freescale MMA7260Q, Bluetooth, Integrated TCP/IP stack for 802.15.4, tilt / vibration sensor, Integ. Li-ion battery manag.	280mAh Li-On batt.

Table 2-1 contains a features comparison of some commercially available sensor network *motes* pioneers (only designs with wireless capabilities were included). However, the features and requirements of these *motes*, tend to be either limited or unnecessary, forcing the project to mold to the characteristics of the device instead of the other way around. Custom solutions are a viable alternative thanks to easy-to-use development kits (such as break-out

and evaluation boards), combined with the formation of multidisciplinary research groups. Such approaches when associated with visual based programming languages (Visual Basic, LabVIEW, etc.) contribute to accelerate the prototyping phase and the proliferation of custom solutions.

The fast pace development of BSN moves hand in hand with advances in what could be considered the most challenging obstacles (Lo & Yang, 2005) (Lo & Yang, 2007) (Tufail & Islam, 2009): biosensor design and packaging, power sources and energy harvesting, low power wireless communication, intelligent sensing and data fusion, standards and integration. In order to gain improved insight into WMT strategies a synopsis of WMT solutions, architecture, and sensor considerations follows.

2.1.1 *Wearable Monitoring Technology Solutions Overview*

It is clear that numerous systems have been (and are currently being) developed for monitoring patients, athletes and individuals in general, with a wide range of objectives. Some seek to monitor biosignals for particular health conditions as a preventive manner, while other seek to optimize the performance of an athlete, and yet others seek to avoid injuries and accidents among rescuers and fighters. In order to appreciate the possible impact of such technology lets consider the case of stroke survivors' rehabilitation.

There were an estimated 10.3 million first-ever stroke survivors in 2005 worldwide (Strong, Mathers, & Bonita, 2007) and stroke is projected to remain a leading cause of disability-adjusted life years (DALYs) (Lopez, Mathers, Ezzati, Jamison, & Murray, 2006) through 2030. Stroke care represents a major burden on global healthcare expenditures, representing roughly 3% of healthcare costs (Evers, et al., 2004). Despite the cost, there exists a general agreement on the importance of addressing the sequelae of stroke. Evidence exists that stroke rehabilitation programs are effective at restoring functional abilities and reducing external dependency (Jette, 2005). A crucial aspect guiding a physiotherapist's clinical reasoning, and thus rehabilitation intervention process, is the assessment of motor performance. A number of viable assessment strategies are currently available (Rivermean Motor Assessment, Fugl-Meyer Motor Assessment, Postural Assessment Scale for stroke patients, and Reach Performance Scale), however they are seldom applied due of time and human resource limitations. Wearable monitoring devices and quantitative based tele-rehabilitation strategies can be developed in order to alleviate the pressure on existing clinical infrastructures, while maintaining a supervised rehabilitation process (Bonato P., 2005) (Patel, Park, Bonato, Chan, & Rodgers, 2012).

Qualitative methods have dominated the fields of medicine, rehabilitation, sports, etc., over quantitative strategies, thus hindering pattern recognition, standardized computational methodologies and other approaches. Presently, there exists a tendency to move away from qualitative scales to quantitative based strategies; in order to avoid subjective or observational approaches, dependent on the specific experience of the viewer and underlined

environmental conditions (Bilas, Santic, Lackovic, & Ambrus, 2001) (Knorr, et al., 2005) (Powell, Hanson, & Lach, 2007) (Turcato & Ramat, 2011). Healthcare, for instance, has greatly benefitted from a large number of researches and products designed for prevention, monitoring and assisted diagnosis (Bonato P., 2005) (Hao & Foster, 2008) (Pantelopoulos & Bourbakis, 2010).

In contrast, the reception of wearable technology within sports has presented resistance. Although, most sports seem receptive to scientific/technological contributions, a slow integration and acceptance process, as to protect the integrity of the event, is observed on athletes, coaches, venue owners (fields, courts, stadiums, sport complex, arenas, etc.), and the public in general (Chi, 2005), alike; the line between honourable improvement and unjust advantage is not always clear. Where does technology stop being a contribution and becomes a hindrance to the purity of the game? It is because of this delicate balance that research in the area of sports monitoring must take an inclusive approach, involving the athletes, coaches and other individuals that are directly affected by the introduction of change.

Regardless of the applicable field, WMT in general can be classified in four intermixing subgroups as seen in Figure 2-1:

- *Reproducibility:* referring to applications that seek to reproduce an event from acquired measurements, such as 3D modelling and personal positioning.
- *Feature Extraction*: applications that seek to establish that an action, pattern or statistically significant occurrence took place (applicable for recognition applications for control, diagnostic, etc.) through a quantifiable scale.
- *Indexing/Performance:* applications that seek to scale the measured actions in order to assess or compare with pre-established references; possible objectives are prevention of unwanted event or determination of closeness to desired limit.
- *Comparison/Progress* Monitoring: applications that seek to compare and contrast measurement occurred in dissimilar scenarios, i.e. taken from varying individuals (or against pre-established reference), on different times or under altered conditions.

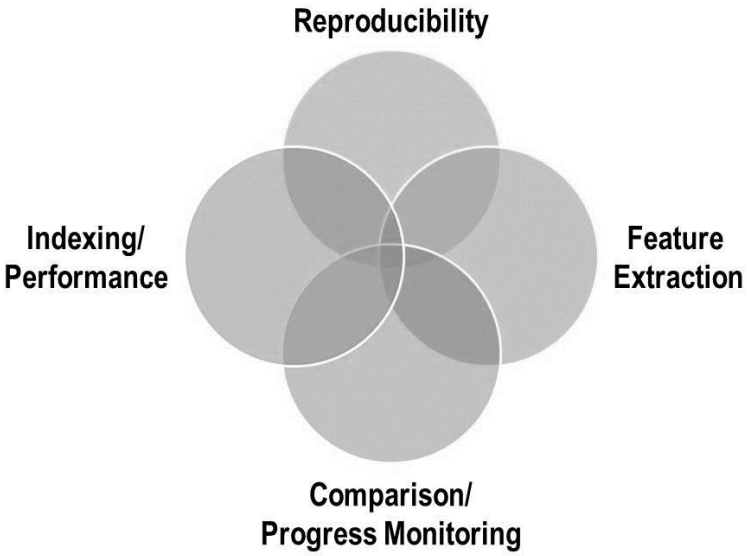


Figure 2-1 — Monitoring solutions objective subdivision.

The presented classification, by no means official, can be extracted from the current trends. Such grouping allows for an improved understanding of wearable technologies overall goals and how their inherent limitations can be circumvented depending of the target objectives. From this study's perspective, it allows for an understanding of the common ground shared by current projects and the foreseen advances within the field. Table 2-2 presents a small sample of WMT projects (with diverse functional objectives) and their characteristics, illustrating their commonalities and differences.

Table 2-2 Wearable monitoring technology overview.

Projects	Target	Sensors	Location	Objective
WEALTHY (Paradiso, Longa, & Taccini, 2005)	Physiological Monitoring	ECG and Impedance pneum. textile electrodes	Torso	Monitoring ECG and respiration.
ClimBSN (Pansiot J. , King, McIlwraith, Lo, & Yang, 2008)	Climbing	3-axis acc.	Ear-worn	Independent threshold trigger and global angle trigger reference for movement extrapolation
OFSETH (Grillet, et al., 2008)	MRI scanning	Silica and polymer optical fibers; Fiber Bragg gratings (FBG)	Torso	Assessment of vital parameters of sedated or anesthetized patients under medical resonance imaging (MRI)
Physiological Monitoring System (Charles & Cain, 2009)	Physiological Monitoring	Temp. and humidity sensors, strain gauges. Optional: conduct. sensor, sphygmom, acc., and pulse-oximeter.	Torso Optional modules: Wrist and ankle	Physiological system with embedded garment sensors suitable for training and performance assessment in sports and for home healthcare
SwimMaster (Bächlin, Föster, & Tröster, 2009)	Swimming	3-axis acc. and feedback modules	Upper and lower back, right wrist	Monitoring swim performance and providing feedback to achieve the desired workout goals
WalkinSense (Tomorrow Options, 2012)	Walking and postural monit.	8 FSR and 3-axis acc.	Shoe insole and ankle level node	Monitoring of plantar pressure and walking speed.
BIOTEX (Coyle S. , Lau, Moyna, & al., 2010)	Physiological Monitoring	Absorbance detection, on-skin pH meter, sodium content sensor	Waist	Fluid handling system for sweat collection and real time pH monitoring, and sodium measurement system
Bioharness (Zephyr Technology Corporation, 2012)	Physiological Monitoring	3.axis acc., temp., breathing rate, ECG	Chest	Performance analysis through physiological and inertial data acquisition for research or physical status t monitoring.

Acc.: accelerometer; Temp: temperature; Conduct: conductivity; Monit: monitoring; Sphygmom.: sphygmomanometer; Pneum.: pneumography

2.1.2 *Wearable Monitoring Technology Architectures*

Following (Pantelopoulus & Bourbakis, 2010), a WMT can be encountered in multiple forms, and from a design perspective one could emphasize:

1) **Microcontroller based design***:* systems based on microcontroller boards (evaluation, commercial, breakout or custom), which serve as control and data collection centres for wired sensors.
2) **Smart textile based design***:* where the sensors are embedded within the clothing, such as vest, shirts, shoes, legwear.
3) **Sensor node based design:** BSN system using sensor nodes for collection and a central node or remote base station for data gathering.
4) **Adapted commercial technology designs***:* such refers to systems based on cell phones, PDA, tablets, smart watches; which add monitoring functionality through smart sensors, generally interconnected through strategies such as Bluetooth or Zigbee.
5) **Intermixture of the above:** such as an embedded mote-based strategy having as central node cell phone.

From a functional perspective we can divide the WMT architecture in four (4) layers (as seen in Figure 2-2) (Bourdenas & Sloman, 2009):

- **Sensor layer:** elements involved in the acquisition of environmental, positional, inertial or physiological parameters.
- **Processing/Interconnect layer**: elements involved in the conditioning, compression or feature extraction process, including routability aspects.
- **Transmission layer:** components involved in the transmission and/or control process, which can occur with local or remote systems.
- **Feedback/Response layer:** elements that respond to the produced data in order to generate a feedback to the user (in these cases the user depends on the perspective, since it could be the person wearing the system, an individual monitoring the data or inter-WMT subjects), or the system itself (safety control elements, power saving, etc.).

The before mentioned layers can be found separate, intermixed or integrated depending on the design, but the objectives of their functions can be readily separated. Until recently, the sensor layer (which will be further discussed in the following section) was composed of sensors and supporting elements, leaving the conditioning to the processing layer. However, it is hard to distinguish between the two in modern smart sensors, which through integration now transform most sensors to complete modules with digital processed outputs. Strong examples of the before mentioned is the Analogue Devices' ADAS1000, which provides a complete ECG analogue front end with respiration and pace detection and Invensense's MPU-9x50 a 9-axis MEMS motion tracking solution contained in a single chip a complete inertial

monitoring solution. These ICs consolidate a number of elements that would, until recently, be considered part of different functional layers.

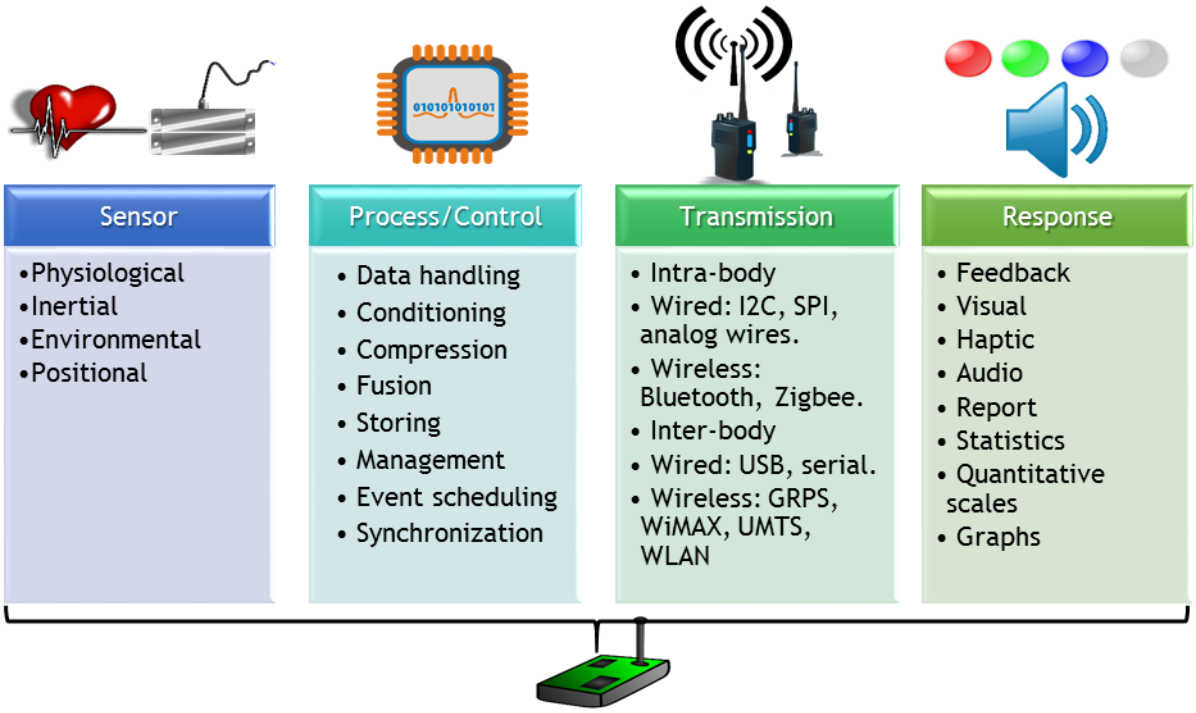


Figure 2-2 — WMT architecture functional layers.

A WMT can be composed of multiple interconnecting modules following a centralized or distributed approached, or even a multi-level mixed approach; Figure 2-3 provides a high view of the WMT elements distribution. It is not uncommon for a central unit to be present, serving as a gathering point of all the acquired data allowing for a centralized management. The central unit could be found locally, as part of the wearable elements, remotely (e.g., an access point or server) or both in the case a local central unit, which communicates with a remote counterpart. The different levels outwards from the sensor communicated through different strategies, being the first group related to wired strategies, analogue (wires, ABUS) and/or digital (I2C, SPI, etc.), connecting the sensor units to their corresponding local control unit (sometimes integrated within the same package or module). From there forward, more complex communication links can be utilized such as ANT, 6LoWPAN, DASH7, ONE-NET, ZigBee, Z-Wave, Wibree, WirelessHART, among many others; including the IEEE 802.15 for Wireless Personal Area Networks (WPAN) and its Body Area Networks task group 6 (Heile B. , 2012). The acquired data can then be utilized for real-time feedback, such as alarms, or stored for post-processing.

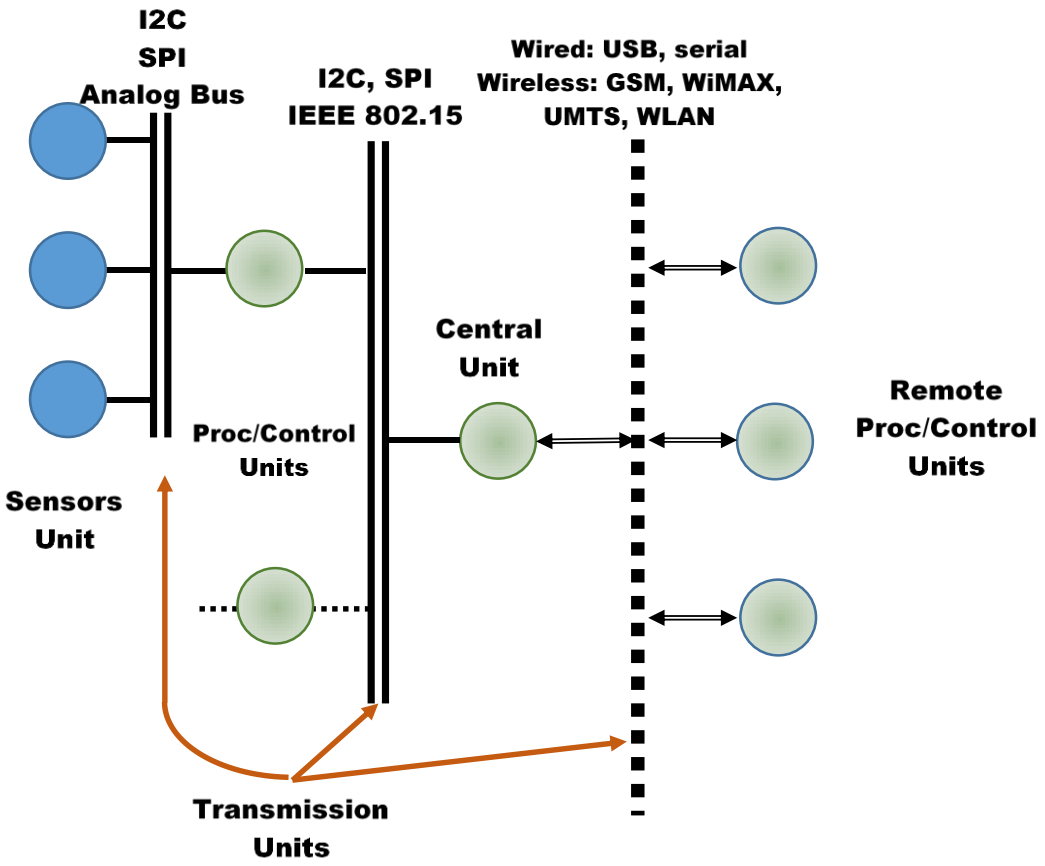


Figure 2-3 — High-level view of WMT architecture.

2.1.3 *Wearable Monitoring Technology Sensing*

Advances in micro-fluidics, material science, nano-structures, micro-electromechanical devices, bioelectrical interfaces, and others, have contributed to a new generation of wearable and implantable sensors. Non-invasive minimally intrusive approaches are the preferred choice, for obvious reasons, and consideration of their positioning, calibration, noise, offset, and deviation, are concerns (Thankler & Kanoun, 2001) (Yang, Lo, & Thiemjarus, 2006). Within WMT, sensors can be broadly classified in four groups (Pantelopoulos & Bourbakis, 2010) (Rehman, Mustafa, Javaid, Qasim, & Khan, 2012) (Lara & Labrador, 2013):

- Chemical or Physiological: also referred to as biosensors (Patel, Anastassiou, & O'Hare, 2006), allow for ECG, glucose, blood pressure and pH monitoring; proving an intrinsic view of a subject's condition. The target stimulus is generated by the human body and it is captured by direct or in-direct contact.
- Inertial: such as accelerometers, gyroscopes, inclinometers, magnetometers. They provide referential information regarding the body's position, movement (speed and directionality), and orientation.
- Location: through relation with external references such as global positioning systems (GPS) or through personal positioning strategies (namely mapping and queries).

- Environmental: refers to cases where the target stimulus relates to the surrounding of the subject, such as temperature, sounds, humidity, and light levels,

From a conceptual perspective, a sensor's structure can be subdivided in four general sections (Thankler & Kanoun, 2001) as seen in Figure 2-4: sensor element, pre-processing, processing and interface. The sensor element is susceptible to predictable output changes due to external influences commonly referenced to specific environmental and situational parameters. The direct output of the sensor element needs at times to be pre-processed in order to transform the measured quantity into a workable signal, generally analogue in nature. Depending on the system, further processing is required and commonly the usage of analogue-digital converters (ADC) is introduced, in order to facilitate the signals handling by obtaining a digital equivalent. Although these stages are enough for a number of setups, it is becoming more and more common that an interfacing stage be added in order to permit the sensor structure to communicate with other elements in the system, common protocols that form part of sensor packages are serial peripheral interface (SPI) and I2C.

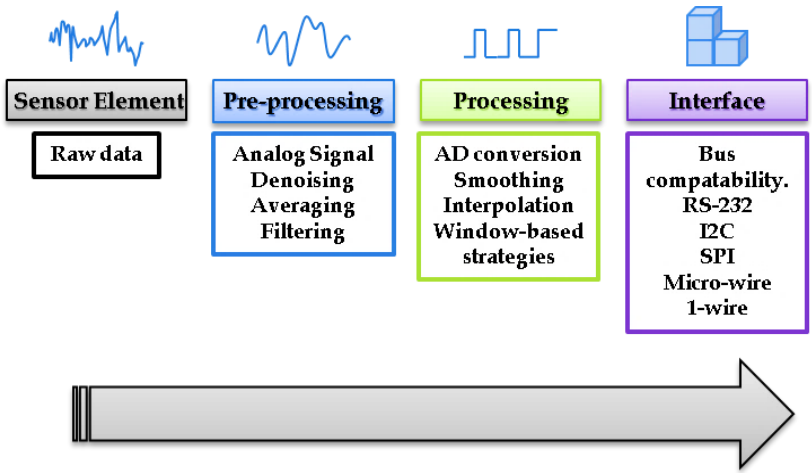


Figure 2-4 — General sensor sections.

Due to environmental and physical factors, sensors can suffer permanent or temporary fluctuations on their measurements which can be addressed during the pre-processing and/or processing stage through compensations and other strategies based on known influences. Such practice is generally referred to as calibration, and is required in order to establish a known and predictable relationship between the sensor element variation and the output signal measurement of the sensor structure. General usage, aging, thermal drift, offset and gain errors, connectors/wires breakage, parasitic elements,) represent real causes for concern. These factors affect the sensors' dynamics, requiring re-calibration of the sensor. Self-testing and self-calibration modules can address such eventualities by comparing the sensor's behaviour with known values and tendencies, and introducing the necessary adjustment or declaring the sensor inoperable if that is the case. Such feedback based modules extend a sensor's reliability and lower processing overhead, thus safeguarding against drifting or deviating data and possibly reducing the power consumption of the overall system. A general

overview of a sensor structure with a self- test/calibration module can be inspected in Figure 2-5.

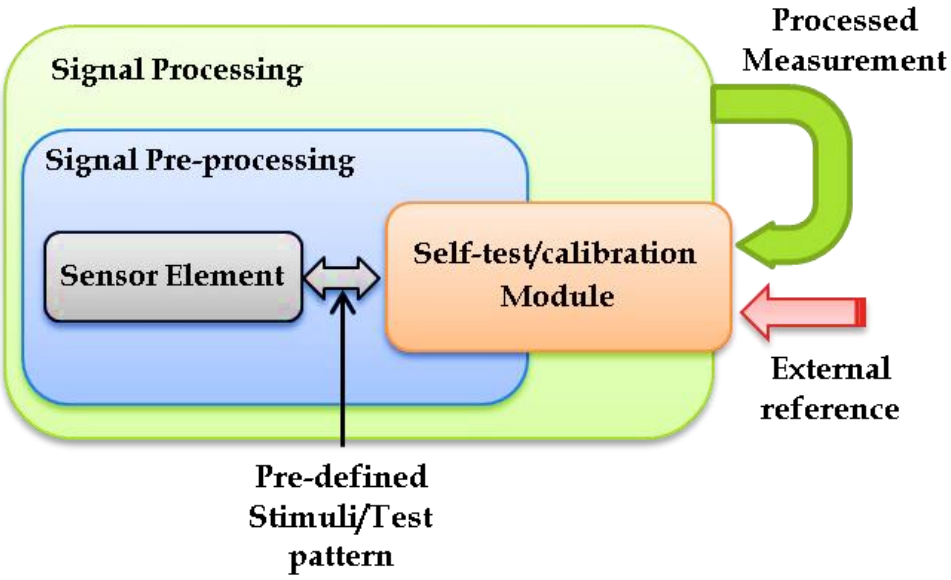


Figure 2-5 — Self-test/calibration module, based on illustration from (Thankler & Kanoun, 2001).

It is true that a number of today's sensors, such as accelerometers, gyroscopes, and magnetometers, include self-testing commands for the purpose of calibration and electrical/mechanical testing; nevertheless, such procedures are seldom readily applicable for in-situ usage (at least not without additional measures). For example, in the case of the ADXL345 Analogue Devices accelerometer (Analog Devices, 2011) the component includes a self-test command that applies an electrostatic force over the mechanical sensor, thus mimicking acceleration. Such self-testing action is additive to the acceleration experienced by the component and dependent of the actual configuration, therefore controlled scenarios are required if one intends to extrapolate test data. Additionally, no internal referencing exists, consequently the resulting data itself requires of processing by an external agent in order to determine a course of action, if required. For the presented case, a true self-test module would permit a comparison against pre-established thresholds under similar conditions, in order to determine if a fault scenario has occurred or if a calibration is required. In order to establish similar testing scenarios the information of additional sensors might be required, extending the testing procedure to elements outside the component part of the same system.

2.2 Mixed-Signal, Analogue and Sensor Testing

Much can be said on the importance of testing and design for testability in this age of Systems on Chip (SoC), System in Package (SiP), mixed-signal ICs, smart sensors, heterogeneous systems, and hybrid technologies. Considering that pervasive technology seeks long-term monitoring, the need for well thought *in-situ* testing strategies for fault diagnosis,

be it fault detection, localization or prediction, becomes a necessity, representing the first step towards true self-maintainability. Not only the systems are expected to be reusable (multiple uses and/or multiple users), and therefore require initialization and calibration mechanisms, but due to the duration of the monitoring, features such as self-calibrating, self-testing, fault-tolerant, high reliability are goals to strive for.

Most sensors are analogue in nature, having at least one signal whose instantaneous voltage is non-deterministic. The imprecise nature of analogue signals, produced by the parametric tolerance of the involved components, requires different testing approaches than their digital counterparts. Typical sensor specifications include sensitivity, resolution, linearity, response time, offset, range, hysteresis, among others (Hosticka, 2007), which need to be sometimes verified *in-situ*, in part due to the lack of formal fault models (Wang, Wu, & Wen, 2006). Traditionally, analogue faults are classified as hard (catastrophic) or soft (parametric) referring to the trace continuity status. However, following several authors (Rogers, 2003) (Feng, Qu, & Potkonjak, 2004) (Bourdenas & Sloman, 2009) (Sharma, Golubchik, & Govindan, 2010) (Warriach, Tei, Nguyen, & Aiello, 2012), when considering sensors we can define four classes of faults from a data centric point of view:

- ***Constant or dead*:** measures provide invariant arbitrary values, uncorrelated to the observed phenomenon.
- ***Random noise*:** increased variance of the target sensor measurements.
- ***Short*:** sharp momentary irregularities between measurement points.
- ***Accumulative or drift*:** continuous deviation trend from the correct value, expressible through a deterministic relation with true value, possibly caused by age, decay, damage, etc.

Moreover, transitory or intermittent faults also represent a concern, such as the ones caused by motion artefacts, which could invalidate a segment of the data while not affecting the rest. Sensors are subject to such transient variations (temperature changes, motion artefacts, positioning fluctuations, sensor contact variation) that can alter a measurement and mask permanent faults or worse, a good sensor, thus testing strategies should consider temporal and hardware redundancy. Although these transitory conditions make it difficult to assure a fault-free sensor status; on a per sensor basis, certain fault conditions can be readily identified (Koushanfar, Potkonjak, & Sangiovanni-Vicentelli, 2003).

Analogue test strategies can be classified in structural and functional, both based on time domain, static or dynamic measurements (pulses, DC or AC stimuli, respectively for instance), in order to assess a number of responses. The main difference between the two lays on fault derivation and modelling strategies (Bushnell & Agrawal, 2000). The functional approach focuses on a specification level perspective, while the structural focuses on element based catastrophic or parametric faults. From an analogue fault diagnosis perspective, two traditional approaches can be mentioned: simulate-before-test and simulate-after-test. The former refers to fault simulation in order to produce a fault response

set to serve as reference, namely to build a fault dictionary; while the later, inverse maps faults based on a theoretical behavioural models (Milor L. S., 1998). While others discuss terms such as range checking, analytical redundancy, model-based fault detection, and fault trees, when referring to sensor fault detection strategies (Rogers, 2003). Regardless of the before mentioned classifications, testing strategies can be clustered based on broader classes from a system perspective: intrinsic and extrinsic (Baker, Richardson, & Dorey, 2002). The intrinsic or divide-and-conquer approach, which has proved fundamental for digital testing, seeks the isolated test of elements following a bottom to top tactic. Such approach manages to compartmentalize the complexity of the problem and permits simple measure to be taken on a per block basis. However, some analogue elements cannot be readily isolated or effectively tested independently from operating conditions; moreover in the case of WMT.

Sensor networks (BSN, WSN, and WMT) present unique challenging characteristics such as numerous heterogeneous distributed components in multi-layer unconventional setups. Concepts such as autonomic sensing, context awareness and data fusion have been utilized in order to address such characteristics (Yang G.-Z., 2006). Since it is natural that the behaviour of an individual has direct effects over the physiological data collected, one can optimize the monitoring elements configurable aspects based on the contextual scenario; in this way saving resources and improving the value of the data being transmitted or stored (Thiemjarus, Lo, & Yang, 2005). For example, when capturing an ECG signal additional information is captured as well, such as breath rate, noise, among others. Such interference or superposition complicates efforts of feature extraction, pattern recognition, and machine learning. Tactics such as source recovery have been introduced in order to solve these issues; and to gain improved insight into multi-source signal variation (Lo, 2006). These concepts can also be utilized for calibration and fault detection purposes by taking advantage of redundancy (following a known good device, KGD, approach), correlation of faults to detected events (such as detecting motion artefacts in a signal through inertial event detection), or a holistic testing approach (multi-level analysis for fault location).

2.2.1 *Data centric Testing Approaches*

Multi-modal sensor fusion strategies can be categorized in: competitive, complementary and cooperative (Yang & Hu, Muti-sensor fusion, 2006). Competitive approaches provide mechanism for *in-situ* calibration and fault detection through sensor data redundancy. Multiple sensors providing equivalent data open the way for statistical schemes that permit localization of outliers, noise rejection and other group perspective methods. On the other hand, cooperative multi-fusion approaches data consistency (were multi-sensor data are combined to generate information not readily attainable by any individual sensor) are quite sensitive to individual sensor inaccuracies, and the application of methods such as maximum likelihood or Bayesian approach can distinguish between a random noise or a faulty element. Such approaches can be used to address scenarios where the corresponding sensor stimuli is

outside the electrical domain, thus complicating any direct testing methodology; e.g., temperature, light or force sensors; and even alleviating the need for theoretical analytical models. A review of sensor networks fault detection efforts follows.

Koushanfar, Potkonjak and Sangiovanni-Vicentelli (Koushanfar, Potkonjak, & Sangiovanni-Vicentelli, 2003) presented an on-line sensor fault detection strategy for an arbitrary system of heterogeneous sensors with an arbitrary type of fault model, which takes advantage of multi-modal sensor fusion strategies by evaluating the inconsistency degree when removing a sensor at a time from the fusion minimization. The premise being that, if a sensor removal from the minimization significantly reduces discrepancy, the most likely conclusion is that the sensor is faulty. Separately, Rogers (Rogers, 2003) presented comparable detection approaches following the same premise, based on standard deviation and signal-to-noise ratio (SNR) evaluation; however from a specific sensor perspective. Alternatively, Bychkovskiy and his co-authors (Bychkovskiy, Megerian, Estrin, & Potkonjak, 2003) presented a collaborative approach to in-place sensor calibration (i.e., colibration) by formulating a pair-wise amplitude based sensor relation through temporal correlation during co-measurable events, then attempted simultaneous consistency consolidation of the group of pair-wise relations. Other, such as the strategy presented by Feng, Qu and Potkonjak (Feng, Qu, & Potkonjak, 2004), follow a nonparametric stochastic approach through error models based on probability density functions leveraging kernel density estimation and the maximal likelihood principle, for sensor bias compensation. While Kulla's (Kulla, 2013) approach models each sensor in a network using the minimum mean square error estimation and the multiple hypothesis test utilizing the generalized likelihood ratio for sensor fault identification (modelling common fault such as bias, drift, precision degradation and gain).

Sharma, Golubchik and Govindan (Sharma, Golubchik, & Govindan, 2010) effectively summarize the different sensor faults detection methods for generic sensor networks: "Rule-based methods leverage domain knowledge to develop heuristic rules for detecting and identifying faults. Estimation methods predict *normal* sensor behaviour by leveraging sensor correlations, flagging anomalous sensor readings as faults. Time series analysis based methods start with an a priori model for sensor readings. A sensor measurement is compared against its predicted value computed using time series forecasting to determine if it is faulty. Learning-based methods infer a model for the "normal" sensor readings using training data, and then statistically detect and identify classes of faults."

Each of the before mentioned approaches has their particular benefits and disadvantages. While rule based methods can be effective and efficient through result driven classification and decision making, they are dependent on domain knowledge extraction which could prove to be a daunting task in wearable scenarios due to the complexity of the data and wide variability for inter and intra case scenarios. On the other hand, estimation methods provide a stochastic approach that proves advantageous for stable scenarios, where sensor behaviour is contained within predictable domains. However, factors such as drift, hysteresis and sharp

momentary variations could produce unreliable determinations. Time series analysis based methods can contend with drift and hysteresis, however the assumption that forecasting is possible imposes a serious limitation when considering the ever changing wearable sensors scenarios. Learning-based methods, such as machine learning, required of numerous iterations covering all targeted associated scenarios, which is not always possible or realistic. That said, they remove the need for model definition, domain analysis or even sensor correlation, simplifying the task.

Although a number of the mentioned sensor network strategies are, in theory, suitable for some WMT scenarios, some inherent limitations must be considered. Within WMT, sensor redundancy, density and distribution might proof insufficient (when compared to WSN scenarios assumptions), not to mention the heterogeneousness of the sensors involved (not only in type, but also in location and measureable targets). Kim and Prabhakaran (Kim & Prabhakaran, 2011) considers the particularities of BSN and iterates fault scenarios with a different perspective:

- Fault is localized and detectable by one sensor, without previous trend knowledge;
- Fault is detectable through comparison with sensor trend history;
- Fault not detectable on sensor readings, nonetheless the recorded activity differs from the individual's trends.

Such alternative perspective allowed fault identification and isolation for motion sensors, through the application of a sliding window technique for data segmentation, and the extraction of relative positional distance (between correlating nodes), power spectral density and singular value decomposition, with history support for the latter two.

Bourdenas and Sloman (Bourdenas & Sloman, 2009) presented a BSN fault detection strategy through variance analysis (for short and constant faults) and regression methods combined with domain knowledge (for accumulative faults), however avoiding the assumption of equivalent local neighbourhood phenomenon monitoring (i.e., local neighbourhood sensor redundancy). Föster's groups considered sensor displacement for wearable systems and developed an adaptive online unsupervised classifier self-calibration algorithm, using a nearest class centre classifier (Föster, Brem, Rogen, & Tröster, 2009). Mahapatro and Khilar (Mahapatro & Khilar, 2011), on the other hand, focused on transient faults, since they represent 80% of fault occurrences. His groups exploited mutually correlated information from multiple sensors, not necessarily related by type or localization. For instance, hemodynamic signals and ECG have mutually correlated information of the heart, thus can be utilized to verify each other's state. An adaptive algorithm was utilized to fine tune the detection parameter as to properly observe the fault, under the assumption of transient faults tend to become constant eventually.

Nonetheless, while some aspects are more restrictive within WMT other present some relaxation. For instance, on the past decade IBM reported that cell phones needed to be tested in less than one-third of a second as to achieve an economical competitive edge

(Koushanfar, Potkonjak, & Sangiovanni-Vicentelli, 2003). In contrast, WMT on-line testing is not subject to such speed or throughput, since human activities are measured in terms of seconds (even minutes) well outside the expected sensor sampling rate of hundreds of Hertz (Lara & Labrador, 2013). The before mentioned fault detection and calibration approaches have a data centric focus, while powerful and useful for some applications rely exclusively in data processing, which might be limited for WMT scenarios. From a hardware perspective, specific considerations must be taken to address the management of sensors, including resource sharing, data transport, synchronization, and in this case: testing. Regardless of the fault detection strategy, observability and controllability are common obstacles traditionally addressed through design-for-testability (DfT) strategies such as analogue test buses, scan methods, built-in-self-test blocks and test instruments.

2.2.2 *Design for Testability*

"*The collection of techniques that comprise Design for Testability are, in some cases, general guidelines; in other cases, they are hard and fast design rules. Together they can be regarded essentially as a menu of techniques, each with its associated cost of implementation and return on investment*" (Williams & Parker, 1983). Although some researchers limit the extent of DfT to those methods that "aim to improve the controllability and observability of internal nodes" (Milor L. S., 1998), thus separating DfT strategies from BIST, DfT strategies vary depending on the design and specific objectives of the target system, and can be classified in structured and non-structured. Structured strategies strive for generalized adaptable solutions, while non-structured follow a custom approach. In general, there are specific goals that DfT aim for, such as stimuli generation (associated with BIST and embedded test instruments for *in situ* strategies), access to response (observability), test control, signals routing and isolation (controllability). A general BIST structure can be observed in Figure 2-6, illustrating the before mentioned elements.

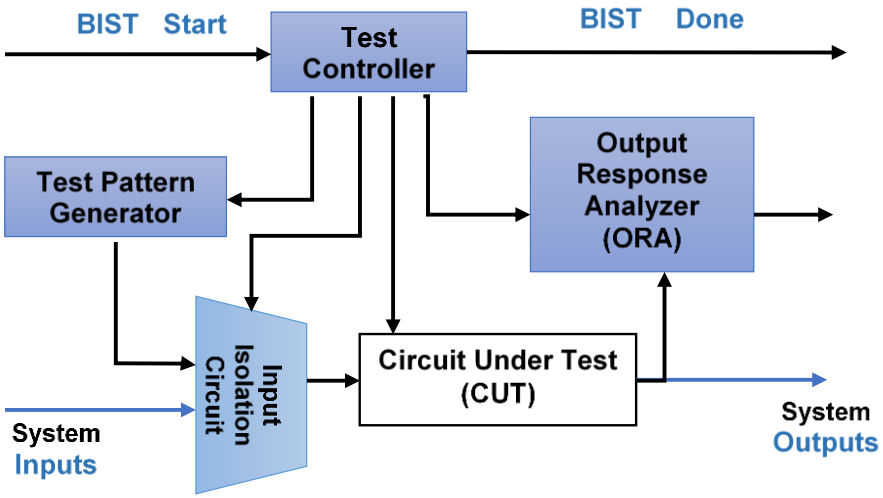


Figure 2-6 — General BIST structure (Stroud, 2012).

The last decade has witnessed a shift on testing approach paradigms, opting for embedded system access versus more traditional approaches such as in-circuit test and flying probes, driven by the increase in complexity, not only of electronic designs, but also of the packages themselves (International Technology Roadmap for Semiconductor, 2011). Multi-die integrated circuits in system on chip (SoC) structures or complex 3D (three dimensional) system in package (SiP), accompanied by multi-layer boards have greatly limited the access to internal circuit nodes. Such trend has been emphasized by *in-situ* strategies through the use of test instruments. In this work, test instruments encompass all hardware based modules that improve testing capabilities, following a Built-in-Test (BIT) approach. Such instruments could serve multiple purposes and are not limited to testing functionalities. Strategies such as BIST are becoming commonplace at all levels of design consideration. These strategies incorporate a local detection and diagnosis module which can make decisions independently or form part of a larger testing mechanism. The growing complexities, escalating heterogeneous nature of systems and space limitation found on today's modern ICs and electronics have left traditional testing strategies unprepared and insufficient, transporting the solution towards the interior of the systems themselves; proving an obstacle for the development of streamlined testing solutions (International Technology Roadmap for Semiconductor, 2011) (Sunter S. , 2011).

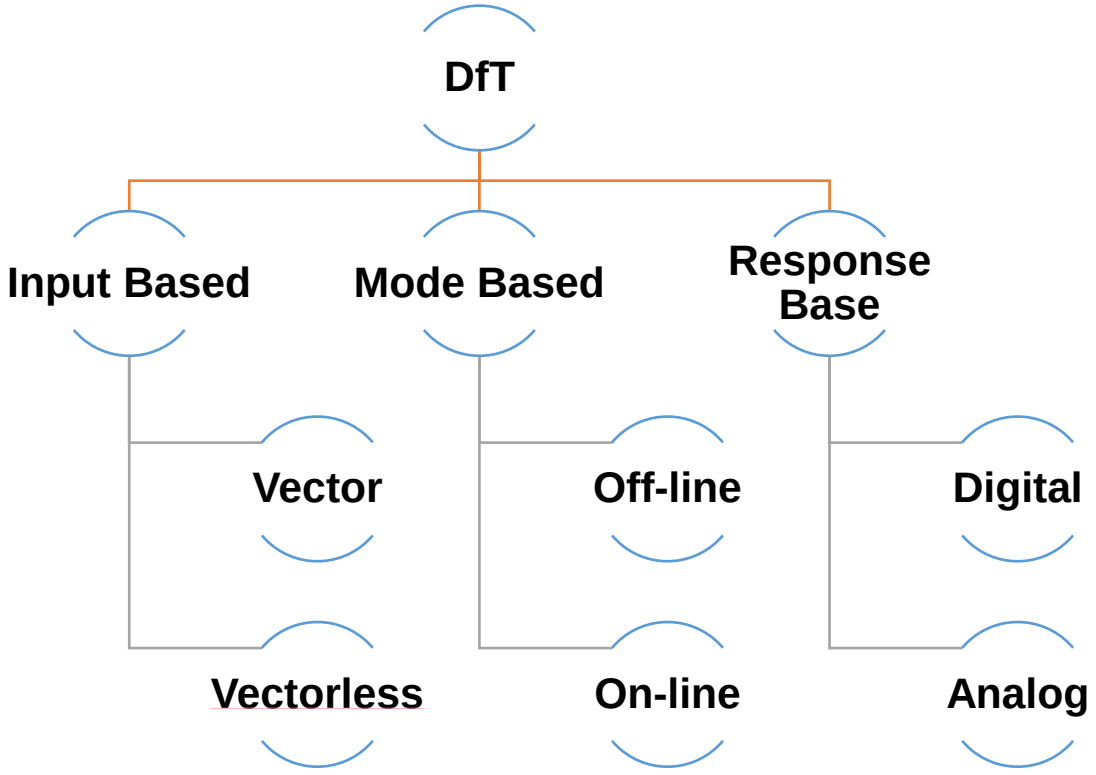


Figure 2-7 — DfT strategies classification.

Figure 2-7 encompass DfT strategies classification based on the stimuli, operation mode and response (San-Um, 2010), illustrating their flexibility and variety. Follows an overview of each type:

- ***Vector Input Based*:** refers to strategies that utilize a direct stimuli for test generation, by means of a test pattern generator. The stimuli can have a time-domain, DC or AC nature. Within the digital strategies test vectors selection focus on redundancy minimization and coverage optimization through test models consideration; however analogue testing cannot readily take advantage of such strategies. The imprecise nature of analogue signals also represents a challenge when generating analogue test stimuli, which in principle requires being an order of precision above the target element.
- ***Vectorless Input Based*:** refers to strategies that do not require an input stimuli for test generation; achievable through circuit reconfiguration. Oscillation BIST (OBIST), first introduced by Arabi and Kaminska (Arabi & Kaminska, 1996) (Arabi & Kaminska , 1997) and more recently adapted by Das and his co-authors (Das, et al., 2007) and Arbet and his group (Arbet, Stopjakova, Majer, Gyepes, & Nagy, 2013), exemplifies such strategies by applying circuit reconfiguration to induce an oscillatory state of the target element, whose associated frequency can be used for parametric variation determination. Another known technique is through reference comparison of the DC quiescent current (I_{DDQ}) between the target and the supply (Rajsuman, 2000).
- ***Off-line Mode Based*:** refers to strategies that utilize a test operation mode in order to isolate the target element from normal operation. Such strategies are widely used for digital and analogue scenarios, and permit the testing of the target element without directly affecting the surroundings elements. A more comprehensive review of classic structured DfT multi-mode frameworks can be found towards the end of the chapter.
- ***On-line Mode Based*:** refers to strategies that perform testing concurrently with normal operation. Such strategies are not generally applicable to most testing scenarios due to normal operation signal integrity considerations, especially when considering embedded scenarios. However, strategies such as the presented by Degen and Jackel (Degen & Jackel, 2008) and (Kim, et al., 2010), for continuous electrode-skin impedance monitoring for ECG acquisition systems, illustrate the effectiveness on such alternatives. In both cases, the electrode-skin impedance variations were monitored concurrently with normal operation through the injection of a stimulus frequency outside of the normal operation frequency range of interest.
- ***Digital Response Based*:** refers to strategies whose test response takes place in the digital domain. An archetypal strategy is the Hybrid BIST (HBIST) (Ohletz, 1991), as seen in Figure 2-8, which uses built-in logic block observer (BILBO) or linear-feedback shift registers (LFSR) for hybrid test signal generators (HTSG), and analogue

multiplexer for isolation and stimulus routing. Other strategies utilize sigma-delta (ΣΔ) digital signature generation, sometimes combined with multi-input shift register (MISR) for compression (Mir, Lubaszeweki, Liberali, & Courtois, 1995).

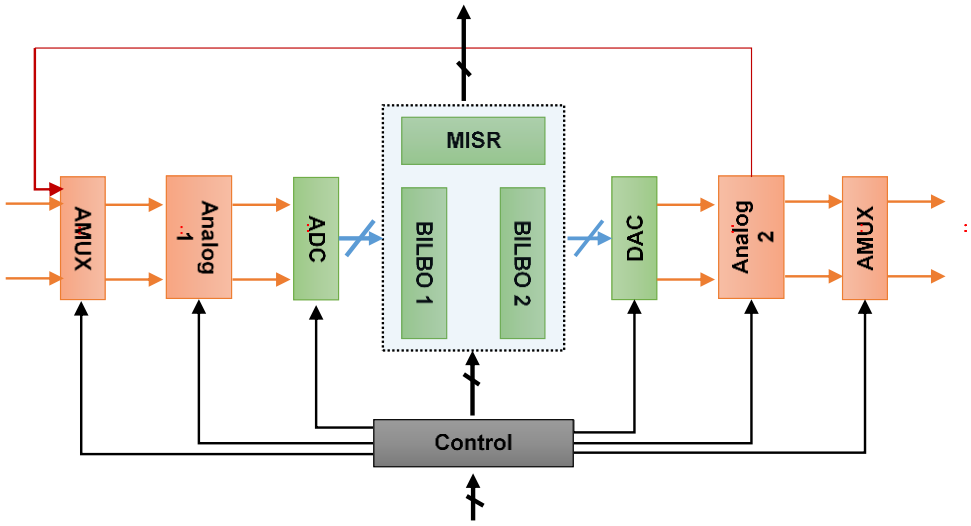


Figure 2-8 — HBIST Structure, based on figure from (Mir, Lubaszeweki, Liberali, & Courtois, 1995), concept from (Ohletz, 1991)

- ***Analogue Response Based:*** refers to strategies whose test response is of an analogue nature. Translation-BIST (Slamani & Kaminska, 1993) for example, is a structured strategy which manages test stimuli/response through analogue multiplexers, in order to use detection and translation circuits that convert functional test responses into proportional DC voltages, that can be then compared to references and its response allocated in a digital shift register. The ABIST strategy on the other hand, introduced by Wey (Wey, 1990), follow an analogue scan path approach where voltages are stored in scan cells, composed of sample-and-hold circuits. An alternative current based scan path was later presented by Wey and Krishnan (Wey & Krishnan, 1992) and later Soma (Soma, 1995), based on current-mirrors.

Regardless of the specificities of the test or design, mechanisms for test control are key for managing the involved elements. Although, no wide-spread strategies currently exist for structured analogue or mixed-signal testing (International Technology Roadmap for Semiconductor, 2011) (Sunter S., 2011), from an embedded, board, or WMT perspective; a number of standards have served as the basis of a number of efforts, including recent international projects such as the NanoTEST, TOETS and ELESIS international projects.

2.2.3 *Structured Design for Testability Standards*

Testing and design for testability is in itself an effort that has counted with the support of academy, industry and designers; which allowed for the formulation of several protocols that seek to alleviate the problems of accessibility and space within this increasingly complex scenario. Among the most known protocols for testing digital and analogue interconnections and inter-module elements one finds the: IEEE 1149.1, 1149.4. 1149.6, 1149.7, 1500 and 1687

test bus standards. The 1149.X standards serve as building blocks for testing and self-maintenance strategies, in this rapidly developing field; introducing reusability and compatability, key elements for the fast paced advancement in any research area.

The IEEE Standard 1149.1 represents the cornerstone of boundary-scan testing methodologies. Introduced in 1990 (IEEE Std 1149.1-1990, 1990) and recently revised in 2013 (IEEE Std 1149.1-2013, 2013), it has taken 20 years for an augmentation to arrive, the 1149.7 (IEEE Std 1149.7-2009, 2009); although, industry acceptability will truly define it as a replacement. The 1149.1, also referred to as JTAG (Joint Test Action Group for the task force that proposed it), was originally intended for alleviating board-level interconnect testing complexity, however today JTAG seems more associated to in-circuit programming strategies than testing itself. Multi-layer boards and increasing high density scenarios left a reduced space for testing points and other traditional methods for interconnect testing. Nowadays, board-level and chip-level complexity is orders of magnitude higher, compare to the early 90's, and yet the 1149.1 is still the workhorse of digital interconnect testing at board and chip level. The 1149.7 introduces a set of new testing and debugging features, divided in class structure, while remaining backward compatible with the 1149.1. The 1149.1 takes advantage of a boundary-scan strategy, using an array of small modules, which intersect the data flowing through the IC pins. A small state machine, in combination with a reduced set of instructions and registers, permits controllability and observability to the input/output (I/O) of the IP cores and IC packages.

The IEEE 1149.4 and 1149.6 test buses seek to address the challenges of mixed-signal design testing. The 1149.4 could be seen as an extension on the 1149.1 which offers "to improve the controllability and observability of mixed-signal designs and to support mixed-signal built-in test structures in order to reduce both test development time and testing costs and to improve test quality" (IEEE 1149.4-1999, 2000). On the other hand, the 1149.6 also extends the 1149.1 in order "to improve the ability for testing differential and/or ac-coupled interconnections between integrated circuits on boards and systems" (IEEE Std 1149.6-2003 , 2003). So, while 1149.4's modules allow access to perform voltage and current measurement through the injection of current and/or voltage at strategic points, the 1149.6 concerns itself with the effects of increasingly faster clock frequency which are converting well-behaved digital signals into pseudo-analogue forms, thus increasing the handling complexity.

On the other hand, in order to maintain the simplicity of the before mentioned standard (by avoiding numerous instructions and structure complexity) and to address inherent limitations due to SoC architecture and embedded instruments, strategies based on wrappers and network access registers resulted on standards such as the IEEE 1500 and the IEEE STD. 1687.Such approaches permit a standardized interface to shared networks, thus contributing to partition-based and testing reusability.

Next subsection presents technical overview of some of the before mentioned standards.

IEEE Standard 1149.1

The increasing complexity of electronic units during the 1980's, caused by decreasing size of the packaging, multi-layer printed circuit boards and increasing number of pins, caused test time to increase and bed-of-nails apparatus (the standard testing system of the time) to become inefficient. In order to resolve this accessibility problem, the Joint Test Action Group (JTAG) was formed in 1985; and the result of this industry collaboration was the IEEE Standard Test Access and Boundary-scan Architecture, or IEEE Standard 1149.1, sometimes referred to as JTAG. The standard defines: "Circuitry that may be built into an integrated circuit to assist in the test, maintenance and support of assembled printed circuit boards and the test of internal circuits is defined. The circuitry includes a standard interface through which instructions and test data are communicated. A set of test features is defined, including a boundary-scan register, such that the component is able to respond to a minimum set of instructions designed to assist with testing of assembled printed circuit boards. Also, a language is defined that allows rigorous structural description of the component-specific aspects of such testability features, and a second language is defined that allows rigorous procedural description of how the testability features may be used" (IEEE Std 1149.1-2013, 2013).

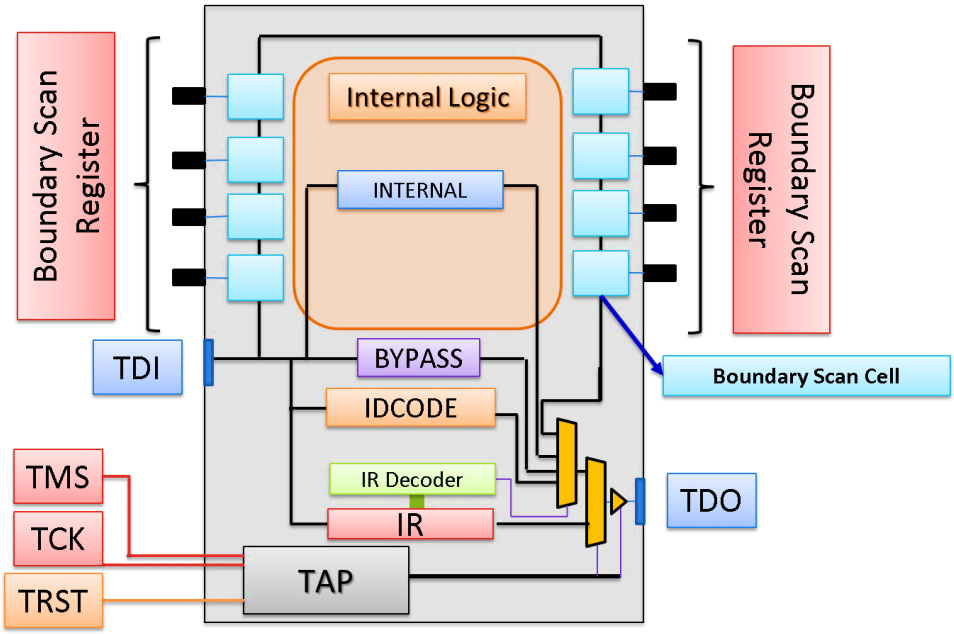


Figure 2-9 — IEEE 1149.1 compliant architecture (IEEE Std 1149.1-2013, 2013).

The mentioned circuitry, seen in Figure 2-9, permits the input/output of data through a shift register chain, referred to as the boundary-scan register on a module basis. The boundary-scan register is composed by boundary-scan cell, as seen in Figure 2-10, which provided controllability and observability, depending on its target function, through scan test principles. Multiple 1149.1 compliant modules can be daisy-chained together in order to form a unified test bus. The architecture counts with 4 mandatory lines and one optional, referred

to as the test access port (TAP): TDI (Test Data In), TDO (Test Data Out), TMS Test Mode Select, TCK (Test Clock) and TRST (Test Reset, which is optional).

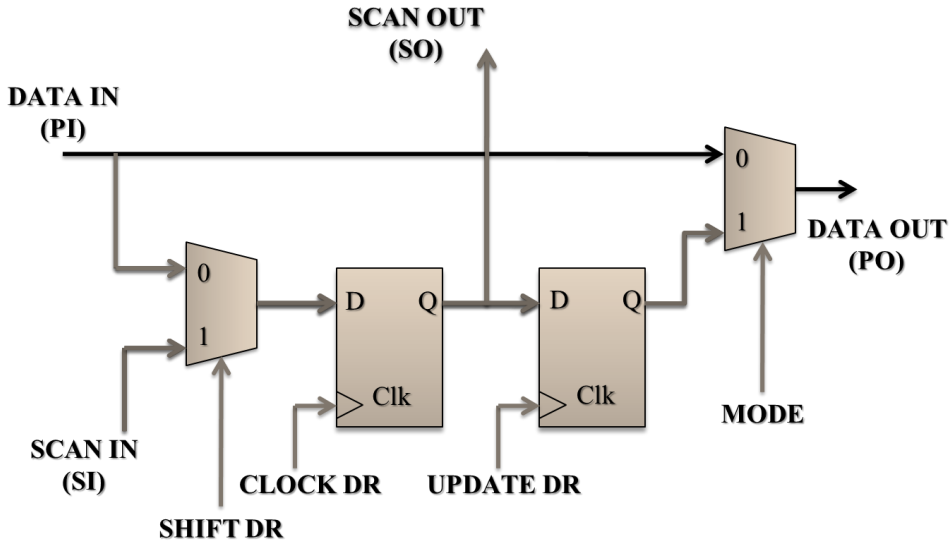


Figure 2-10 — Generalized boundary scan cell (IEEE Std 1149.1-2013, 2013).

The TCK and TMS signals control the TAP Controller, a synchronous finite state machine (seen in Figure 2-11). The TAP Controller regulates the flow of data from the TDI to the TDO, with several potential register allocated in between depending on the target instruction. There are two types of registers in a boundary-scan compliant device, which are the instruction register (IR) and the test data registers (TDRs). The instruction register is utilized to select the test to be performed or the test data register to be access or both, by permitting the shift of an instruction into the module. At least two TDR must be present, the Bypass Register and the Boundary Scan Register, although register expandability is one of the strong elements of the 1149.1.

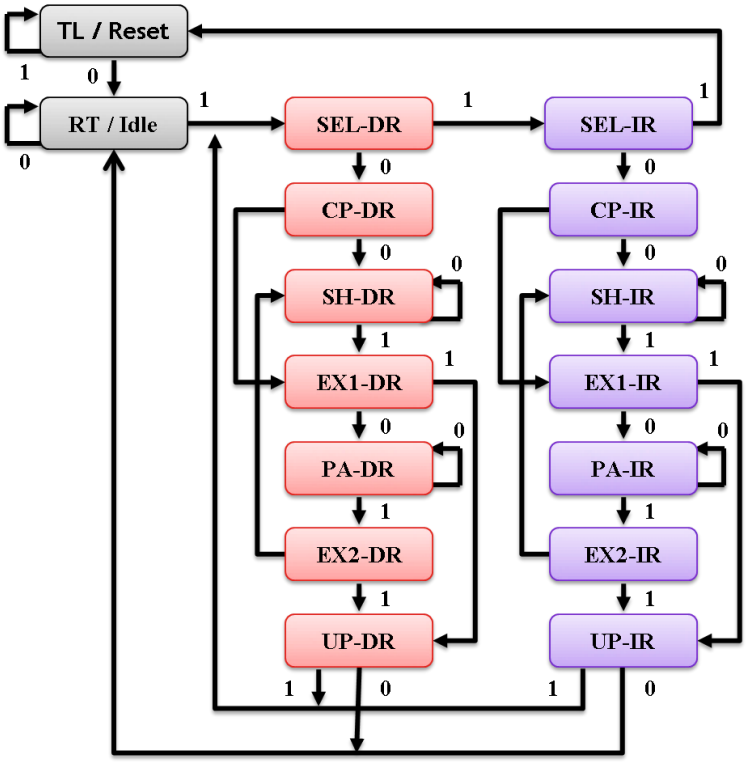


Figure 2-11 — Test access port controller (IEEE Std 1149.1-2013, 2013).

There are 4 mandatory instructions, BYPASS, SAMPLE, PRELOAD and EXTEST as of 2001 and a number of declared optional instructions (INTEST, IDCODE, USERCODE, RUNBIST, CLAMP, INIT_SETUP, ECIDCODE, etc.). The BYPASS instruction selects the BYPASS register to be connected between TDI and TDO. This effectively shortens the chain to 1 bit, reducing the test time if this particular device is not involved in testing at that moment. The remaining mandatory instructions select the boundary-scan register:

- **SAMPLE:** takes a snapshot while the device is functionally active.
- **PRELOAD:** allows data to be loaded to the boundary-scan register prior to a test instruction.
- **EXTEST:** intended for off-module circuitry testing (opposed to the INTEST optional instruction), generally preceded by a PRELOAD instruction in order to establish a test stimuli.

IEEE Standard 1149.4

The IEEE Standard for Mixed-signal Test bus, first released in 1999 and revised in 2010 (IEEE Std 1149.4-2010, 2011), extends the 1149.1 through the incorporation of a two wire analogue bus, analogue boundary modules (ABM) and a test bus interface circuit (TBIC), as seen in Figure 2-12. The 1149.4 aims to standardize interconnect, parametric and internal testing, through the stimulation and observation of analogue nodes in the continuous current and voltage domain (Hannu, Hakkinen, Voutilainen, Jantunen, & Moilanen, 2012). The TBIC structure is utilized to connect the modules internal analogue bus with the external analogue boundary bus, as well as providing noise reduction, interconnect test and validation, as well

as bus calibration capabilities, as seen in Figure 2-13. The ABM provides controllability and observability of the associated analogue pins, as well as core isolation, interconnect test (through reference voltage assignment), 1-bit voltage representation of the pin through threshold comparison, and parametric measurement capability through a voltage reference, as seen in Figure 2-14. The digital boundary modules offer the same functionality as provided by the boundary-scan cells of the 1149.1 architecture. The instruction set includes the 1149.1 mandatory instructions and an additional PROBE instruction meant for real time monitoring of a target digital or analogue pin, while maintaining core functionality. The optional 1149.1 instructions are adapted to serve for both the digital and analogue pins, such as INTEST, CLAMP, HIGHZ, RUNBIST, IDCODE, USERCODE, etc.

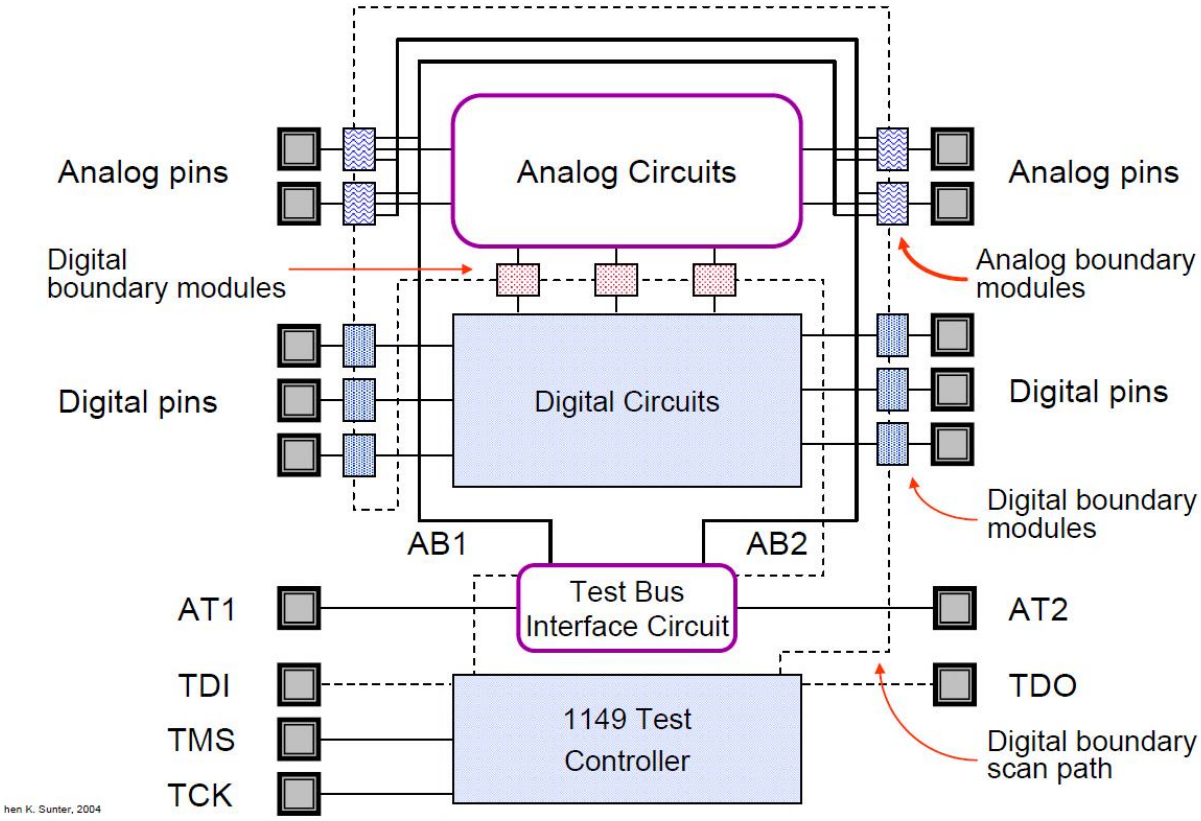


Figure 2-12 — IEEE standard 1149.4 architecture. Extracted from (Sunter S. 2004), concept from (IEEE Std 1149.4-2010, 2011).

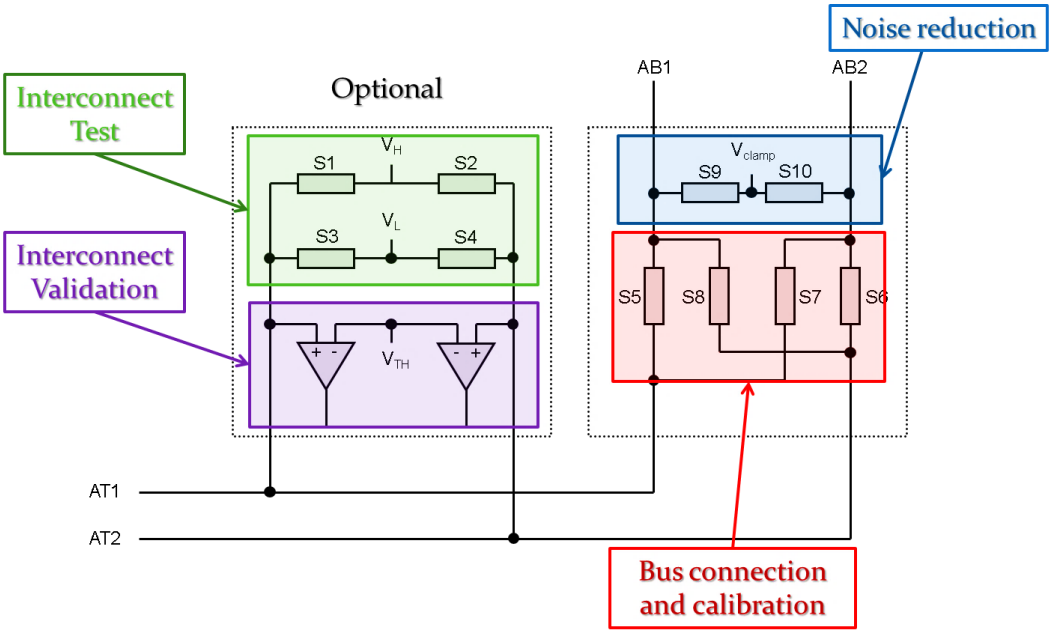


Figure 2-13 — Test boundary interface circuit (IEEE Std 1149.4-2010, 2011).

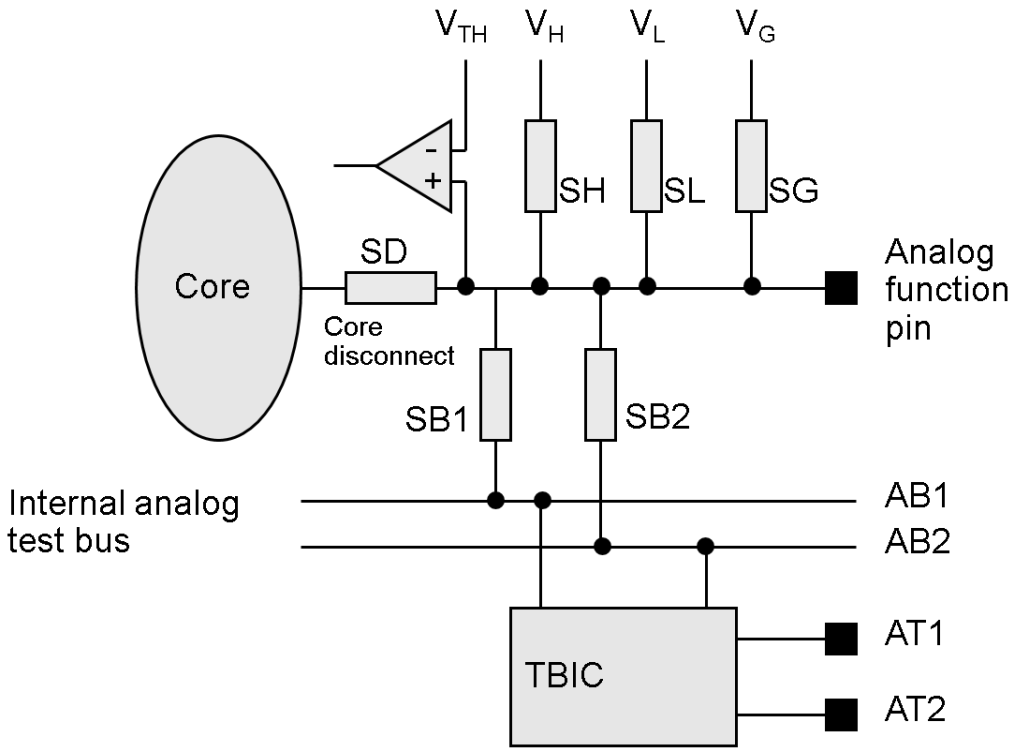


Figure 2-14 — Analogue boundary module structure (IEEE Std 1149.4-2010, 2011).

IEEE Standard 1500

The IEEE Standard Testability method for Embedded Core-based integrated circuits: "*Defines a scalable architecture for independent, modular test development and test application for embedded design blocks and also enables test of the external logic surrounding these cores. It can also be used to partition large design blocks into smaller blocks of more manageable size and to facilitate test reuse for blocks that are reused from*

one SoC design to the next" (IEEE Std 1500-2005 IDAMS 3.5 test, 2012). The 1500 standard differs from the 1149.X standards in that, it assumes that all issues related to TAM are addressed by the designer; although it is sometimes paired with the 1149.1. Conceptually, cores within SoC equiparate to chips within boards; and although a number of strategies applied to the latter translate to the prior, some fundamental differences arise. While chips can be tested prior to board insertion, cores cannot, thus their testing must occur *in-situ*. Additionally, a number of issues need to be considered, such as (Lee K. J., 2006): mixing technologies, deeply embedded cores, hierarchical cores, different core providers, IP protection, parallel test, test scheduling, etc. From a hardware perspective, multiple non-mergeable cores testing aspects can be homogenized through the use of a core wrapper structure (on each core), test patterns source/sinks, and an undefined TAM, as seen in Figure 2-15, addressing test reusability (and a number of issues) while providing core interoperability and plug-and-play consideration (DaSilva, Zorian, Whetsel, Arabi, & Kapur, 2003).

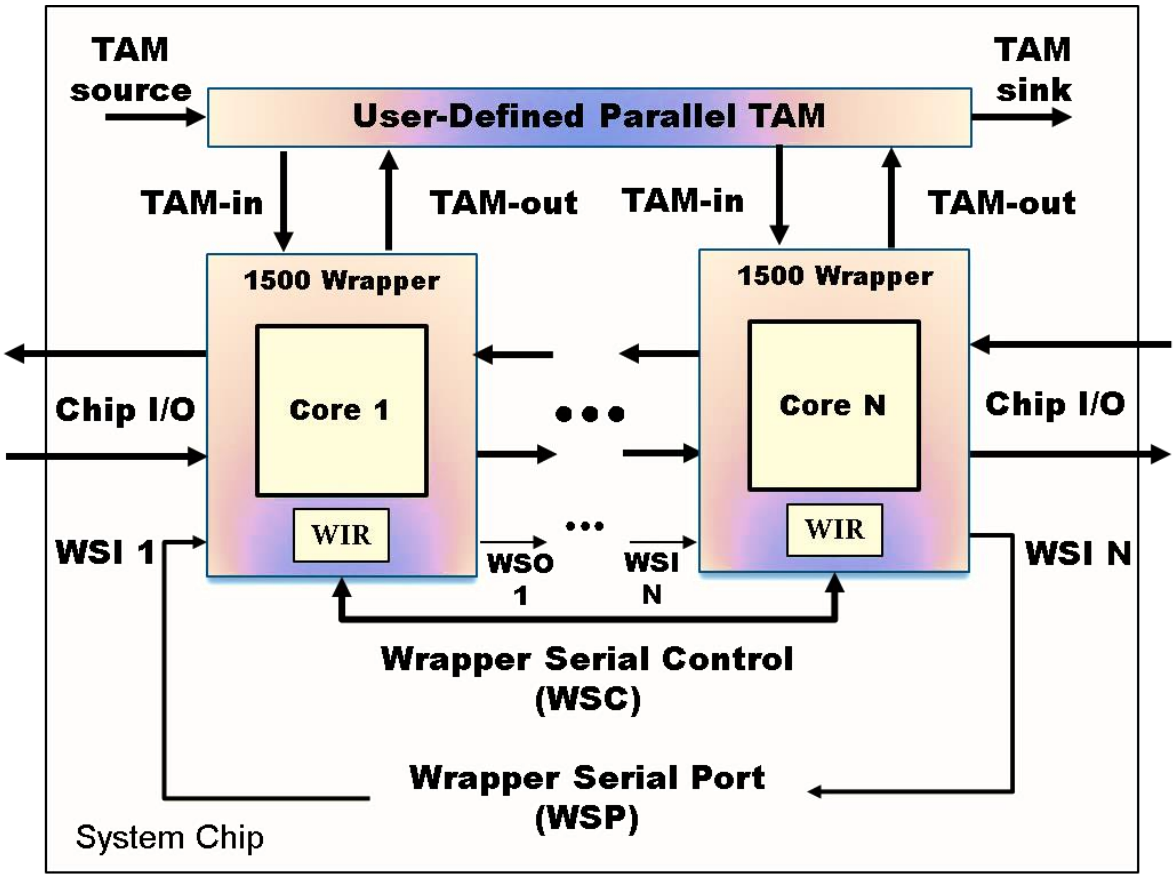


Figure 2-15 — IEEE 1500 overview (IEEE Std 1500-2005 IDAMS 3.5 test, 2012).

The IEEE 1500 infrastructure supports both serial and parallel data/control signals (although serial elements are mandatory), and is composed by three registers (while additional core data registers are permitted), a wrapper serial port (WSP) and an optional wrapper parallel port (WPP). The WSP is comprised by the wrapper serial input (WSI), the wrapper serial output (WSO), and the wrapper serial control (WSC). The IEEE 1500 does not count with a finite-state machine, such as the IEEE 1149.1, so the control signals are

produced by a combination of the current instruction and the WSC signals. The WSC is composed by six mandatory signals, optional auxiliary clocks and an optional control signal, as seen in Figure 2-16. The wrapper instruction register (WIR), holds the instruction in a two stage process (in order to avoid a new instruction being shifted in from affecting the current instruction); while the wrapper bypass register (WBY) serves an equivalent role as its 1149.1 counterpart. The wrapper boundary register (WBR) also follows the 1149.1 scheme, and is composed by wrapper boundary cells (WBC). Each WBC has four data terminals: cell functional input (CFI), cell functional output (CFO), cell test input (CTI), and cell test output (CTO), also seen in Figure 2-16; which support five "events" (shift, capture, apply, transfer, update). Associated with such "events", the IEEE 1500 has a larger instruction set than the 1149.1, and many such instructions have additional parallel options.

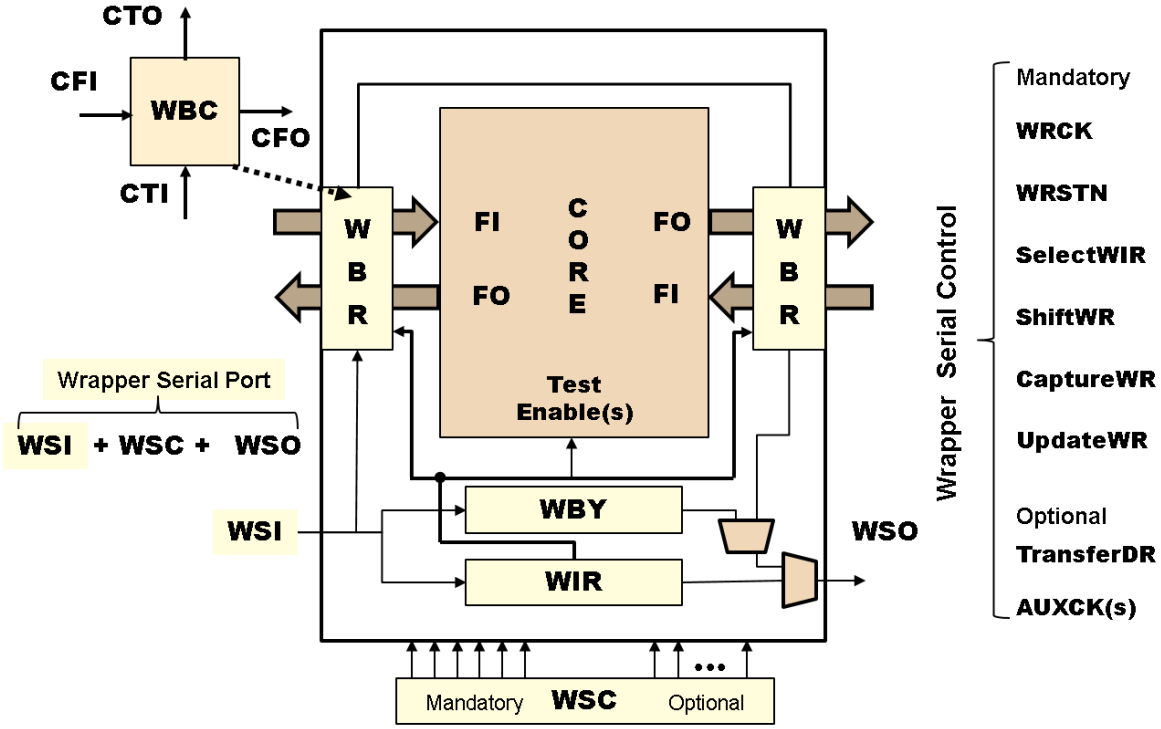


Figure 2-16 — IEEE 1500 wrapper structure overview (IEEE Std 1500-2005 IDAMS 3.5 test, 2012).

In order to alleviate the core-provider/core-user design level interaction, the core test language (CTL) was developed as to standardize the description design-specific data required for test purposes of the target core, interconnects and any user-defined logic surrounding the core. The CTL, also known as the IEEE P1450.6, is an extension to the standard test information language (STIL), the IEEE 1450; providing test protocol from test data in a modular manner and considering the core as a black-box. Although the IEEE 1500 was conceived as a digital focused methodology, it has been utilized for analogue testing as well (Braga, Da Silva, Alves, & Matos, 2004) (Xing & Fang, 2010).

IEEE Standard Proposal 1687

A hierarchical scan chain approach, eases chain-length (as opposed to the 1149.1), through modules referred to as segment insertion bit (SIB), composed by a multiplexer and a

single-bit controlling register that includes or excludes a segment of a scan chain in the active shift path. Such scheme allows for segments to be inserted or excluded, providing a homogenous access through wrapper-like test data registers which serve as adapters for observability/controllability to embedded instruments (Rearick, 2006), such as:

- Phase Locked Loop Circuits.
- Voltage/current sensors.
- Clock Control Blocks.
- Peak detectors.
- Memory/Logic BIST Controllers.
- Jitter detectors.
- Power sensors.
- Process Monitoring and Speed Binning circuits.
- I/O Bit Error Rate Counters.
- A/D and D/A converters.
- SERDES.

The IEEE STD. 1687 proposal (Posse, et al., 2006) (Ley A. , 2011) aims to facilitate the use and re-use of internal instrumentation by providing an architectural standard for embedded instruments access and a standard descriptive language for hardware and procedural description. Figure 2-17 illustrates the flexibility of the IEEE STD. 1687 approach where SIB modules are used to control the flow towards instrument gateways (referred to as test data registers or TDR), for the four instrument archetypes considered.

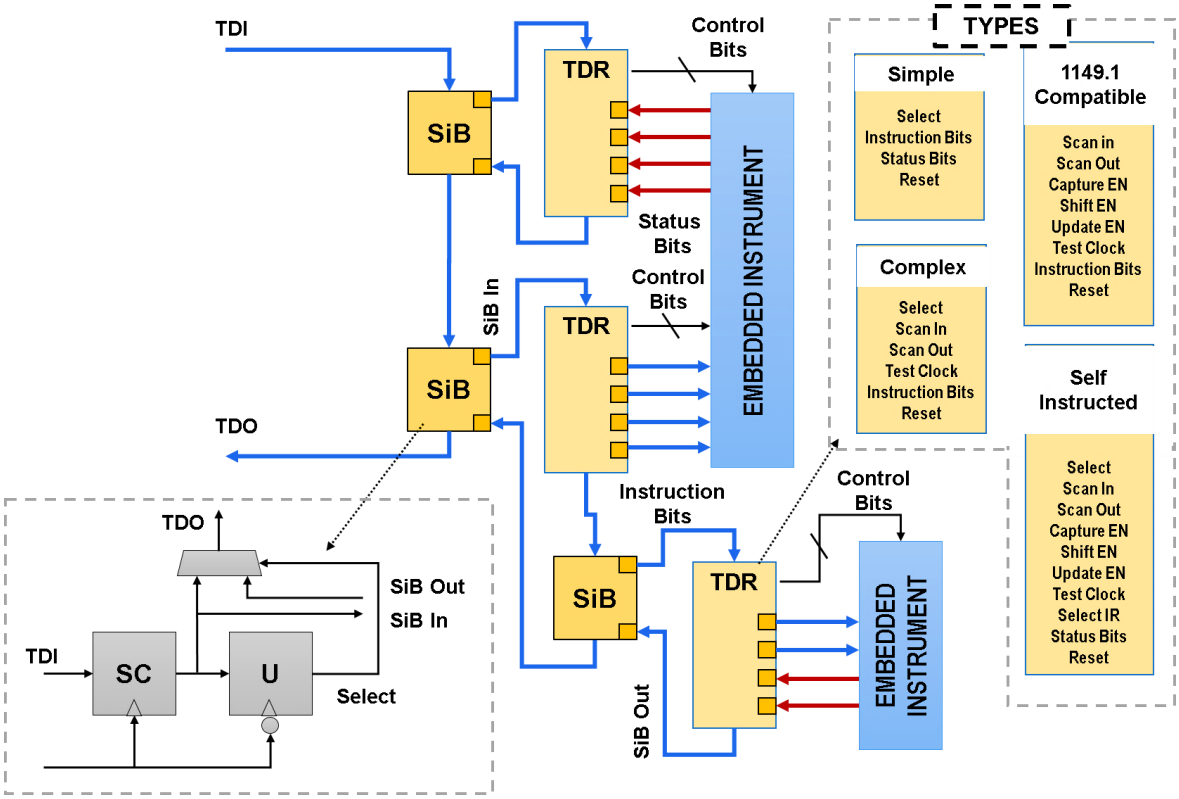


Figure 2-17 — IEEE standard 1687 architecture overview. Enhanced from (Crouch, 2011).

Usage Example – IEEE Std. 1149.4

For the sake of clarifying the objectives and improved understanding of the continuing chapters, an overview of the procedures involved for a test operation is presented for the case of the IEEE Std. 1149.4. Let us consider a two-wire impedance measurement scenario, where a target impedance is located within two IEEE Std. 1149.4 compliant cores, as seen in Figure 2-18. A number of elements come into play for the appropriate setup to be configured and the measurements performed.

In first place, the test controller needs a priori understanding of the elements involved, in this case IC1 and IC2, and their associated elements, such as the structural composition of the ABM and TBIC; i.e., the scenario formed by the ABM and TBIC composed by 4 analogue switches each. Moreover, within boundary-scan scenarios a complete understanding of all involved elements is necessary in order for the appropriate instruction and data sequence to be formulated by the test controller, including the elements not directly involved within a specific measurement. Thus, the initial step might require introducing the remaining cores and/or ABMs in a BYPASS state as to reduce the width of the instruction line feed serially to the chain or avoid inappropriate connections to the analogue bus, respectively. For the present example it will be assumed that the only elements involved are the two ABMs from IC1 and IC2 and their corresponding TBIC and associated control elements (TAP controller, TDO, TDI, TMS, TCK, registers, etc.).

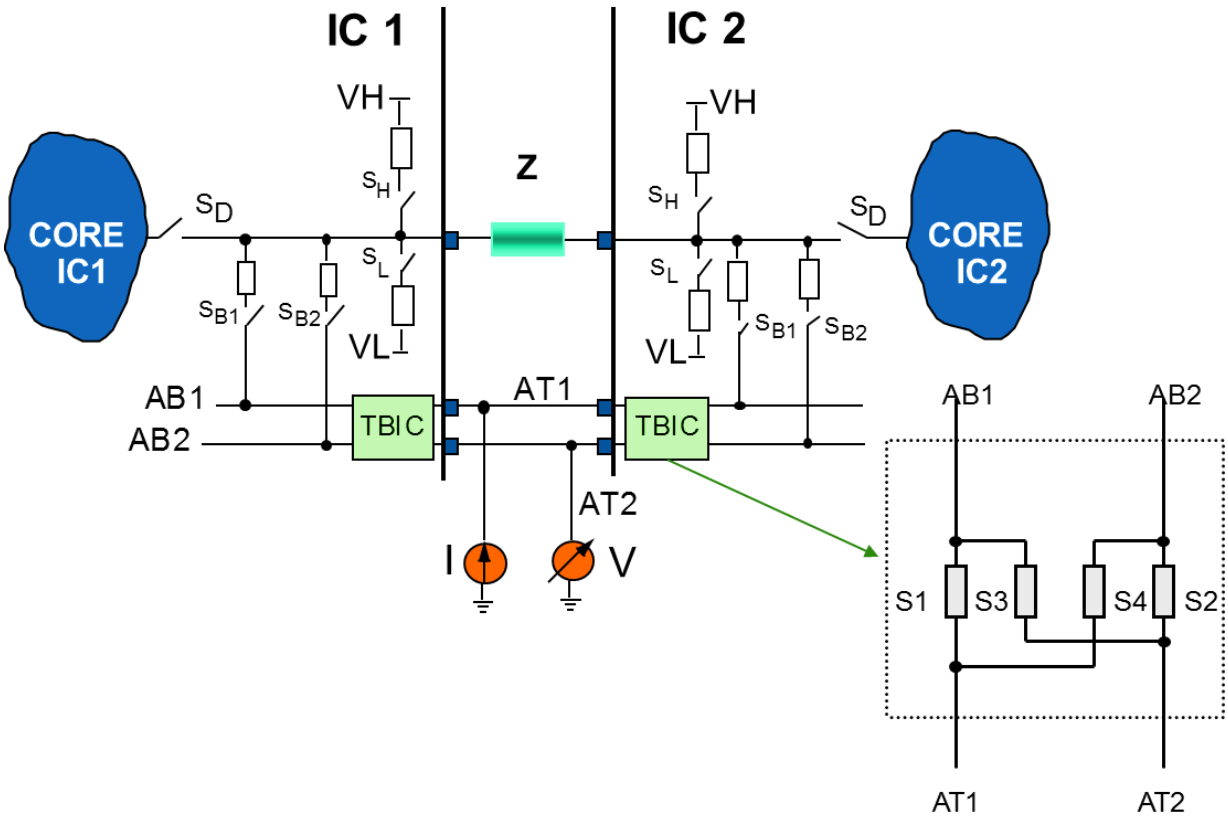


Figure 2-18 — Parametric testing scenario for IEEE std. 1149.4 compliant cores.

In order to enable the appropriate switches, one would follows:

1. Reset the TAP controller through the use of the$\overline{TRST}$, if available, or five continuous logic 1's in the TMS (on consecutive rising edges of the TCK).
2. Reach the Run-test/Idle state in the TAP controller by introducing an additional 0 through the TMS.
3. Introduce the EXTEST instruction by placing the TAP into the Shift-IR stage (1100 on the TMS), and shifting all 0's through the TDI (done with repeating 0's in the TMS at the rising edge of the TCK). Followed by 110 in the TMS as to reach the Run-test/Idle state once more.
4. Now we introduce through the TDI the sequence for enabling the switches (by reaching the Shift-DR stage in the TAP through a 100 in the TMS).

It should be noted that the before mentioned sequence has to occur simultaneously for both ICs, thus the sequence introduced by the TDI must account for both ICs. Now that the sequence of events for enabling the switches has been established, let's consider the steps for actual measurements.

In Figure 2-18, we observe an impedance Z, between the pins of two ICs. Assuming we had a current source, we could determine the value of Z by injecting a known current (I_s) and measuring the voltage differential across:

$$Z = (V_1 - V_2)/I_s \qquad \text{Equation 2-1}$$

In order to perform the measurement of the voltage differential we would require:

1. Connect the current source (I_s) to AT1 and voltage meter to AT2.
2. Enable a path from the current source, through the impedance Z to ground. Achieved by enabling S1 in the TBIC and SB_1 of IC1, while enabling S_L on IC2. The TBIC structure can be seen in Figure 2-13.
3. Enable a path from the voltage meter to the pin in IC1, by enabling S2 and SB_2 on IC1, as seen in Figure 2-19, and making the measurement of V1.
4. Enable a path from the voltage meter to the pin in IC2, by enabling S2 and SB_2 on IC2, as seen in Figure 2-20, and making the measurement of V2.

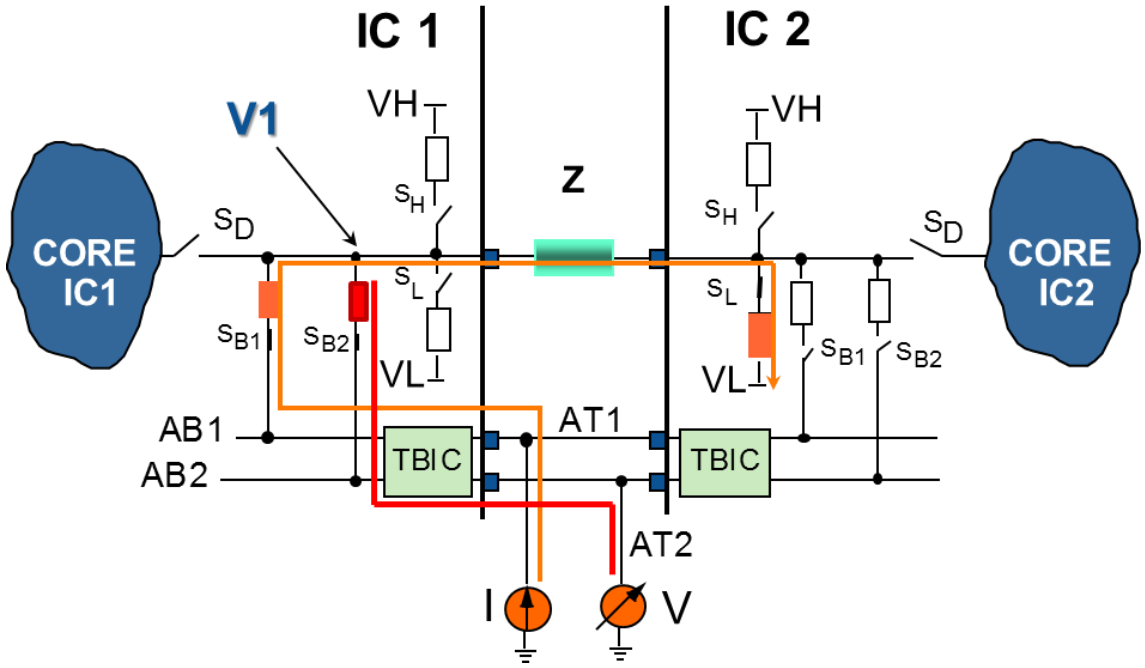


Figure 2-19 — IC1 side voltage measurement of Z impedance voltage differential.

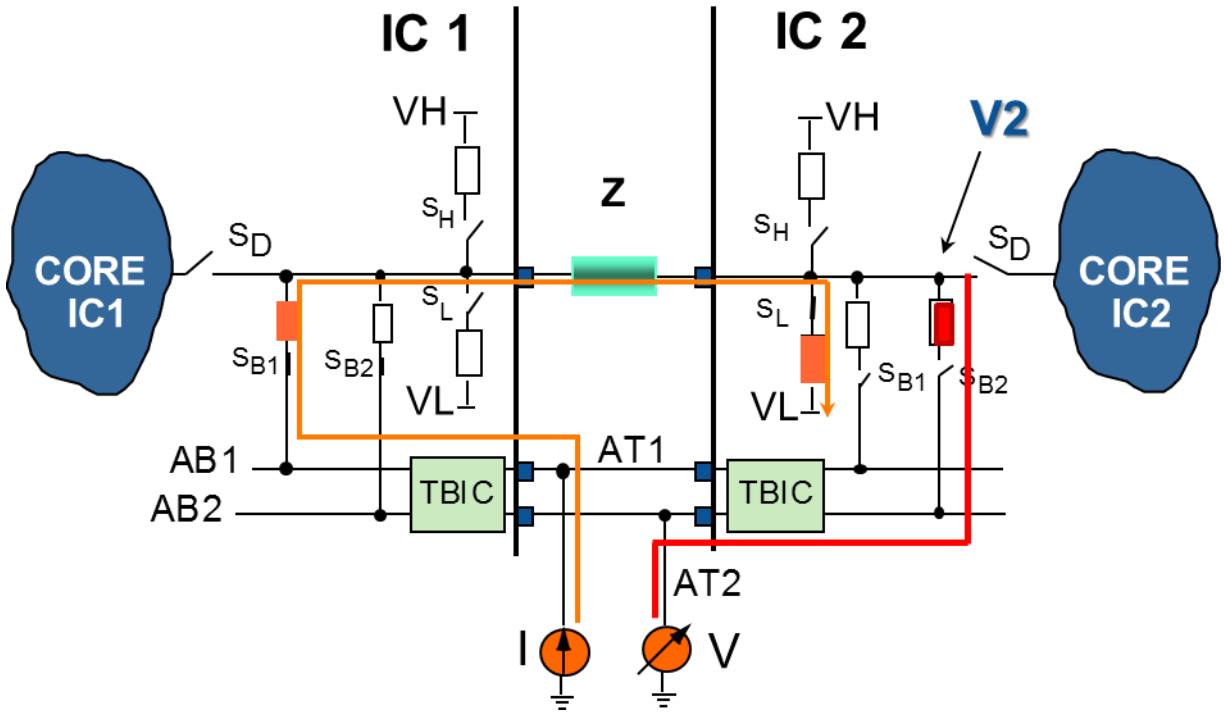


Figure 2-20 — IC2 side voltage measurement of Z impedance voltage differential.

Once, both measurement of V1 and V2 have been achieved on can calculate Z using Equation 2.1. It should be noted that additional approaches can be taken when performing the above measurement, such as only using one ATB wire. Also noteworthy is that the control of the current source and the voltage meter is not associated to the IEEE Std. 1149.4 and is generally assume to be part of an ATE.

2.3 Chapter Remarks

The summary presented within this section strived to encompass an overview of wearable monitoring technology and diverse strategies for mixed-signal, analogue and sensor testing; as to gain a sense of the variety of approaches to date. Wearable monitoring technology is a wide encompassing field that is quickly evolving thanks to advances in several areas and a demand for transition from qualitative to quantitative strategies in important areas such as medicine and rehabilitation. Although a general architecture was described, the variation in arrangements and upcoming technology insures malleability in design.

Clearly, testing methodologies have been moving towards the DUT and becoming ever more integrated within current electronic structures. Among the present strategies one stands out due to its time tested wide acceptability. The IEEE Std. 1149.1, although conceived as board-level interconnect testing mechanism for digital components, offers insight in the relevant aspects that permit an approach to surpass the test of time and acceptance. It has been argued that the most relevant benefits of the IEEE Std. 1149.1 (the basis for all the IEEE Std. 1149.X and IEEE STD. 1687) are register expandability and standardization of a test bus interface combined with a streamlined protocol (Wenzel & Ehrenberg, 2012). Notwithstanding, one would argue that an additional aspect of relevance is the IEEE Std. 1149.1 “moldability”, which has permitted its expandability (i.e., IEEE Std. 1149.4, 1149.6, 1687) and usage within a number of initially unforeseen scenarios (debugging, programming, etc.). However, the discussed approaches not necessarily present themselves transferable to a wearable monitoring scenario.

In spite of the progress within structured and non-structured approaches, most strategies are heavily dependent on external equipment, complex command syntax and centralized to a fixed test controller. In a production environment such characteristics are comprehensible due to the need for fast, in-depth coverage prior to release. Still, when considering the relocation of testing methodologies to operation time scenarios, certain aspects need to be redefined. Message syntax simplification becomes a key aspect as to permit local test controllers to manage the different resources; as a consequence, decentralization is possible taking the proper measures. Currently, most structured test controller approaches require an understanding of the modules and their structure; moreover, the transaction message composition is dependent on such understanding, introducing a communication overhead and a proportionally increased complexity. Thus, if the overall testing structure knowledge itself is decentralized towards the composing elements, the message complexity burden can be significantly lessen. The present work exploits the concept of group awareness to achieve such knowledge decentralization and providing communication syntax that no longer requires priori knowledge of the detailed specifications of the structure by the test controller; thus permitting it to be embedded, as well and non-static.

Chapter 3

The SCPS Framework

3.1 SCPS Foundation

Consensus exists on the need to invest on testing strategies, in particular for the case of analogue, sensor and mixed-signal scenarios, driven by the cost testing represents on product development and its influence in time to market.

As mentioned in the previous chapter, the past decade seemed to favour ESA solutions and, although a number of BIST, and DfT strategies can be extrapolated from traditional testing (functional and structural alike), especially those aimed for SoC and SiP, key aspects exist that require a different approach when considering heterogeneous systems such as sensor networks. Built-in self-testing/calibration (BISTC) strategies have traditionally focused on performing detection, diagnosis and repair actions for a specific module, section, component, or IP core; however, the rise in embedded instruments, modules and sensor numbers combined with the increase in functional monitoring periods presents complications such as hardware overhead, integration issues, energy consumption, reliability concerns, to mention a few.

Reliability issues due to component degradation, electromagnetic interference, environmental factors (humidity, temperature, etc.), physical stress (friction, pressure, bending, etc.) and general wear and tear, especially in the case of sensors, pose a major complication for high safety systems as well as WMT; moreover, such reliability issues are hard to detect and require continuous fault monitoring. Redundancy strategies serve to address such issues by using multiple hardware copies or multiple time measurements in order to establish a baseline to compare, but they are not always applicable and carry their own complications.

In Figure 3-1, one can observe a number of scenarios which complicate the sharing, simplification and synchronization among multiple instruments. For instance, Figure 3-1 (a) illustrates a scenario with diverging communication protocols and lines types (complicating synchronization and communication simplicity), while (b) and (c) present setups where common element repetition within heterogeneous instruments and possible sharable elements are repeated in multiple instances, due to redundant instrumentation, respectively. In particular, Figure 3-1 (d) illustrates overdesigned instruments which include elements that could otherwise be extracted and shared under the proper scenarios, or rendered unnecessary due to the presence of operation time testing instruments.

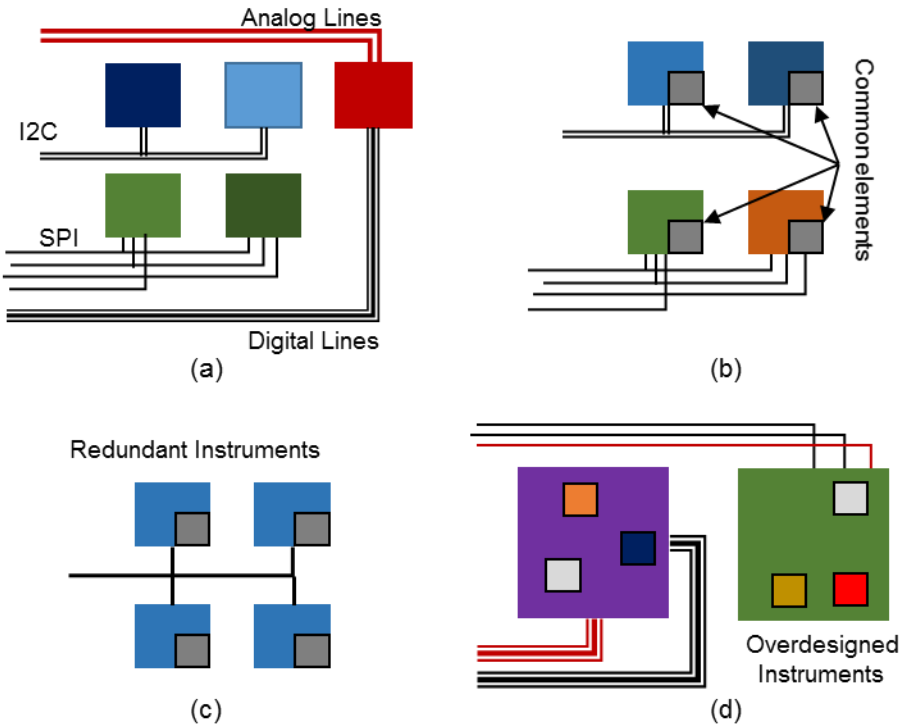


Figure 3-1 — (a) Heterogeneous communication lines. (b) Element repetition on heterogeneous instruments. (c) Redundant instruments with common elements. (d) Overdesigned instruments with common elements.

The hardware overhead can be contended through circuitry re-utilization by multiple instruments, e.g., sharing a stimuli generator. Additionally, test circuitry or elements within, could have an operation time usage, thus serving a dual role. A standardized interface to access and control test circuitry (or elements in general) contributes to solve integration issues, a major bottleneck of present non-digital BIST schemes. Additionally, in-situ operation-time test and calibration strategies can maintain data quality and improve reliability, while at times streamlining a circuit by avoiding the need for overdesign, as well as aiding to localize abnormal degeneration or fault prone sections of the overall system. Figure 3-2 illustrates an idealized scenario that presents standard analogue and digital interfaces while providing circuitry reutilization through shared elements.

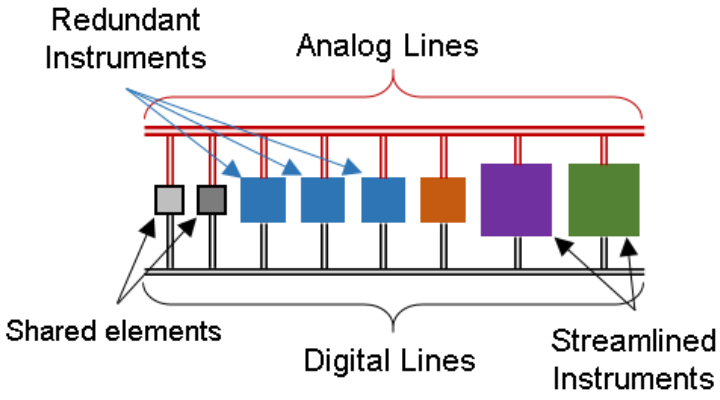


Figure 3-2 — Idealized multiple instrument setup through standardized access and shard elements.

In the case of WMT, such systems can seldom benefit from strategies that are either too centralized, external data/equipment dependent, or component focused. Such statement is based upon the utilization of strategies such as context awareness and multi-sensor data fusion, thus inter-relating the sensors and elements, including testing issues. Such approach, which considers distinct components as parts of a unifying element, can follow to testing and/or calibration strategies by treating components as part of a group. In such a way, one could seek to maintain data reliability through recognition of deviating patterns on sensors, not limited to redundancy comparison, which could provide insight into system problems due to improper sensor positioning, structural flaws and other factors that require the coverage provided by a group and/or multi-sensor approach.

Considering the before mentioned, a measurement/testing framework was proposed inspired on the 1149 standards methodologies, originally intended for passive sensors field testing synchronization, simplification and data sharing. Figure 3-3 illustrates the generalized concept of a multi-sensor scenario with commonly encountered sensor setups, such as: sensors with BIST, sensors with internal testing instruments, group of sensors with shared test instruments, a central processing module (CPM), and optional external test equipment.

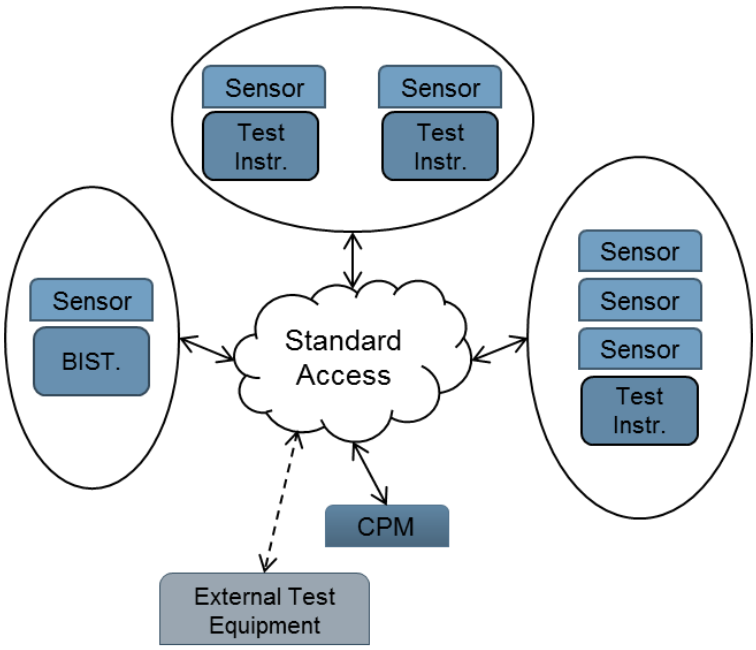


Figure 3-3 — Multi-sensor scenario with standard access generalized concept.

In order to establish a framework that addressed the issues of integration, overhead and reliability, the assumption is made that all digital and analogue tests can be summarized as a characterization or group of characterization processes. That is to say, that a “test” is equivalent to performing a measurement (or series thereof) of a feature from an electronic element. Furthermore, a measurement or set of measurement (and corresponding associated actions) occurs during a defined time to be referred to as event. In order words, an event is defined as start and ending of a specific set of measurements.

Let's consider the scenario of Figure 3-4, where a unifying stratagem is represent by the green wrapper layer surrounding the modules. In this scenario, elements of diverse types can be grouped and synchronized, regardless of their functional differences. In addition, commercial elements, such as an accelerometer, can be augmented through an extension to its normal functionality, accessed through the unifying layer. That is to say, an existing design needs not to be directly modified, the unifying stratagem can serve as an upgrade functional level. This permits the usage of commercial sensors and MEMS as an integral part of the measurement/test event, by providing added information (e.g., a temperature sensor can contribute to the determination of the proper transduction relation). A number of commercial sensors have I2C interfaces, which could benefit of extended functionality. The present approach provides an alternative to IP modifications, by allocating an alternate functional space within the measurement/test framework.

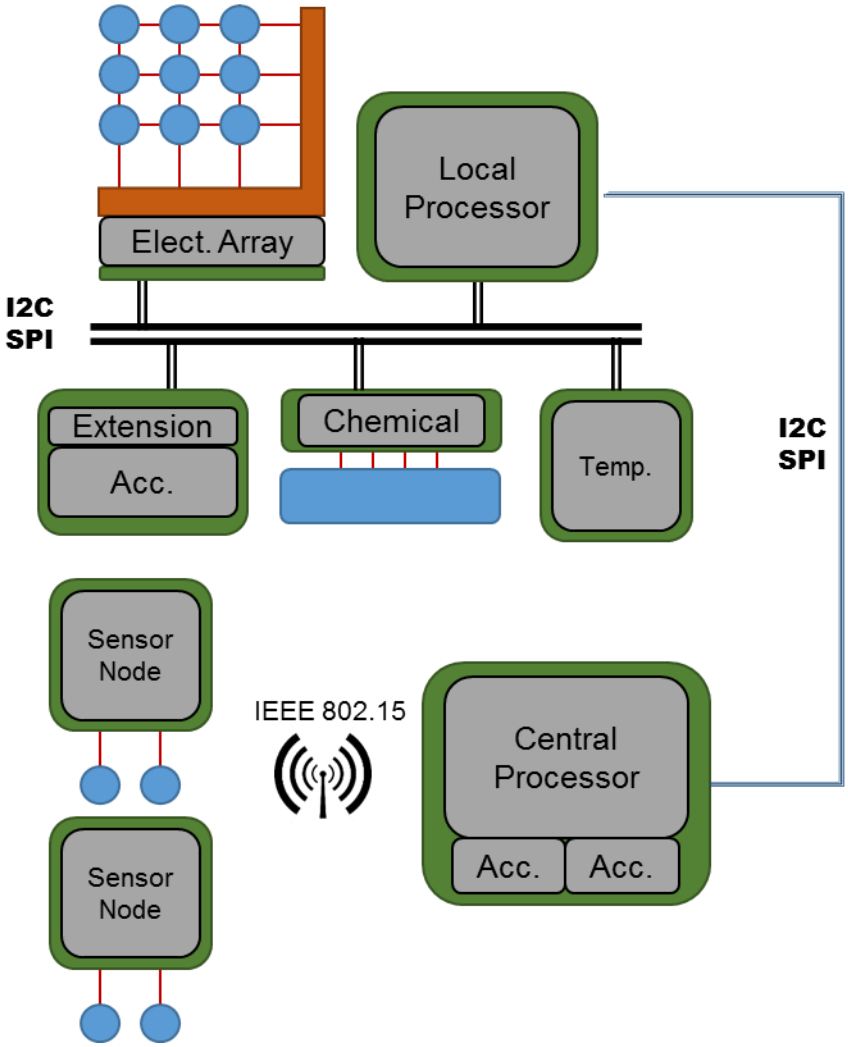


Figure 3-4 — Generic system overview with unifying stratagem.

If the characterization of an element is to be generalized, as to establish the basis of such model, one conceives that within a generic characterization one can cluster the involved elements in five groups, as seen in Figure 3-5. Such groups cover the different roles elements

might have during a characterization and are meant to serve as a guide to understand the inter-relations established, therefore providing insight into the foreseeable circuital associations. For simplicity purposes, an element is said to belong only to one group for any given test; although such statement is arguable given that the roles of some components are dependent on the point of view, e.g., a reference resistor could be considered as a sense element or a support element. However, the classification is meant for ease of circuital visualization and not as an axiomatic declaration. That said, elements are hereby divided in:

- ***Stimuli elements:*** all elements with fixed or programmable characteristics responsible for the generation of stimuli signals, be they, DC, AC, time domain, or otherwise stimulation of the element under test.
- ***Sense elements:*** all elements with fixed or programmable characteristics responsible for the capture of the response signals or features within.
- ***Support elements:*** all elements with fixed or programmable characteristics which bias, reference, conditions, or otherwise, the stimuli/response signals, contributing to the characterization process directly or indirectly while not directly responsible for the generation or capture of the stimuli or response signals.
- ***Target elements:*** all elements with fixed or programmable characteristics which are the target of the characterization.
- ***Routing elements*****:** all elements with fixed or programmable characteristics which serve for routing of the stimuli/response signals and do not directly affect the signals themselves, except for negligible effects, e.g., resistance of an analogue switch or parasitic effects.

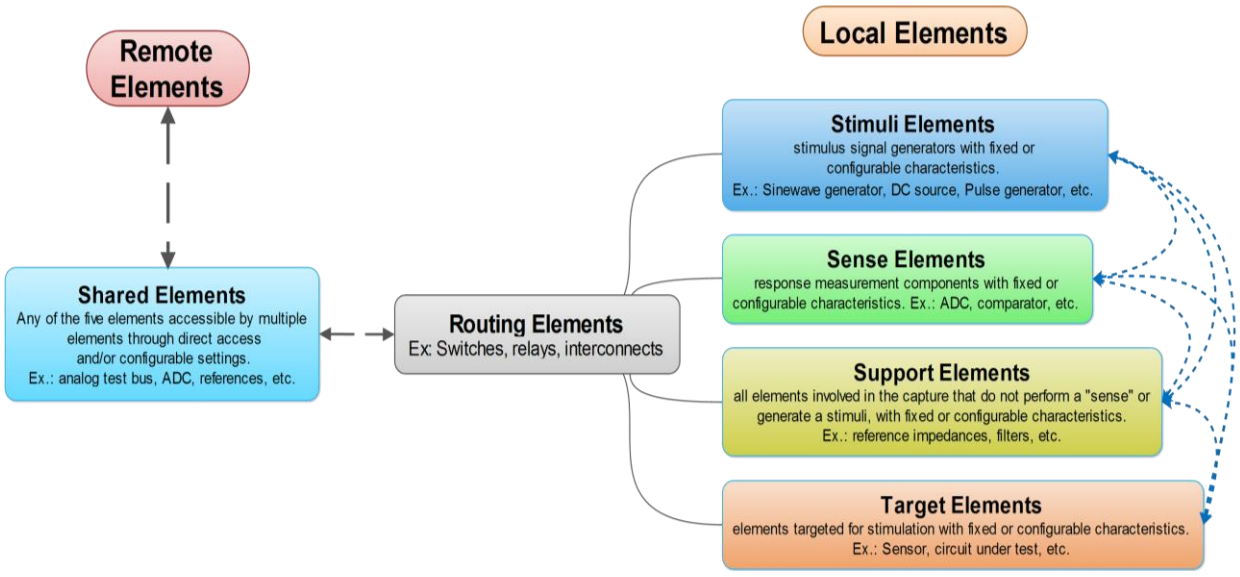


Figure 3-5 — Characterization elements inter-relation.

Additionally, the before-mentioned element classes can be further classified depending on their relative location with respect to the target, in: local and remote elements. Such reference denotes the relative proximity to the target element and the possible presence of routing elements between the target element and the referred element. Moreover, an

element that is communal to multiple characterization setups will be referred to as a shared element.

It should be mentioned that the initial focus was on passive sensors, defined as those that can be modelled as a combination of passive components, and consequently do not require an external source of energy in order to establish a predictable response based on an external stimulation. Accordingly, two types of element dependencies were considered for the purpose of the present research: independent elements and inter-dependent elements. The terminology of independent and inter-dependent refers to the inherent relationship between elements for considered characterization setups. From Figure 3-6 a) and b) one can observe that the dependency factor affects the strategy for characterization of the target element.

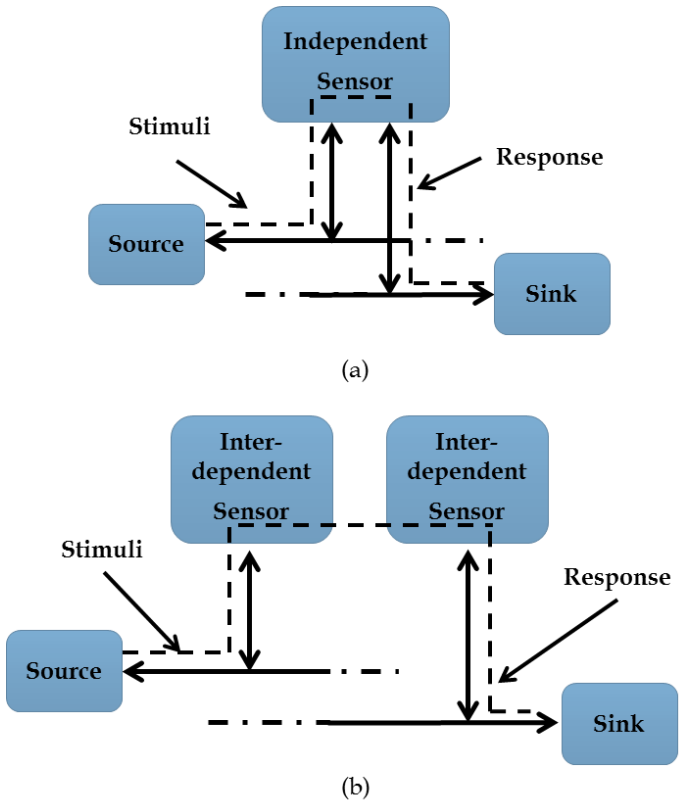


Figure 3-6 — a) Independent sensor stimuli/capture scenario. b) Inter-dependent sensor stimuli/capture scenario.

That is to say, that there exists or not a necessary dependency between elements in order to complete the stimulus/response signal transport. For the considered case studies, disposable surface electrodes and force sensing resistor (FSR), one can define them as inter-dependent sensors and independent sensors, respectively. That is so because electrodes conventionally require pairing, even if one is to consider the scenario of an isolated electrode, which then is paired to a reference ground electrode. The dependency classification serves the purpose of declaring possible relations between elements, in particular with those that can be "paired" (such as the case of electrodes) with multiple partners and thus would require a dynamic routing setup. In the case of an FSR no such

dependency exists since they can be measured independently from one another, although one could muster a scenario that would require the "pairing" of multiple elements in a specific characterization, such as the case of an initialization setting for chained sensor inspection.

A similar dependency relation also exists between elements involved in a characterization setup, since it is through their interconnections and functional features that the procedure can be achieved; thus, a group sense exists which can be exploited for operation simplification. That can be achieved by incorporating group-aware controllability and accessibility aspects that permit to simplify the setup/operation of the involved elements. Figure 3-7 illustrates a multiple element scenario, where Group 1 (consisting of module 1, 3 and 4) and Group 2 (consisting of module 1, 2, 3 and 5) represent elements associated by an operation that requires their participation as a group, as in the case of functional characterization. This group awareness permits to consider the treatment of multiple elements as a single entity, and if extended to addressability aspects, such approach can lower communication overhead through compression and/or fusion of control and data messages. Therefore, multiple levels of addressability such as broadcasting, multi-casting and unicasting, introduce an exploitable flexibility. For instance, when sharing analogue lines, as in the scenario in Figure 3-7, the ability of controlling the two groups through unified instructions would permit the usage coordination of the shared element (the analogue lines in this scenario) by setting one of the group in "standby" while the other performs a "characterization" operation; and if addressed as a group, the described operation would therefore be reduced to two operation instructions instead of a module specific instruction queue.

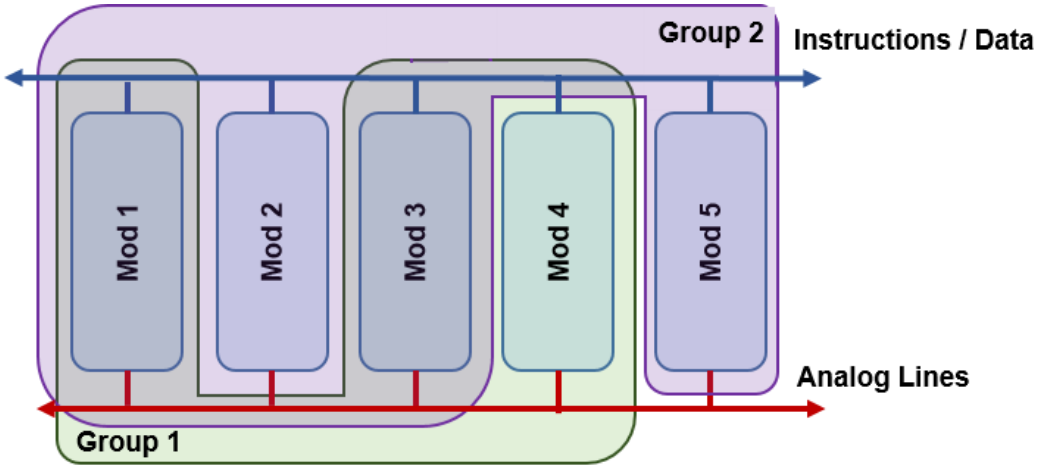


Figure 3-7 — A multiple element grouping scenario.

The classifications and properties described up to now permit a modular conceptualization of a system, where guiding aims can be summarized as: simplification, synchronization and sharing. Considering such goals, from a procedural point of view, the characterization process is to be considered divided in four stages, hereby referred to as: Setup, Capture, Process and Scan. This classification in procedural stages follows substantiation on 1149.1 methodologies,

which utilize mandatory instructions such as PRELOAD and EXTEST for test setup and capture. In order to gain understanding of the referred stages and overview follows:

- ***Setup:*** refers to actions intended for configuration of settings for all stages prior execution. This stage is reflective of the use of the boundary-scan chain and the PRELOAD instruction for preloading of the data into the boundary scan register prior an EXTEST instruction. Examples of possible actions include measurement parameter configuration, participating element selection, signal/pattern configuration, sampling settings, among others.
- ***Capture:*** reminiscent of the EXTEST instruction, this stage entails actions such as signal/pattern loading/generation, data collection and/or BIST activation.
- ***Process:*** intended for data processing and allocation on decision making registers. This stage seeks to manage the comparison of collected data through updates of registers that can be used to follow sensor history, global reference upkeep or specific reference comparison. Localized algorithm/heuristics such as least mean square strategies, Kalman filters, Markov's chains, etc., can be activated and processed at this stage.
- ***Scan:*** associated with data and instruction transport. The scan stage is perceptibly reflective of the boundary-scan usage as a data/instruction transport mechanism.

The *setup* and *scan* stages are utilitarian in a manner of speaking, since they perform what could be considered secondary roles, such as configuration and data transport, which depending on the specificities of the case at hand, might not be required. In contrast, the *capture* and *process* stages can be viewed as action focused, since they seek the production of a result in the form of a response measurement/comparison or path selection. That said, overlapping functionality can be present at times due to the inherit relation the process creates between the before mentioned stages.

3.2 SCPS Structure

The main objective of the SCPS framework is to provide a unifying methodology for managing and synchronizing testing scenarios, while considering a number of possible setups as presented in Figure 3-8. The initial vision of the SCPS structure, named after the initials of the four declared stages (Setup, Capture, Process and Scan), includes an analogue bus managed through digitally controlled interconnected modules, following approaches such as the IEEE 1149.4 standard. The structure should foremost provide implementation flexibility, while permitting compatibility with numerous commercial sensors through the use of a commonly used communication bus. Such approach permits the inclusion of commercially available components within the testing/calibration strategies by expanding their functionality; consequently offering, a mixed-signal test infrastructure.

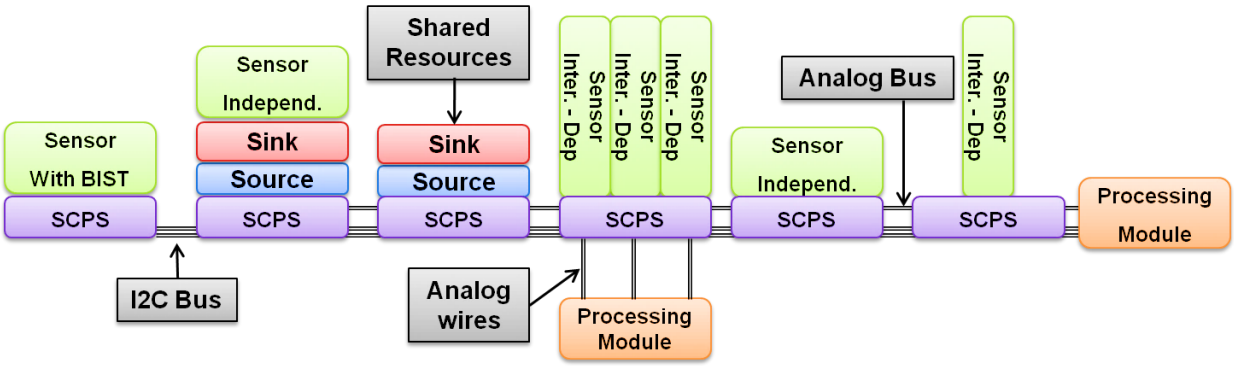


Figure 3-8 — Multiple sensor types scenario linked through SCPS modules.

Analogue busses are required, and their presence has been considered, for a number of analogue DfT scenarios (Milor L. , 1998) (Roberts, 1996) (Sunter & Roy, 2011) (Andlauer & Vu, 2002), therefore a number of methods have been proposed and are available for analogue test bus (ATB) implementation (IEEE 1149.4-1999, 2000) (da Silva, Costa, Behrens, Kickhofel, & Maltione, 2009) (Zivkovic, van der Heyden, Gronthoud, & de Jong, 2008), as well as ABIST strategies (Slamani, Kaminska, Courtois, & Lubaszewski, 1995) (Lubaszewski, Mir, & Pulz, 1997) (Kaminska & Arabi, 2003). However the particularities of analogue scenarios tend to reduce their wide applicability. Even after the introduction of the 1149.4 standard, there exists no wide spread approach for analogue testing, revealing the complexity of the issue. For WMT the issue does not simplify, although a number of critical restrictions inherent to small-die and IC structures can be loosen (noise introduction, cross-talk, area consumption, etc.) which provides opportunity for strategies traditionally not considered due performance hindrance; additionally, the nature of the applications can itself provide leeway regarding the precision and regularity of the testing methodology. Complicating the issue one counts the need to present a broadly applicable mechanism, flexible enough to accommodate a wide number of testing strategies and approaches, while external test equipment independent. By encompassing an analogue bus within a framework that considers group awareness, the aspiration was to simplify controllability by transferring the specificities related to routing and instruction response towards the instrument. Thus, the SCPS framework seeks to establish a standardized relation among compliant instruments and not the particular connectivity of an instrument with its surroundings. Figure 3-9 (a) illustrates a generalized structure of an SCPS compliant embedded instrument, while (b) presents a general layer view. The generalized structure includes a communication bus interpreter and associated registers, a SCPS interpreter and associated registers and control mechanisms, as well as instrument specific control logic and input/output channels. The vision is to permit collaborative integration with known standards such as IEEE 1500 and IEEE STD. 1687 by expanding upon their functionality with group awareness aspects; similar to controlling the 1500 wrapper using IEEE 1149.1 (Higgins, MacNamee, & Mullane, 2008).

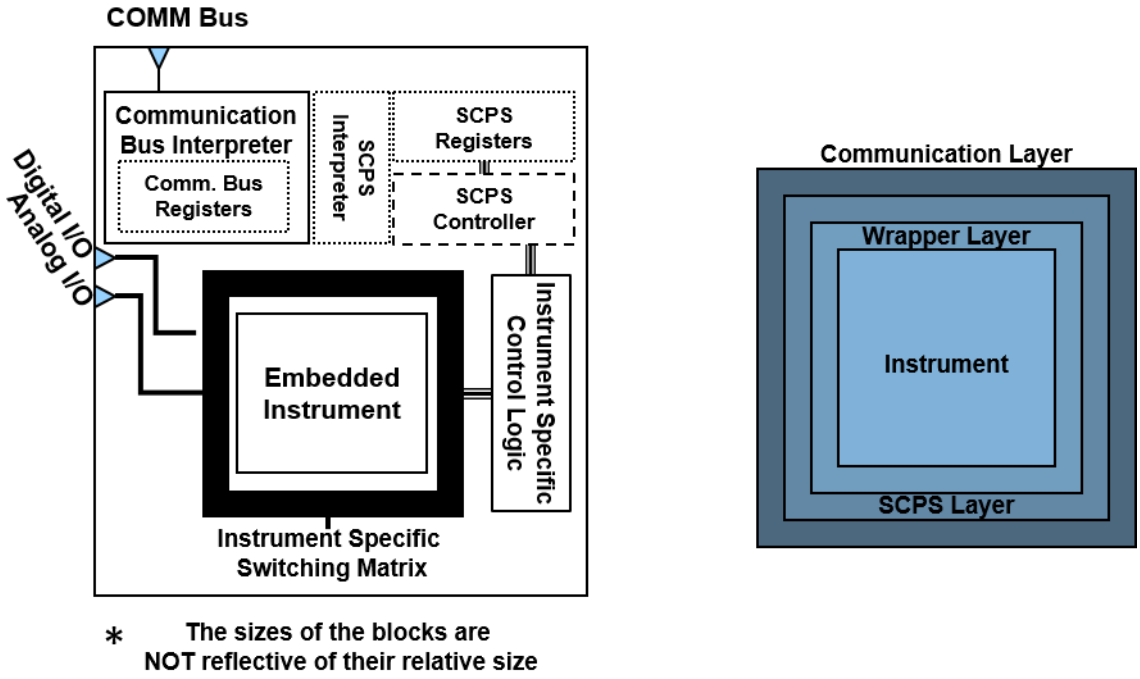


Figure 3-9 — (a) Generalized view of a SCPS compliant instrument. (b) Generalized layer view of a SCPS compliant instrument.

From a functional perspective, the SCPS framework is dependent on a *communication layer*, which provides the mechanism to reach the devices and/or instruments targeted. There exist currently in the market a number of digital communication buses compatible with multi-level addressing strategies, thus appropriate for integration within the SCPS framework. Some examples are the inter integrated circuit (I2C), controller area network (CAN), serial peripheral interface (SPI) and even the up and coming 1149.7 standard.

From a hardware perspective the SCPS framework layer essentials are considered divided in:

- ***Interpreter section*:** denoting the hardware aspects intended for SCPS message recognition and handling; relatable to the test access port (TAP) state machine and associated structure of IEEE 1149.1.
- ***Register set*:** all registers associated with the SCPS framework; a register strategy follows from standard digital control approaches, including the IEEE 1149.X standards, which utilizes registers for data/instruction transfer.
- ***Controller section*:** features associated to the control of instrument/device specific aspects. Originally considered as an adaptable structure such as the boundary scan cells of IEEE 1149.X standards. Instead, the specifications of a controller section are considered to be defined within an instrument specific control logic, limiting the SCPS control aspects to a minimal set of flags to act as an internal communication window between the SCPS hardware and the instrument itself; analogous to the test data registers (TDR) from IEEE STD. 1687, which serve as an instrument interface.

Additionally, a wrapper layer could exist, permitting compatibility with methodologies such as the presented by the IEEE 1500 or IEEE STD. 1687. The idea is to utilize the advantages provided by such approaches, such as standardization at the instrument/device interface level. Although conceptually considered, this layer interfacing will not be discussed within this document and left for future works in the subject.

3.2.1 *Embedded Instruments*

The concept of embedded instrumentation has gained newfound strength in recent years, as a method for addressing the present and evolving testing and measurement challenges of our day (Waller, 2010). Strategies such as BIST could be considered among the earliest embedded instrumentation instances, although it is until recently that standards such as 1149.7 and IEEE STD. 1687 have focused their attention to embedded instrumentation, postulating an open instrument interface and access mechanism. The before-mentioned protocols built upon time test standards such as 1149.1 and 1500, evidenced the rooted presence of embedded instruments within testing and measurement strategies, although seldom fully utilized.

In general, embedded instrumentation seeks to expand and/or replace traditional testing/measurement equipment functionality. For example, let's consider a generic source and sink scenario; traditionally, the stimulus generation and acquisition aspects of a testing measurement are produced by automatic testing equipment (ATE) external to the device in question. A number of possible source and sink configurations can be thought for analogue bus scenarios, not to mention the combination of both source and sink into one module for ease of accessibility and synchronization (e.g., permitting measurement of phase, to be performed with reduced complexity). Figure 3-10, presents a general concept of a source/sink module or instrument, where a number of stimuli generation mechanisms are present and selectable, while a clock synchronized dual ADC setup permits for measurements directly from a voltage/current controlled source (requiring an one wire analogue bus) or a two analogue bus wire approach with separate lines for source and sink. Combined source/sink scenarios could prove useful when considering local shared resources for characterization, which are not readily accessible due to routing issues or due to performance issues. A wide number of stimuli generation strategies, both digital (Salazar, et al., 2011) (Lampasi, Moschitta, & Carbone, 2008) (Koukourlis & Voulgaris, 1989) and analogue (Barragán, Vásquez, Rueda, & Huertas, 2010) (Mancini; 2000) (Mancini & Palmer, 2001), have been proposed in the literature.

In the WMT context a more pressing issue are the possible effects of such stimuli to the user, in particular when considering characterization strategies that involve current injection or similar. The characterization of an unknown impedance is by all means not a necessarily simple task and a wide number of approaches exist (Agilent Technologies, 2009) (Tisdale, 1999) (Keithly Instruments Incorporated, 2011) each with their own pros and cons. When

considering a varying scenario such as the case of WMT, some strategies may not be applicable, especially if the safety of the user is to be guaranteed.

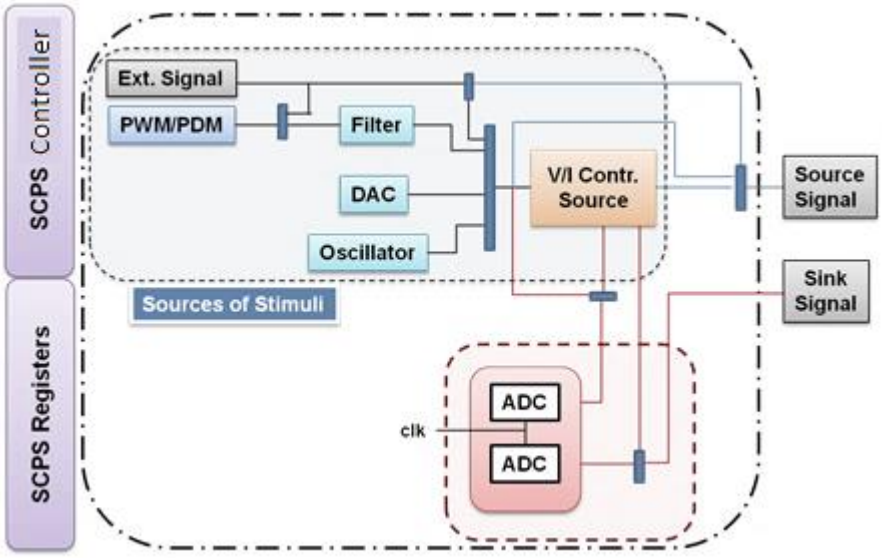


Figure 3-10 — SCPS source/sink module general overview.

Not all devices require the availability of an analogue bus for testing or data capture, but they might benefit of the SCPS features for augmenting self-testing functions or adding a self-test option where none exists, as in the case of commercially available sensors. As seen in Figure 3-11 (a), the device can remain independent from the analogue bus while being part of the communication bus through a SCPS module. Figure 3-11 (b) presents a scenario where the device is accessed directly, bypassing the SCPS module; while Figure 3-11 (c) presents the scenario where the communication is interpreted by the SCPS module which negotiates with the device for the established event.

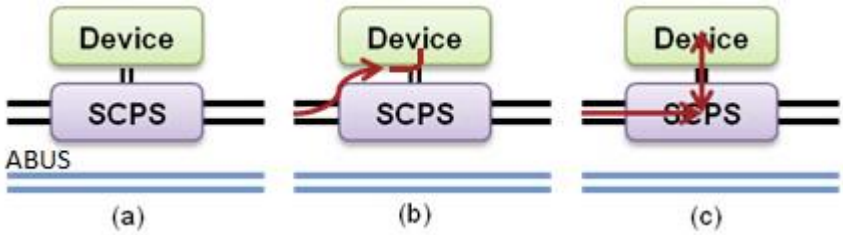


Figure 3-11 — SCPS modules configurations for analogue bus independent device. (a) General view. (b) Bypass configuration. (c) SCPS related configuration.

3.2.2 *Communication Bus*

The Inter-IC bus, commonly known as I2C (NXP, 2014), is widely used on current commercially available sensors and has become a standard half-duplex two wire communication venue for most microcontrollers and adaptable for FPGA usage (Fatang & Linyu, 2011) and not a stranger to wearable setups (Righetti & Thalmann, 2010). It is then an adequate communication bus for the proposed methodology. Moreover, the idea of using the

I2C in testing/measurement scenarios is not recent. Phillips S.A. had considered the idea of associating the IEEE 1149.1 and the I2C bus, in order to reduce the pin overhead (Baker, Richardson, & Dorey, 2002). However, boundary scan approaches reliance on static measurement schemes and system level control requirements (functional activity suspension) prove an unsuitable complement under the considerations of the moment. In addition Nai-Chi Lee from Phillips Electron had to say:

> *"Notice, however, that the digital control lines in all proposed analogue test bus schemes are used only to setup the status of analogue switches before the actual test. For those mixed-signal chips that already have a digital control bus such as the I2C, the existing bus can easily be used to control the status of analogue switches … The requirement for adding four digital pins just to maintain compatibility with IEEE 1149.1 becomes unnecessary overhead. The irony of our present situation is: although the proposed test bus standard (referring to IEEE 1149.4) represents a great effort towards structured testing methodology, applying it to any circuit requires detailed design analysis and even modification on a case-by-case basis. In this sense, it is still ad-hoc." (Lee N. C., 1993)*

Alternatives such as the 1149.1, or even the 1149.7, offered a number of advantages, especially considering formal address-less communication; however, the same could not be said for true closed loop scenarios (no external handling of the TAP), not to mention the need for adapters for communicating with commercially available sensors which seldom handle 1149 protocols. Other strategies considered were CAN (controller area network), SMBUS (system management bus), and Access.BUS, and while they offer addressing and exception handling strategies, they were not chosen mainly due to the sensor market drive. In addition, I2C offers an un-tapped potential by permitting multi-cast synchronization of elements that can be treated and accessed as a group structure; although the I2C bus was not conceived with such communication strategy in mind. In fact, a number of addresses have been reserved on the I2C address map for future enhancements, such as the ones being proposed, as well as 10-bit addressing and general calls; providing a pre-established opportunity for extending its functionality.

Since no limitation exists on the acknowledgment response of a target address (regarding source) or any restriction regarding which slave components respond to a command, the possibility for cluster or group commands remains open. Concerns regarding addresses (commercially available components generally come with limited pre-established address for I2C communication), bus length limitations, hot swapping, can be solved through the introduction of I2C bus extenders such as the P82B715 from Texas Instrument (Texas Instrument, 2007 Rev. 2008), which allows to circumvent the 400 pF bus capacitance limit (allowing for low cost wiring or possibly textile wire), or I2C multiplexers such as the PCA9544AA of the same company (Texas Instrument Inc., 2005 Rev. 2008); however these

issues are outside of the scope of this research. The following sub-section presents a number of features of the I2C bus, in order to gain perspective.

3.2.3 *Inter-Integrated Circuit Implementation*

As stated by the NXP's UM10204 version 5, "I2C-bus specification and user manual" (NXP, 2014):

> *"The I2C-bus is a de facto world standard that is now implemented in over 1000 different ICs manufactured by more than 50 companies. Additionally, the versatile I2C-bus is used in various control architectures such as System Management Bus (SMBus), Power Management Bus (PMBus), Intelligent Platform Management Interface (IPMI), Display Data Channel (DDC) and Advanced Telecom Computing Architecture (ATCA)."*

The inter-integrated circuit bus, also referred to as IIC, I^2C, or I2C (the later will be utilized in this document), was originally developed by Phillips for communication between integrated circuits present in the same board. Features such as master generated bus clock (with no strict baud rate), true multi-master (with arbitration and collision detection), requiring only two lines, and, in general, its simplicity and flexibility, permitted the I2C bus to gain popularity and to be also utilized in cable communications.

Originally the I2C bus was limited to a 100 Kbit per second, speed that is still sufficient for a wide number of devices, and is referred to as the *Standard-mode*; the work hereby presented was based on a *Standard-mode* configuration. However, a number of alternative modes have been defined that permit an increased speed, such as:

- **Fast-mode:** up to 400 Kbit/s, remaining downward compatible to the standard-mode, with the same format, logic levels, maximum capacitive load and protocol.
- **Fast-mode Plus (Fm+):** up to 1 Mbit/s and increase in total bus capacitance. Remains fully downward compatible with Fast- and Standard-mode. The main hardware variation is the drivers' strength to satisfy the timing specifications within a 400 pF bus.
- **High-speed mode (Hs-mode):** up to 3.4 Mbit/s remaining fully downward compatible with the previous modes, preserving the protocol and data format. However, a number of hardware level and protocol exceptions are present in order to achieve the before mentioned speed (e.g., arbitration and clock synchronization are excluded during Hs-mode transfer and combination pull-down pull-up hardware is for shortening the clock line rise time).
- **Ultra Fast-mode (UFm):** up to 5 Mbit/s, by eliminating the pull-up resistor through the use of push-pull drivers. The same protocol and data format is preserved.

One of the most attractive features of the I2C is the requirement of only two lines, referred to as the serial data (SDA) line and the serial clock (SCL) line. As their names imply, the SDA is utilized for transfer of data and the SCL is utilized for clocking purposes. Both lines

are bidirectional and meant to be connected to positive supply voltage through pull-up resistors or current-sources. The default state of the lines is HIGH, and a wired-AND compatibility is expected by the devices connected to the bus, with input reference levels of 30% and 70% of V_{DD}. A generalized view of the SDA/SCL line setup between two devices can be observed in Figure 3-12, where Rp, Rs, Cp, Cc, stand for pull-up resistance, serial resistance, wire capacitance, cross channel capacitance, respectively.

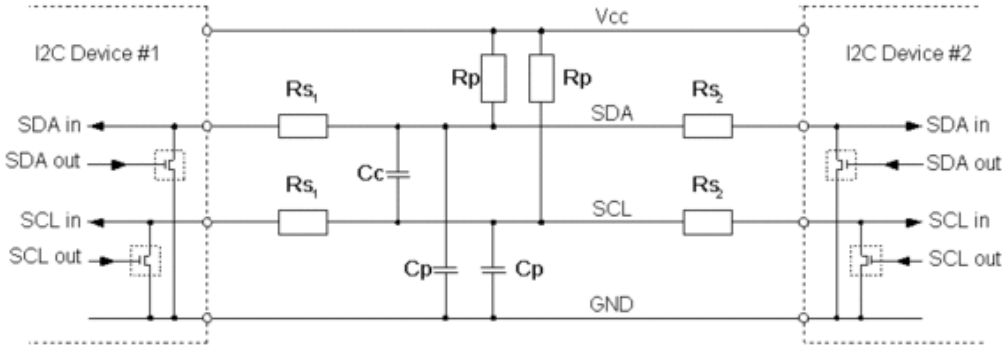
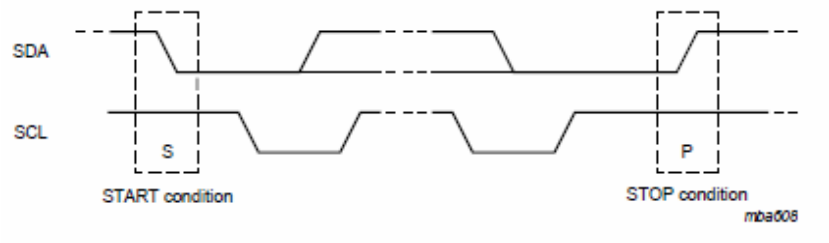
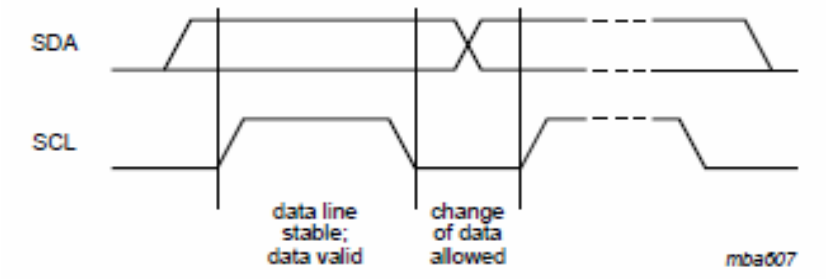


Figure 3-12 — I2C generalized line setup. Extracted from (I2C-bus.org).

The I2C bus protocol is based on two types of transactions, READ (R) and WRITE (W), initiated and terminated by START (S) and STOP (P) conditions produced by a change in the SDA line during the HIGH period of the SCL line. A HIGH to LOW transition on the SDA line produces a START or Re-START (Sr) condition, indicating the beginning of a new transaction (the Sr condition occurs when the master initiates a transaction prior to a P condition), and a LOW to HIGH transition produces a STOP condition. Otherwise, the SDA line must be maintained stable during the HIGH period of the SCL line, as to insure data validity, as seen in Figure 3-13 (b).



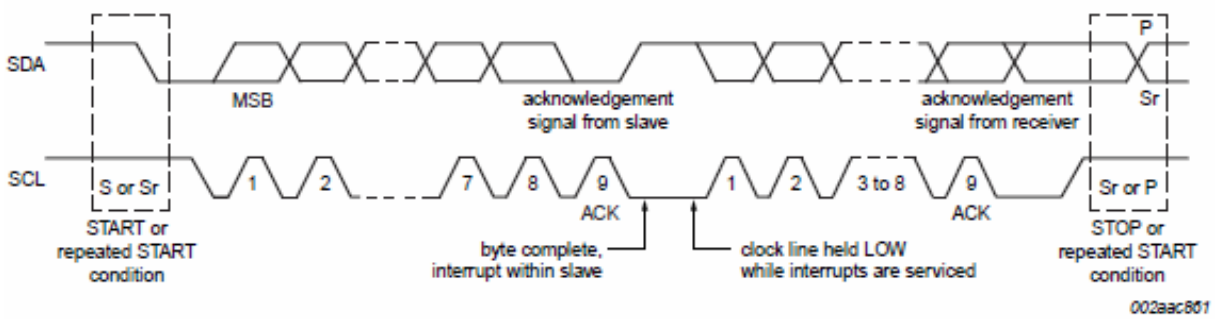
(a)



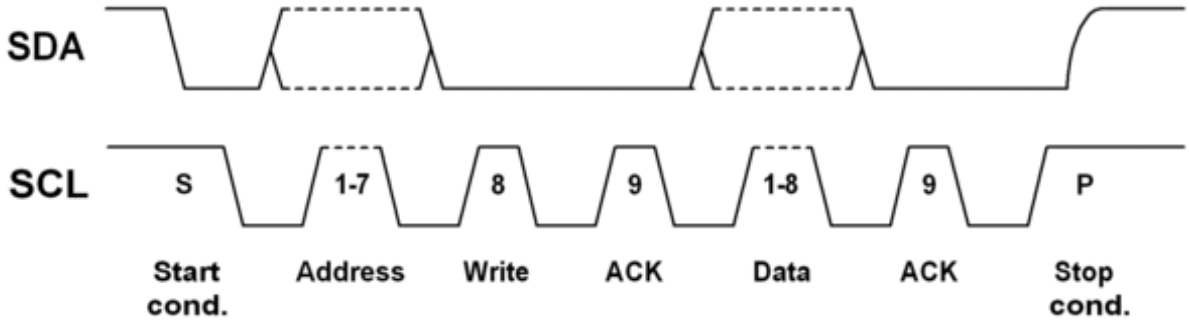
(b)

Figure 3-13 — (a) START/STOP conditions (b) Data validity. Extracted from (NXP, 2014).

Transactions are initiated by a S or Sr condition (as previously indicated), and are composed of nine (9) bit segments, eight (8) of which are intended for data and a ninth (9^{th}) for acknowledgement purposes, as seen in Figure 3-14. The first data byte of a transaction contains addressing information, which can be either a seven (7) bit address followed by a R/W bit, or a reserved address (such as a general call, START byte, CBUS address, different bus format, Hs-mode code, device ID or 10-bit slave addressing). Additional bytes are used for the exchange of data, depending on the type of transaction, i.e., a WRITE transaction sends additional information for writing to a register of the target module and a READ transaction permits the target module to send the requested data to the master. The ACK bit allows the target module to acknowledge the message (with an LOW) and serves as a way of confirming proper message reception. During a READ transaction the master module ACKs the additional bytes, while a NACK (not acknowledgement) indicates to the slave that no additional data is required.



(a)



(b)

Figure 3-14 — (a) I2C general transaction, extracted from (NXP, 2014).
(b) I2C write general transaction, extracted from (I2C-bus.org).

In the present work, the 10-bit addressing capability was utilized for SCPS related transactions, and the general format for the WRITE and READ transactions are illustrated in Figure 3-15 and Figure 3-16, respectively.

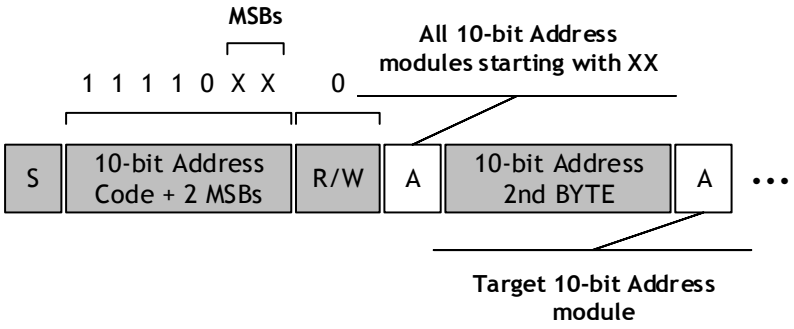


Figure 3-15 — 10-bit Address WRITE transaction.

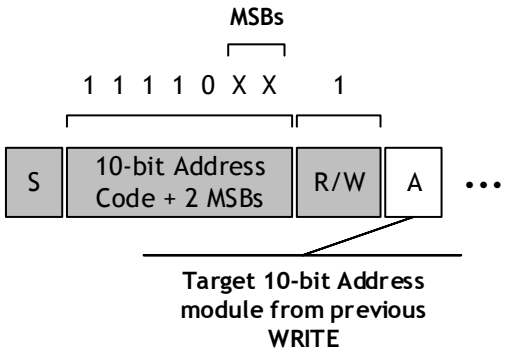


Figure 3-16 — 10-bit Address READ transaction.

The assignment of addresses is seen by some as a limitation, in particular 7-bit address formats. That is due to the limited number of available addresses, introducing the problem of address collision for components of different vendors. Dynamic solutions, such as that provided by the SMBus have not been widely supported and 10-bit address formats are also limitedly utilized (thus the latter's attractiveness for this project).

A Verilog I2C interpreter was implemented based on a Steve Fielding's Opencore.org project[1]. The referred project provided a stable standalone minimalist I2C slave IP core, fully simulated and FPGA tested; its state machine can be seen in Figure 3-17, Figure 3-18, and Figure 3-19.

[1] named I2Cslave, created on Nov. 7th, 2008 and last updated on Dec. 18th, 2013

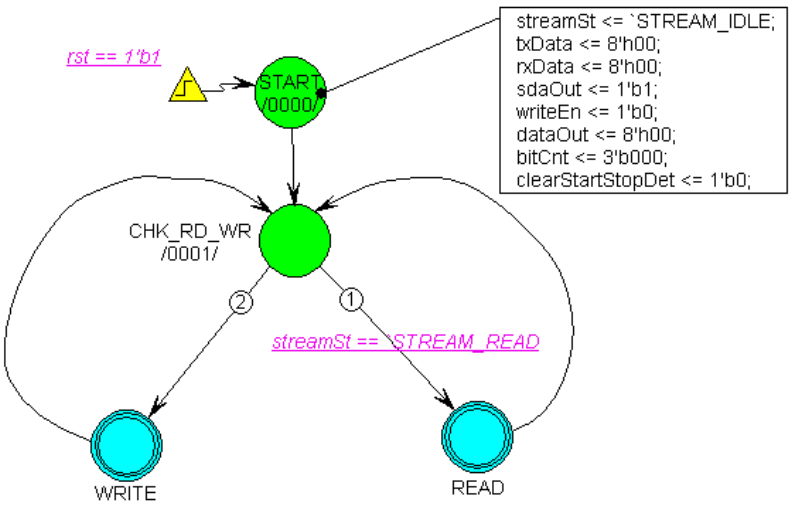


Figure 3-17 — Top level view of I2C state machine

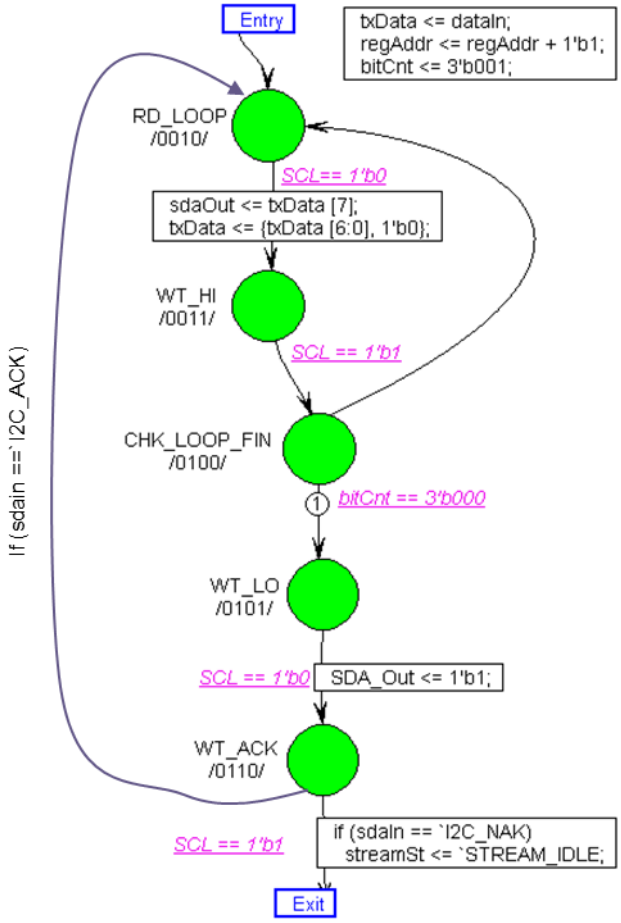


Figure 3-18 — I2C READ transaction state machine.

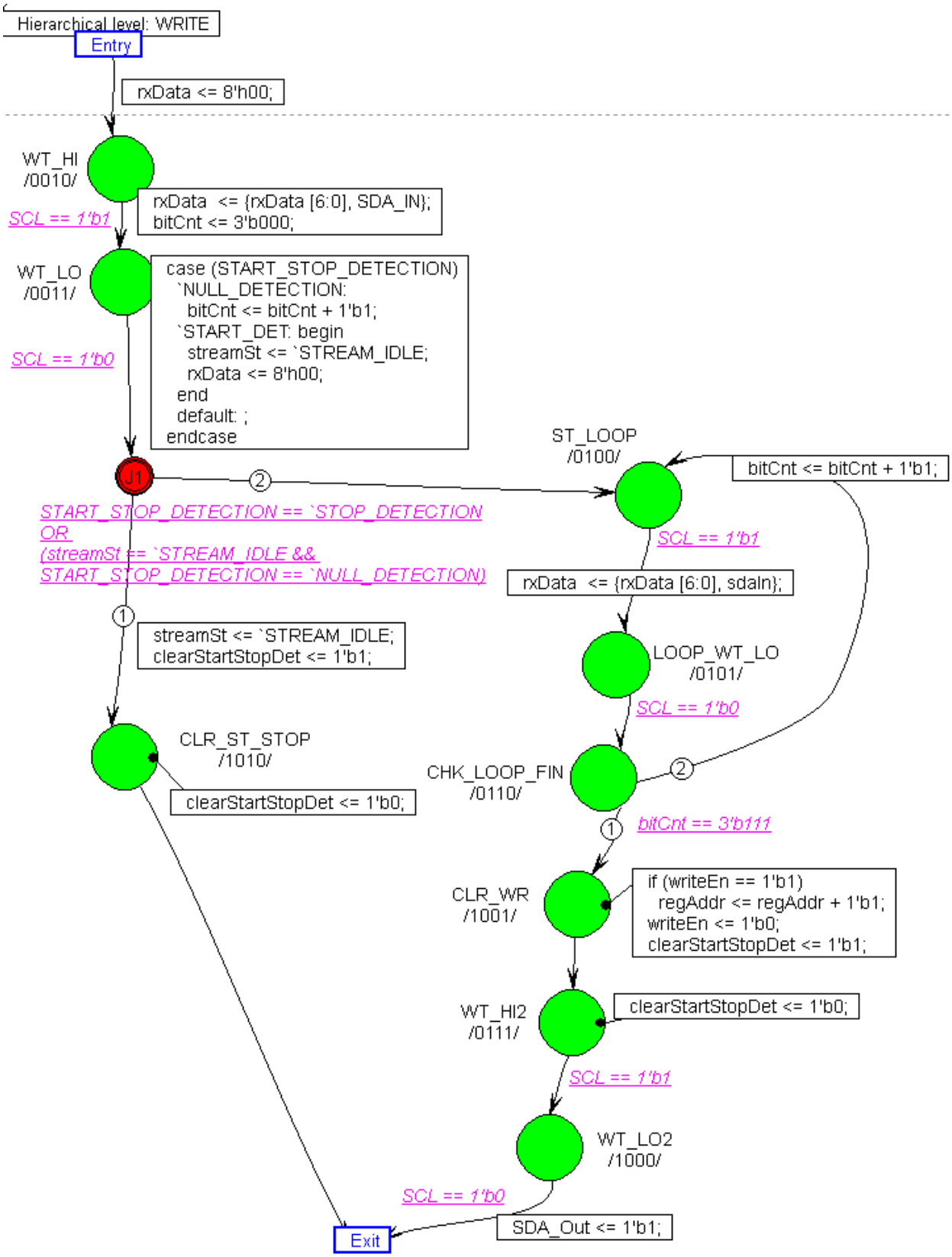


Figure 3-19 — I2C WRITE transaction state machine.

3.2.4 *SCPS Generalized Structure*

Following the considerations declared within this section, Figure 3-20 presents a generalized view of the before declared elements interacting within a SCPS framework scenario. The instrument/device illustrated on the upper section of the figure coordinates actions through the communication protocol, while the SCPS module interprets the message and offers the instrument specific registers and flags that can be utilized for control and functionality management.

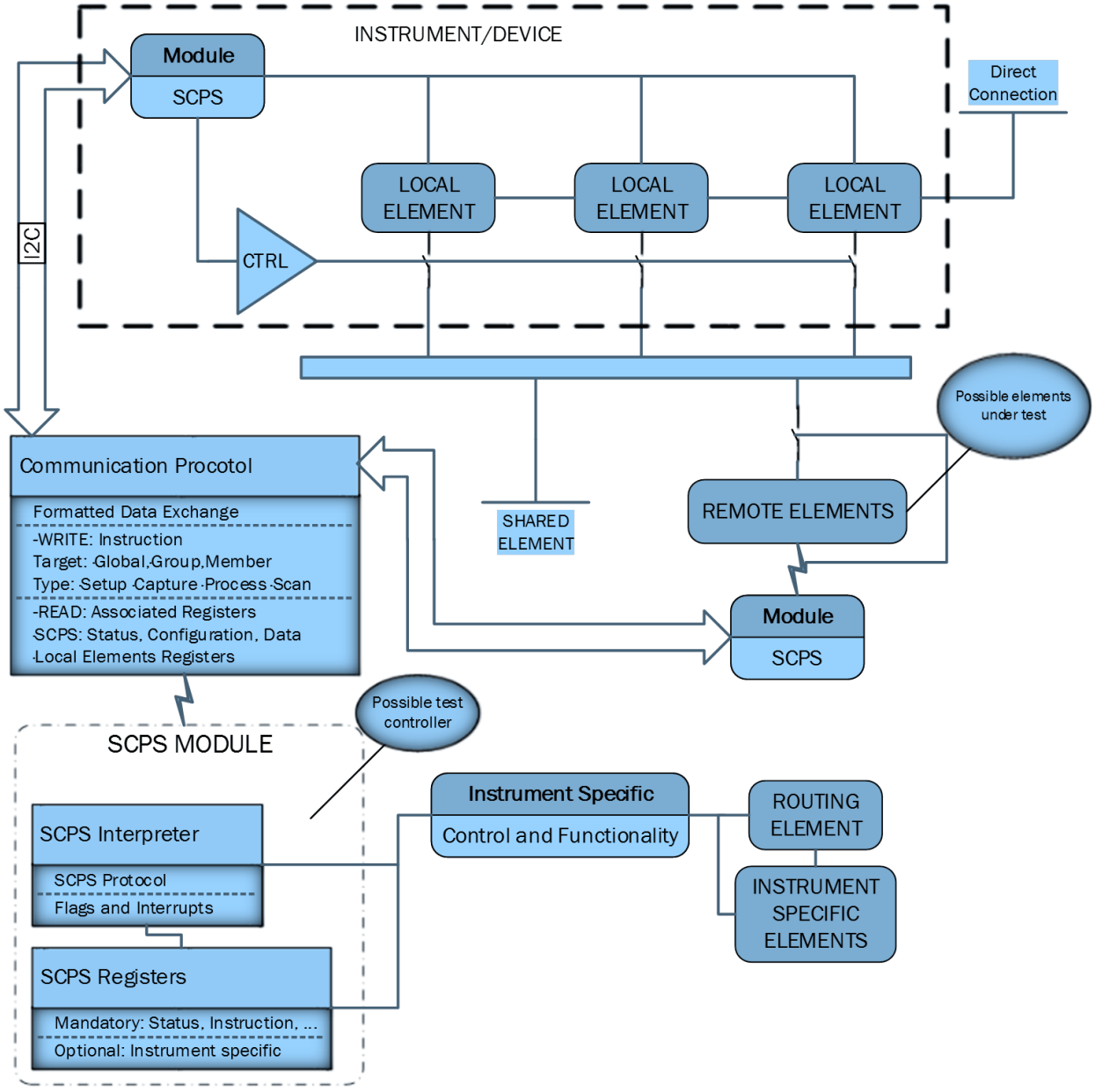


Figure 3-20 — General view of a SCPS framework scenario.

3.2.5 *SCPS Command Structure*

A command structure composed by mandatory and optional instructions serves to manage the register, flags and other aspects of the SCPS module. The instructions are considered

divided into four sub-groups, relating to the previously defined procedural stages (Setup, Capture, Process and Scan); in order to attend the requirements of each of the stages of the event progression. The SCPS command division follows the inherent separability of inter/intra modular strategies; from a functional perspective, the commands and their associated functional region can be separated as observed in Figure 3-21.

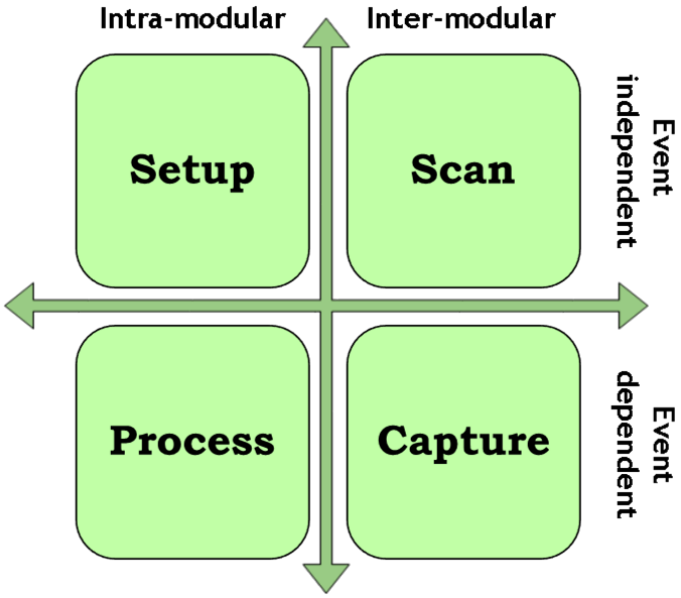


Figure 3-21 — Command functional separation overview.

A driving concept is that a preliminary setup stage (related to an initialization or similar phase) is advantageous, focused on the configuration and loading of settings, so that capture related instructions can proceed with minimal procedural delays as to permit a continuous process of acquisition for both monitoring and testing data. The process instructions are thus intended for decision making strategies at the SCPS module level, such as bypassing a specific node due to unacceptable results or setting appropriate flags for status communication. An overlap of stage functionality is considered at the instruction level, through the consideration of "on-the-fly" instruction specifier configuration, as to permit multi-stage procedures. On-the-fly refers to the alternative provided by some instructions to consider specifiers with the instruction, as to perform a procedure without the need of previously established parameters, e.g., as to setup a new reference within a specific module for a non-repetitive event or selecting the target members of an operation. Lastly, the scan instructions, as their stage name implies, are related to the communication and data exchange.

An additional concept introduced within the framework is the consideration of known *states* or pre-establish/configure settings. By states one refers to a known configuration of the SCPS module from a control perspective, i.e., associated local elements and functional aspects are setup in a known manner; this is of particular importance when considering routing elements configuration. Such follows from the assumption that for certain scenarios a repetitive procedure will be mostly utilized from monitoring the state of the system's

elements; from which follows that some actions will seldom require to conform to a wide array of configurations. For example, in the case of a sensor array connectivity check, the procedure would continuously cycle among the targeted sensors while the setup remains mostly the same. So in this manner the specificities of local controllability and observability can be moved to the instruments themselves, while utilizing the framework for communication synchronization, simplification and shared resource management; as opposed to pain staking setup of all the involved elements. Furthermore, the use of *states* can be utilized for managing events with non-SCPS compliant modules, e.g., a BYPASS state can be imposed through a global instruction as to set everyone to a known transparent state and permit non-SCPS compliant devices to share a resource without conflicts. The use of specifiers, or instruction associated parameters, is accordingly introduced to cover the need for additional control at the instruction level.

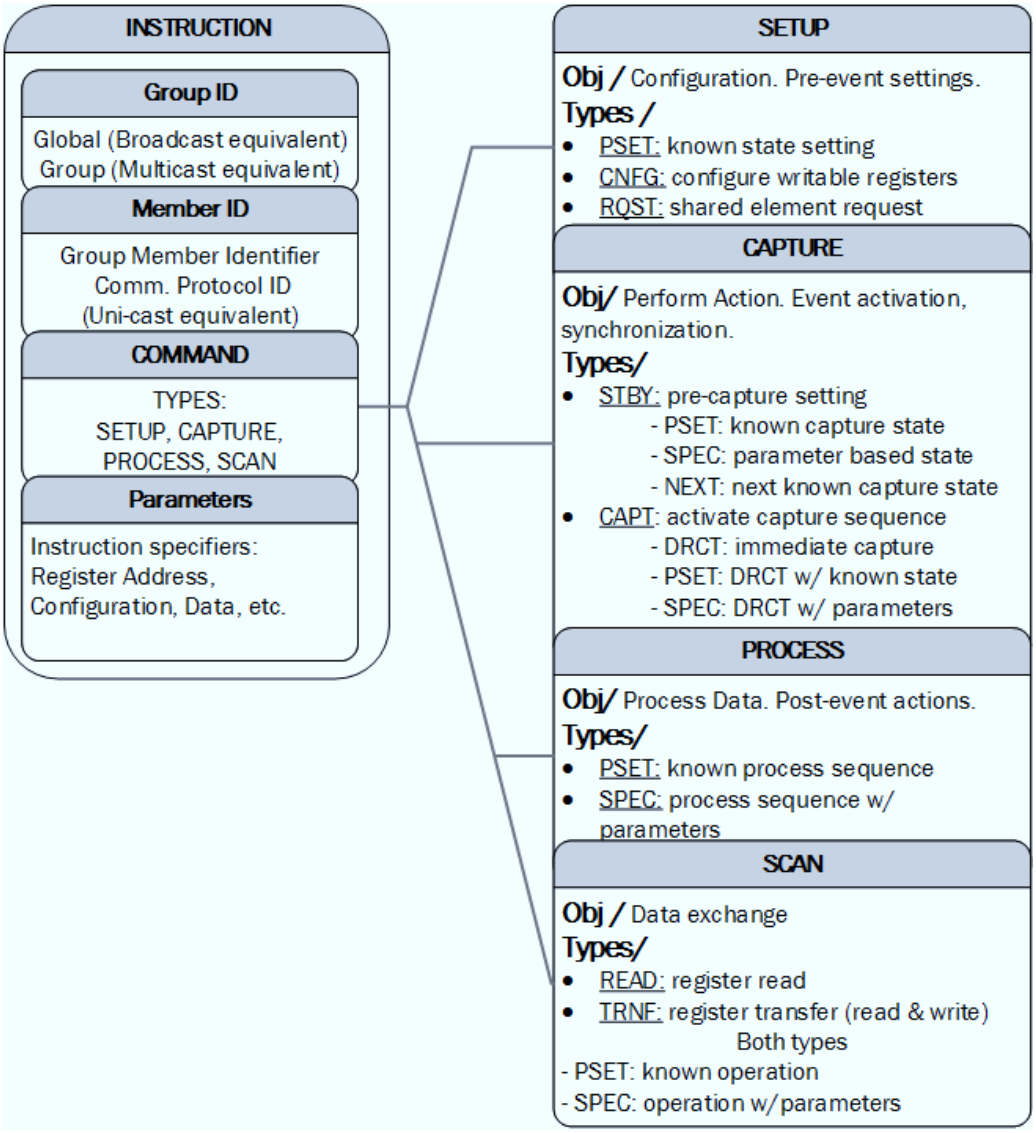


Figure 3-22 — SCPS commands structure.

Based on the target of the command itself, the commands can be classified in: General, Group and Specific. The general commands are intended for structure-wide calls, such as

initialization and global level actions; while group commands have an element sub-group as target and can serve for multi-module management and synchronization, as opposed to module specific commands (the natural format of I2C bus communication). Through the introduction of group-aware addressability, procedural simplification can be achieved, e.g., managing group level setups and multiple instrument/device test strategies (synchronizing multiple modules for a particular measurement strategy). An overview of the command structure can be visualized in Figure 3-22; due to the use of associated registers it is predictable that most commands will be associated to actions directed to read/write (R/W) registers, similar to strategies observed on microcontroller through bit-setting.

3.2.6 *SCPS Register and Pointers*

The SCPS register and pointer sets represent a key element of the proposed structure, since they can be used to define the overall associated events. If one is to consider synchronizing inter-modular events it is foreseen that a minimal set of registers and pointers are required to facilitate coordination. In suit with most standards there exist a need for identification registers (in the presented scenarios such identification registers would be required at multiple level, i.e., group and member levels). Additionally, inter-modular event management can be achieved through registers and pointers that permit sequential progression; providing information regarding the present state of the module and the status of different processes, serving a key informative role. Finally, configuration and event associated registers are a proven strategy to structure internal procedures and store data. Figure 3-23 presents one of the preliminary considerations of the status register, intended for conveying the state of the SCPS module.

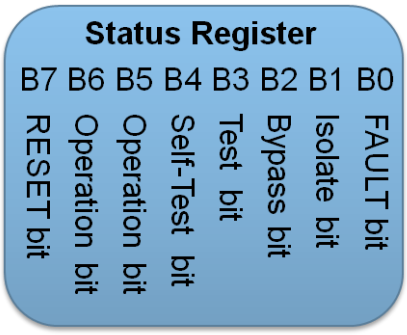


Figure 3-23 — Status register overview.

The SCPS registers and pointers can be subdivided based on mandatory permissions and functionality. The mandatory registers and pointers are required among all SCPS compliant devices; consequently forming a set of known structures that can be utilized for synchronization and action simplification. The communication bus specific control registers can be considered within this group since they would be required in all the participating instruments/devices; however certain aspects such as addressing could not be strictly required, e.g., the 7-bit address of an I2C module.

Besides the identification registers, the STATUS and STATE registers are the only mandatory SCPS registers; considering minimal instruction and data registers as being part of the communication bus structure. In any case, the STATUS register, as its name infers, serves as an internal information gathering location and can be externally read as to summarize the status of the SCPS module. For instance, the current state of the capture action can be reflected through bits of the STATUS register as to permit an external observer module to determine when to schedule another event or retrieve the result. In contrast, the STATE register is intended to serve for internal purposes as a mechanism to declare the current state of the module, thus functioning as a control mechanism.

The identification (ID) registers represent an important aspect for the overall strategy since they define the accessibility to the SCPS modules. A device info ID register, similar to the one present within IEEE 1149.X strategies, can contribute to the identification of the associated devices type (sensor, source, sink or processor, to be discussed ahead) and its specific aspects (such as sensor type, i.e., two wires or 1 wire sensor, or source type, i.e., voltage versus current source), however at this point is considered as optional. All SCPS compliant instruments/devices are required to have two identification addresses: a group ID and a member ID. Optionally, a communication bus specific ID (CBID) for SCPS independent operations, could be also present as previously mentioned.

Supplementary to the before mentioned registers, one could group additional registers based on their stage dependence. For instance, setup registers are all those to be used for configurable aspects and settings, such as thresholds references, timer initialization, processing strategy arrangement, stimuli amplitude and frequency specifications.

Capture and Process registers, on the other hand, refer to those related to the capture or process stages respectively, such as data holders and extended status information of the stage, e.g., sample measured, group deviations, or even history averages of the specific module. It should be noted, that multiple capture strategies or instances could be associated to a module, thus an associate array of registers could also be present.

Lastly, one expects a number of instrument/device specific registers to be present associated to local elements or for functional purposes that not necessarily have SCPS functional association. Figure 3-24 summarized the before mentioned registers description.

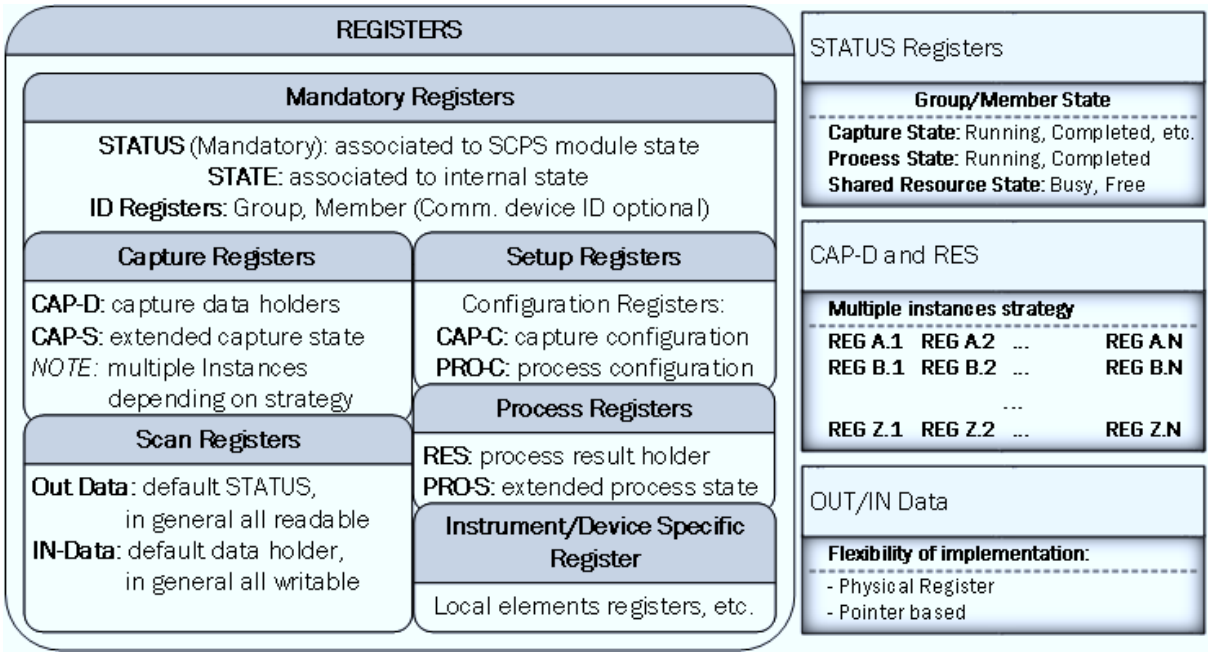


Figure 3-24 — SCPS registers overview.

Complementary to the register set, the SCPS structure is dependent on a pointer set, which are basically registers that are sequentially incremented or decremented, as to serve for event and group action sequence management. The purpose of the pointer set is to establish an inter-modular sequential reference. For instance, in order for a group-aware read action to occur, the members of the target group require knowledge of their turn to output specific data. Another case of interest is for *state* control, such as the scenario of multiple-steps captures; Figure 3-25 provides a summary of the referred pointers.

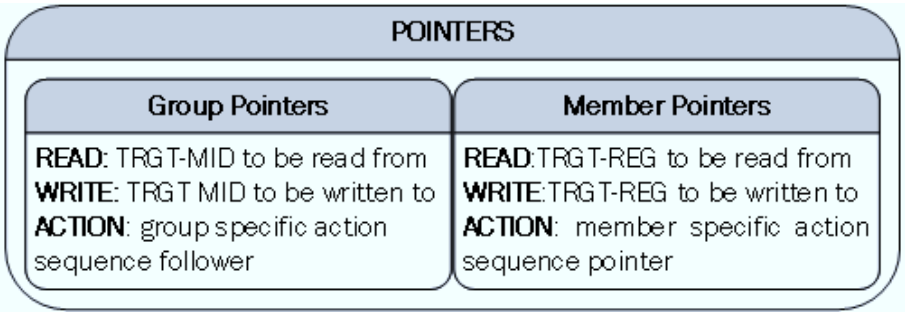


Figure 3-25 — SCPS pointer overview.

The commands and registers/pointers described up to this point, serve as the basis of the SCPS module strategy presented; however, although a minimal set of commands/registers are to be defined as mandatory, the specific functionality of each SCPS module is dependent on the functional objective of the device associate. The four types of associated modules being considered are: sensors, sources, sinks and processors (and combinations of the four mentioned). The processors devices listed refer to control centres for the SCPS operations, which could be present locally, centralized or encountered as part of a mixed device strategy. In general, any device that will serve as a master of the I2C bus at any given time will be thought of as being a processor or combined with a processor. Such approach allows

for strategies where a member of a group can serve multiple roles or assume new roles dependant of certain scenarios; e.g., when unforeseen fault scenarios cause the locally responsible processor module to malfunction and unable to schedule events, a redundancy attribute of a group member node allows it to assume the role of processor module (or at least a partial role).

3.2.7 SCPS Benefits

In a broader perspective, the SCPS has inherited advantages over other strategies such as IEEE Std. 1149.1, IEEE Std. 1149.4, IEEE Std. 1500 and IEEE Std. 1687, in three specific scenarios:

- **Event inter-modular synchronization flexibility**: group awareness provides a mechanism for communication and resource overhead minimization, as to permit rearrangeable inter-modular configurations with minimal associated instructions. Although strategies such as the presented by 1149.X also present inter-modular synchronization during events, such are achieved at the cost of high transaction complexity, that require a specific knowledge of the architecture and boundary module availability; furthermore, they are seldom applicable to *in-situ* test management scenarios.
- **High module activity complexity**: most structured strategies impose implicit limitations to the modular activity to be associated to the methodology or serve as a local BIST strategy activation mechanism. The advantage offered by the SCPS approach resides on the decentralization of the modular activity definition, permitting inter-dependent pseudo-BIST approaches.
- **Decentralized test management**: conventionally there exists a central test manager which controls the test data path, thus controls all the associated resources present (e.g., boundary modules and analogue test bus). The SCPS approach provides flexibility in such respect, permitting floating test manager scenarios; thus, introducing a highly flexible reconfigurability.

With regards to the specificities of the implementation of the SCPS (described in detail in Chapter 4), the before mentioned registers, pointers and features represent an augmentation to an I2C bus interpreter, with extended features which maintain full backwards compatibility; while maintaining flexibility to be modified according to the IC designer's purposes. A number of benefits are incorporated, such as:

- Enables a master of a I2C bus to read or write, as well as control through a given set of instructions, all slave modules, groups of slave modules or any slave module individually, that is connected to the I2C bus; thus, adding granular accessibility to I2C.
- Enables a master of an I2C bus with synchronized access to multiple slave modules connected to the I2C bus.

- The SCPS handler add-on, also allows the same effects as two previously mentioned benefits, to be extended to analogue and/or digital elements of the IC, by adding a controllability and observability management source handled through the SCPS module.
- Speeds up the communication, in certain scenarios, between a master and several slaves by reducing the length of the involved sequences. Particularly in cases where the target READ/WRITE register has the same address among the involved modules, reducing the operation to one group sequence (SCPS WRITE Transaction or a SCPS READ Transaction depending on the case) instead of multiple device specific sequences.
- Speeds up and simplifies the slave to slave transfer of data, by adding the capability of a master controlled transfer of a register from one slave (which provides the register) to another (which receives the register) in a single operation.
- Facilitates the synchronization of inter-module actions from a global and group specific perspective, by providing pointers, registers and optional control elements that facilitate the coordination of inter-module actions through a common instruction set format and resources.
- Facilitates the implementation of token strategies through the use of global instruction set for resource request, which instantiates a mechanism for resource availability verification.
- Provides operation locking mechanism, i.e., a sub-set of instructions permits to reduce the functionality of the SCPS module as to limit a module's response. Such is intended to serve as a mechanism for isolating a member of group in case of detected mal-function or fault.
- Expands the I2C established GENERAL CALL instruction set as to permit RESET or global impacting actions (such as modules isolation, bypass, etc., required during an initialization or re-calibration event for example).
- Facilitates inter-module sequential and instantaneous operations through an instruction sub-set (i.e., CAPTURE instructions), which when properly utilized can synchronize the individual module actions as to permit a group operation, which can be updated sequentially through user defined parameters and specific instruction flow, thus reducing the communication sequences and possibly reducing resources by permitting synchronized re-utilization.
- In certain scenarios, reduces the resources that would be required to perform the same operations within multiple modules by permitting resource re-use through the inter-module action synchronization and management.
- Reduces the need for individual 7-bit I2C addresses through the use of a shared group address (10-bit or 8-bit) and the member address, thus providing flexibility in the

individual addressing scheme and reducing dependence to the available 7-bit address domain.

3.2.8 *SCPS Costs and Restrictions*

Any design for testability strategy adds cost due to the associated resources. In the case of the SCPS such cost is related to the structures defined on the previous sections of this chapter (*Sections 3.2.4* through *3.2.6*). For the case of an I2C based implementation of the SCPS framework, such as the one to be presented in *Chapter 4*, a number of elements need to be added to the standard I2C structure:

1) SCPS interpreter: composed by counters and glue logic, which sequence the received data and maps it to the appropriate flags, registers and pointers. The most basic I2C slave would include a minimal amount of logic in order to interpret the data and associate it to a register address and register contents, as well to include additional logic for auto-increment (which is usually present). That said, SCPS does include a more complex structure that requires in bit-wise association of the incoming data to elements such as flags, as well as the need to assign the mandatory registers and pointers the appropriate value.
2) SCPS Register/Pointers: once more one could argue that any I2C slave would count with a number of associated registers and resources for data input/output. In the case of SCPS a small number of mandatory registers and pointers are needed.

In order to provide a sense of the impact in resources of the SCPS inclusion to a module, Table 3-1 presents the slice resource cost per module in the I2C SCPS implementation of Chapter 4. As can be seen, SCPS has a reduced impact on the available resources and when weighted against the benefits, such as communication overhead reduction and overdesign simplification, it has the potential of reducing the overall silicon area.

Table 3-1 SCPS Spartan 6 resource utilization.

Logic Utilization	Additional cost	Percentage of FPGA Available Resources
Number of Slice Registers	125	0.2 %
Number of Slice LUTs	424	1.6 %
Number of occupied Slices	145	2.1 %
Number of LUT Flip Flop pairs used	432	N/A. Reflection of the optimal usage of configurable logic blocks

The SCPS module assumes that non-SCPS compliant devices connected to the shared I2C bus are compliant with the UM10204 I2C standard. As with any protocol, some restrictions and assumptions are taken, such as:

- All electrical and timing considerations are the responsibility of the IC designer and should comply with the UM10204 I2C standard and any additional standard being applied.
- In the case of using a 10-bit I2C address format for the identification of the systems group, it is assumed that the address is unique in the system and does not coincide with a non-SCPS compliant devices connected to the shared I2C bus.
- In the case of using a 8-bit I2C address format for the identification of the systems group, it is assumed that the use of the alternate protocol reserved 7-bit address will not conflict with additional alternate protocols connected to the shared I2C bus, i.e. the only devices that respond to the alternate protocol address are SCPS compliant.
- Optional I2C features such as arbitration and clock stretching are the responsibility of the IC designer and should be implemented in such a manner that does not conflict with SCPS operations.
- The I2C interpreter is implemented in such a manner that provides the SCPS module sufficient controllability and observability of the SDA and SCL lines.
- The registers associated to the I2C interpreter (those accessible through standard I2C sequences) should, when considered within the SCPS register set, be directly accessible to the SCPS module.
- The user defined registers and parameters are properly formatted.
- The IC response to SCPS operations is the sole responsibility of the designer.
- Any routing conflict which might occur due to unforeseen configuration applied through the SCPS module is the sole responsibility of the system designer.
- When using the SCPS module for token strategies, it is assumed that the involved modules will verify the availability of the resource prior to usage and it is the responsibility of the designer to implement any related safeguards.
- All safeguards related to system and/or user safety are the sole responsibility of the system designer.
- Inter-modular event coordination has the assumption either the participating modules were designed with an understanding of their event associated procedures and responses through direct coordination of the designers or through shared documentation.
- All electrical and timing considerations that might need to be considered during inter-module operations are the sole responsibility of the system designer.
- The SCPS module, operations and framework are intended for facilitating inter-module data operations, measurements and testing; however, the specific actions of the involved instruments are the sole responsibility of the designer, including electrical and timing considerations.

3.3 SCPS Procedural Flow

The previous sections provide an appreciation regarding the associated SCPS structure; in contrast this section focuses on the procedural flow, as to ascertain a sense of how the events are managed. There exists flexibility with regards of the associated workflow of the before described structure, however, the intention is the simplification of inter-modular actions and event management. Although, apparently complex, while compared to the simplicity of a two operation strategy such as the one presented by the I2C UM10204 (through the use of WRITE and READ operation, ignoring optional special operations such as GENERAL CALL, START BYTE, etc.), the SCPS instruction set expands upon the functional capabilities of its associated communication bus protocol. The use of a common interface structure among instruments permits that the associated flags, registers, pointers and functional responses serve a standardizing role that minimizes the internal mechanism knowledge required to interface instruments that are intended to be used by multiple modules, thus reducing the overall need for resources (through instrument reuse) and communication overhead (by simplifying the communication scheme).

A general perception of the workflow of the SCPS module can be seen in Figure 3-26, where the SETUP, CAPTURE, PROCESS and SCAN stages cover the inter-modular and intra-modular operations; and as illustrated, there exists no unique path, a flexibility that permits for a wide number of measurement approaches. The effects of each stage on the associated registers/pointer and elements in general, is dependent on the target functional objective of the procedural stage, as previously discussed. That is to say, that some stages affect each module independently from each other, i.e., intra-modular, while other stages require the active collaborate of the modules, i.e., inter-modular. Moreover, when referring to event dependency, one refers to stages where the associate instruction or operation activates a process which is independent of the SCPS structure and its conclusion is not necessarily immediate; e.g., submitting a capture instruction to a module could imply a number of operations, including signal stabilization and/or multiple measurement instances averaging, which would take an indeterminate period of time. On the other hand, certain operations such as a read/write register operations, although might require an acknowledgement depending on the communication bus, are not generally expected to occur with a significant delay after the instruction has been communicated. The rest of this section will focus on the particular flow of each stage.

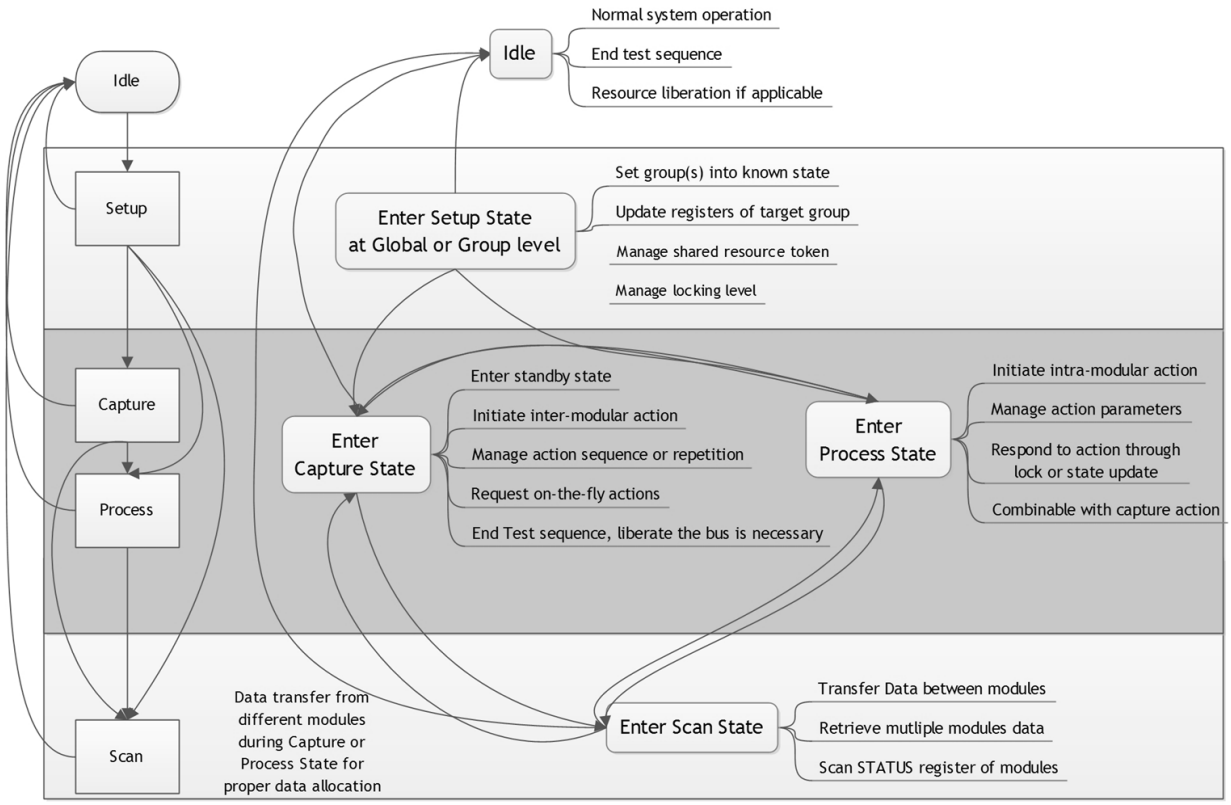


Figure 3-26 — Overview of the functional SCPS flow.

The **SETUP** stage responds to the need for configuring the settings and state of the module prior to or in between events; Figure 3-27 presents its general flow. Three types of setup instructions are considered:

1) **Select:** utilized for setting the modules to known states, e.g.: reset, bypass or isolate. Associated actions: Registers updated based on pre-established user defined values (fixed or programmable), routing elements could be affected on such instruction type in response to the change of the module's state.
2) **Update:** used for direct register data updating, which updates the targeted registers based on the data provided as a specifiers. Actions: Registers updated based on pre-established user defined values (fixed or programmable). Routing elements shouldn't be affected on such instruction type.
3) **Lock:** utilized for management on the response of the module in general. Such instruction style provides a mechanism for controlling the general behaviour of the module, e.g., avoiding that a mal-functioning instrument/device responds to SCPS group commands.

A special case instruction is associated to the global addressing, where a token strategy is consider for shared resource request, e.g., requesting exclusive access to an ATB.

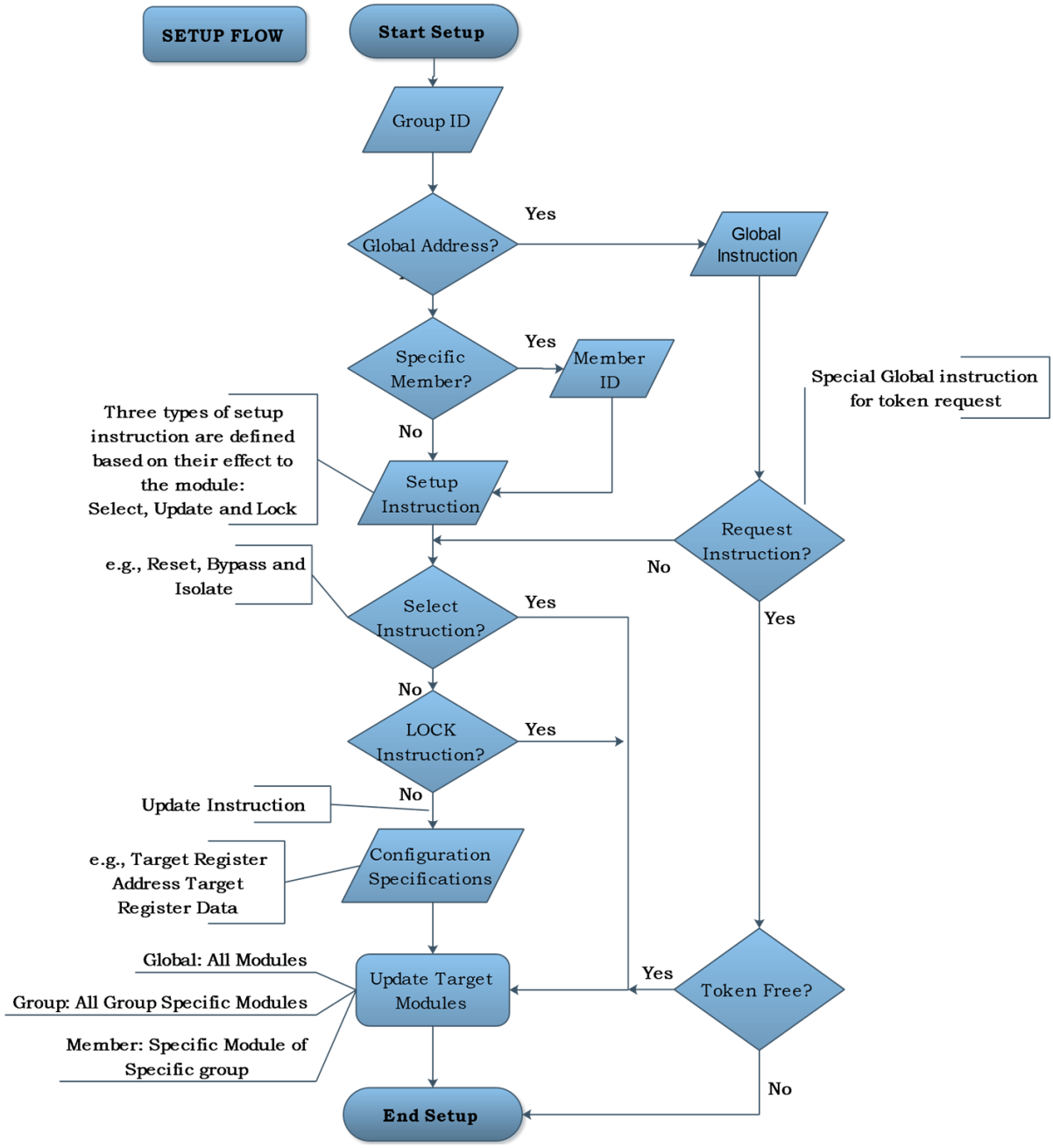


Figure 3-27 — SCPS SETUP stage flow.

The **CAPTURE** stage responds to the need for synchronizing the group members for a capture event. Three capture instructions types are considered and their flow is presented within Figure 3-28:

1. **Standby:** meant for generating a transitional period for pre-event activities or specifications updates. Associated actions: activates the routing and involved elements (stimuli, support, shared), except sense style elements which are not intended to perform a measurement at this step (however could be utilized to perform pre-event measurements). The module remains in waiting for a capture or end-capture instruction, while updating the status register to reflect its state.
    a. *Select:* utilizes pre-established user defined states for updating registers/pointers, routing, stimuli and capture involved elements of all

target modules. Non-involved modules are taken to a capture default state (such as bypass).

b. *Configurable:* capture specifications are provided following the instruction in order to update the involved elements. Non-involved modules are taken to a capture default state.

c. *Next:* utilizes the next pre-set user designed state for updating associated elements of all target modules. Non-involved modules are taken to a capture default state. This instruction satisfies the need for sequential testing/measurement steps, such as in the case of frequency sweep or repetitions for noise compensation.

2. **Capture:** intended as a start event action for synchronizing the different members or elements involved. Associated actions: when following a standby it activates the sense elements of the capture event, while updating the status register and associated data register. In the case that it is not preceded by a standby instruction, it should activate all involved elements as well.

    a. *Direct:* utilized as a start capture event action, generally preceded by a standby instruction, and activates the sense elements followed by an update of the associated data register and status register.

    b. *Select:* utilizes pre-established user defined states for updating the routing and involved elements.

    c. *Configurable:* capture specifications are provided following the instruction in order to update the involved elements

3. **End-Capture:** indicates the end of a testing/measurement event and releases the shared elements and returns all modules to their default state.

Note: The updating of the associated data registers needs not to be immediate and the status register will reflect the state of the capture.

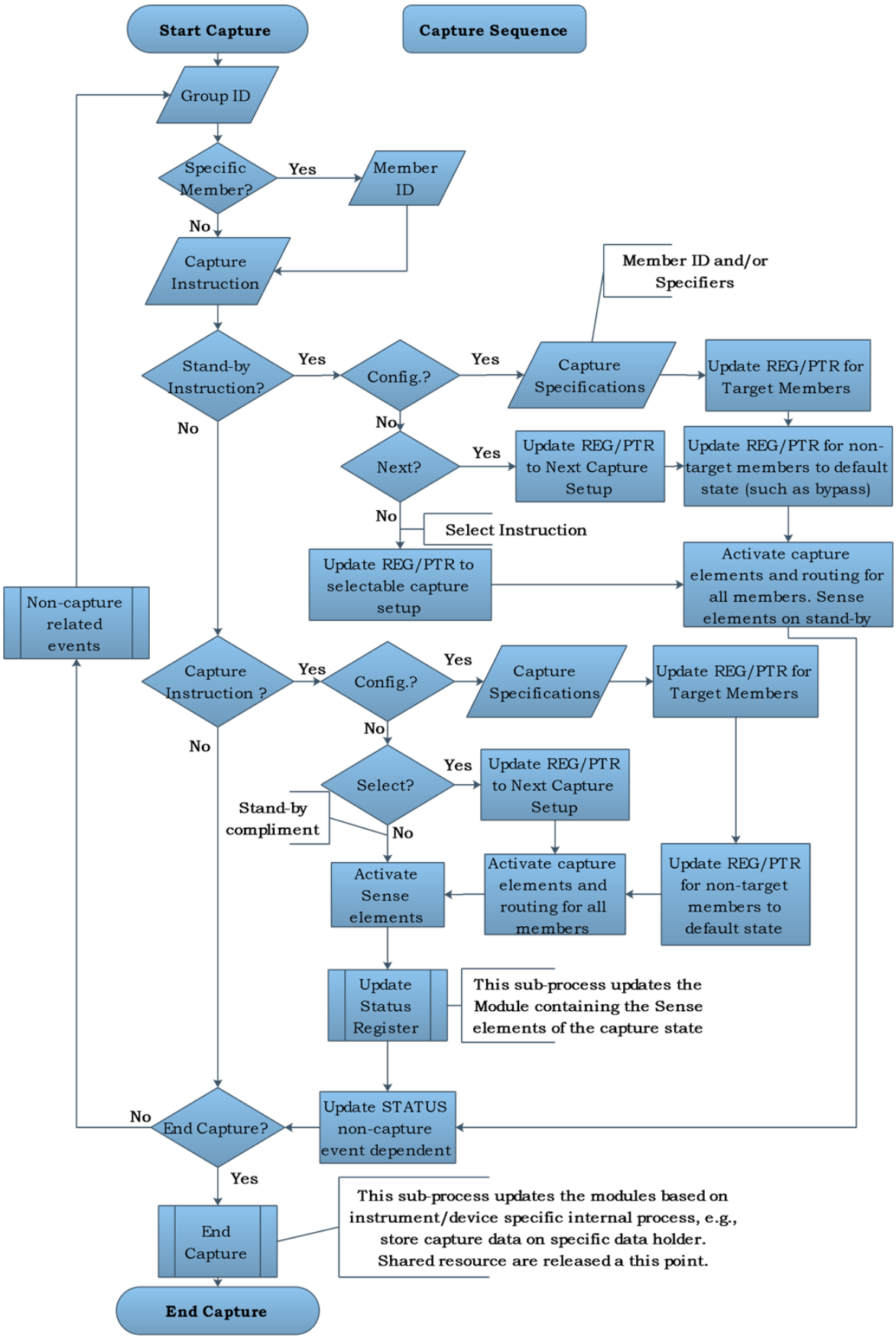


Figure 3-28 — SCPS CAPTURE stage flow.

The **PROCESS** stage responds to the need for synchronizing the processing of the captured data, thought for decision making strategies. For that purpose, two types of instructions are considered and their general flow can be observed within Figure 3-29:

1. **Select:** assumes the use of pre-established user defined states. Associated actions: activates the processing control sequence. Depending on the user defined connected strategy, certain register/pointers and elements could be updated.
2. **Configurable:** accepts specifications for the processing strategy through the instruction. Associated actions: updates processing related registers/pointers prior to activating processing control sequence. Depending on the user defined connected strategy, certain register/pointers and elements could be updated.

Note: register/pointer updates need not to be immediate, however the status register should be updated to reflect the state of the processing event.

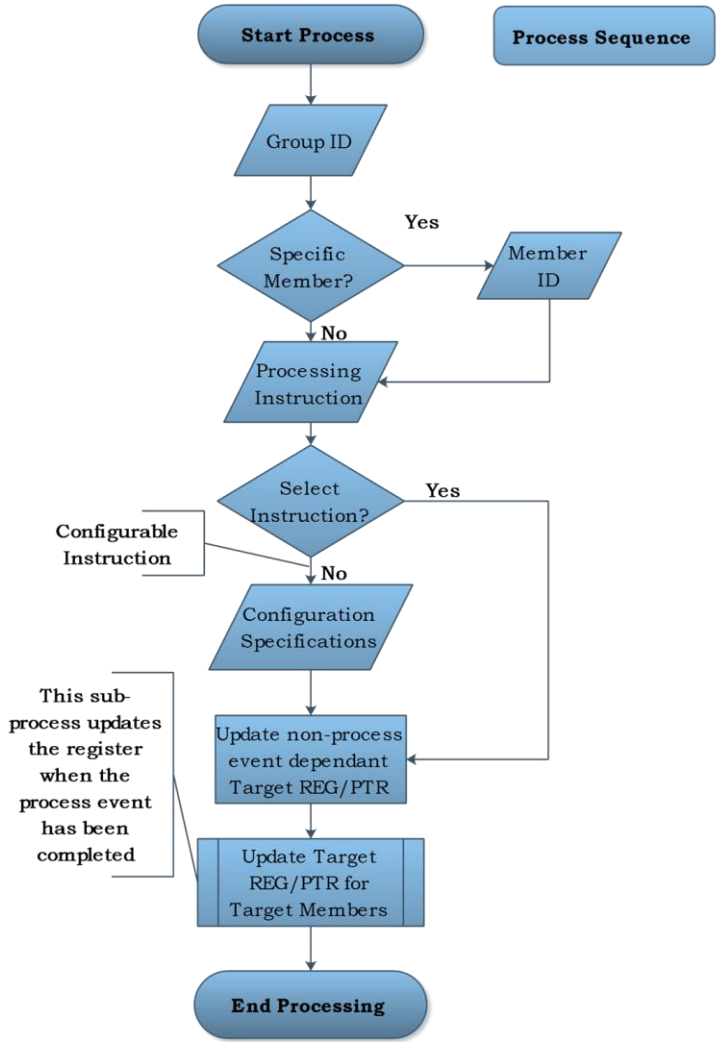


Figure 3-29 — SCPS PROCESS stage flow.

The **SCAN** stage responds to the need for exchanging data from or between modules. For that purpose, two types of scan instructions are considered and the general flow can be observed within Figure 3-30:

1. **Read:** retrieves data from group/member. Associated actions: updates the out data chain of the target member.
    a. *Select:* utilizes pre-set user defined configuration for scan control sequence. Associated actions: updates out data chain, sequential group/member reads are to be considered through corresponding pointer updating.
    b. *Configurable:* accepts specifications of target member/data. Actions: updates out data chain, sequential group/member reads are to be considered through corresponding pointer updating.
2. **Transfer:** retrieves data from group/member to be written elsewhere on group.
    c. *Select:* utilizes pre-established user defined configurations for scan control sequence (data source member and data target member and corresponding register address have been pre-set), sequential group/member transfers are to be considered through corresponding pointer updating.
    a. *Configurable:* accepts specifications of source and target member/data. Associated actions: updates out data chain, sequential group/member transfers are to be considered through corresponding pointer updating.

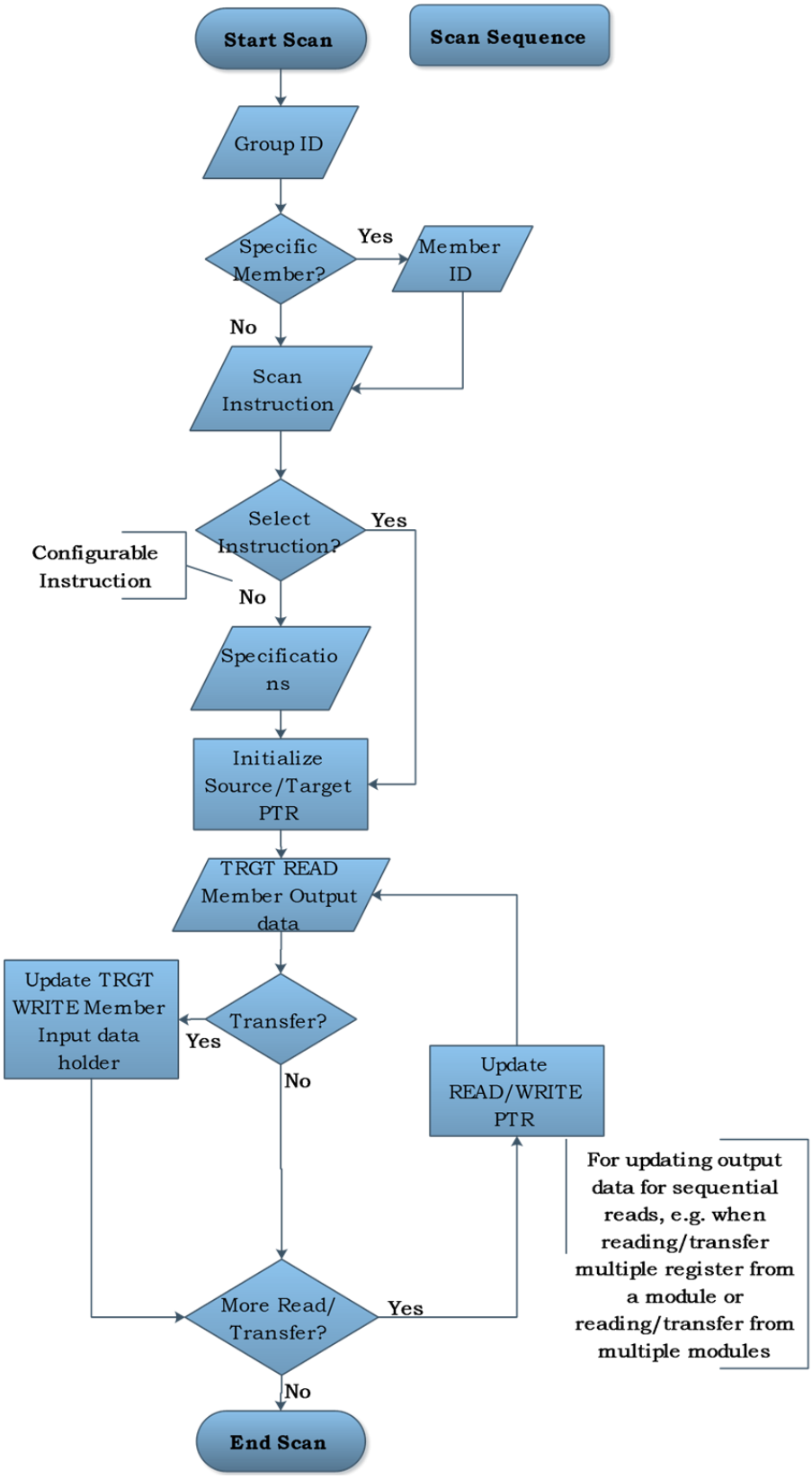


Figure 3-30 — SCPS SCAN stage flow.

3.4 SCPS Example

In order to gain an improved understanding of the concepts, structures and flow, the present section depicts some examples. The first example illustrates a simplified scenario with four modules forming a group, where the target events are the measurement of modules 2 and 3 internal impedance (target elements), with module 1 determining the stimulus type, containing a source signal generator, and module 4 acting as a sense type, containing a reference element and an ADC; a connecting ATB is considered as a shared resource (see Figure 3-31). The example intends to exemplify the flow of the SCPS modules from an instruction, register and routing perspective. Table 3-2 contains the sequence of steps, associated instructions, status of the modules, module's data holder and routing state; as to provide a view of the changes that occur during the different steps. It should be mentioned that some steps summarize multiple actions as to streamline the table. The corresponding visualization of the events described in Table 3-2, are presented in Figure 3-31.

Let's assume that the SCPS modules are in an unknown state prior to the start of a testing operation. It is then advisable to initialize them and proceed to request the use of the shared resource, which in this case is an ATB. Once we have the SCPS modules in a known state and the ATB has been assigned to the target group, we can proceed to enter such group in a known measurement setup, through the STANDBY command using setting PRESET 1 for instance. Such setting enables the appropriate switches in the different modules and activates the stimulus. A CAPTURE DIRECT command then indicates the modules that a measurement event is taking place, i.e., module 4 proceeds to take the appropriate measure which in this case is associated to the value of Z2. Once Z2 value has been "capture" one can proceed to the next pre-established setup by issuing a STANDBY NEXT command. This standby state also permits the opportunity of a SCAN TRANSFER, where the data captured by module 4 can be transferred to module 2, where the Z2 impedance is located. During the transfer a central testing controller could also intercept the data as to keep a history of measurements. An additional CAPTURE DIRECT command now permits the capture of the value associated to Z3 by module 4. Finally, another SCAN TRANSFER sends the data to module 3 and an END CAPTURE command indicates the end of the testing sequence and releases the token of the shared resource.

The key aspects intended to be highlighted are the group addressed instructions, removing the need for module specific instructions, and the user defined specifications. The later mentioned, refers to the module specified behaviour in response to the instructions, such as register initialization and BYPASS state response at the routing level (switches enabling settings). Further simplification for steps 6 and 8 (referring to the data transfer), where a default understanding of the source and target of the data transfer can be associated to the specific PRESET state.

Table 3-2. SCPS framework example 1.

Step	Instr.	Status of Module	Data Register	Routing State
1	Normal operation prior to SCPS	All modules in unknown state. The SCPS status information has been ignored during normal operation events.	All in unknown state. All module data register contain information unknown	All in unknown state. The routing elements are enabled in an unknown setup
2	GLOBAL RQT & SETUP DFLT BYP	All in default status. The SCPS modules are driven to a known state, i.e., BYPASS in a global level. Additionally, the shared resource has been requested activating a token.	All initialized. The data register are set to a known initialized value, e.g., 8H00.	All in BYPASS. The switches are enabled as to permit a BYPASS of the shared resource.
3	STBY-PSET 1	All indicate STBY. The specified group enters in a STANDBY status, specifically for PRESET setting 1.	All initialized. No event has occurred that changes the current value of the data registers.	Each to specific PSET 1 state. Each member module of the specified group activates the settings for PRESET 1 based on the user definitions.
4	CAPT-DRCT	Mod. 1-3 indicate CAPT. Since modules 1 through 3 do not have a sink element they continue indicating a CAPTURE status indefinitely. M4 indicates CAPT ongoing until finalized. M4 has a sink and will FLAG the end of the capture when the associate sink element indicates.	For Mod. 1-3 no event has occurred that changes the current value of the data registers. M4 has captured the value of $Z_{2.}$	All modules remain in the PRESET 1 settings.
5	STBY-NEXT	All indicate STBY. The specified group enters in a STANDBY status, specifically for PRESET setting 2.	For Mod. 1-4 no event has occurred that changes the current value of the data registers.	Each to specific PSET 2 state. Each member module of the specified group activates the settings for PRESET 2 based on the user definitions.
6	SCAN TRF M4 to M2	All indicate STBY. The specified group enters in a STANDBY status, specifically for PRESET setting 2.	M1 & M3 remain with initialized data registers. While M2 & M4 now both have value Z_2	Each to specific PSET 2 state. Each member module of the specified group activates the settings for PRESET 2 based on the user definitions.
7	CAPT-DRCT	Mod. 1-3 indicate CAPT. Since modules 1 through 3 do not have a sink element they continue indicating a CAPTURE status M4 indicates CAPT ongoing until finalized. M4 has a sink and will FLAG the end of the capture when the associate sink element indicates.	M1 & M3 remain with initialized data registers. M2 remains w/value Z_2 M4 captures value Z_3	Each to specific PSET 2 state. Each member module of the specified group activates the settings for PRESET 2 based on the user definitions.
8	SCAN TRF M4 to M2 & CAPT END	All modules are taken to a default status, through the end of the capture sequence. The token bit is cleared, thus freeing the shared resource.	M1 remains initialized M2 remain w/ value Z_2 M3 & M4 both have value Z_3	The routing structures are taken to a default setup for capture end.

RQT: request; SLT: select; BYP: bypass; PSET: pre-set; STBY: standby; DRCT: direct; CAPT: capture; M: module; TRF: transfer; DFLT: default.

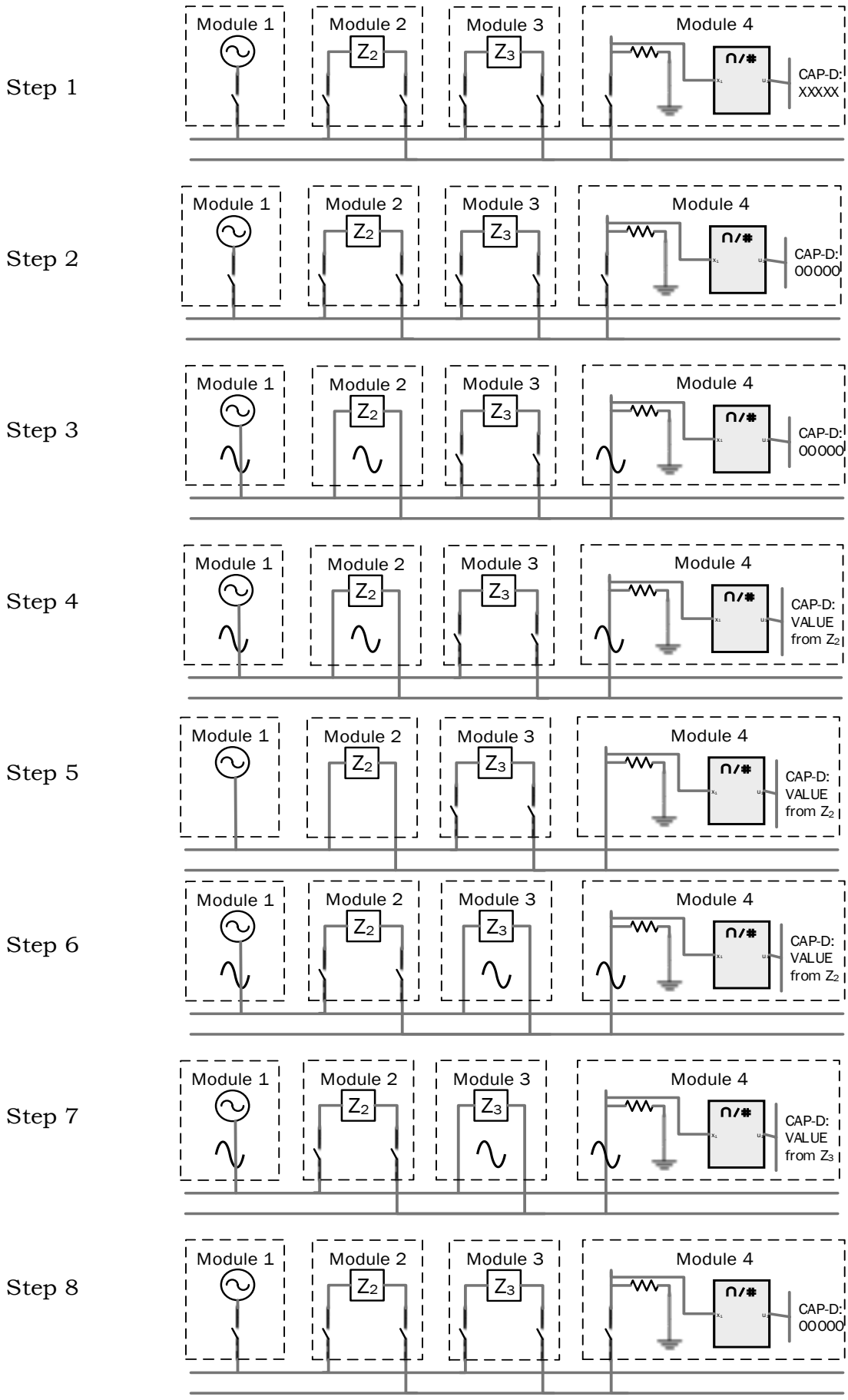


Figure 3-31 — SCPS framework example.

Let's consider that instead of the target elements being separated in different modules, such as in the previous scenario (module 2 & module 3), the target elements are part of an array, such as the one illustrated in Figure 3-32. In such scenario the approach itself does not change, instead the module handling the sensor array will interpret step 6 as a command to switch from one element in the array to another. In this scenario the transfer of the measurement to the module might be complemented with a change in the data holder location based on the PSET state, as to store the measurements of the array members in a data array.

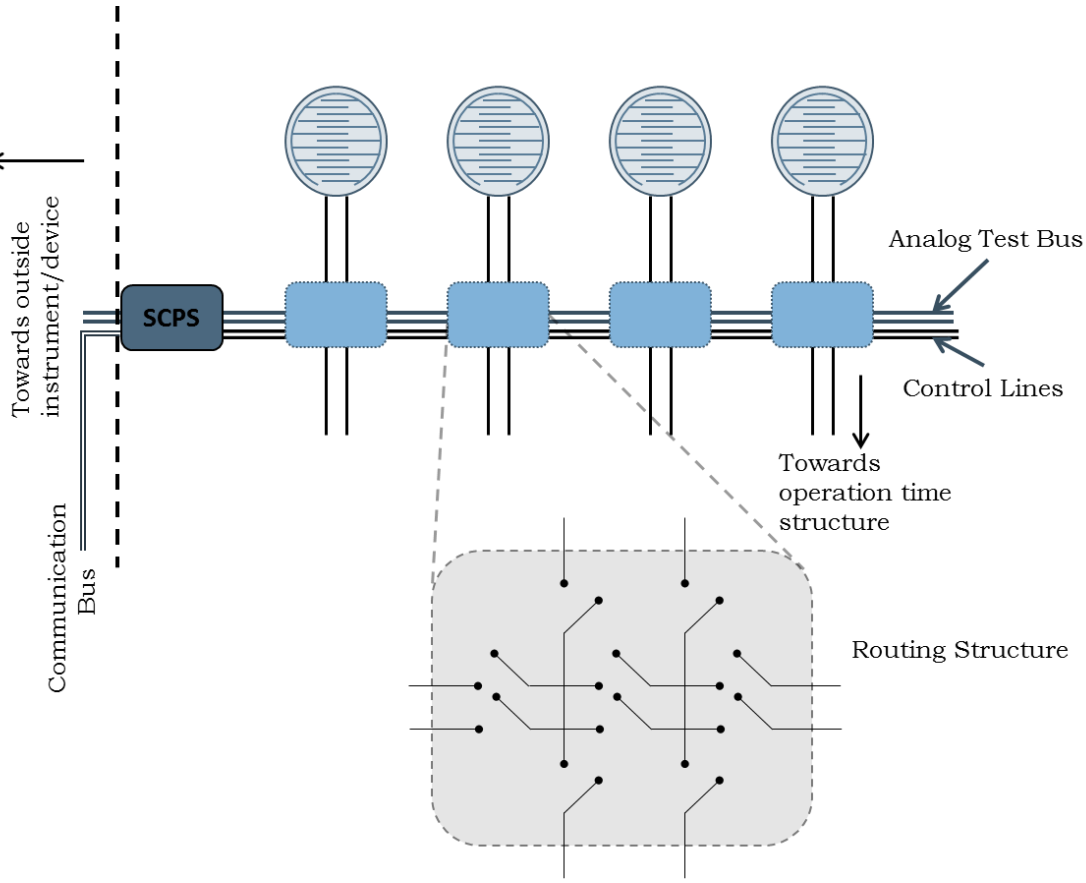


Figure 3-32 — SCPS framework sensor array scenario.

Yet another scenario can be observed within Figure 3-33, where instead of independent target elements, one finds an embedded test instrument integrated to a biosignals measurement section. In this particular scenario two test mechanisms are present within the instrument, one for electrode-skin impedance verification and one for the signal processor (e.g., instrumentation amplifier and filters) section. In this case, the overall approach remains the same; however, the user-defined parameters associated with the SCPS module will activate a different testing setup based on the PSET stage, achievable through the STBY instruction. In this scenario the STANDBY commands lets the embedded test instrument know the intended test, permitting the internal routing to adjust and the specific elements to activate accordingly. The CAPTURE command thus permits the proper measurement to take place, while the SCAN TRANSFER sends the results to the CPM.

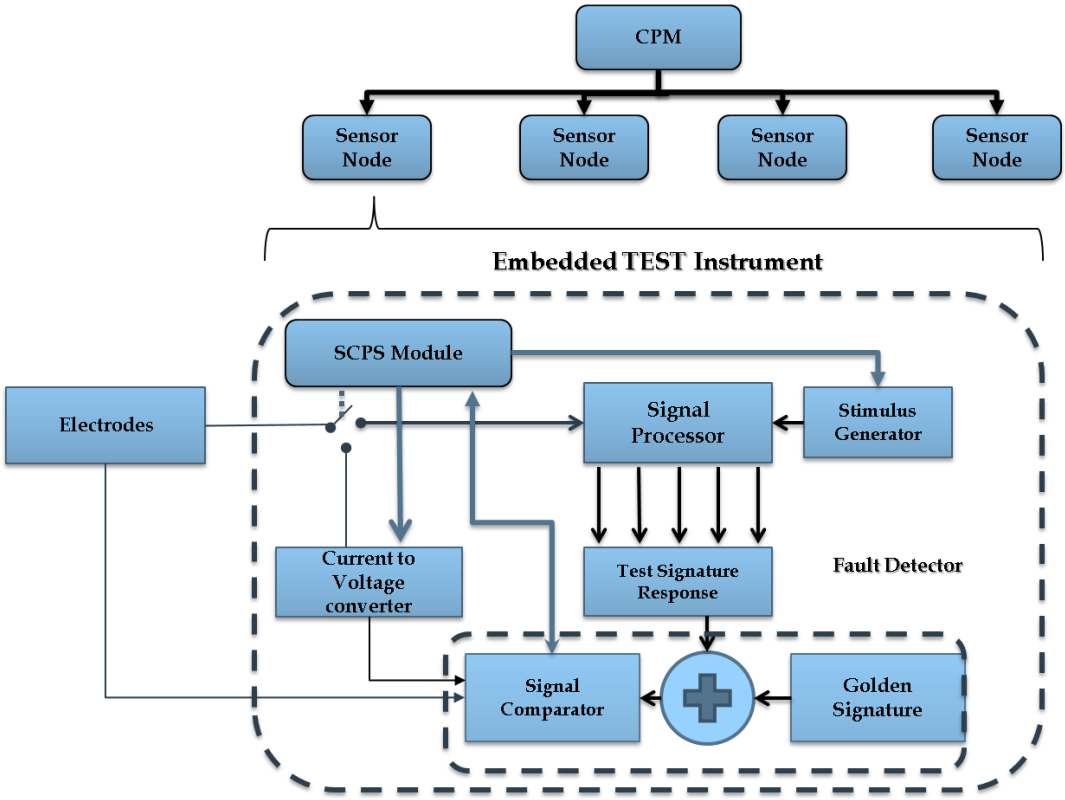


Figure 3-33 — SCPS framework multiple embedded test instruments example.

3.5 Chapter Remarks

Although the SCPS framework has its foundations based on proven industry standards, such as the IEEE 1149.X standards, and number of preceding approaches discussed within the previous chapter, it is from the identification of the existing gaps and fallacies that the SCPS framework gains its strength. In principle the SCPS frameworks strives to provide a unifying syntax between digital and analogue approaches, while remaining flexible in order to adapt to emerging technology and displacing dissimilarities towards the core designs; such aspiration is strived for through the general structure presented within this chapter. That said, the following chapter provides an exemplification of the SCPS framework, based on the I2C communication bus. The before mentioned implementation seeks to illustrate the structures and nuances of the SCPS infrastructure in a practical design.

Chapter 4

SCPS Framework Implementation

A number of procedures, methodologies, experiments, designs and implementations crossing multiple disciplines are part of the resulting efforts from this thesis. The present chapter focuses on describing the SCPS framework adaptation considering the I2C communication bus as the digital interlinking commonality, as well as a number of the required circuits and elements for the related experiments and proof-of-concept, and overview of the efforts can be seen in Figure 4-2.

Before advancing, a brief overview of the generic SCPS arrangement will serve to gain understanding of the different choices that were made regarding the implemented circuits and modules. As can be seen in Figure 4-1 a generic SCPS setup is composed by a test controller and several test instruments. The test controller needs not to have SCPS functionalities and is only required to be capable of serving as an I2C master. On the other hand, all test instruments that are to be integrated within an SCPS arrangement are require to be SCPS compliant through the inclusion of a specific infrastructure further described within section 4.1. It is also possible for a test instrument to assume the role of test controller (or even for multiple test controller to be present) in which case the SCPS compliance must be guarantee assuming a dual role (master and slave) if such is required, e.g., a impedance analyser module that serves as a test controller needs to respond, as a SCPS group member, to the SCPS commands that it transmits to the SCPS group. This said, for the purposes of proof-of-concept a straightforward arrangement will be considered, where the test controller does not form part of the test itself.

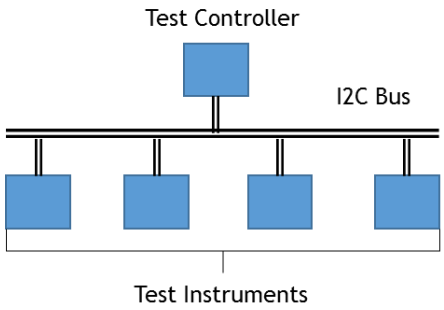


Figure 4-1 — Generic SCPS arrangement.

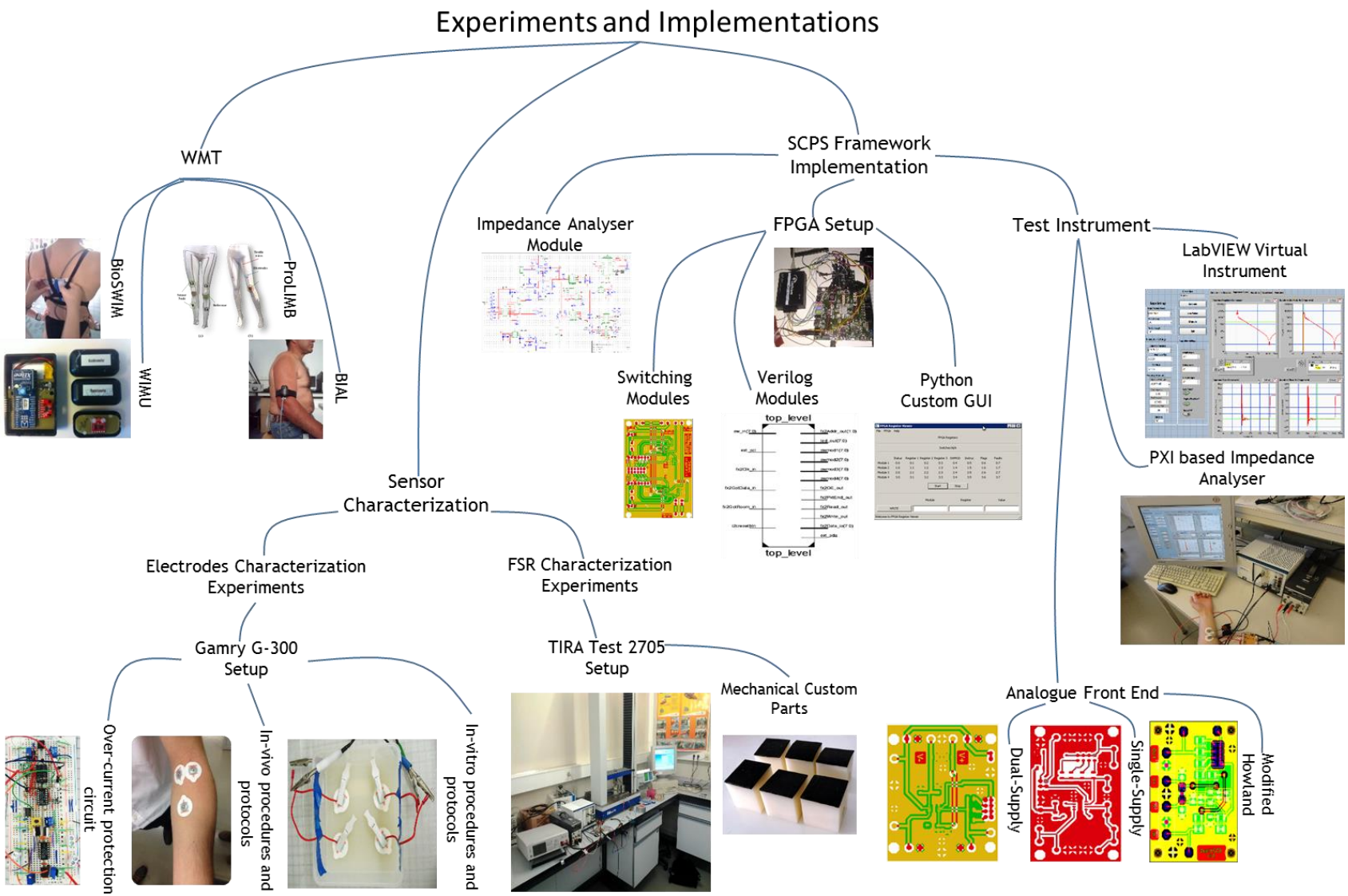


Figure 4-2 — Overview of experiments and implementations.

The proposed SCPS framework was implemented in an FPGA-based proof-of-concept setup as illustrated in Figure 4-3. A modular approach was followed, through extension of the I2C core described in the previous chapter. The entire FPGA implementation was written in Verilog 2001 and contained within one FPGA chip. Additional modules were instantiated, which permit communication with a computer through a USB cable and a custom-built graphical user interface written in Python 2.7. Hardware-wise, a number of circuits and corresponding printed circuit boards (PCB) where designed and constructed, including analogue switching modules, which serve as routing structures, and a number of analogue front ends (AFE) for impedance measurement, such as an inverting amplifier and auto-balancing bridge setups. An impedance analyser unit was based on a National Instrument (NI) PXI 1033, which contains an arbitrary function generator board NI PXI-5401, a digital oscilloscope board NI PXI-5112 and a 5½ digital multimeter NI PXI-4060. A LabVIEW virtual instrument was adapted to serve the purpose of a virtual test instrument. Other support circuitry were also designed and constructed, such as an overcurrent detector circuit for adapting a Gamry S-300 Potentiostat/Galvanostat for safe human experimentation, and other miscellaneous modules and parts for sensor measurement setups. A number of experiments were performed on disposable Ag-AgCl electrodes and FSR as to established appropriate testing strategies, such experiments are explained in the next chapter. Moreover a complex impedance measurement module was designed, although not implemented, and will be briefly described. The SCPS communication functionality was verified through functional simulation and property checking, as well as line level observability using a DigiView™ DV-100 Portable Logic Analyser (an USB based programmable multifunction logic analyser) and a digital signal generator CWAV USBee ZX test pod in I2C master controller mode, as well as the before mentioned custom Python-based GUI for internal SCPS modules' register observability. The GUI permits also direct programming through the USB cable utilizing the open source FPGALink's modules, the Cypress FX2 circuitry and associated Python bindings.

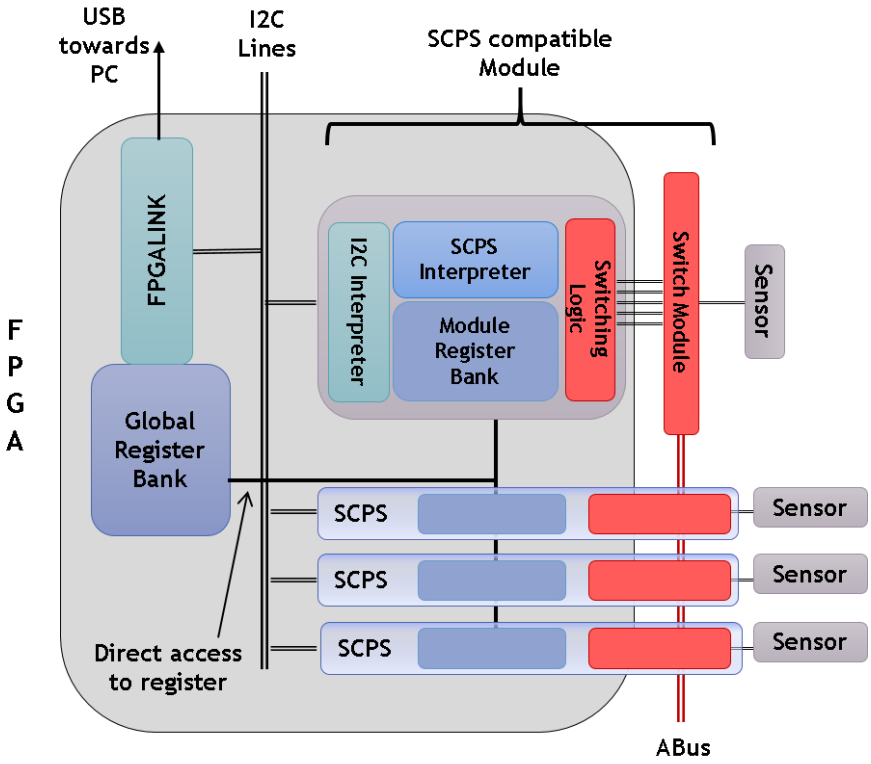


Figure 4-3 — SCPS framework FPGA-based proof of concept overview.

The implemented data transport structure was composed by an analogue bus, managed through I2C interconnected modules. The SCPS modules themselves are subdivided in four sections: I2C interpreter, SCPS interpreter, SCPS switching/control, and registers. The structure provides implementation flexibility, while remaining compatible with commercial I2C compliant components. Multi-level addressability is achieved through the SCPS interpreter, considering a group approach mechanism that relates multiple modules through a shared address. A command set, managed internally through registers and associative pointers, permits the synchronization of events, while allowing the sharing of common resources (such as an analogue bus) by token request through broadcast instructions.

The different SCPS modules were implemented within a Spartan-6 FPGA (Atlys and Nexys3 boards from Digilent Inc. were used), and the analogue bus interfacing section was based the on Analogue Devices' ADG173 single-supply analogue switches. The USBee ZX was utilized as an I2C master controller for I2C sequence input and master level observation, while the DV-100 Logic Analyser was used for the SDA and SCL line level observation and signal capture. A National Instruments PXI based impedance analyser, with the corresponding virtual instrument (VI), was implemented for test stimuli generation and capture, to serve as a conceptual test instrument. All the before mentioned will be further explained in the present chapter.

4.1 SCPS Implementation Description

The present SCPS implementation consists of extensions to the previously mentioned I2C interpreter and an associated superset of command sequences to access the extended features of the thus augmented module. Although the SCPS module was thought for the mixed-signal measurement/testing framework described in the previous chapter, the set module can be utilized independently of such framework for a variety of purposes. All elements of the SCPS module will be referred to as SCPS elements in order to differentiate from the I2C external elements and those specific to instruments. By instrument it is referred any core/circuit, embedded or at board level, which performs a set task (or number of tasks) independently from other instruments except for input/output connectivity.

4.1.1 *SCPS Module Implementation Functional Overview*

The **SCPS module,** from a general perspective, is composed by two add-ons sections to current I2C compatible designs, with option for a third one, which are described as follows:

1. **I2C Interpreter add-on (SCPS interpreter):** this section counts with the mechanism for a sequence identifier for SCPS associated command sequence recognition, as well as the corresponding response mechanism for updating flags, registers, pointers and elements of the SCPS module, and I2C signal responses that are SCPS associated (e.g. proper acknowledges to SCPS instructions); both for write and read I2C sequences, which, from now on, will be referred to as SCPS Write Transaction (SWT) and SCPS Read Transaction (SRT), respectively, when such I2C sequences are associated to a SCPS sequence. The interpreter identifies three types of addressing formats:
   - ***Global*** — referred to as GENERAL CALL within the I2C specifications UM10204 (NXP, 2014).
   - ***Group*** — reachable through two types of selectable alternatives.
   - ***Specific*** — associated to I2C 7-bit address format or through the use of a group member identifier through SCPS instructions.
2. **Register Bank add-on (SCPS registers):** SWT/SRT sequences access associated registers (hereby referred to as SCPS registers) for their corresponding retrieval and update, some of which updated in a sequential manner and will be referred to as pointers. Pointers have a reserved number 00H which are used as a hold position (one which does not increment). The default size of SCPS registers is 8-bit (optional byte multiple sizes are foreseen for future compatibility). Additionally, a set of USER DEFINED PARAMETERS, or UDP, serve as the source for a module state response. UDP refers to all parameters that are instrument specific, such as the default starting pointer positions and register values (e.g., the default fall back value of a register after a RESET or the pre-established starting pointer address for specific instructions).
3. **[optional] Element bank add-on (SCPS handler):** an optional add-on can be integrated into the SCPS module as to serve as switching/element library, as to

manage controllability and observability through switches and the functionality of other elements. These elements can be either digital or analogue and their configuration is the responsibility of the designer. The SCPS handler is to be controlled mainly through the STATE, allowing to pre-establish a configuration to manage routability and functionality of the instrument. An example of such add-on would be a routing dictionary connected to the enable pins of analogue switches, which permit access to an analogue bus. The dictionary would then translate a STATE to a target connection scheme; additionally, such library could also activate a BIST mechanism or other functional aspect of the instrument. This add-on is optional, since direct usage of SCPS module's flags and registers (internally accessible by the instrument) can be used directly for the same purposes in simple scenarios. In the present proof-of-concept scenario, the SCPS handler manages the ATB connectivity.

The before mentioned add-ons are illustrated and highlighted in Figure 4-4 and Figure 4-5. Figure 4-4 presents the different elements present within a SCPS compliant embedded instrument; in this scenario the communication bus is the I2C. The SCPS interpreter interacts with the I2C interpreter in order to determine if an appropriate command has been received, and in such case the response to the command can be deduced by the instrument specific control logic and used to enable the switching matrix in an appropriate specific pattern.

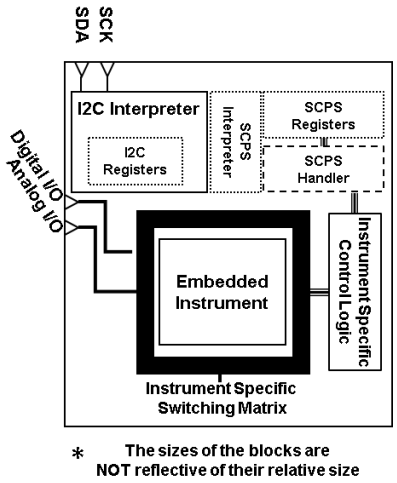


Figure 4-4 — Embedded instrument view of associated SCPS module.

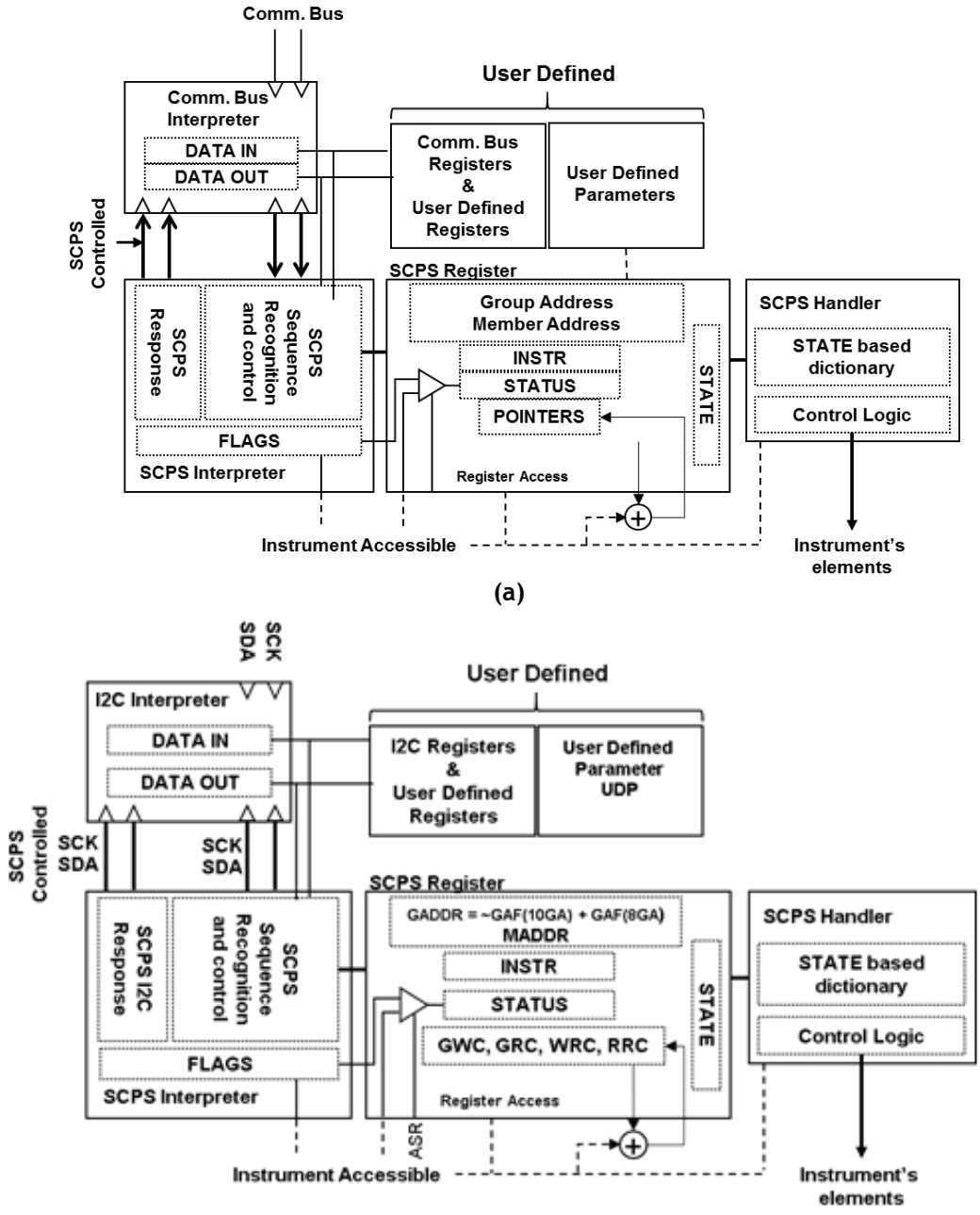


Figure 4-5 — General view of SCPS module sections. (a) Generic communication bus. (b) I2C communication bus.

In Figure 4-5 we can observe an expanded description of the different elements involved, such as the user defined parameter, which contains the instrument specific information that allows associated control logic to determine the appropriate response to a specific SCPS state, as presented by the SCPS handler. In general, associated identification, instructions, registers and pointers (Figure 4-5-a) are dependent on the related communication bus, adapted the specificities of such. The scenario presented by Figure 4-5 (b), is specific to the I2C implementation, where the register and pointers have been declared.

4.1.2 *Implemented SCPS Flow*

The elegant two-operation strategy presented by the I2C UM10204 (NXP, 2014) (through the use of only read and write operations, ignoring optional special operations such as GENERAL CALL, START BYTE, etc.), serves as basis for the SCPS instruction set, with its SWT and SRT, expanding upon the functional capabilities of the conventional I2C write and read operations. The SCPS adds a third operation referred to as TRANSFER, where READ and WRITE operations occur in parallel, which will be considered as a type of SRT or SWT for flow streamlining. A common interface structure among instruments permits that the associated flags, registers, pointers and functional responses serve a standardizing role that minimizes the internal mechanism knowledge required to interface instruments that are intended to be used by multiple modules, thus reducing the overall need for resources (through instrument reuse) and communication overhead (by simplifying the communication scheme).

The traditional I2C 7-bit address remains fully compatible for such instruments that have an associated 7-bit address, and will cause the SCPS interpreter to ignore any sequence accompanying such, thus permitting the instrument to be accessible through direct I2C means (thus no additional referring in this document to such type of addressing will be included). For global addressing, the SCPS interpreter will expect a formatted SCPS Global Transaction (SGT) after a GENERAL CALL (all zeroes as defined by I2C specifications, i.e., 8H00) and acknowledged accordingly. Several mandatory SGT are defined and are associated to specific updates of the internal flags and registers, as well as optional elements. A list of the corresponding SGTs and their actions can be found in the SWT section.

Regarding group addressing, two group addressing formats were considered: 10-bit addressing format and an alternate protocol format. The 10-bit addressing format provides access to a group through a shared 10-bit I2C address referred to as 10-bit Group Address (10GA). In the case of the alternate protocol format, the reserved 7-bit I2C address 7'b0000010 (for using different protocols and formats) can be used as a sequence starter for the SCPS protocol after which an 8-bit group address can be introduced as a second byte. Only the 10GA approach was implemented for the present proof-of-concept, however the alternate protocol approach is mentioned to illustrate implementation flexibility. Regardless of the group addressing format, access would remain the same for the SWT and SRT sequences that permit the write and read in a group manner, as well as interdependent synchronization and independent actions among SCPS compatible instruments. This is achieved by the use of the internal flags and mandatory registers. The SCPS sequences follow I2C compatible write/read sequences formats, thus remaining fully compatible with I2C compliant devices, and noted variations on the expected format must not affect I2C compliant devices (insured by following compliance with I2C UM10204).

The general sequences for the SWT and SRT can be seen in Figure 4-6 (a) and (b) respectively. As can be noted in Figure 4-6 (a), the SWT general sequence follows a similar approach to that of most I2C components, i.e., a three byte sequence with optional trailing

data bytes. The first byte is compliant with the I2C 10-bit address read/write format, where the all 1's most significant nibble follows a 0 and the two MSB of the 10-bit address (alternatively one would use the alternate protocol, 8H02, byte). The second byte completes the address (or provides the address in case of the alternate protocol approach) while the third byte contains the instruction, followed by additional data or specifier bytes, based on the instruction's requirements. SGT has a similar approach with the second byte being used for the instruction itself (since no additional address information is required). The SRT follows the same strategy as in the I2C 10-bit address, where a previous WRITE operation defines the target slave module, so after the first byte, data is expected from such targeted module.

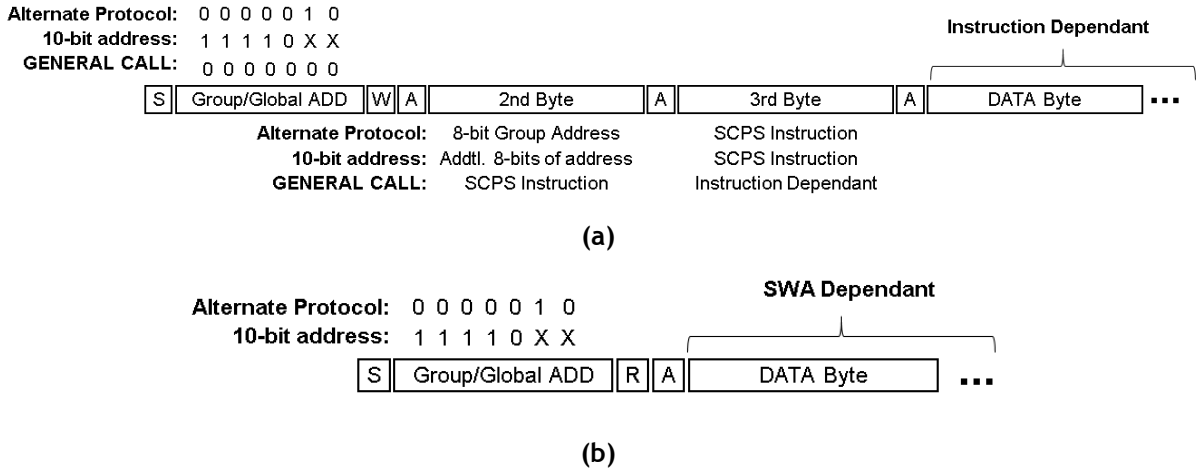


Figure 4-6 — (a) SWT general sequence. (b) SRT general sequence.

4.1.3 *SCPS Transactions*

The before mentioned transactions, SWT and SRT, regulate the stream of information and functional control of the modules, structured to follow the I2C protocol. In order to better understand their characteristics and flow, Figure 4-7 presents a diagram summarizing the before mentioned transactions. Within the figure one can observe that for a non SCPS sequence, the modules respond as any I2C compliant slave; however in the case of a SCPS sequence, two possible paths are available, that of a SRT or a SWT, which depend on the R/W bit (8^{th} bit of the first byte received after a START or RE-START event).

In the case of a SRT, a group READ or TRANSFER operation takes place, based on the assertion of the STANDBY Flag (for a TRANSFER). The members use the UDP in order to establish the register and pointer default values; and proceed to compare their own member address with the READ source and target WRITE modules. In case of a match, such module performs the corresponding transmitter or receiver tasks (depending if they match with the READ source or the target WRITE respectively). The ACK for these scenarios are managed by the MASTER module, except for the initial ACK that is performed by the READ source module. This implementation includes an auto increment feature, where the source module address is incremented by one, while in the case of a TRANSFER it is the source/target register which is

incremented by one. This feature permits quick scans of the STATUS register (used as default) of all the members of a group, without the need to access them specifically one by one.

In the case of a SWT, the complexity increases when the modules accept an instruction from a MASTER. Depending on the instruction, different actions are taken by the member modules; that is discussed in detail in the instruction sections. In general, the behaviour of the modules follow a streamlined pattern, for group instructions all members of the group update their FLAGS, registers and pointers based on the associated UDP for the given instruction, while for a member instruction, only the specific member responds accordingly. Additionally, the SCAN instruction has the members reacting somewhat differently, by becoming source or target of a TRANSFER operation (in the case of a READ, the TRANSFER is assumed to have the MASTER modules as target).

The SCPS TRANSFER Transaction (STT) differs from the conventional I2C operations in that slave modules are simultaneously performing READ and WRITE operations. However, as mentioned previously, it will be referred to as a sub-class of the SRT and SWT. In order to illustrate the advantages of a TRANSFER transaction within a group approach versus standard I2C transactions, Figure 4-8 illustrates the difference between a conventional inter-slave module transfer of data and a group approach transfer of data. The upper sequence of operations showcases three types of transfers, considering the inclusion of specifiers regarding target and source modules and/or registers. In the most complex scenario for the STT we have eight 8-bit I2C transactions, compared to nine for the conventional method. However, if multiple bytes are to be transferred, each additional byte incurs a two 8-bit I2C transaction penalty compared to only one for the STT. Moreover, if the transfer taking place is part of the UDP definitions the STT can be further reduced to four 8-bit I2C transactions plus one additional transaction per additional byte. Additionally, the current implementation of the SCPS considers a QUICK TRANSFER, for certain scenarios, such as in a STBY event (following the same pattern shown in Figure 4-6-b). Such a QUICK TRANSFER operation permits, through UDP, to produce data transfers with just two 8-bit I2C transactions, dramatically reducing the communication overhead.

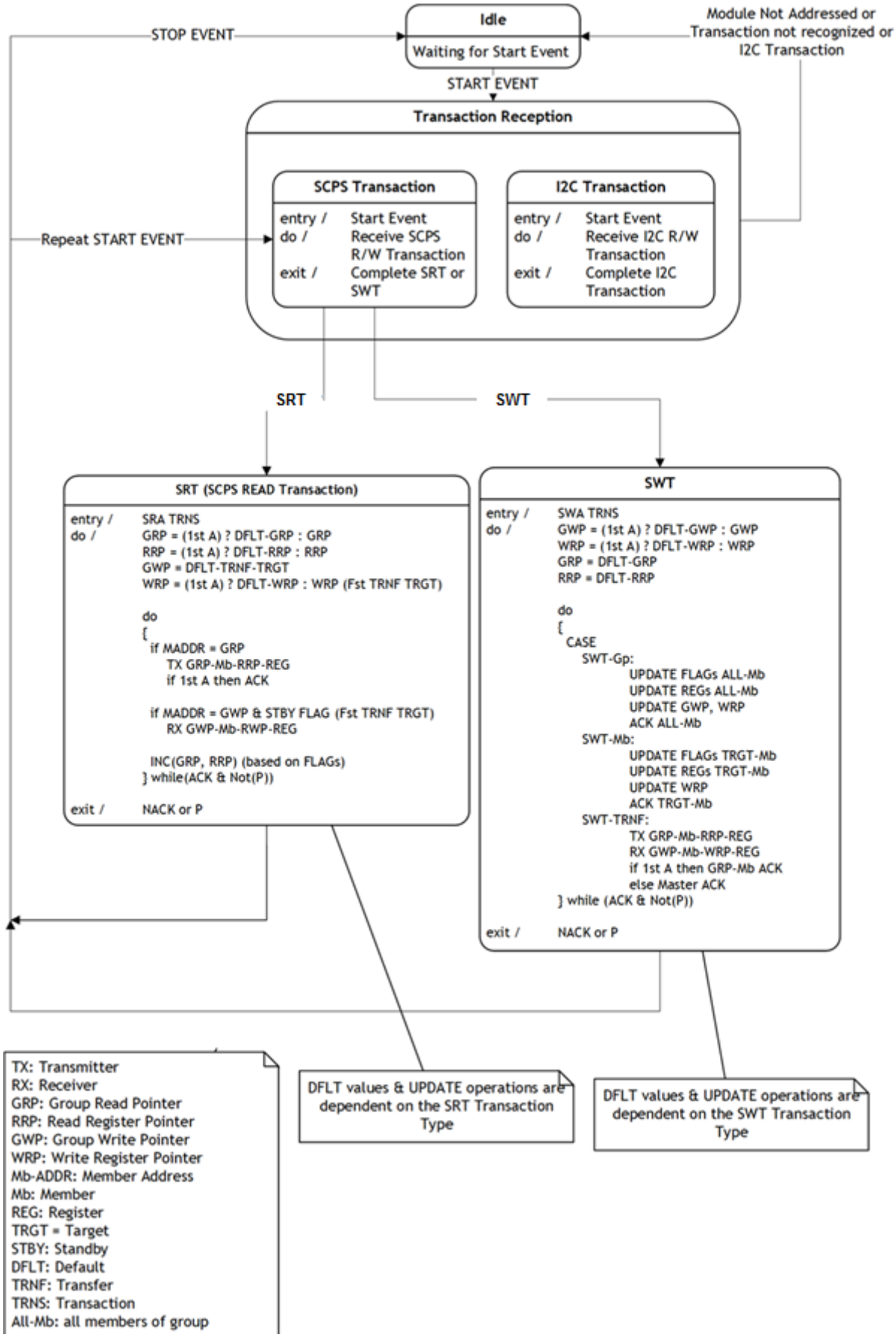


Figure 4-7 — SCPS transactions overview.

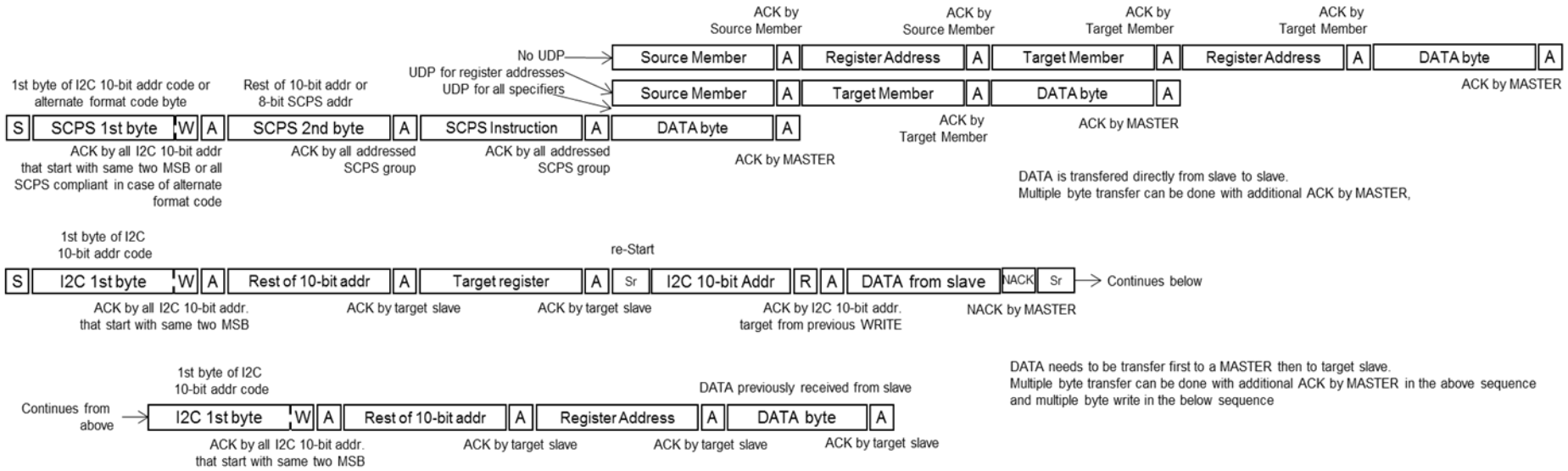


Figure 4-8 — SCPS TRANSFER operation overview

4.1.4 *Registers and Pointers*

The register and pointers represent a key aspect of the SCPS framework, since they denote the unifying cross-modular commonality, which permits inter-modular coordination without explicit synchronous management of the involved components. The specificities, in this respect, of the I2C based SCPS implementation can be summarized in a number of mandatory registers and pointers:

- **INSTRUCTION REGISTER or INSTR:** stores the last valid SWT entered instruction. The INSTR resets to 8H00 value as default, indication that no valid SCPS instruction has been received or a RESET action has been requested. This register is updated through SWT sequences and is internal to the module.
- **STATE REGISTER or STATE:** stores the current state of the instruction, definable through an optional user-defined state library (containing UDP) or through data bytes included within certain instructions. The general purpose of the STATE register is to serve as a control register that permits internal setting configuration of the instrument. The STATE is used by specific instructions to define the selected instrument "state" for a specific action. It is normally an internal register, however in the description of the RTL implementation it is exported as the SWMOD output of the module.
- **STATUS REGISTER or STATU:** is the default READ output register, i.e., when a SRT sequence is received by a group with no specification of the target register (allowed for certain instructions or if only a 2-byte SWT sequence is sent prior to set SRT). It is by default composed by a grouping of defined internal flags, which reflect the internal status of the SCPS module. Optionally, an alternative of the default STATUS register can instead be accessed (e.g., through a selectable pin). A representation of the default STATUS register can be seen below in Figure 4-9:

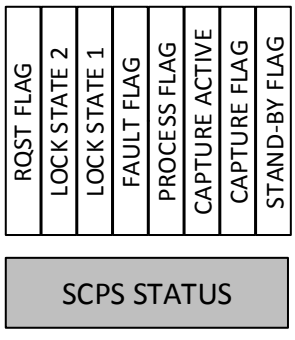


Figure 4-9 — STATUS register.

- **GROUP ADDRESS or GADDR:** the previously mentioned 10GA. This register contains the group address information of the module and can be dynamic (i.e. programmable). Additionally, there is no restriction imposed to the number of associated 10GA. The address 8H00 is reserved as a NULL address and cannot be assigned to any group.

- **MEMBER ADDRESS or MADDR:** this register contains the member address information of the module, i.e. the relative position of the module within the group, and as the GADDR, it can be dynamic. In the case of an instrument having multiple 10GA, it is left to the designer to provide the mechanism for proper associative MADDR to be selected. The address 8H00 is reserved as a NULL address and cannot be assigned to any module.
- **WRITE REGISTER POINTER or WRP:** stores the target register address to be written to. It can be updated through certain instructions and instructions' specifiers, or by extending a WRITE for certain instructions (i.e., as when an ACK and additional SCL pulses are sent after the first data write byte of an I2C write sequence). The value 8H00 is reserved as a NULL address and signifies that no action will occur to the pointer during this instruction sequence. The initial value of the pointer during a specific instruction is set by UDP, if none it should default to 8H00. All matters concerning increment and decrement of the pointer are to be addressed by the user through interaction with the SCPS register section.
- **READ REGISTER POINTER or RRP:** this register stores the target register address to be read from. Such register can be updated through the use of certain commands or extending a read sequence (i.e., as when acknowledgement and additional SCL pulses are sent after the first read byte of an I2C read sequence). The value 8H00 is reserved as a NULL address and signifies that no action will occur to the pointer during this instruction sequence. The initial value of the pointer during a specific instruction is set by UDP, if none it should default to 8H00. All matters concerning increment and decrement of the pointer are to be addressed by the user through interaction with the SCPS Register section.
- **GROUP WRITE POINTER or GWP:** this register stores the member address to be written to. The match of the GWP to the MADDR indicates the module that the DATA BYTE is to be stored at the WRP address. The update of the GWP is instruction specific and its initial value is dependent on the instruction and UDP. Certain instructions can auto increment the pointer in a style reflective of the I2C register pointer auto increment (left to the user within the I2C standard), which is used by most I2C complaint mechanism to simplify multiple read and write operations. The value 8H00 is reserved as a NULL address and signifies that no action will occur to the pointer during this instruction sequence. The response of the module for an 8H00 GWP is equivalent to a NO match scenario. The initial value of the pointer during a specific instruction is set by UDP, if none it should default to 8H00. All matters concerning increment and decrement of the pointer are to be addressed by the user through interaction with the SCPS register section.
- **GROUP READ POINTER or GRP:** this register stores the member address to be read from. The match of the GRP to the MADDR indicates the module's RRP register DATA

BYTE is to serve as an OUTPUT in the upcoming I2C READ sequence. Certain instructions can auto increment the pointer in a style reflective of the I2C register pointer auto increment (left to the user within the I2C standard), which is utilized by most I2C complaint mechanisms to simplify multiple read and write operations. The value 8H00 is reserved as a NULL address and signifies that no action will occur to the pointer during this instruction sequence. The behaviour of the module for an 8H00 GRP is equivalent to a NO match scenario. Such register can also be incremented by extending a read sequence (i.e., as when acknowledgement and additional SCL pulses are sent after the first read byte of an I2C read sequence); however, as within I2C the increment or decrement is left to the user.

- **(optional) TOKEN REGISTER or TKR:** stores the information of the associated resources that have been assigned to a specific module. The purpose is to use this register as a TOKEN space where each bit represents a specific TOKEN. In the case of only one shared resource (such as an analogue bus) then there is no need for the TKR since the RQST flag would suffice.
- **USER DEFINED REGISTERS or UDR:** refers to all registers associated to the instrument itself and therefore defined by the designer. Such registers include all instrument I2C accessible registers that have been defined by the user. If access through the SCPS module is intended by the user, then allocation within the SCPS registers is required, by providing addressable retrieval and update to its user defined location. Such UDR registers are by definition not standard thus remains the responsibility of the designer to establish the necessary hardware and flow if intended for cross-module actions.

4.1.5 *SCPS Write Transactions and SCPS Instructions*

The associated instructions, which are introduced through SWT, are divided in four categories: SETUP, CAPTURE, PROCESS, and SCAN[2]. Each instruction is followed by specific updates of the associated flags, registers and pointers, which are described in this instruction section. The SRT has specific responses depending on the current valid instruction (SWT introduced) as to permit a simplification of the transfer of data or STATUS report, depending on the scenario. Additional instructions can be introduced through the use of the SCPS instruction format that is not reserved. Such optional instructions should expect no response by the SCPS registers set, flags and other elements; although, they can be directly interpreted by the instrument upon examination of the I2C data in the register.

In all cases (SGT, SWT or SRT), the specific instrument response is not defined, and it is to be specified by the instrument designer based on the mandatory and optional flags, registers

[2] Such categories are so named because of the SCPS framework methodology, however they represent four distinct instruction types independently of the scheme utilized

and pointers. The standardized behavioural flow among SCPS compatible instruments permits tasks and event synchronization based on inter-module coordination. The instructions will be described based on the address type, be it global (from a GENERAL CALL), group or specific. It is also possible to select a specific member of a group for an isolated action, which is of use when the group members do not have an associated I2C 7-bit address. From this point on, such style of addressing will be referred to as member-specific addressing, which entails a subsection of the permissible instructions.

Within the presented SCPS implementation the SCPS instruction byte follows a defined format, as seen in Figure 4-10, where the four MSB are used for instruction type selection and the remaining four least significant bits (LSBs) for instruction specification and command selection.

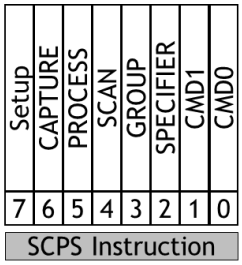


Figure 4-10 — SCPS instruction format.

Global Instructions

The global instruction set is meant for actions that affect all SCPS recipient modules (e.g., a RESET or initialization request), although specific instrument response is dependent on the particularities of their design; e.g., in the case of a RESET instruction, not all instruments are expected to follow an identical sequence for resetting their registers and internal elements (for instance, SCPS registers will reset based on specific UDPs). For the current implementation, some possible global requests are BYPASS and ISOLATE, referring to operation time transparency and module isolation from analogue buses respectively. The global instruction is introduced after a GENERAL CALL (all zeroes in the first byte, i.e., 8h00), and uses the software GENERAL CALL space by having the least significant bit set to 'zero'. In order to avoid conflict with I2C UM10204 established instructions, the most significant bit is set to 'one', as can be seen in Figure 4-11, where Figure 4-11 (a) presents a generic global instruction format, and Figure 4-11 (b) presents the implemented case specific format.

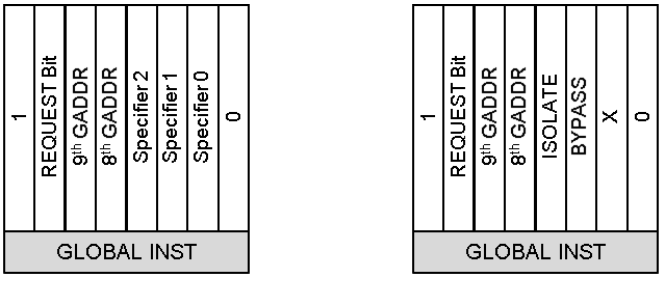


Figure 4-11 — Global instruction format: (a) Generic extended format. (b) Simplified implemented format.

The following is a summary table of instructions and their description:

Table 4-1. GLOBAL instructions summary.

Vector	Instruction Type	Description
10000000	SCPS General RESET	Indicates a SCPS general RESET.
10??XXX0	STATE Instruction	Modifies the STATE register as to permit a general action to take place such as a RESET, ISOLATION or BYPASS setup. The instruction clears the pointers and INSTR to 8H00, STATE is updated with the corresponding instruction associated UDP, which has the default of 8H00. The internal flags are cleared and all TOKEN flags are released, except for the GLOBAL flag which is set. All recipient SCPS modules ACK such instruction. Additional bytes can follow; however, will be ignored by the SCPS module (as to be used by user defined instruction extensions). In the present case only two such instructions were defined which where ISOLATE and BYPASS to be activated independently from each other (i.e., the 10??11?0 is considered to be an ignore instruction).
11XX???0	REQUEST Instruction	Differs from the previous instructions, since only members that have the associated TOKEN assigned to them produce an ACK, if no ACK is received the MASTER continues with a 2nd byte that contains the rest of the 10-bit group address. The group specified then sets its RQST flag and corresponding TKR. The purpose is for multiple groups to be able to coordinate the use of shared resources through availability verification.

Group and Member Specific Instructions

The group instruction set is meant for inter-module actions and for member specific actions as well. The instruction is introduced at the 3rd byte of a SWT, and follows the format previously presented in Figure 4-10. The four MSBs are reserved to indicate the instruction type, which is restricted to only one set ('1') bit at a time. Multiple ones (1's) in these four MSBs, of the instruction byte, are treated as a mal-form instruction and ignored by the SCPS Module. In such a case the GROUP flag would remain set as in the case of a two byte SWT, generally used to precede a SRT. The 4th LSB (GROUP bit) indicates, if set ("1"), that the instruction is a group wide instruction; if unset it signifies a member specific instruction, in which case the 4th byte contains the member address and any data byte after such would be associate to specifiers. The 3rd LSB is associated to a specifiers based instruction, indicating that the instruction will require an additional set of data bytes for its completion. An unset SPECIFIER bit would imply non-specifiers based instructions, which are related to pre-established strategies based on UDP, utilized from streamlining repetitive actions and avoiding long and complex instructions repetition. Any additional data byte after the INSTRUCTION byte for a non-specifiers instruction will be ignored by the SCPS module. The 1st two LSB of the INSTRUCTION byte are utilized for command identification (future revisions might consider an additional INSTRUCTION byte, in order to significantly extending the command domain). Follows a description of the group instruction set:

Setup Instruction Set

The setup instruction set or SIS, is reflective of operations intended to write or update the registers of the involved modules. Such can be achieved through the use of pre-established UDP or through direct WRITE of the registers. Additionally, a RELEASE and LOCK functions permit to control the manner in which an instrument responds to the SCPS instructions. In general, the involved modules acknowledge the INSTRUCTION byte; however in the case of member-specific instructions, only the target member will acknowledge its MADDR and specifiers. Table 4-2 summarizes the SIS, followed by a description of the different instructions. In the present implementation only the STATE1 and STATE2 cases where implemented with a BYPASS and ISOLATE state respectively.

Table 4-2. SETUP instruction summary.

INSTRUCTION BYTE 1000XXXX					
Group 10001XXX			Member 10000XXX		
Code	**Function**	**Parameters**	**Code**	**Function**	**Parameters**
000	RESET	N/A	000	RESET	N/A
001	STATE1	N/A	001	STATE1	N/A
010	STATE2	N/A	010	STATE2	N/A
011	STATE3	N/A	011	STATE3	N/A
100	WRITE	REG-ADDR	100	WRITE	REG-ADDR
101	reserved	reserved	101	reserved	reserved
110	LOCK	TYPE	110	LOCK	TYPE
111	RQST RELEASE	TOKEN	111	reserved	reserved

SIS Description:

- RESET: the RESET instruction clears the pointers, flags and restore registers to their default value (8H00 by default if no UDP). Only the GRP flag remains set as to permit a follow-up SRT.
- STATE: the STATE instruction updates the STATE register and the INSTR register, the only flags updated are the GROUP flag, identifying if it is a group or member specific targeted instruction. They are intended to serve for pre-establish setup access through UDP. In the present implementation only two states were implemented: BYPASS and ISOLATE.
- WRITE: these instructions are used for direct register writing through the use of the register address as a specifier; in the same manner one would write to an I2C associated register (which is the case for instruction 8b10000100). In the case of a GROUP instruction, the difference lays in that multiple modules update simultaneously. The strategy for auto increment or decrement of the register address

(in a manner consistent with most I2C compliant devices) is left to the designer as stated previously (keeping in accordance to the I2C UM10204).

- LOCK: permits the change of the LOCK level of the module (information stored in the LOCK flags). The LOCK levels are thought for access and functionality limitation of the group or module, such in case of detected fault or malfunction of the module. The LOCK levels are defined has follows:
  - LOCK level 0: no limitation.
  - LOCK level 1: minimal level LOCK, i.e., thought for minimal functional limitation. For example, member participates in group sequences; however the SCPS handler remains in BYPASS mode.
  - LOCK level 2: mid-level LOCK, i.e., thought for detected associated element FAULT. The SCPS functionality is mostly suspended. For example, the CAPTURE and PROCESS instructions are suspended and the module remains in BYPASS mode, however still accepts SETUP and SCAN instructions.
  - LOCK level 3: full level LOCK, i.e., no SCPS functionality, only valid sequences are STATUS READ, RESET or RELEASE commands (GLOBAL, GROUP or member specific).
- RQST RELEASE: permits the release of a specific shared resource, through the clearing of the group holder TOKEN bits and RQST flag, which is also achievable through the use of a GLOBAL RESET or STATE.

Capture Instruction Set

The capture instruction set, or CIS, is reflective of operations intended to synchronize inter-module actions that show functional dependency among them; e.g., synchronized measurements from multiple modules or a measurement that requires multiple modules to participate. This can be done through the use of pre-established UDP dependent STATES or through “on-the-fly” setups through the use of specifiers. The instructions are sub-divided into two types: stand-by or STBY and capture or CAPT. Depending on the module, and the instrument response, the two instruction could serve identical functions, they differ mainly in the flag setting and in their conceptual purpose. The STBY instruction is meant for actions that require a waiting period, e.g., a settling period for a stimulus, as to permit a proper measurement. The CAPT instruction is meant to indicate the start of a measurement or test (possible following a STBY). Additionally, an END-CAPT instruction has been included to signal the end of a capture event, useful in cases where the capture event is not instantaneous and requires an intentional interrupt of the process. The involved modules acknowledge the INSTRUCTION byte; however in the case of member-specific instructions, only the target member will acknowledge its MADDR and specifiers. The clearing of the STBY and CAPT related flags only occur after an END-CAPT or a RESET style instruction (allows for setup, process and scan actions in parallel). Table 4-3 summarizes the CIS, and their specific description follows.

Table 4-3. CAPTURE instruction overview.

INSTRUCTION BYTE 0100XXXX					
Group 01001XXX			Member 01000XXX		
Code	**Function**	**Parameters**	**Code**	**Function**	**Parameters**
000	STBY-Dflt	N/A	**000**	STBY-Dflt	N/A
001	Nxt - STBY	N/A	**011**	Nxt - STBY	N/A
010	CAPT-D	N/A	**001**	CAPT-D	N/A
011	END-CAPT	N/A	**010**	END-CAPT	N/A
100	STBY-P	STBY-Specifier	**100**	STBY-P	STBY-Specifier
101	STBY-S	Mb + PRMT + …	**111**	reserved	reserved
110	CAPT-P	CAPT-Specifier	**101**	CAPT-P	CAPT-Specifier
111	CAPT-S	Mb + PRMT + …	**110**	reserved	reserved

Mb: member; PRMT: parameter; STBY: stand-by; Dflt: default; Nxt: next; CAPT: capture

CIS description:

- **STBY:** this instruction has several versions; including a version that requires no specifier and utilizes default UDP based information (as to minimize the need for setup for repetitive actions). The Nxt-STBY updates the STATE register and permits access to sequential STBY setups (e.g., for modifying the routing of a sensor array as to permit sequential measurements of its elements or performing a multiple steps measurement as in the case of a frequency sweep). With regards to specifiers the STBY-P permits direct access to a specific pre-arranged STBY setup, while the STBY-S allows to send "on-the-fly" setup parameters to a list of members. The STBY-S instruction differs from the regular instruction format in that it has no pre-established length, and only the pertinent member will acknowledge after its MADDR and the next DATA byte. That is to say, all members read the incoming DATA bytes in groups of two, the 1st byte representing the MADDR, and the 2nd byte the specifier.
- **CAPT:** the instruction has several versions, including a version that requires no specifier and assumes the setup has been previously established through a STBY instruction. It is also possible to use the CAPT-D instruction without a previous STBY in cases where no setup is required. As previously described, the END-CAPT permits to end the capture action. Similar to the STBY-P and STBY-S, the CAPT-P and CAPT-S permit "on-the-fly" setup and capture, the different being on the CAPT flags being set as to indicate the start of the capture action instead of the STBY flag.

Process Instruction Set

The process instruction set, or PrIS, is reflective of operations intended to synchronize inter-module actions that have no direct inter-module dependency, e.g., synchronized internal module operations for multiple modules or the processing of a FAULT status by the

involved modules (as to permit the overall FAULT status of a group).This can be done through the use of pre-established UDP dependent STATES or through the use of specifiers, both at a group level or member-specific. Although not strictly forbidden, the process instructions are meant to follow a successful capture as to properly update the FAULT flags; however, no restriction is made of the instruction sequence usage since work flow flexibility is a key aspect. Table 4-4 summarizes the process instructions set, and their specific description follows.

Table 4-4. PROCESS instruction overview.

INSTRUCTION BYTE 0010XXXX					
Group 00101XXX			Member 00100XXX		
Code	Funct.	Parameters	Code	Funct.	Parameters
000	**PSET**	N/A	**000**	**PSET**	N/A
001	**PSET1**	N/A	**001**	**PSET1**	N/A
010	**PSET2**	N/A	**010**	**PSET2**	N/A
011	**PSET3**	N/A	**011**	**PSET3**	N/A
100	**PSET**	Target TEST (TT)	**100**	PSET	Target TEST (TT)
101	**PSET**	TT + Spec A	**101**	PSET	TT + Spec A
110	**PSET**	TT + Spec B	**110**	PSET	TT + Spec B
111	**PSET**	TT + Spec A +Spec B	**111**	PSET	TT + Spec A + Spec B

PrIS Descriptions:

- **PSET:** the instruction has several versions, both with and without specifiers, and at group and member-specific level. It is similar to CAPT in behaviour, although updating the FAULT and PROC flags instead of the CAPT flags. The FAULT flags are directly updated by the instrument and are intended to serve as a FAULT status indicator, however the details and usage are left to the instrument designer. Additionally, the PrIS does not update the STATE register, thus a capture and process operation could take place in parallel. In case that the FAULT flags or the internal FAULT state determination of the instrument requires an action affecting the "state" of the module, the designer could force a STATE register bypass to a response specific UDP, outside of the SCPS interpreter (within the instrument itself or by intercepting the SCPS interpreter to SCPS handler path). The PSET (code 000) instruction activates the process action with the last parameters utilized, while the PSET# instructions utilize UDP for pre-established process action setups. The Spec-A, Spec-B and Spec-C referred to in the table, stand for a generic specifier that serve as a parameter to the process action. The combination in the different PSET versions allow to enter a number of varying parameters for different scenarios, e.g., selecting different operations, thresholds, ranges, etc. It should be mentioned that process

action can be made STATE aware, as well as utilize the SCPS flags for initiating process actions only on the modules of interest, e.g., updating the FAULT status of the module that is a test target while in a STBY process.

Scan Instruction Set

The scan instruction set, or ScIS, is reflective of operations intended to read or transfer (read from and write to) registers of the involved modules. This can be done through the use of pre-established UDP or the use of specifiers. The involved modules acknowledge the INSTRUCTION byte; however in the case of member-specific instructions, only the target member will acknowledge its MADDR and specifiers. Table 4-5 summarizes the ScIS, and their specific description follows.

Table 4-5. SCAN instruction overview.

INSTRUCTION BYTE 0001XXX					
Group 00011XX			Member 00010XX		
Code	Function	Parameters	Code	Function	Parameters
000	READ1	N/A	**000**	READ1	N/A
001	READ2	N/A	**001**	READ2	N/A
010	TRNF1	N/A	**010**	READ3	N/A
011	TRNF2	N/A	**011**	READ4	N/A
100	READ	REG-ADDR	**100**	READ	REG-ADDR
101			**101**		
110	TRNF	TX-Mb + RX-Mb	**110**		
111	TRNF	TX-Mb + REG-ADDR + RX-Mb + REG-ADDR	**111**		

TRNF: transfer; REG: register; ADDR: address; TX: transmitter; RX: receiver.

ScIS Description:

- READ: the read instruction allows for a register to be read from multiple modules or a member-specific module through the I2C bus. It differs from conventional I2C strategies which simplifies the read operation through the R/W bit in the 1st byte of the transaction, allowing for register selection through the last write operation. In this case, the variation permits the chain read from multiple modules, significantly reducing the transaction bytes since no back and forth read and write instructions must be performed. This is achieved by using the pointers to determine the target module and target register to be read from; however, instead of the increment or decrement altering the target register as in conventional I2C strategies here the target module can be updated permitting a READ instruction to contain chained information from multiple modules. The READ# allow the use of UDP for reading pre-established registers and even changing the module read order, since the increment

or decrement of the modules is left to the designer. The READ instruction with specifiers allows for selecting the target register to be read from. For the present implementation only the READ1 and TRNF1 instructions were instantiated.

- TRNF: the transfer instruction allows for a register to be read from a module and written from a different module (depending on the UDP). It differs from conventional I2C strategies which only consider master-slave operations and not slave-to-slave data transfers. As with the READ#, the TRNF# allows for pre-established transfers. The specifier variation allows choosing the source and destiny modules (assuming default or UDP established registers for the code 110 and through direct register address specification for the code 111). During a transfer the 9-bit ACK is controlled by the Master in order to avoid the RX and TX modules to ACK themselves, thus impeding a Re-Start of Stop event and locking the I2C bus.

4.1.6 *SCSP Read Transactions*

The SRT transactions by default read the STATUS register from the modules in a group, in the order determined by the UDP; however, the update of the pointers is left to the designer (as stated previously) so information from the SCPS flags and STATE register can be used to permit user-defined reads, which are referred to as “quick-reads”. This is permitted deliberatively and can be extended to transfer operations as well (the write pointers need not to be set to 8H00 upon the start of a SRT, although it is a default value), which are referred to as “quick-transfers”. An example of a useful “fast-transfer” is when a module is responsible for the digitalization of a measurement (contains an ADC for instance), however the data needs to be allocated on a different module (the target of the measurement for instance), in this manner a “quick-transfer” permits to hold the elements in a STBY, transfer the data and continue with a different measurement (through a STBY-NEXT or CAPT instruction). The before-mentioned fast-transfer was implemented within the presented proof-of-concept, and is activated through a SRT after a STBY-NEXT state.

Figure 4-12 presents and overview of the SRT, one can differentiate five distinct paths: No previous SWT, (1) STATUS check operation, (2) READ operation, (3) STBY READ operation, (4) CAPT READ operation. As the before mentioned figure illustrates, the absence of a previous SWT would leave the SCPS compliant modules (or the I2C modules for that matter) without enough information to determine the target of the READ operation, thus it is ignored.

As indicated, presence of specific flags differentiate the path taken by the modules, where if group selection is present, (through a 2-byte SWT or a different operation not CAPT or STBY related), a group STATUS check operation activates, where the members of the target group transmit their STATUS in an order established by the UDP. Whenever a READ instruction is specifically sent to a group, the associate action to such instruction carries priority over other READ paths, including in the presence of STBY and CAPT flags (referring to quick reads and transfers).

The STBY and CAPT flags are utilized by the SRT to facilitate the data exchange process during a measurement. In the case of a STBY, the modules can assume the need to perform a “quick-transfer” of a previous measurement to the target module. In contrast, during a CAPT, a Master modules might want to inquire on the status of the capture process itself (if it has ended or not), and the specific order for a STATUS check, might be dependent of the specific STBY setting.

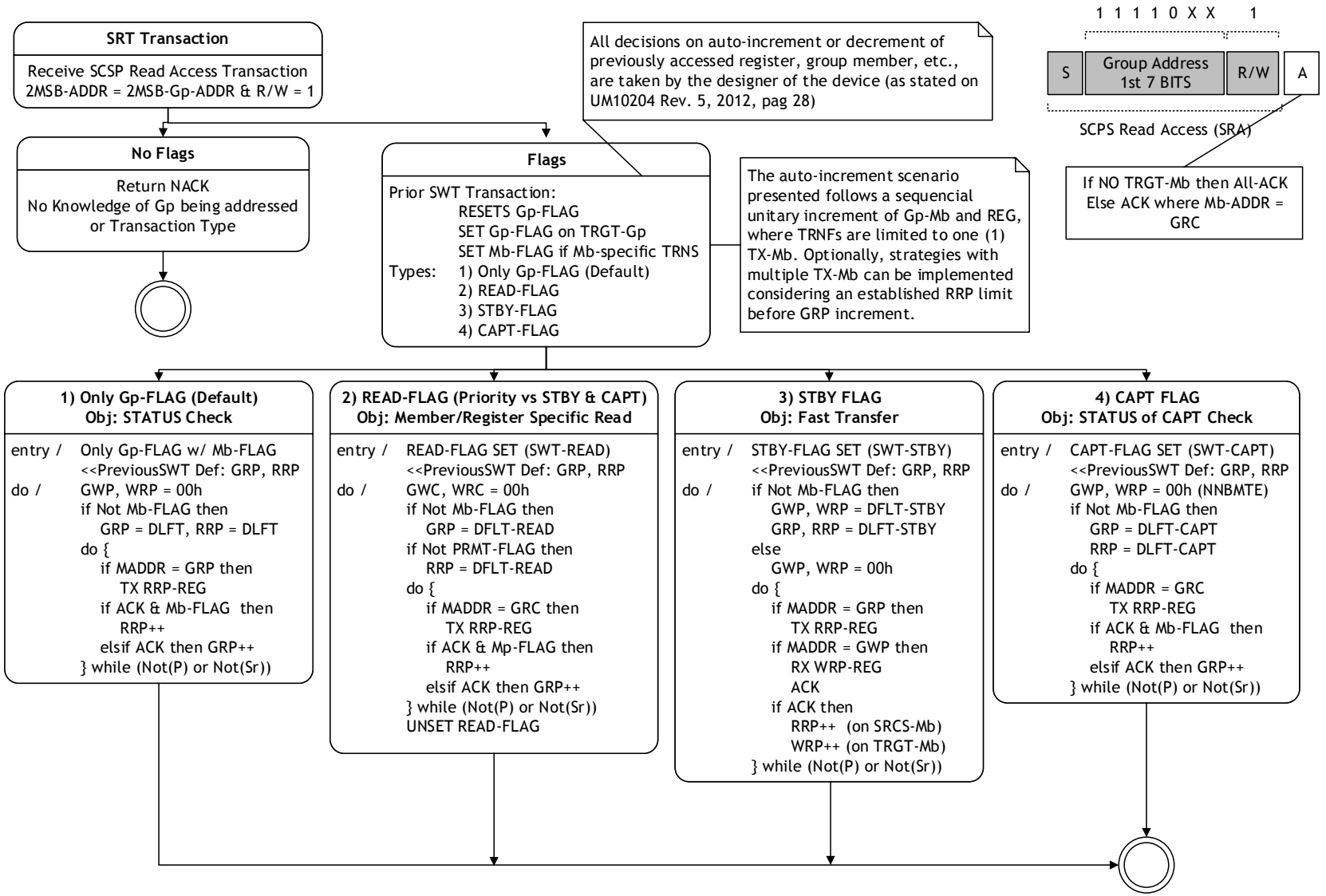


Figure 4-12 — SRT Transaction overview.

4.1.7 *RTL Representation and Simulation*

The proof-of-concept was instantiated following a modular approach through extension of the I2C core described in the previous chapter. The design was rule checked, synthesized and simulated using Xilinx's ISE and associated ISIM 14.7 (application version P.20131013), a front-to-back FPGA design solution and Verilog simulator. Besides complete verification of all instructions and associated actions, a number of sequences were property checked in order to insure proper functional behaviour of the modules. Follows the module block representation of the implementation and some sample simulations scenarios.

Figure 4-13 shows the top-level module block of the resulting SCPS proof-of-concept compilation. The main signals are the ***ext_scl*** and ***ext_sda*** which connect to the I2C external bus. Additional signals of interest are the ***swmod***, which carries the switching module state information, in order to connect through a PMOD port (Digilent Inc.) to the corresponding switching module structure. The remaining signals connect with the on-board Cypress EZ-USB FX2LP, a single-chip USB 2.0 peripheral, and other board related elements utilized for debugging purposes, such as switches, LEDs and reset button.

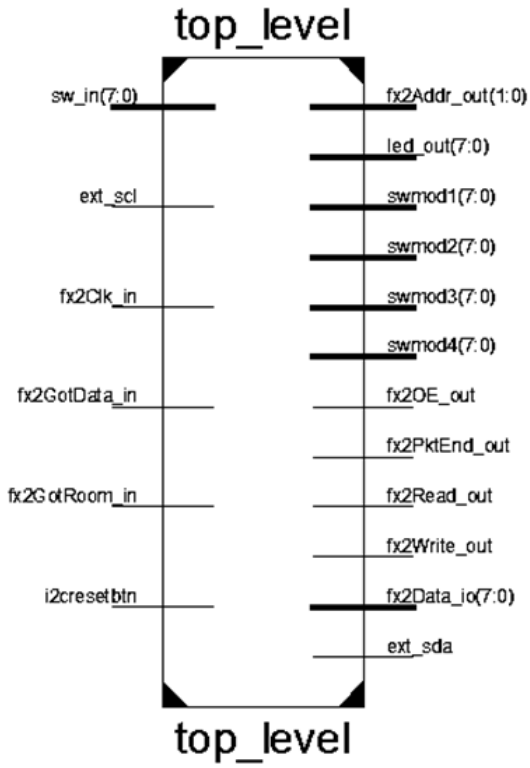
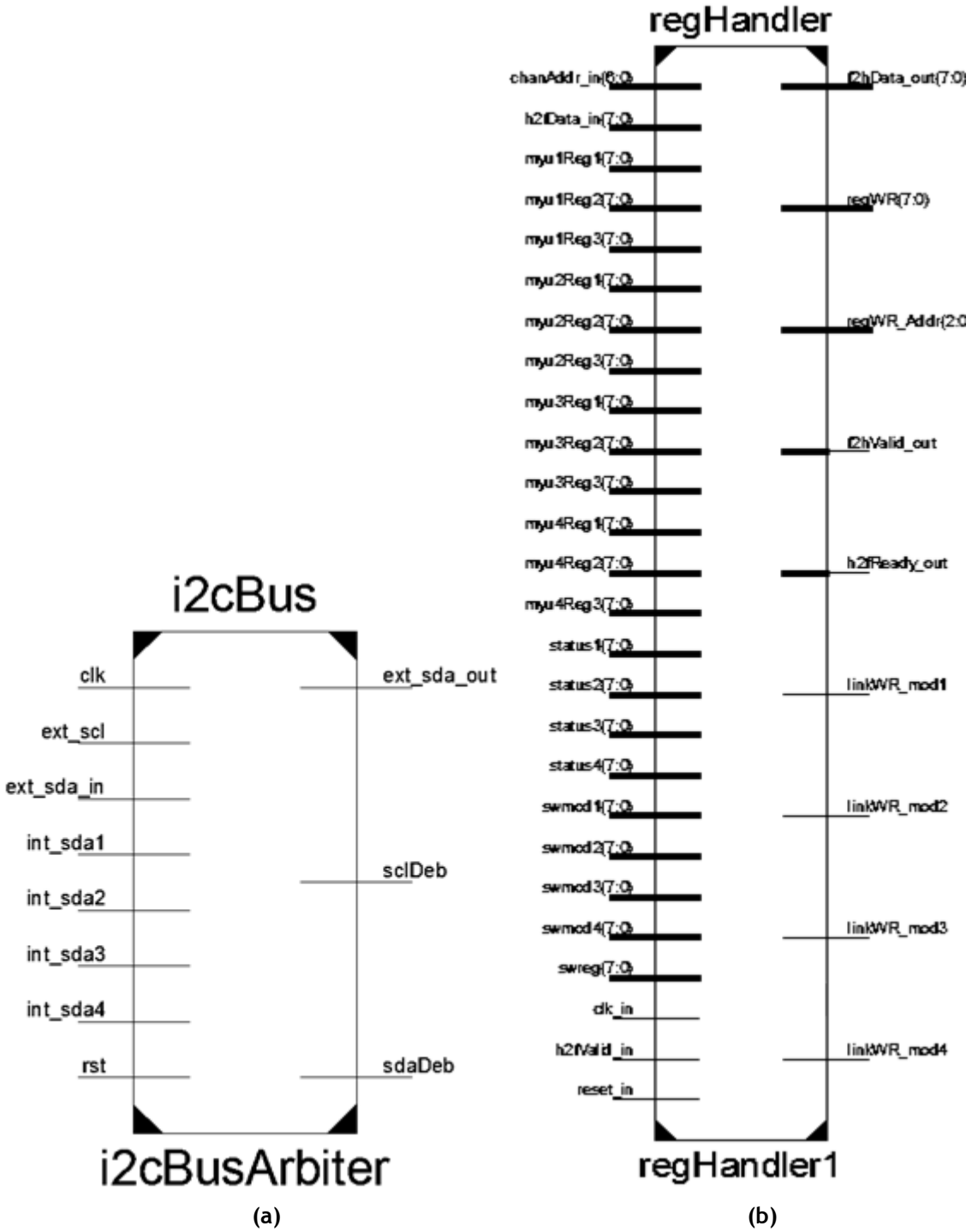


Figure 4-13 — Module block of top level implementation.

Figure 4-14 (a) presents the module block of the I2C bus arbiter module which debounces the incoming SCL and SDA signals and controls the state of the SCL and SDA signals internal to the FPGA. In Figure 4-14 (b), the Global Register Bank is represented by the Register Handler module, which manages access to the registers of the SCPS compliant modules, by the Cypress FX2 communication module. The Register Handler module also generates the appropriate signals for writing to the internal registers of the I2C slave modules. These

utilitarian modules provide a support role in order to manage the FPGA emulation of the SCPS proof-of-concept environment. Additional to the I2C bus arbiter and Register Handler module, a Communication FPGA to/from FX2 module (comm_fpga_fx2) and Button Debouncer module (btdebounce) were also included, used for communicating with the Global Register Bank through the USB port and debouncing the reset button, respectively.



(a) **(b)**

Figure 4-14 — (a) Module block of the I2C bus arbiter. (b) Module block of the register handler or global register bank.

Figure 4-15 presents the SCPS compliant I2C slave module. Noteworthy, is the presence of two SDA related signals. Since no clock stretching or SCL slave based control of the SCL is

implemented (referring to I2C optional features) in the present setup, the SCL line is solely an input oriented line. The SDA however is a bidirectional signal, and it is handled internally by the FPGA through the I2C Bus Arbiter module. Thus, ***sda_out*** is the generated SDA signal from the module (towards the I2C Bus Arbiter module), while ***sda*** and ***scl*** are input signals to the module. The signals ***regWR***, ***regWR_Addr*** and ***linkWR*** serve for writing to the module's register through the USB accessed Global Register Bank (represented by the Register Handler module). The output bytes ***regStatus*** (which provides the ***STATUS*** register output) and ***myReg[1,2,3]*** (internal configurable registers of the module) normally would not be present and remain internal to the module, accessible only through I2C, however they are present as outputs in order to preserve good coding style practices as they are utilized by the Register Handler module.

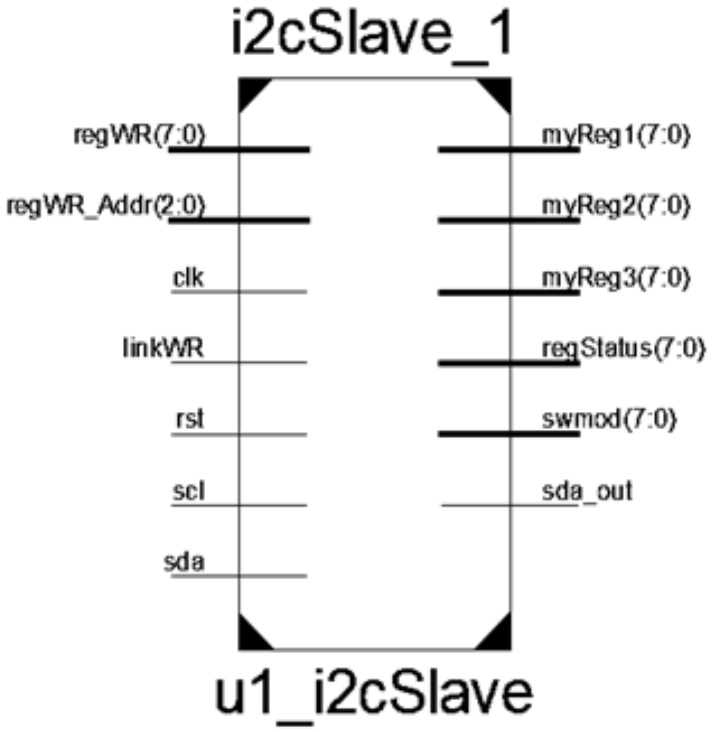
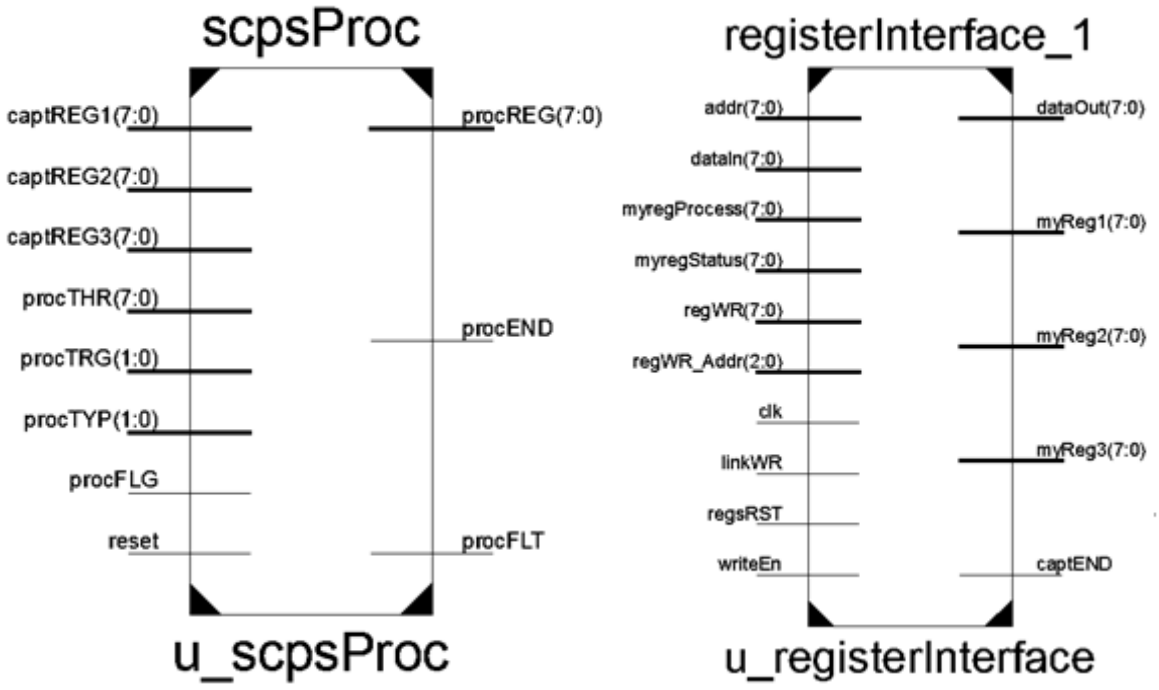


Figure 4-15 — Module block of I2C slave component.

The I2C slave module is itself subdivided in three sub-modules: the Register Interface, the Serial Interface and the SCPS Processing sub-modules. The Register Interface module handles internal registers access, while the SCPS Processing sub-module serves the role of the fault state decision making section, both seen in Figure 4-16 (a) and (b) respectively. For the present implementation, the SCPS Processing sub-module is based on threshold comparison. The threshold is provided through the ***procTHR*** input, while the ***procTYP*** input determines the comparison operation (greater than, less than, different from, equal to) and the ***procTRG*** input specifies the ***captREG*** target to be considered for comparison. The ***procREG*** output provides the results with additional setup information, while the *procEND* and ***procFLT*** outputs serve as flags (possible interrupts) indicating the processing stage completion (in this

particular case the processing takes place in one clock due to simplicity, however the ***procEND*** flag was instantiated as to indicate the possibly asynchronous nature of the operation) and fault detection respectively.



(a) **(b)**

Figure 4-16 — (a) Module block of the SCPSp sub-module. (b) Module block of the register interface sub-module.

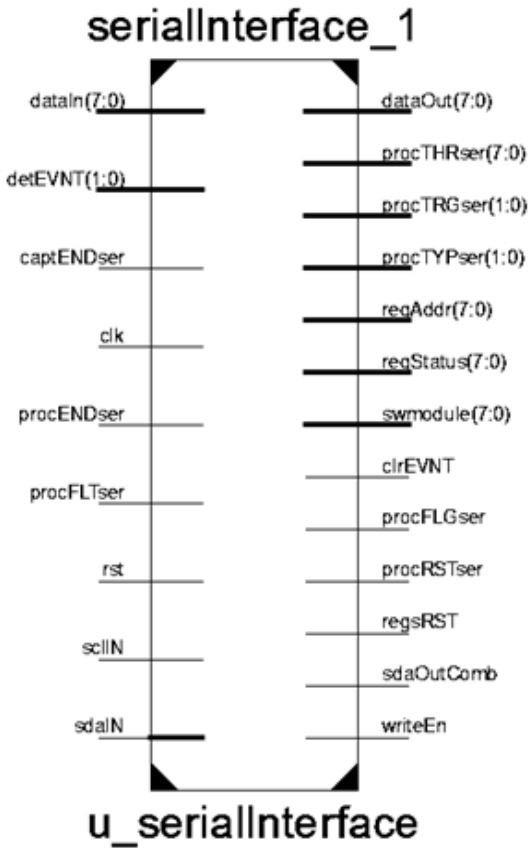


Figure 4-17 — Module block of the serial interface sub-module.

The Serial Interface sub-module presented in Figure 4-17 serves as the main operation section of the I2C interpreter, and follows the finite state machine presented in the previous chapter (Subsection 3.2.3, Figure 3-17, Figure 3-18 and Figure 3-19). The sub-module was modified in order to pass the appropriate signals to/from the SCPS Processing sub-module, interfacing with the Register Interface and addition of the internal sub-module, the SCPS handler.

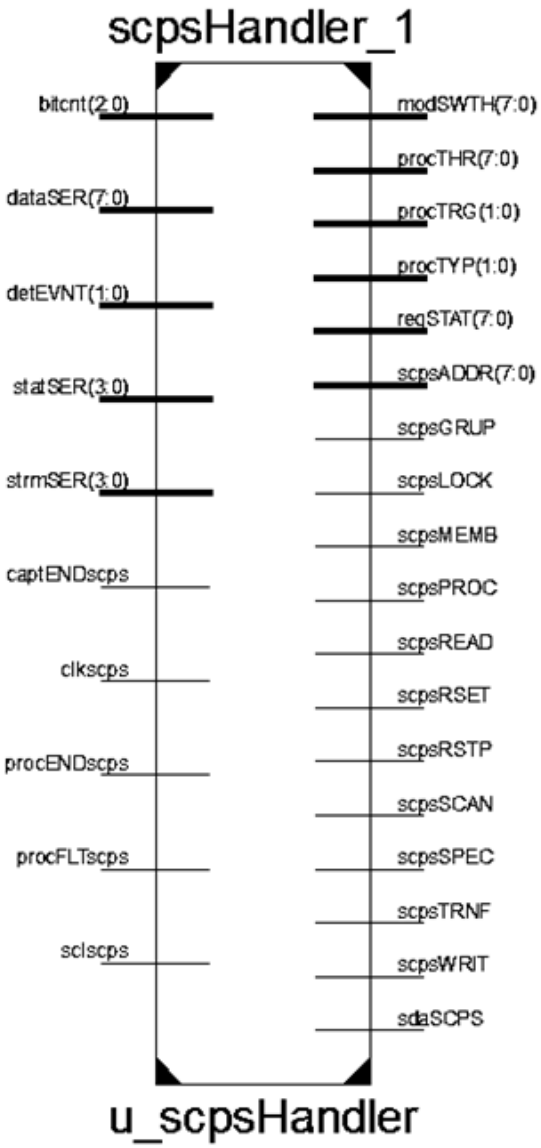


Figure 4-18 — Module block of the SCPS handler sub-module.

Figure 4-18 presents the module block of the SCPS Handler, the main SCPS section which incorporates the SCPS interpreter and SCPS handler sections. The SCPS Handler sub-module generates the appropriate flags and registers based on the command type and associated provided specifiers. A more in depth explanation of the register and pointer structure, command structure, flow and associate specifiers can be found in Section 4.1.5.

The before-mentioned modules were verifies for behavioural syntax, synthesized and implemented with no errors or warnings of relevance. All functions and features of the SCPS

and I2C aspects were verified through functional simulations and implementation verification, some of which follow with discussion. The conceptual overview of the implemented aspects can be found in the preceding sections, providing a more in-depth understanding of the following simulations, the command sequences and format.

Figure 4-19 presents the waveforms for several I2C General Call commands. Each general command, in this example, is compose by two groups of 9-bits (8-bits for data/address/command and 1-bit for ACK), where the first group (8H00) complies with the I2C standard and indicates a GENERAL CALL, while the second is used as a SCPS general command (all SCPS general commands start with a 1 in the MSB as to differentiate them from possible I2C general commands).The leftmost blue marker delimits an I2C general call with a "RESET and write programmable part of slave address by hardware" (8H00 followed by 8H06, in this case no writing follows the RESET for this I2C operation); one can observe how all the I2C slave modules respond to this command through the acknowledgement (ACK) on their int_sda[1,2,3,4] signals (the internal response of each module on the SDA line); furthermore, the swmod[1,2,3,4] signals modify their content to match the requested RESET operation. The blue markers delimit a general SCPS ISOLATE operation (8H00 followed by 8H88), while the following black marker delimits a general SCPS BYPASS operation (8H00 followed by 8H84). The sequence ends with an SCPS RESET command (8H00, 8H80).

Figure 4-20 showcases SCPS group operations, such as a predefined TRANSFER operation and a group READ operation with specifiers; within this scenario the I2C slave 1, SCPS1, is not a member of the group being accessed. The SCPS group commands are introduced by sending the 10-bit address of the group (i.e., 10H008 in this example) in the first two bytes (which translate to 8HF0, 8H08 based on the I2C standard) and then the SCPS command in the third byte (i.e., 8H19 for a group TRANSFER pre-settings 1 with no specifiers) where the group bit (4^{th} LSB) is set, indicating a group operation. In this scenario the pre-defined parameters assigned member 1 of the group (i.e. module SCPS2) the task to transmit the 2^{nd} register of its register bank, concurrently member 2 of the group (i.e. module SCPS3) is assigned as a receiver and stores the transmitted data within the 1^{st} register allocation of its register bank; the blue markers indicate the change in the internal register of module SCPS3. It should be noted that an auto-increment of one is applied, thus an ACK to the transmitted byte causes a second byte to be read from module SCPS2 and written to module SCPS3. During a transfer operation any ACK must be performed by the instruction master, avoiding never-ending loops (such as in the case of the receiving module always ACK the transfer). The group READ operation with specifiers (8HF0, 8H08, 8H1C, 8H02) can be seen on the right side of Figure 4-20, where four sets of 9-bit SCL clocks take place (first two for group address, third for command and fourth for specifiers). The response of each individual member to the group READ commands can be seen on the right side, where each member transmits their second register (since the specifier was 8H02) in a predetermined order (in this scenario the order follows from member 1, SCPS2, to member 3, SCPS4).

Figure 4-21 shows a SCPS TRANSFER operation with two specifiers type 3 (8HF0, 8H08, 8H1F), which differs from the previous scenario given that the command sequence includes additional information, i.e., the target and source members and registers. In this sequence the specifiers indicate a TRANSFER from the second member's (SCPS3) fourth register to the first member's (SCPS2) second register (i.e., 8HF0, 8H08, 8H1F, 8H02, 8H04, 8H01, 8H02). The black and blue markers towards the middle of the figure, mark the register update within the SCPS2. At the rightmost side one can observe a SCPS member specific WRITE (8HF0, 8H08, 8H84). Although it addresses the entire group only one member acts upon the instruction (as can be seen by SCPS2's ACK towards the right side of the waveform). In this case the fourth byte is the member address (8H01) and following bytes represent specifiers (8H01 in this case as well, indicating first register). The sixth byte (8H0F) represents the value that is to be written to the first register of the first member of the group with address 10H008 (as can be seen at the rightmost side of the figure).

Figure 4-22 presents a more complex scenario involving a CAPTURE sequence with captured data TRANSFER during the operation. The leftmost marker delimits a general call SCPS token request (8H00, 8HC0, 8H08). The SCPS command byte (i.e. the second byte) was not acknowledged (i.e. an ACK response was not received in the 9th bit of the I2C sequence), therefore the token is considered available and a third byte with the remaining group address bits is provided. The members of the corresponding group ACK (i.e. acknowledge by asserting the SDA line during the 9th bit of the I2C sequence) the third byte and update their STATUS register with the token bit set. Follows a group STBY default command (8HF0, 8H08, 8H48) trailed by a group CAPTURE direct command (8HF0, 8H08, 8H4C). The centre black marker and the next right side blue marker delimit the period awaiting for the capture to take place, indicated by the STATUS register of SCPS2 updating the capture flags. Only the modules that are performing a CAPTURE operation update their flag STATUS, however a SCPS READ Transaction (SRT) during a CAPTURE command initiates the transmission of the member's STATUS, such data can thus be utilized for cross-module remote referencing of the CAPTURE status (i.e. a SRT during CAPTURE can alert all modules in a group of the current state of the operation through inspection of the member's STATUS). The following command is a STBY-NEXT (8HF0, 8H08, 8H49) which sets the modules to the next CAPTURE settings, while a SRT permits a "quick" TRANSFER of data based on UDP (i.e., from SCPS2 to SCPS3 in this scenario). The sequence ends with a CAPT-END command (8HF0, 8H08, 8H4B) which releases the token and leaves the modules in a predetermined state.

Figure 4-23 starts with a general SCPS token request (8H00, 8HC0, 8H08), followed by a STBY default (8HF0, 8H08, 8H48) and CAPTURE direct (8HF0, 8H08, 8H4C) as before. However, after the CAPTURE command a SRT (8HF1) is sent, a sequential READ of the group members STATUS register is performed (as can be seen between the two rightmost blue markers). After the READ a CAPTURE is completed by the SCPS2 (reflected by the update of

its STATUS and one of its writable registers. A second SRT is performed, which reflects now the change in STATUS by module SCPS2.

Figure 4-24 presents a similar sequence, with a TOKEN request, STBY default, CAPTURE direct, STBY next and “quick” TRANSFER, followed by a CAPTURE end. One notes similar behaviours as with the prior sequence, however at the end of the sequence a member specific PROCESS with two specifiers is sent. The before mentioned command (8H26, 8H02, 8H01, 8HF0) intends for the second module (SCPS3) to perform a type 1 processing (is register lesser than threshold) of the default register against the threshold 8HF0. In this scenario the register compared, 8HCC, is actually less than 8HF0, which causes a FAULT to occur and default LOCK conditions to be active. Figure 4-25 provides a close-up of the before mentioned actions caused by the PROCESS instruction.

These examples sequences are meant to provide insight into the flow of the SCPS I2C implementation, and of the different elements which participate in the process.

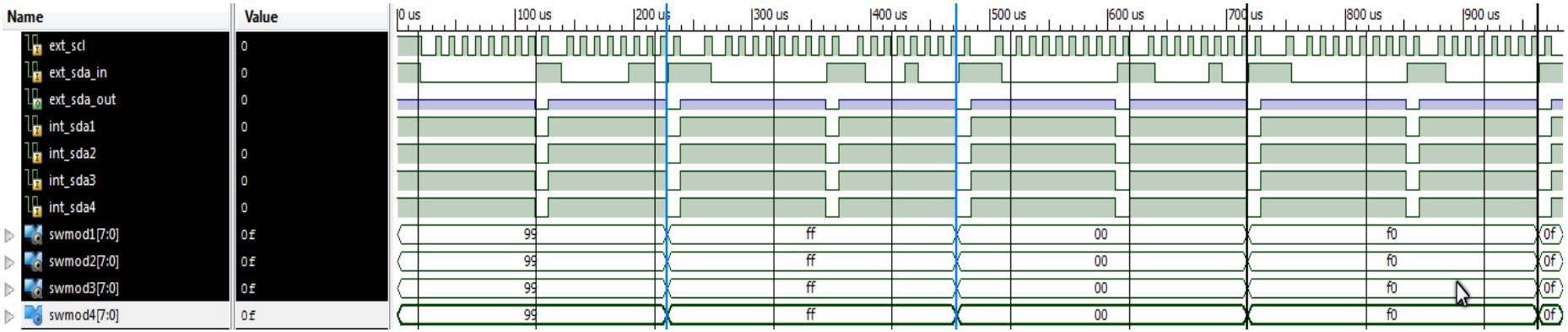


Figure 4-19 — Functional simulation of I2C general calls followed by a SCPS general RESET, ISOLATE and BYPASS command.

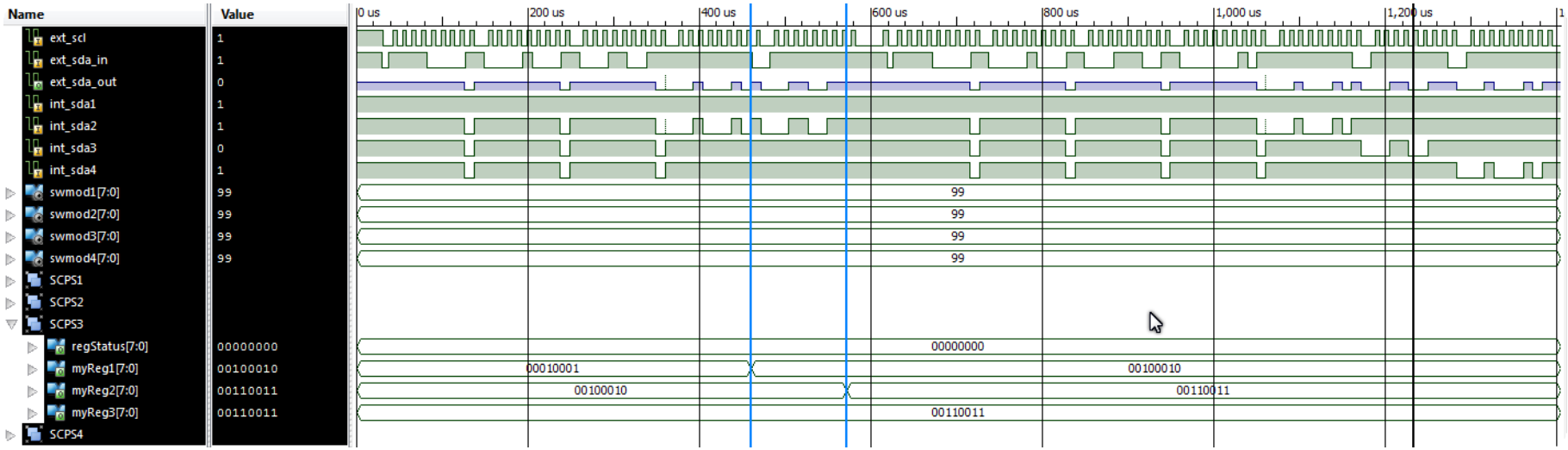


Figure 4-20 — Functional simulation of a SCPS transfer operation and group READ with specifier.

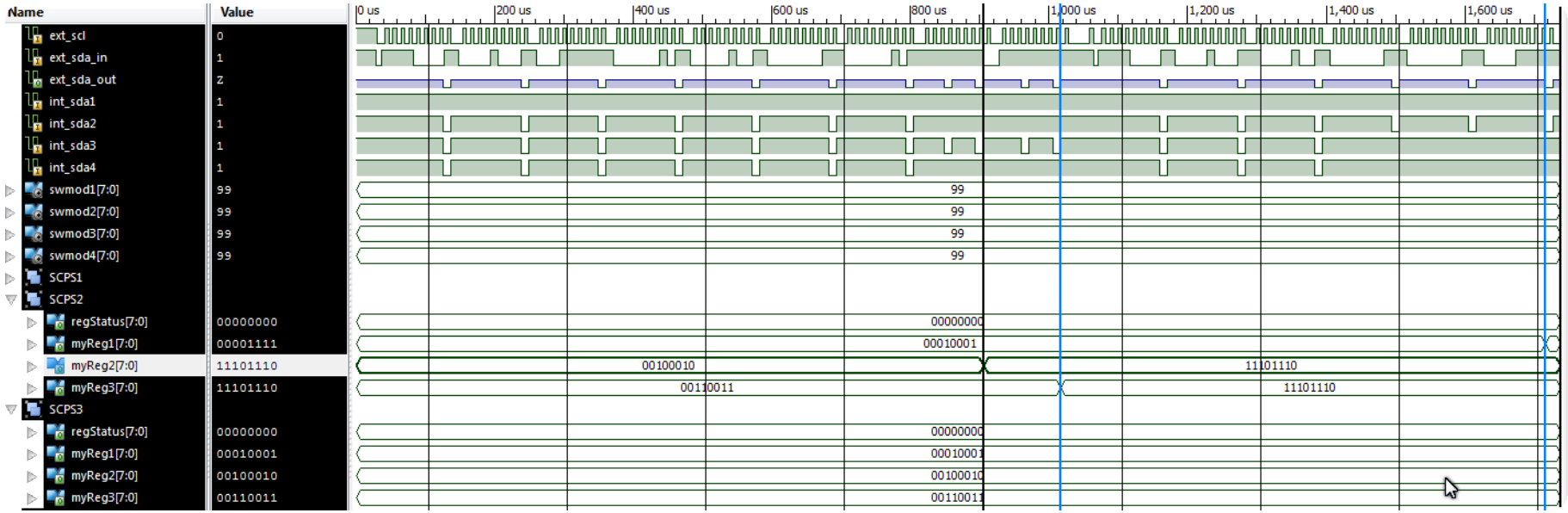


Figure 4-21 — Functional simulation of a SCPS transfer with specifiers and SCPS member specific WRITE.

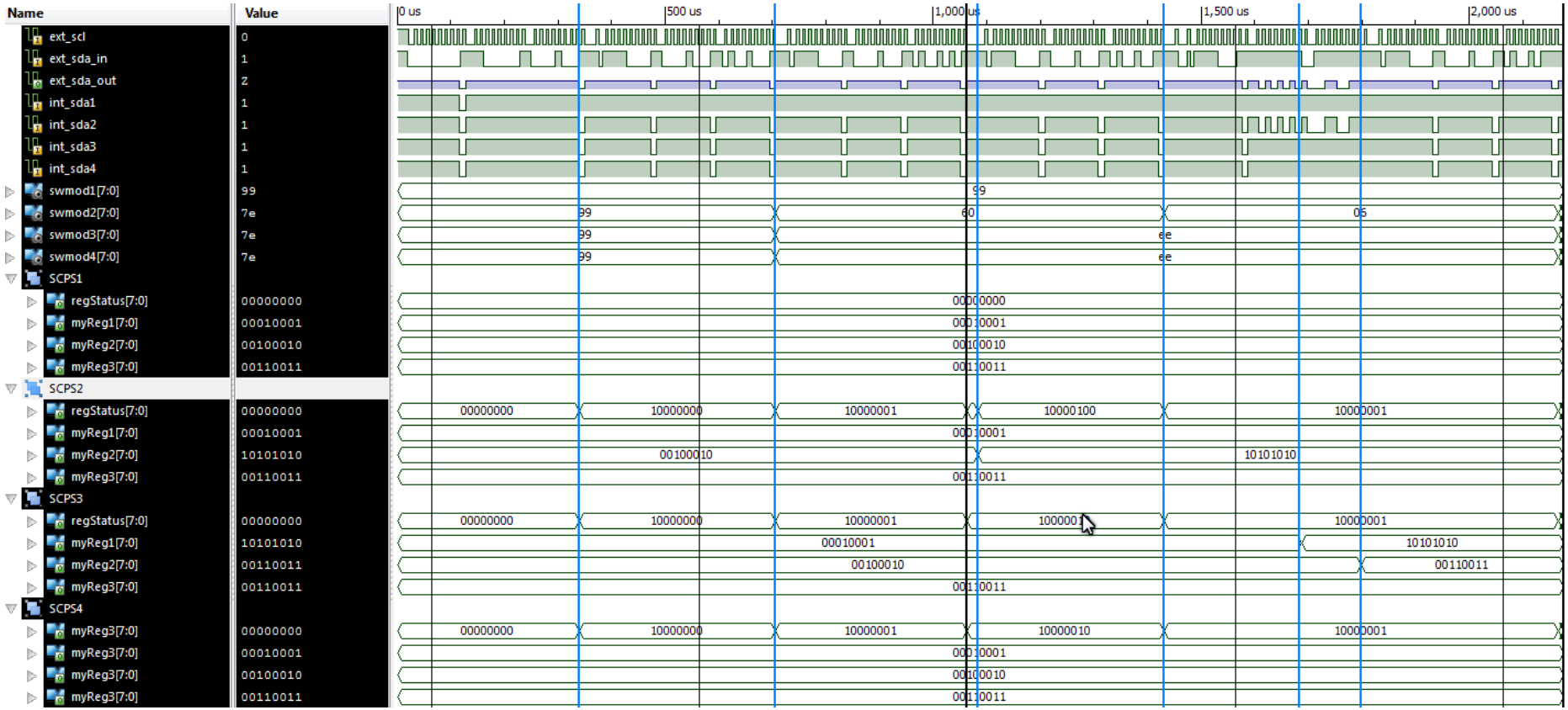


Figure 4-22 — Functional simulation of a SCPS group CAPTURE sequence with STBY stages and data TRANSFER.

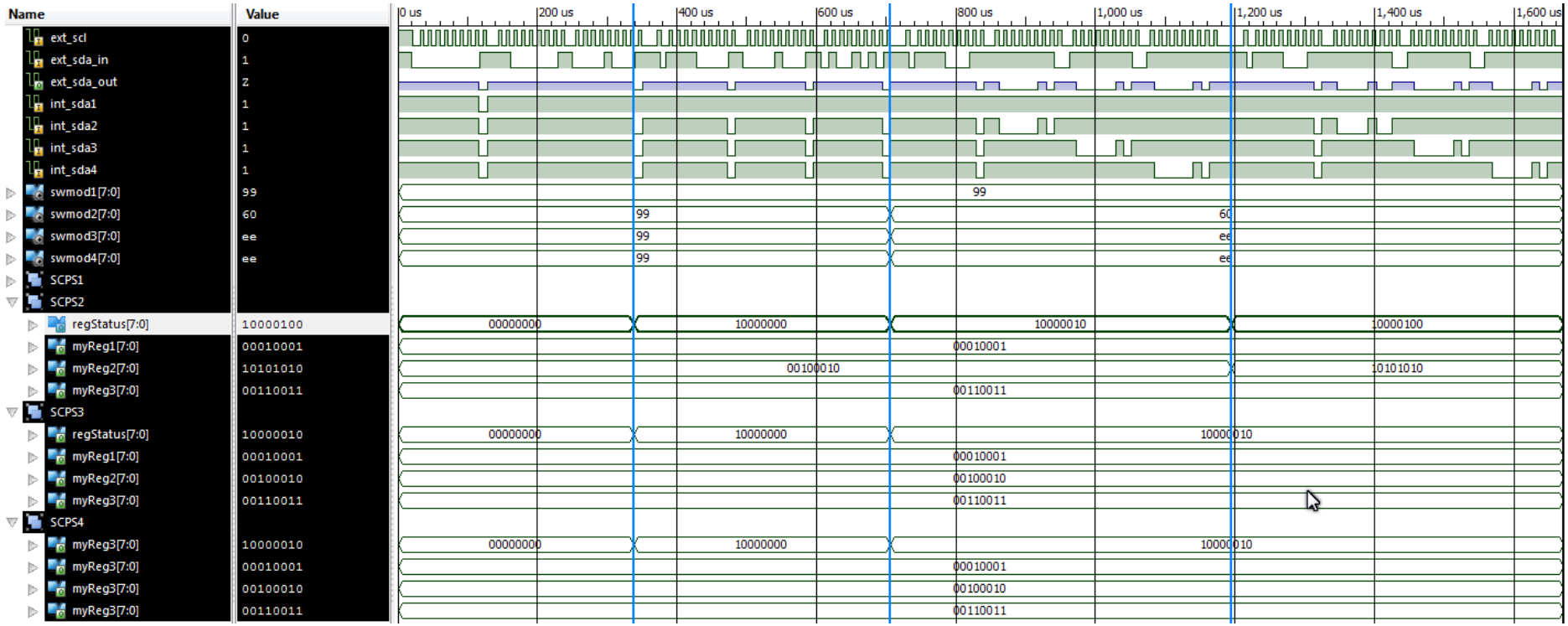


Figure 4-23 — Functional simulation of a SCPS difference of read in capture and in standby.

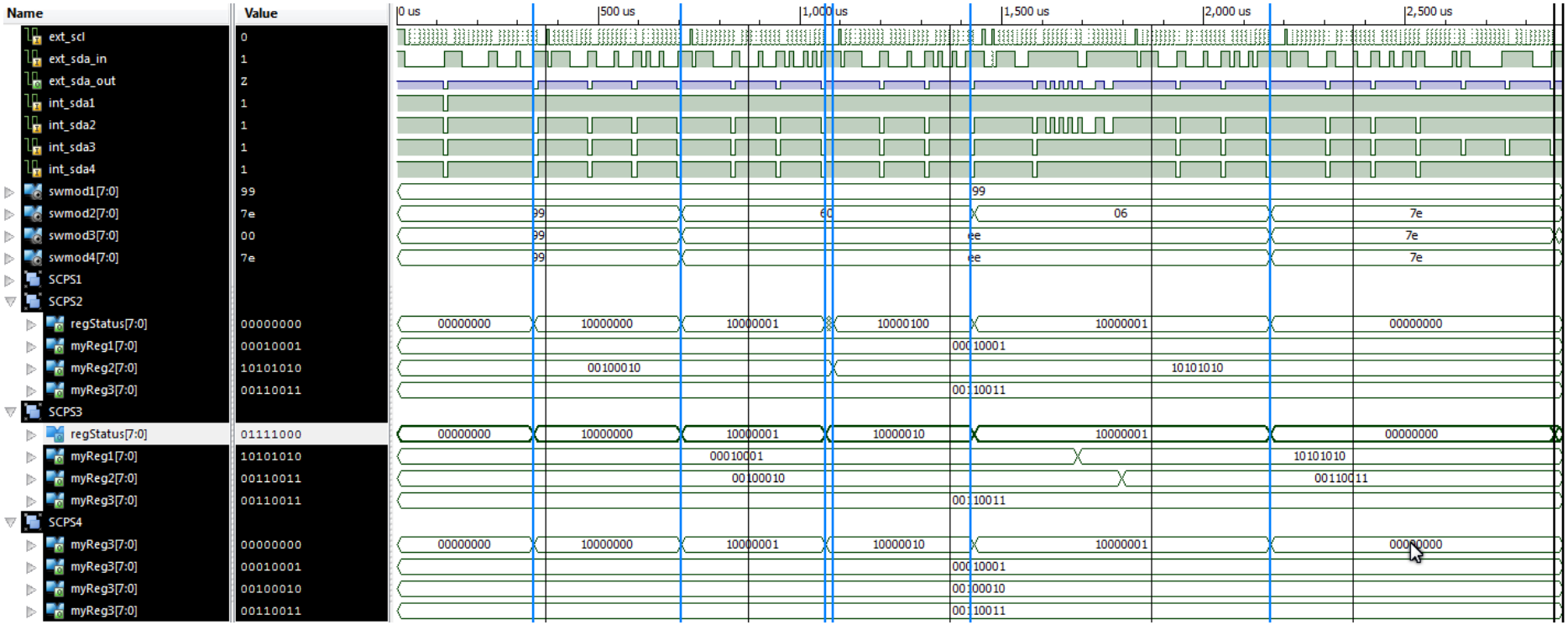


Figure 4-24 — Functional simulation of a SCPS CAPTURE, “quick” TRANSFER and PROCESS sequence.

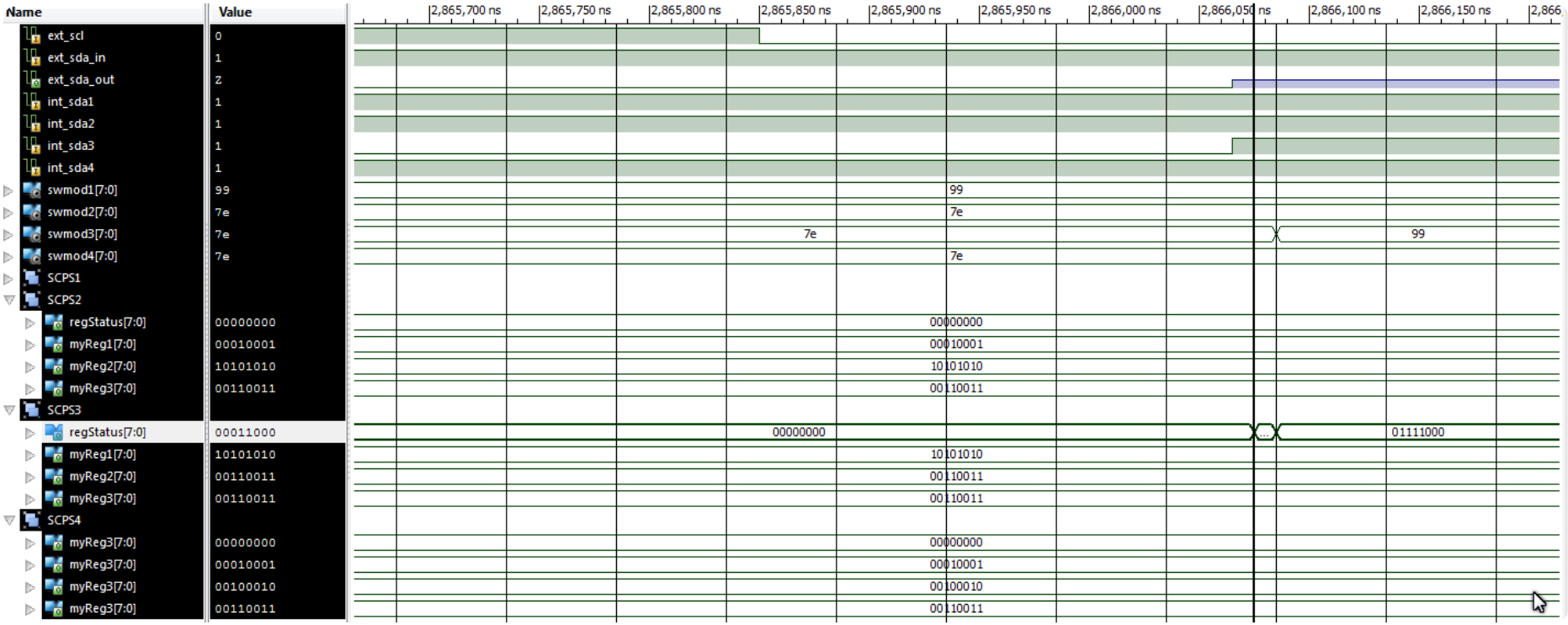


Figure 4-25 — Close-up of PROCESS section of the sequence of Figure 4-24.

4.2 Switching Module

The SCPS module permits not only the functional expansion of the conventional I2C operations, through its instruction set, but also, through the SCPS handler; thus serving to synchronize and manage functional and routing aspects of the instruments as well. A key aspect when incorporating a bus structure is a switching arrangement, in particular for the case of an analogue bus. A universal analogue switching module was designed and implemented, with flexibility and adaptability in mind, as seen in Figure 4-26. The structure is intended to cover one wire (such as the case of an electrode connection) and two wires (such as the case of an FSR) sensor scenarios, while considering up to two wires analogue buses. Local ground, VCC and additional reference pins were allocated, for permitting local referencing and circuit loop closing. Additionally, a path independent from the analogue bus was incorporated, in order to expand the possible scenarios.

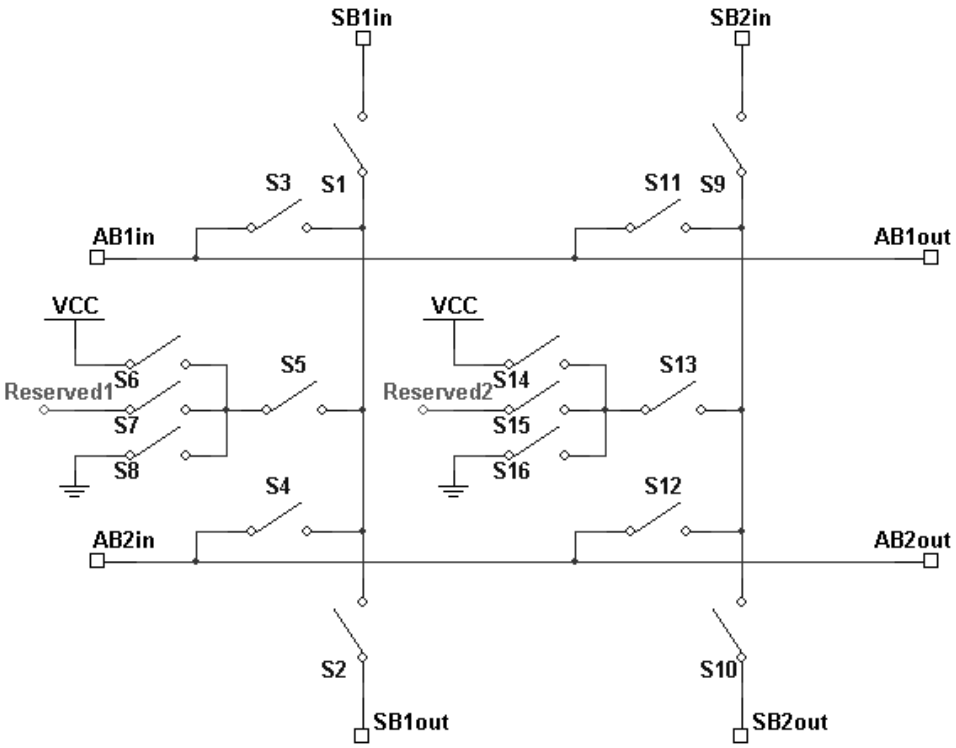


Figure 4-26 — Universal switching structure.

The circuit was designed and simulated using Multisim 11.0 from National Instruments; while Ultiboard 11.0 was utilized for the PCB designed. The FPGA PMOD interface was used for connectivity, thus limiting the number of control lines to eight. It was decided that switches S2, S6, S7, S8, S10, S14, S15, S16 would be implemented through the use of physical jumpers, since the sensor measurement scenarios considered did not require such features. A complete schematic of the final switching module can be seen in Figure 4-27, based on the analogue single supply CMOS low voltage ADG713BR switches from Analogue Devices (Analog Devices Inc., 2011).

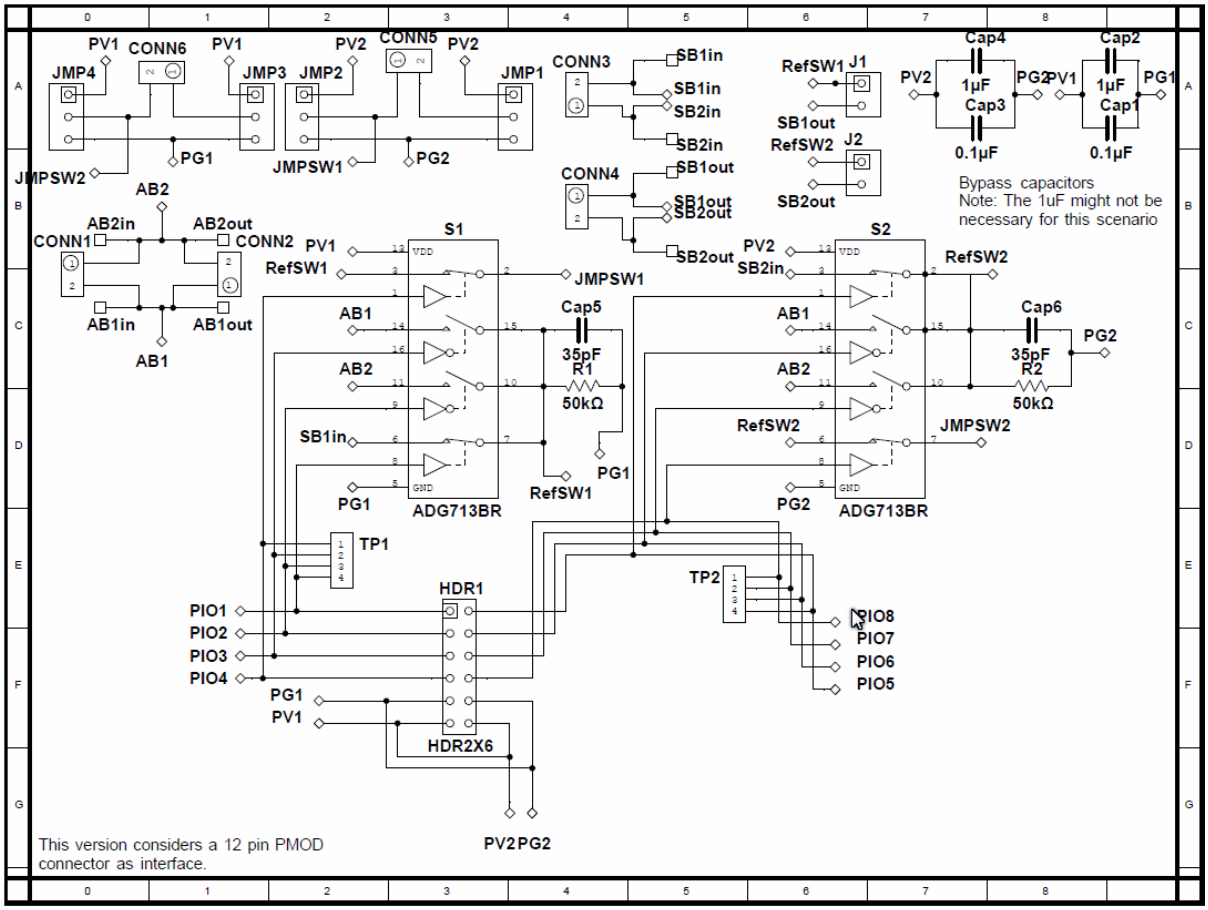
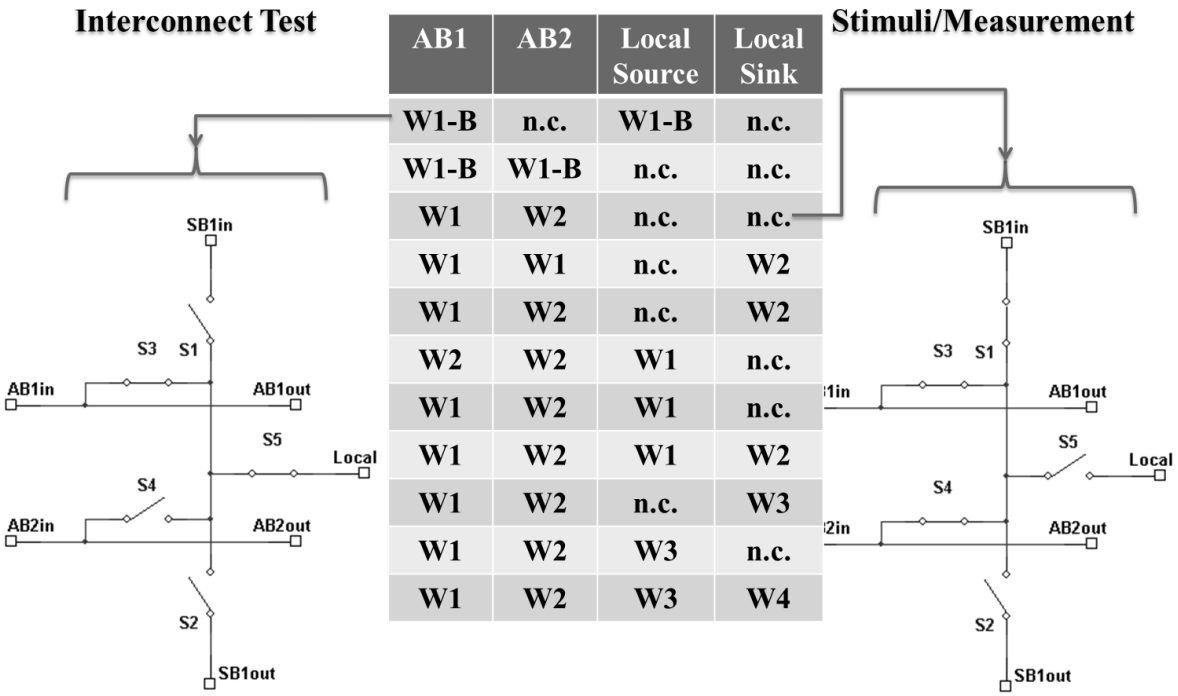


Figure 4-27 — Schematic view of SCPS switching module.

The PCB was designed with dual ground planes, minimizing the number of trace crossings. The switching module was tested for continuity and response within the 10Hz to 1 MHz range, verifying low on resistance within the range indicated in the datasheet (less than 4 Ω on resistance).

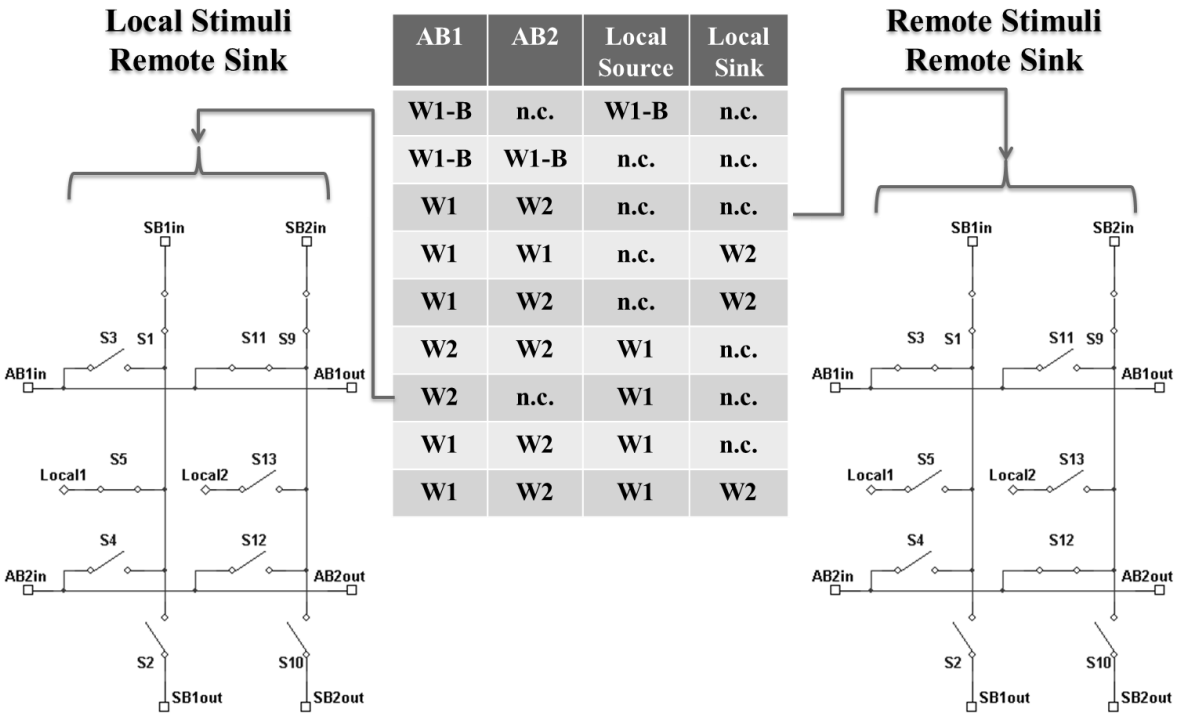
The flexibility of the switching structure is evidenced by observing Figure 4-28 and Figure 4-29, where single-wire and dual-wire setup scenarios are summarized and illustrated for particular cases. For instance, on the left side of Figure 4-28, one observes a setup that allows for an interconnect test where the analogue bus line 1 (AB1) is connected to a local source through switches S3 and S5, following a similar approach than the IEEE Standard 1149.4 test bus interface circuit. In contrast the right side of Figure 4-28 presents a stimuli-measurement scenario, where access to the sensor is achieved through the S1 switch and both S3 and S4 connect to the AB1 and AB2 lines respectively. This setup allows for the injection of stimuli through one of the analogue bus lines, while performing a measurement through the other (in this scenario the measurement would most likely be a high-impedance voltage measurement in order to avoid stimuli current deviation). A number of other possible setups is summarized in the table shown in the middle of the figure, where n.c. stands for “not connected” and the B refers to the “bridge” segment between the SB1in and SB1out.



AB1	AB2	Local Source	Local Sink
W1-B	n.c.	W1-B	n.c.
W1-B	W1-B	n.c.	n.c.
W1	W2	n.c.	n.c.
W1	W1	n.c.	W2
W1	W2	n.c.	W2
W2	W2	W1	n.c.
W1	W2	W1	n.c.
W1	W2	W1	W2
W1	W2	n.c.	W3
W1	W2	W3	n.c.
W1	W2	W3	W4

Figure 4-28 — Single-wire switching structure various setups.

Figure 4-29 on the other hand presents a dual-wire scenario, where the sensor connects to the analogue bus through two points (typical of most sensors and conventional components, such as resistors, capacitors, etc.). On the left side of Figure 4-29, one observes a local stimulus being used as source through S5, while the sensor's SB2 port is connected to the AB1 line through S9 and S11, thus directing the response towards a remote location. On the right hand side, one encounters that the AB1 line is connected to the SB1in port (through S1 and S3), while the SB2in port is connected to the AB2 line (through S9 and S12), this setup allows for a stimulus to be sent from a remote location, and its response to be captured remotely as well. A summary of a number of additional setups can be observed in the table located in the middle of the figure.



AB1	AB2	Local Source	Local Sink
W1-B	n.c.	W1-B	n.c.
W1-B	W1-B	n.c.	n.c.
W1	W2	n.c.	n.c.
W1	W1	n.c.	W2
W1	W2	n.c.	W2
W2	W2	W1	n.c.
W2	n.c.	W1	n.c.
W1	W2	W1	n.c.
W1	W2	W1	W2

Figure 4-29 — Dual-wire switching structure various setups.

4.3 Impedance Analyser and Analogue Front End Modules

A multi-frequency impedance analyser was designed and implemented in order to properly characterize the target sensors (disposable Ag-AgCl electrodes and FSR in this case). The initial setup was based on a National Instrument's (NI) initiative (McGinney, 2011) built around a PXI, or peripheral component interconnect eXtensions for instrumentation, chassis and boards. PXI is a computer based measurement and automation platform that has become with the years an industry standard. A National Instrument's (NI) PXI 1033 chassis, combined with an arbitrary function generator board NI PXI-5401, a digital oscilloscope board NI PXI-5112 and a 5½ digital multimeter NI PXI-4060, served as the main elements for the impedance analyser system, and can be seen in Figure 4-30.

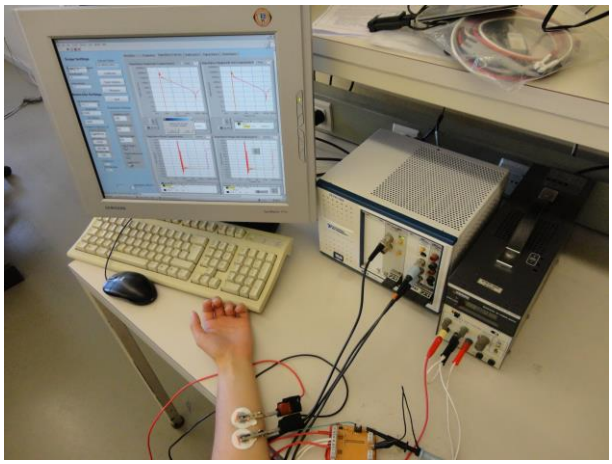


Figure 4-30 — NI PXI based impedance analyser setup.

The signal conditioning was achieved through the use of multiple analogue front ends (AFE), depending on the requirements of the setup at hand.

4.3.1 *Dual-supply PXI Analogue Front End*

Figure 4-31 presents the associated AFE for dual-supply scenarios; based on an inverting amplifier (seen on bottom of Figure 4-31) with parallel unity gain non-inverting follower (seen in the top of Figure 4-31).

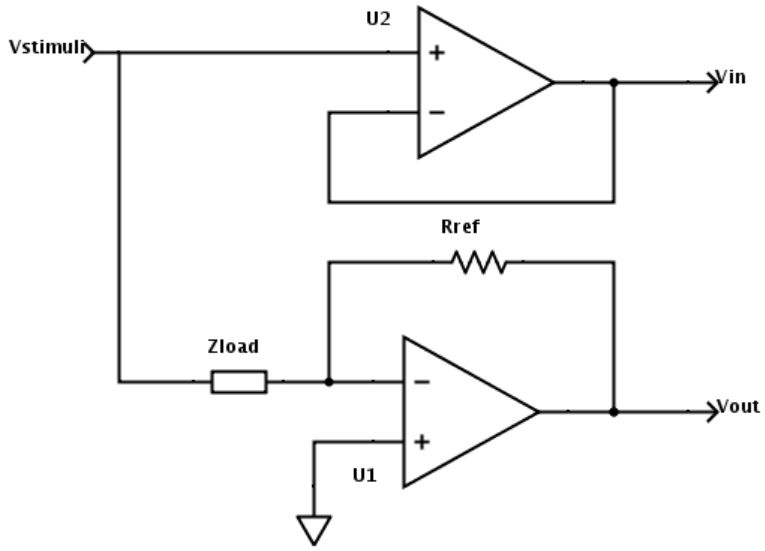


Figure 4-31 — Dual-supply analogue front end for impedance analyser system.

This simple strategy allowed the calculation of the impedance based on the ratio of the two produced signals (reference signal and output from target load). A number of reference resistor options were allocated, in order to adjust to the target impedance range. An unknown impedance (Z_{LOAD}) can be thus measured based on the output voltage of the inverting amplifier by:

$$V_{out} = -\frac{R_{ref}}{Z_{load}} V_{in} \qquad \text{Equation 4-1}$$

$$Z_{load} = -\frac{V_{in}}{V_{out}} R_{ref} \qquad \text{Equation 4-2}$$

The circuit presented in Figure 4-31 (design in Multisim 11.0) was transfer to Ultiboard 11.0 for PCB design based on recommendation from the datasheet of the LMH6622 Dual Wideband, Low Noise, 160MHz, Operational Amplifiers (Texas Instrument, 2013).

Table 4-6 and Table 4-7 present the arithmetic average and average deviation for measurement from a range of resistor values measured with the dual-supply AFE with a 1 kΩ reference resistor. The measurements were performed with start frequency 100Hz and end frequency 1MHz, with a logarithmic distribution of 100 steps. Each measurement was performed with 200 samples/cycle, 40 cycles/record, 40 records/measurement. The values were obtained by application of Equation 4-3, 4-4 and 4-5, while the values in parenthesis are normalized by the nominal value of the impedance in question.

$$\boldsymbol{Aritmetic\ mean} = \frac{\mathbf{1}}{\boldsymbol{n}}\sum_{\boldsymbol{i}}^{\boldsymbol{n}} \boldsymbol{x_i} = \overline{\boldsymbol{x}} \qquad \text{Equation 4-3}$$

$$\boldsymbol{Average\ deviation} = \frac{\mathbf{1}}{\boldsymbol{n}}\sum_{\boldsymbol{i}}^{\boldsymbol{n}} |\boldsymbol{x_i} - \overline{\boldsymbol{x}}| \qquad \text{Equation 4-4}$$

$$\boldsymbol{Average\ error} = \frac{\mathbf{1}}{\boldsymbol{n}}\sum_{\boldsymbol{i}}^{\boldsymbol{n}} \left|\frac{(\boldsymbol{x_{nominal}} - \boldsymbol{x_i})}{\boldsymbol{x_{nominal}}}\right| \qquad \text{Equation 4-5}$$

Table 4-6. Dual-supply AFE 1 kΩ reference magnitude measurements from 100Hz to 1MHz.

Magnitude	200	1K	4.7K	10K	49.9K
Arithmetic Mean	197,56	981,03	4600,90	9945,94	49310,38
Average Deviation	0,40 (0,0020)	1,70 (0,0017)	14,77 (0,0031)	34,31 (0,0034)	948,77 (0,0190)
Average Error	1,22%	1.90 %	2,11 %	0,70 %	2,53 %

Table 4-7. Dual-supply AFE 1 kΩ reference phase measurements from 100Hz to 1MHz.

Phase	200	1K	4.7K	10K	49.9K
Arithmetic Mean	-0,32	-0,12	-0,50	-0,99	-4,95
Average Deviation	0,36	0,08	0,53	1,23	6,17

One can observe that for the overall range the average deviation is percentually low (less than 2% for the 49.9K Ω case), correspondingly the average error also presents favourable results. It is of note that the 1 kΩ case presents the lowest average deviations for both magnitude and phase (considering the normalized average deviation for the magnitude), which is expected since the load value matches the reference impedance.

4.3.2 *Single-supply PXI Analogue Front End*

For the single-supply scenario a different strategy was utilized, the auto-balancing bridge approach. This circuit has the added benefit of controlling the current that traverses the target load, by means of the reference impedance. Figure 4-32 presents the Multisim 11.0 circuit, which was based on the low cost, high speed, rail-to-rail amplifier ADA4891-2ARZ (Analog Devices, 2013).

The circuit also counts with a non-inverting follower to serve as reference; while the unknown load (located between connectors U6 and U3 in the bottom part of Figure 4-32) can be calculated by means of the following equations:

$$V_{out} = -\frac{Z_{load}}{R_{ref}}\left(V_{in} - \frac{V_{DD}}{2}\right) \qquad \text{Equation 4-6}$$

$$Z_{load} = -\frac{V_{out} * R_{ref}}{(V_{in} - \frac{Vdd}{2})}$$ Equation 4-7

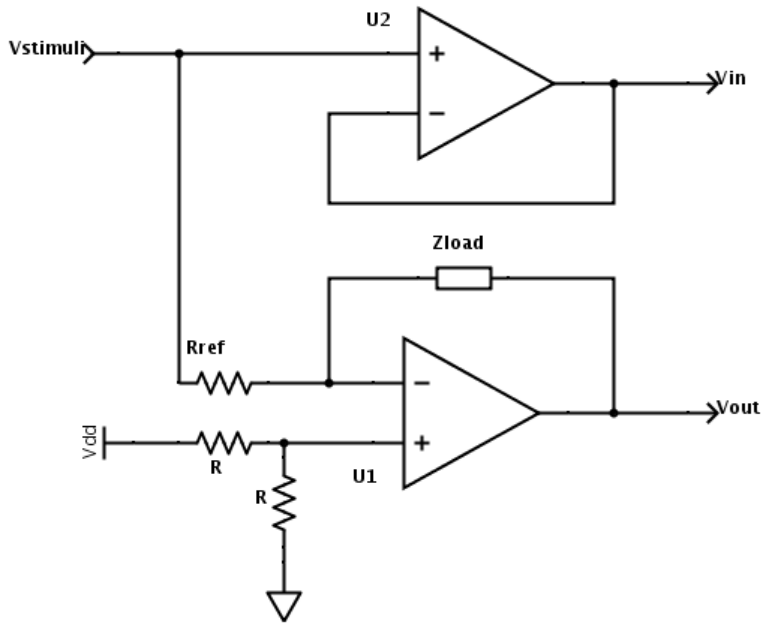


Figure 4-32 — Single-supply analogue front end for impedance analyser system.

The circuit shown in Figure 4-32 was transferred to Ultiboard 11.0 for PCB design, based on recommendation from the datasheet of the ADA4891-2ARZ. For this circuit the normalized average deviation is under the 7%, with an increasing error departing from the reference impedance, which seems to affect the phase as well. That said, the magnitude and phase measurements are within acceptable ranges, considering the target sensors.

Table 4-8. Single-supply AFE 1 kΩ reference magnitude measurements from 100Hz to 1MHz.

Magnitude	200	1K	4.7K	10K
Arithmetic Mean	188,44	1000,73	4765,01	10146,49
Average Deviation	2,05 (0,0102)	8,90 (0,0089)	158,51 (0,0273)	667,23 (0,0667)
Average Error	5,78%	0.89 %	3.02 %	6.91%

Table 4-9. Single-supply AFE 1 kΩ reference phase measurements from 100Hz to 1MHz.

Phase	200	1K	4.7K	10K
Arithmetic Mean	0,08	-0,03	-0,26	-0,37
Average Deviation	0,55	0,55	1,65	3,81

4.3.3 *LabVIEW Impedance Analyser Virtual Instrument*

The software counterpart for the AFE presented in the previous sub-section is an adapted virtual instrument (VI) written in LabVIEW 2010. Although the PXI-chassis was recently

purchased (year 2013), the internal boards were legacies from the previous projects, five to eight years old. Due to the high cost of board replacement (more than five thousand euros for the low-end version), a compromise with the available cards was arranged. This forced the VI to include depredated modules which only function with specific operating system specifications. An overhaul of the entire VI was necessary in order to achieve compatibility, which also included an expansion of its original parameters and improvement in the measurement mechanics (through the inclusion of filters and related strategies). The initial screen can be seen in Figure 4-33, presenting to the left the options for measurement, including peak-to-peak stimuli amplitude, number of measurements, start/end frequency, linear/logarithmic distribution, number of samples per cycles, number of cycles per record, number of records to average per measurement. Additional options include auto-range capabilities, waveform display, and selection of calibration, storing values and performing a measurement.

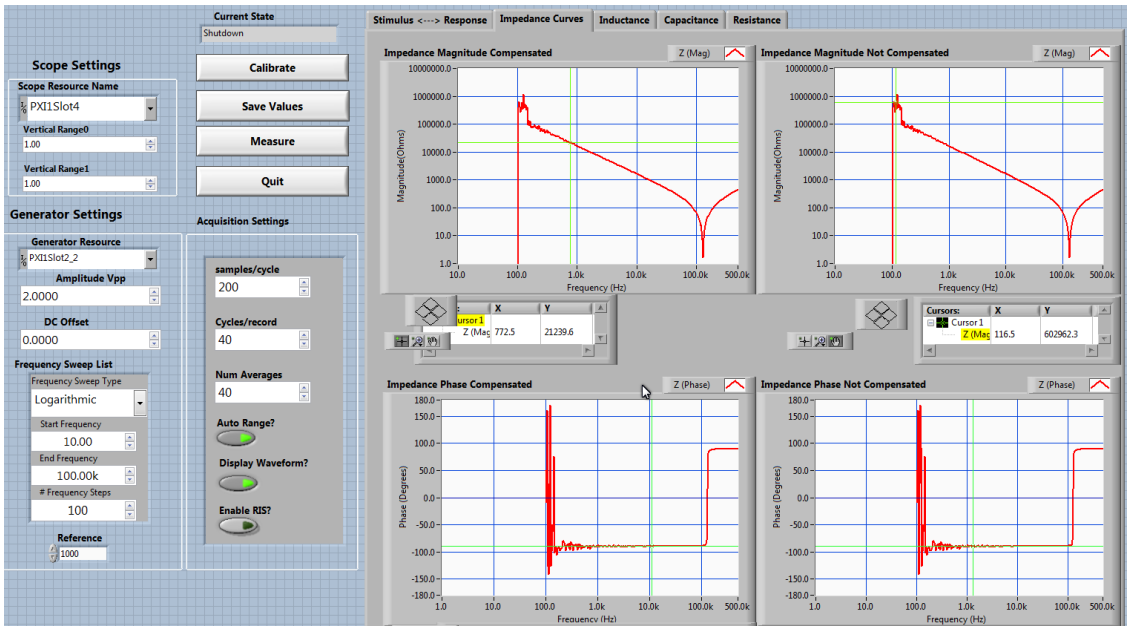


Figure 4-33 — Initial impedance analyser screen-shot.

The perform measurements can be compensated with an open-short-load strategy, which for the scenarios at hand was not utilized, although in Figure 4-33 one notes that the compensated and the non-compensated impedance calculations are presented side-by-side. An additional screen of the Impedance Analyser VI, permitted real-time visualization of the stimuli-response waveforms (seen in Figure 4-34), and inductance, capacitance, resistance components of the measured impedance. The internal mechanics of the VI were based in an intricate combination of Vis both custom and standard, which followed a specific flow insuring the proper setup and activation of each involved component. An internal peak of the Impedance Analyser VI can be seen in Figure 4-35, where the bode analyser block can be seen in the centre, and the flow managers can be seen on the top.

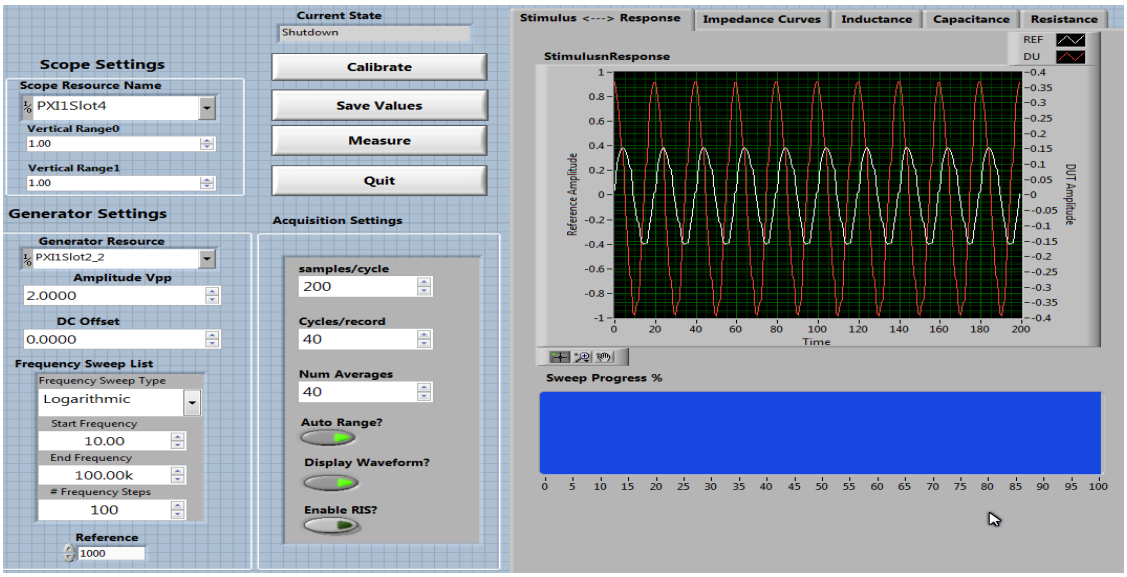


Figure 4-34 — Stimuli-response wave visualization screen of the impedance analyser VI.

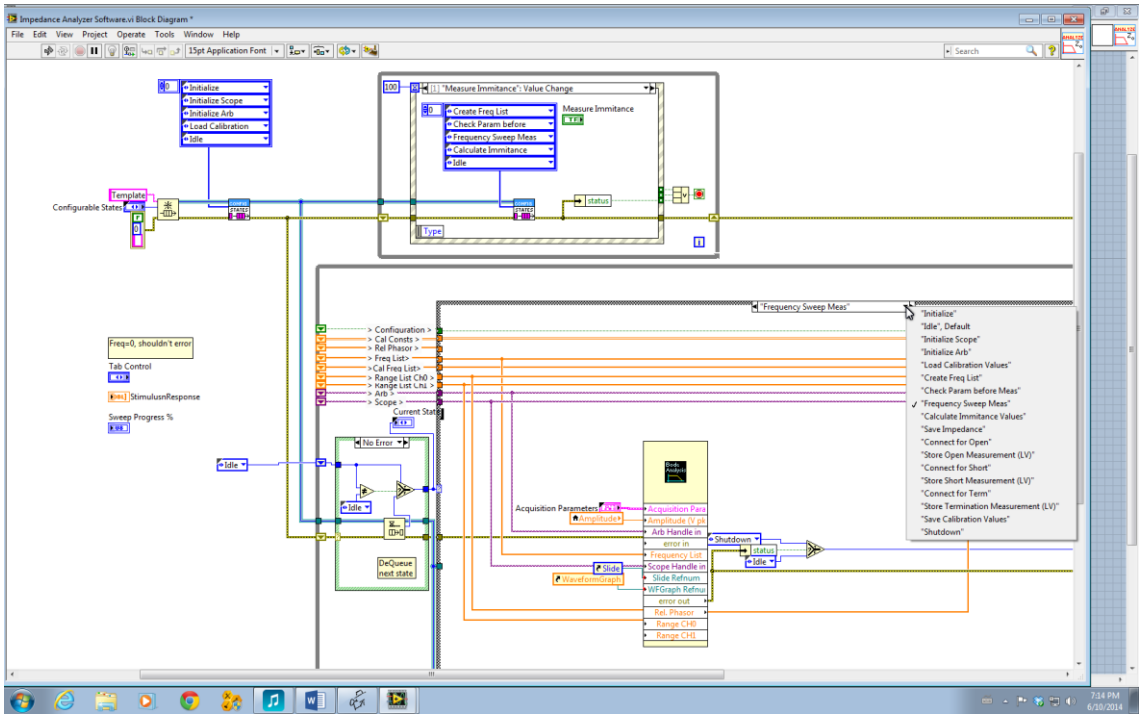


Figure 4-35 — Internal screen shot of impedance analyser VI.

4.4 Over-Current Protection Circuit

During the study of Ag-AgCl disposable electrodes, efforts that will be presented on the next chapter, a Gamry Series G 300 Potentiostat/Galvanostat/ZRA (zero resistance ammeter) was utilized for measurement purposes. The G 300 provides setup connectivity flexibility and a number of measurements options through its configurable interface. Although, the G 300 is quite adaptable its internal circuitry presents a problem for human related measurement, following a low-side reference strategy with negative feedback. The circuit in Figure 4-36 shows the four major blocks (signal generator, control amplifier, electrometer and I/E

converter) of the G 300 potentiostat, capable of up to 20 volts or more than 300 mA. The system has a computer-controlled voltage source that permits the generation of a configurable signal. The signal is continuous compared with a servo amplifier (the control amplifier) against the cell voltage, driving the adjusted current as to maintain equality. The resulting signal was captured by the reference and working electrodes, permit the determination of the voltage and consequent current through the sample. A number of arrangement regarding the electrodes, permit 2-3-4 electrode setups.

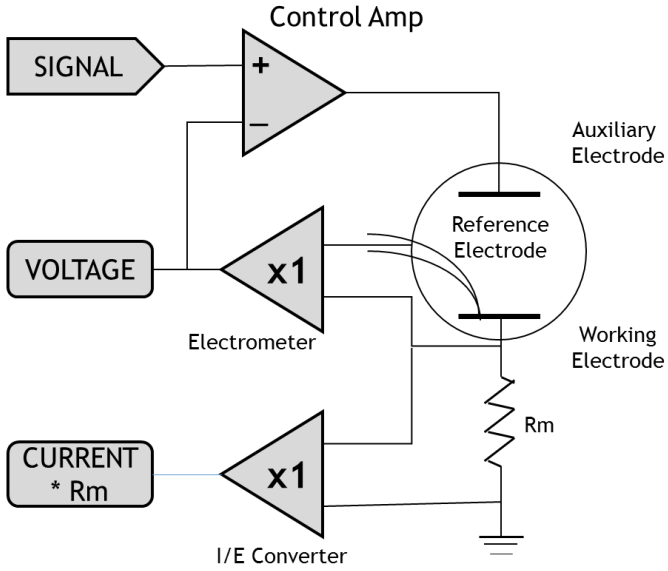


Figure 4-36 — Diagram of Gamry series G 300 potentiostat circuit. Enhanced figure extracted from (GAMRY Instruments Inc., 2010).

The danger for humans comes from the control strategy for the potentiostat, which could overcompensate with excessive current, which thus would cause harm to an individual. In order to guard for such scenario, a straightforward overcurrent protection circuit was designed, improved and implemented. The circuit, seen in Figure 4-37, uses a shunt resistor approach with an INA111, high speed FET-Input Instrumentation Amplifier, for current determination. The LM319, high speed comparator, then compares the resulting voltage from the amplification section with positive and negative references produced by a LM317 (three-terminal adjustable regulator) and LM337 (three-terminal adjustable negative regulator), respectively. Additionally, a low battery safeguard section was included for added protection. If either the overcurrent or the low battery protection section detects a fault state, the fault lock section self-locks and mechanically disconnects the line using a relay. The fault lock section can only be reset through a manual button.

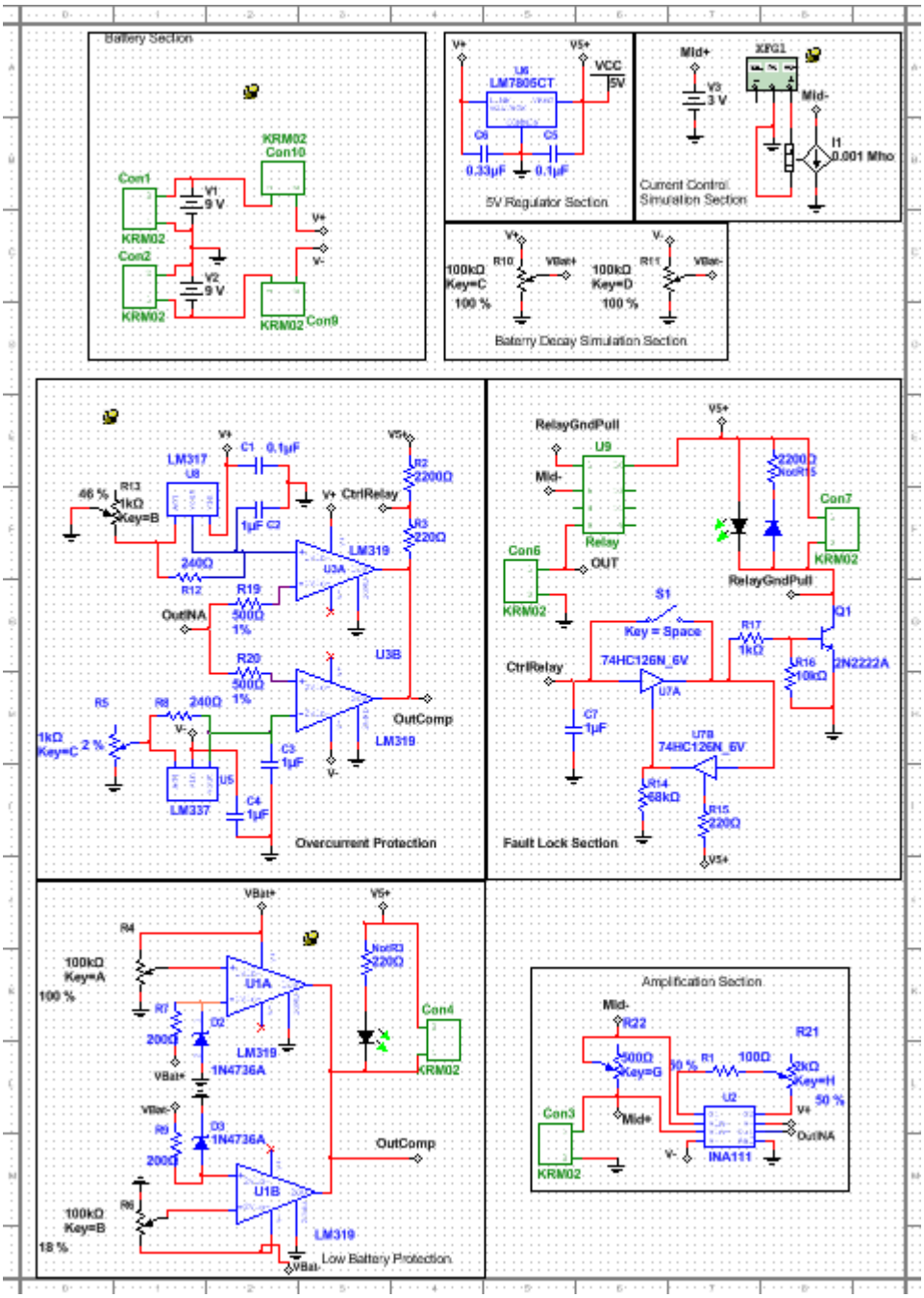


Figure 4-37 — Overview of overcurrent-protection circuit.

During the usage of the circuit, no test subject experimented any shock or excessive current, and since the shunt resistor was high-side situated, no effect on the measurement is observed.

4.5 Impedance Analyser Module

An impedance analyser module was designed, based on two AD5934, 250 kSPS 12-bit impedance converter (Analog Devices, Inc., 2012), however not implemented primarily because it was outside the planned objectives (elevated cost of PCB and component placement was also a consideration). As mentioned, the module was based on the commercially available AD5934, capable of performing complex impedance measurement up to 100 kHz. The AD5933 and AD5934 have been utilized in several systems from structural and mechanical engineering applications (Lee D. D., 2006) (Overly, 2007) to portable bioimpedance measurement systems (Ferreira, Seoane, & Lindecrantz, 2011) (Liu & Liu, 2010) (Margo, Katrib, Nadi, & Rouane, 2013). The AD5934 utilizes a discrete Fourier transform strategy for impedance calculation, based on a calibration measurement for voltage/current determination. The two step process is simplified by the use of two AD5934 working in tandem. The communication (I2C and SCPS), switching control and manage elements was thought for control by an Arduino UNO board. Although not implemented, this design exercise allowed for an improved understanding of possible test instruments associated to the SCPS framework, and the integration steps required. For instance the need of a stand-by state was introduced because of the flow of the AD5934, which reveal the need to consider test instruments that required an intermediary state between setup and direct capture. The resulting concept for the impedance analyser circuit can be seen in Figure 4-38.

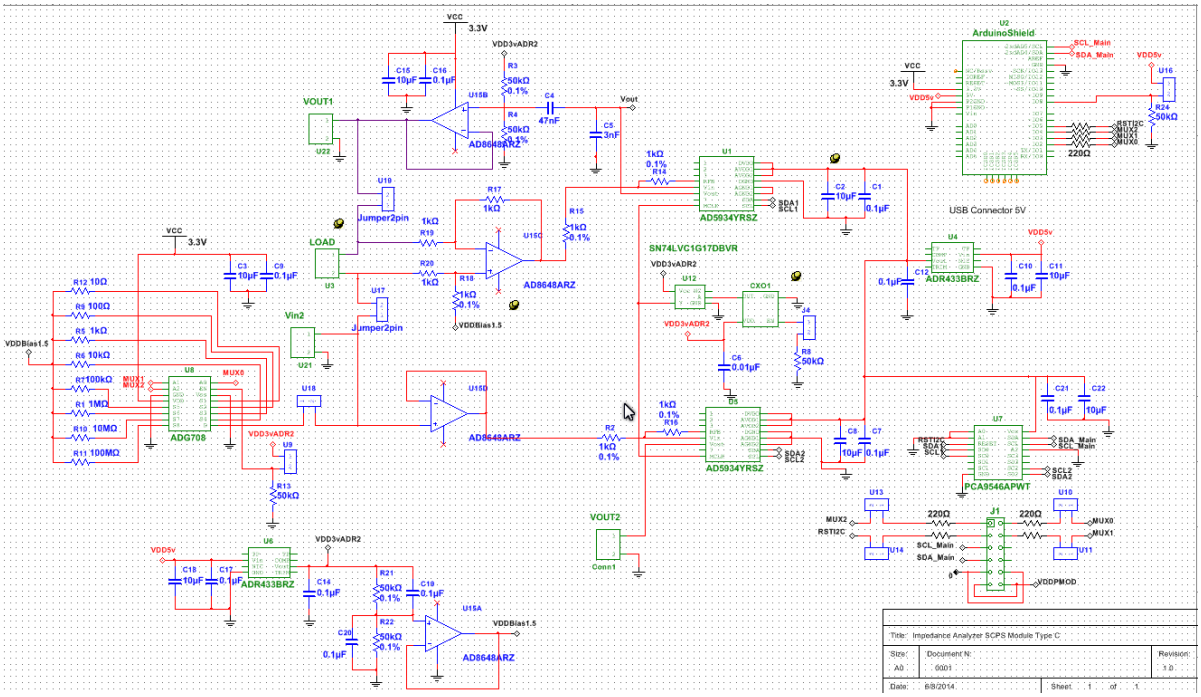


Figure 4-38 — Overview of impedance analyser module.

4.6 Line level Verification Setup

As part of the proof-of-concept endeavours, the RTL modules where synthesized, mapped, placed and routed within an ATLYS Spartan-6 based board (a NEXYS 3 board was also used during debugging) from Digilent Inc. This conceptual exercise was meant to provide a practical overtone to the verification process regularly associated to IP cores. In order to establish a bi-directional communication with the FPGA board in question, a set of RTL Verilog modules, firmware, library and software bindings (in this case Python bindings), where utilized from a GNU Lesser General Public License (version 3 or later) project managed by Chris McClelland (McClelland, 2014), the FPGALink (McClelland, 2012).

The FPGALink takes advantage of the Cypress FX2LP USB microcontrollers found in a variety of commercially available FPGA boards; this high-speed USB interface serves as an adequate venue for FPGA programming, as well as exchanging data between a computer and the FPGA board. Although, the FPGALink project provides the means for data exchange, it was necessary to implement a Python GUI, based on the popular open source wxPython GUI toolkit.

Additional to the ATLYS board, a VmodMIB VHDC module interface board (seen in Figure 4-39) was used to increase the number of PMOD ports available. The VmodMIB permitted direct access to all four SWMOD registers for possible connectivity with corresponding switching modules and/or provide test-point accessibility.

Figure 4-39 — VmodMIB VHDC module interface board.

The USBee ZX Test Pod from CWAV, Inc., provided a commercially available I2C master controller, permitting the generation of appropriate I2C bus transactions, in accordance with the standard (seen in Figure 4-40). Finally, the DV1-100 Portable Logic Analyser from DigiView™, provided an appropriate mechanism for line level observability and signal capture (seen in Figure 4-41).

Figure 4-40 — USBee ZX test pod device. Extracted from website (CWAV Inc., 2013).

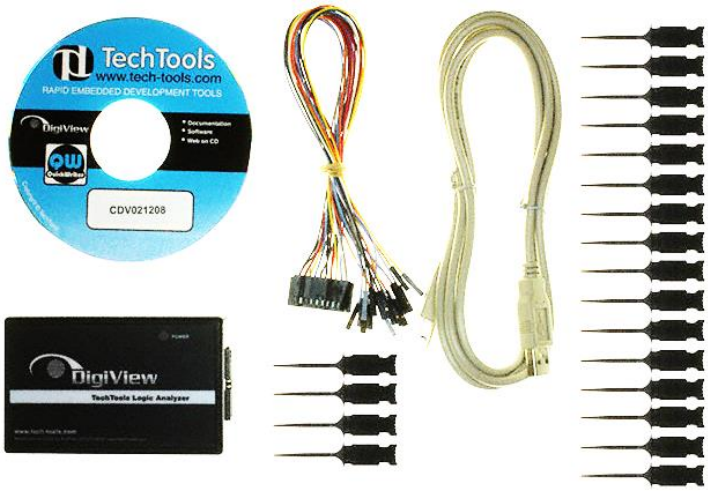


Figure 4-41 — DV1-100 logic analyser. Extracted from website (Digikey, 2014).

4.6.1 *Software Interface*

The before mentioned hardware implement Python GUI, served as a register viewer/writer and FPGA programming venue, and can be seen in Figure 4-42. The script continuously updates the register values (when the Start button is pressed) based on the Register Handler module within the FPGA, while permitting the writing to such register in an individual manner. Additionally, it permits to load the Xilinx XST file to the FPGA, thus facilitating the debugging and experimentation process.

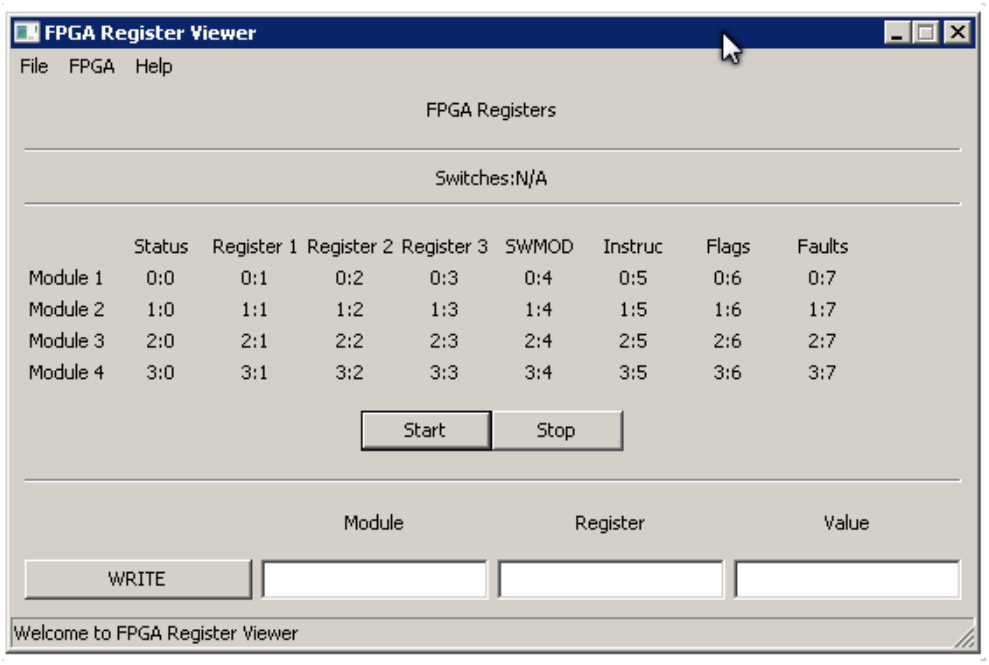


Figure 4-42 — Snapshot of FPGA register viewer.

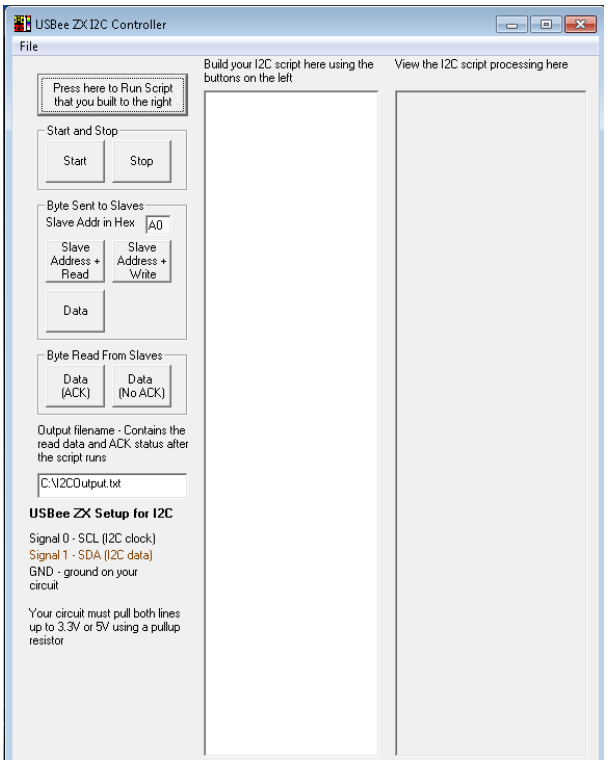


Figure 4-43 — USBee ZX I2C controller interface.

The I2C transactions were introduced through a graphical interface provided with the USBee ZX, as seen in Figure 4-43, which permits transaction building through button sequences, script loading or direct writing in the middle section. Responses to the I2C transactions are captured on the right hand side section of the application, in text format, thus only properly formatted responses are presented.

In parallel a DigiView™ Portable Logic Analyser application, permits the capture of the signals at the line level, including the software configurability to expect I2C transactions, facilitating the verification process (a snapshot of the software can be seen in Figure 4-44).

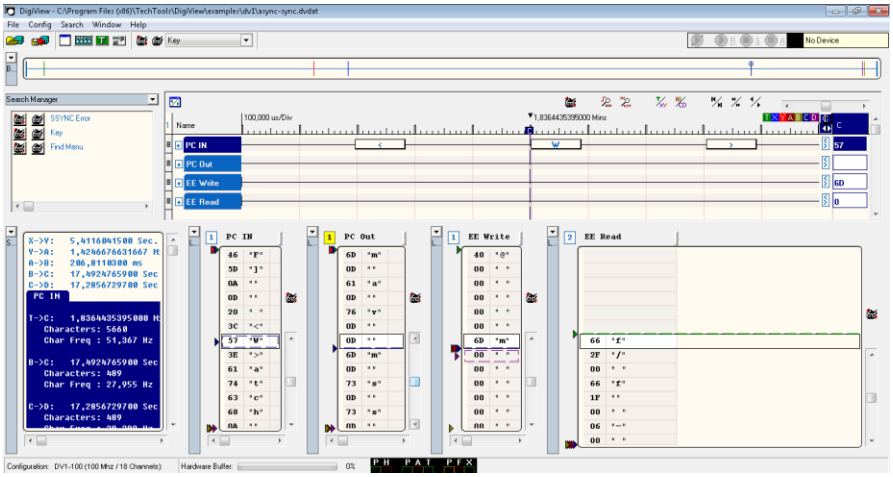


Figure 4-44 — DigiView™ portable logic analyser application.

The previously described setup, both at the hardware and software level, permitted the confirmation of the behaviour of the I2C lines and SCPS registers, allowing for debugging and verification of the SCPS modules behaviour in a physical environment. Although it should come as no surprise that the observations at the line-level matched does of the simulations, the setup permitted an improved understanding of the realities of the I2C transaction dynamics, such as non-homogeneity of the SCL HIGH period. A picture of the setup can be seen in Figure 4-45, where the USBee ZX can be observed on the top right section, while the DV1-100 is located to the left side, one can also observe the VmodMIB board at the top side of the ATLYS board.

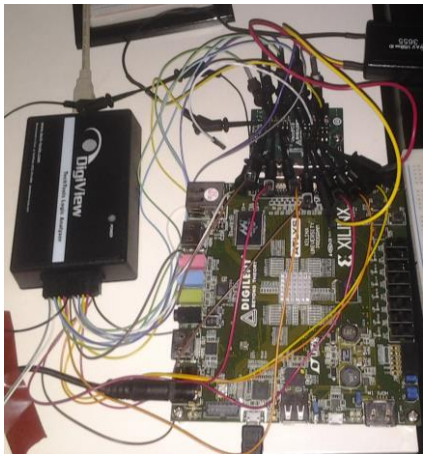


Figure 4-45 — Hardware setup for SCPS module verification.

4.7 Chapter Remarks

A number of inter-disciplinary experiments, designs and implementations represent the body of work related to the present thesis, partially described within the present chapter.

The transition from an abstract concept to a practical implementation can represent a challenge, and mixed-signal, analogue and sensor testing and the fast-paced area of wearable monitoring technology is no exception. As with all prototypes and proof-of-concepts a number of unforeseen obstacles are to be expected, in particular in a field where there is no well-defined models or a comprehensive state of art to fall back upon. A key aspect for successfully surpassing the before mentioned transition is the malleability of the concept as to adjust to the realities of actual constructs. An inter-disciplinary and collaborative approach serves as the guiding principle of the present work, benefitting from knowledge-transfer for a number of methodologies and the experience of a number of consulted individuals. This method not only proved beneficial for the definition of the process flow and subsequent implementations, but for procedural aspects as well, aiding on the experimental side which is presented on the following chapter.

Chapter 5

Case Studies - Characterization Experiments

Much has been said in previous chapters of the importance of testing and design for testing in this age of Systems on Chip (SoC), System in Package (SiP), mixed-signal ICs, smart sensors, and hybrid technologies, as well as the need for analogue, mixed-signal and sensor testing; in spite of the known challenges and the additional obstacles that personal monitoring technology entails. Pervasive technology ultimately seeks long-term monitoring; the need for well thought fault diagnosis strategies has become a requirement. Not only personal monitoring systems are expected to be reusable (multiple uses and/or users) and therefore require initialization and calibration mechanisms, but due to the duration of the monitoring, features such as self-calibrating, self-testing, fault-tolerant, high reliability are goals to strive for. That said, the last decade has witnessed an upsurge on personal monitoring systems, with applications such as medical, rehabilitation, sports, and leisure.

In order to gain insight into the particularities of sensor testing strategies, it was proposed to understand the effects that usage has on the sensors themselves. The premise follows that no testing/calibration strategy can be proposed without a minimal understanding of the changes the target elements undergoes on the expected condition, in this case from an electrical point of view. It should be mentioned that the efforts presented in this chapter represent a preliminary study in sensor degradation for the two selected case studies[3].

5.1 Case study: Disposable Electrode Ag/AgCl

Surface electrodes are likely the most utilized sensors to perform electrical biosignals measurements, such as electrocardiography, electromyography, electro-encephalography, electrooculography, bioimpedance, impedance tomography, among others. A number of studies have presented research on electrode types (Yi-Zhi, Jia-Xin, Long-Fei, Yong-Sheng, & Hong-An, 2010) (Tallgren, Vanhatalo, Kaila, & Voipio, 2005) (Rahal, Khor, Demosthenous, Tozzard, & Bayford, 2009), characterization (Griss, Tolvanen-Laakso, Meriläinen, & Stemme, 2002) (Hoffman, Ruff, & Poppendieck, 2006) (Franks, Schenker, Schmutz, & Hierlemann, 2005), composition, form, circuital modelling (Vauhkonen, Vauhkonen, Savolainen, & Kaipio, 1999) (Boverman, Kim, Isaacson, & Newell, 2007) (Huang & Cheng, 1998) (Cheng, Isaacson, Newell, &

[3] An in-depth study would require significant investment of personnel, resources, and are outside the scope of the research at hand.

Gisser, 1989) (Hary, Bekey, & Antonelli, 1987), for a number of applications (Collete, Humeau, & Abraham, 2008) (Kilgore, Peckham, Keith, & Thrope, 1990) (Harth & Lischinsky, 2011) (Welch, Guilak, & Baker, 2004) (Li, Hu, & Tong, 2008).

The contact impedance achieved between the electrode-skin interface significantly affects the measurements (Zepeda-Carapia, Márquez-Espinoza, & Alvarado-Serrano, 2005) (Degen & Loeliger, 2007) (Degen & Jäckel, 2008) (Li, He, Wang, & Ren, 2008) (Huang & Cheng, 1998), therefore it is a matter of concern, traditionally solved through thorough skin preparation procedures, electrode placement settling, equipment checking, and electrode replacement. Most electrode-based measurement equipment perform a verification of the contact impedance prior to a measurement, there exist even portable verifiers that physicians utilize for such purpose; all that said, the fast pace evolution of personal monitoring technology is affecting the traditional approach towards electrode utilization, in particular when considering extended monitoring periods. Careful skin preparation (which requires thorough cleansing, shaving and sanding of the skin), electrode positioning and continuous verification, which most healthcare personnel are accustom, are not readily applicable to certain subjects, such as elderly, allergenic and paediatric due to their skin sensibility (Assambo, Baba, Dozio, & Burke, 2007), and for the case of personal monitoring technology, might not even represent an alternative; moreover, disparities of the electrode-skin interface impedance are to be expected (Kilgore, Peckham, Keith, & Thrope, 1990). Even under controlled laboratory environment and thorough skin preparation routines, variation of the electrode-skin interface impedance are anticipated (Hewson, Druchêne, & Hogrel, 2001). Furthermore, when considering athlete's performance, daily activities monitoring, and other scenarios where the individuals will have to position the electrodes themselves or the electrodes are integrated within a garment (as in the case of textile electrodes), careful positioning and skin preparation cannot be considered a part of the procedure.

It has been shown that DC stimuli does not represent a practicable option for electrode-skin state determination, thus an AC stimulus remains the viable alternative (Wiese, et al., 2005). A number of models have been developed during the years for representing the impedance of the electrode-skin interface, and even though most concord on the general circuit model, presented in Figure 5-1 (extracted from (Webster J. , 2009)), the complexity and modelling approach can vary greatly depending on the target requirements. For the present scenario of fault detection, a simplified equivalent circuit was adopted, which can be seen in Figure 5-2. Such single time constant model is a common alternative, which provides a good approximation to experimentally observed results (Neuman, 1998) (Mc Adams, 2006). Alternatively the capacitor component can be substituted by a constant phase element, a theoretical element with constant phase anywhere between 0° and 90°, for some models (Grimnes, 2006); representing the capacitive coupling form between the electrode and the conductive tissue, separated by the moderately non-conductive stratum corneum layer.

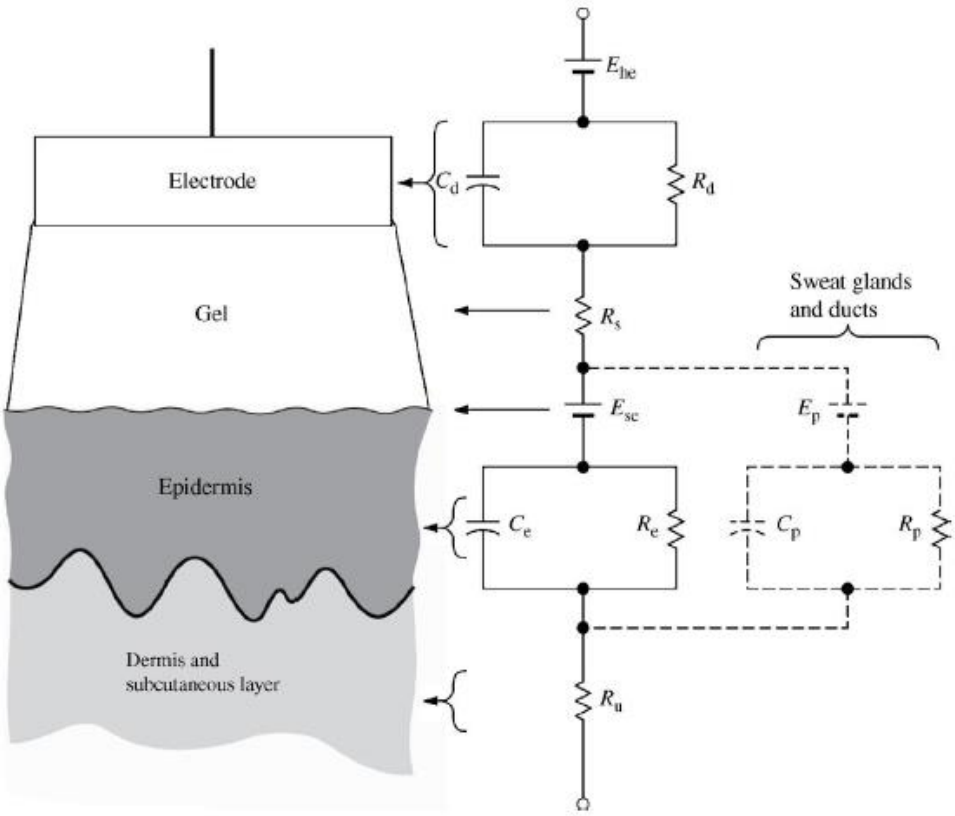


Figure 5-1 — Electrode-skin circuit model extracted from (Webster J. , 2009).

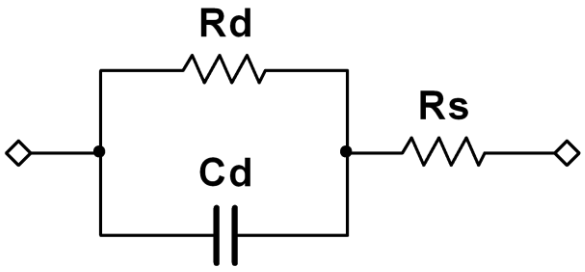


Figure 5-2 — Simplified electrode-skin circuit model.

At the electrode-skin interface, the electron current of the system-side is converted into an ion current, flowing thru the biological system, and vice versa. The electrochemical processes at the interface, and thus the electrical properties and behaviour of the electrode-skin impedance, are strongly influenced by the materials present, as well as by the surface area. The Helmholtz capacitance Cd accounts for capacitive charging effects at the dielectric Helmholtz double layer, which is formed at the interface. The Faraday resistance Rd represents leakage currents penetrating this double layer, caused by reversible and irreversible Faraday reactions. The ohmic resistance of the electrolyte and the bulk material is considered by adding the resistance Rs. The ohmic resistance of the electrolyte and the bulk material are considered within the resistance Rs. A half-cell potential is conventionally added to the model; however, for the case of disposable Ag-AgCl such potential can be assumed to be negligible; thus reducing the electrode-skin impedance to the following equations (seen in Eq. 5-1 and Eq. 5-2):

$$Z_{\mathbb{R}} = R_s + [R_d/(1 + \omega^2 R_d^2 C_d^2)] \qquad \text{Equation 5-1}$$

$$Z_{\mathbb{I}} = -{(\omega R_d^2 C_d)}\Big/{(1 + \omega^2 R_d^2 C_d^2)} \qquad \text{Equation 5-2}$$

The stratus corneum's composition and thickness will have a direct effect of the skin's relative capacitance, the ions concentration and particularities of the gel electrolyte also have a direct effect on the electrode-skin impedance (McAdams, Jossinet, Lackermeier, & Risacher, 1996). This becomes evident when considering that two medium barrier exist, one between the metallic element of the electrode and the gel, and one between the gel and the skin. Further reasoning extrapolates that factors affecting the before mentioned elements, will also have an effect of the electrode-skin impedance. For instance, sweat glands not only introduce moisture, also represent a venue that bypasses the stratus corneum altogether, and have been found to lower the overall impedance after more than 15 minutes of continuous usage (Basio & Prasad, 2006). Such reaction can be clearly explained by the hydrophilic effect the gel has on the skin. Interestingly, skin colour seems to have an effect on the associated capacitance, where light skin individuals seem to have a thinner stratum corneum when compared to darker skin individuals, thus affecting the value, which ranges from 20 nF to 6 nF (McAdams, Jossinet, Lackermeier, & Risacher, 1996). Even gender has a counterintuitive effect, where female skin is found to be 50% thicker (Schmitt & Almasi, 1970), while other factors such as obesity, hydration, neuromuscular diseases, anorexia, etc., seem to also have an effect (Kyle, et al., 2004).

Ag/AgCl electrodes were chosen for the present study since they are among the most common electrodes for biopotential measurements and have been widely studied. They possess a number of convenient characteristics, such as low offset voltage, resistance and polarization, low rate of drift, low noise level; while being suitable for both DC-coupled recording and time-constant AC-coupled recording (Tallgren, Vanhatalo, Kaila, & Voipio, 2005).

5.1.1 *Experimental Methodology*

In order to study first-hand the variability of the electrode-skin impedance, a series of *in-vitro* (Agar based) and *in-vivo* (human assays) experiments were performed with commercially available disposable paediatric Ag/AgCl foam electrodes, of 1 cm of diameter core and 3 cm of diameter foam (DORMO, ref SX-30). A conventional three electrode setup with a Gamry Series G-300 Galvanostat with 50 µA peak to peak AC stimuli compatible with IEC 60601-1 standard and ANSI/AAMI EC12:2000 recommendations (AAMI, 2000), was performed in a controlled environment as to ascertain both inter and intra-individual variability. In order to improve understanding of the experiments described in the following sections, a brief explanation of related experimental methodology follows.

The methodology was conceived in collaboration with the *Escola Superior de Technologia da Saúde do Porto of the Instituto Politechnico do Porto* (ESTSP-IPP), through Prof. Cláudia Silva and Prof. Rubim Santos, who agreed upon characterization strategy and traditional "fault scenarios", such as poor skin preparation and prolonged usage of disposable electrodes. The experiments were performed with collaboration from students of the biomedical program from

the Universidade do Porto, Faculdade de Engenharia (through a supervised project) Miriam Machado and Gonçalo Rios, a visiting ERAMUS student from the *Universidade de Brasília*, Luan Costa, and Prof. Carlos Fonseca of the Departamento de Engenharia Metalúrgica e de Materiais of FEUP.

2-3-4 Electrodes Setup

Depending on the specific target of the measurements, different setups are required; and in the case of electrode involvement there exists an associated taxonomy, where common designations are: Working, Reference and Counter (or Auxiliary) (Gamry Instruments, Inc., 2011). The "working electrode" refers to the electrode under study, while the counter, or auxiliary electrode, denotes the one that completes the current path, most likely connected to the current source or sink. The reference electrodes are the ones utilized as reference points, as to serve for potential measurements. Figure 5-3 illustrates a potential map across a sample or cell, where the letters (A thru E) mark possible potential reference points, and the vertical lines demark the target cell frontiers. Based on the previous descriptions, position A would denote the working electrode, while position E would refer to the counter electrode. The position of the reference electrodes would depend on the specific electrode arrangement, i.e., two-, three-, or four-electrode.

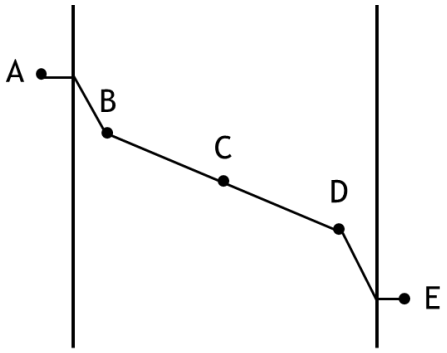


Figure 5-3 — Potential map across a generic sample with mark reference points.

The n-electrode designation refers to the number of reference points considered within the measurement. In the case of a two-electrode setup, only two points are utilized as potential references, which in the case of Figure 5-3, would be represented by points A and E. In the case of the Gamry G-300, this does not signify a reduction in the involved connectors[4] (Figure 5-4 displays the Gamry's available leads), just a specification of the connections arrangement, i.e., the working and working sense (the reference electrode associated to the working electrode) are connected to each other (in reference point A), as are the counter and reference electrodes (in reference point E). The two-electrode setup encompasses a measurement that covers multiple elements, which include the electrodes themselves (both working and counter) and the target

[4] The counter sense lead is utilized for zero current arrangement; therefore it was not utilized in the present measurements. The floating ground was connected to the Faraday cage in combination with the earth ground lead not included in Figure 5-4 display.

cell. The before mentioned setup is convenient for testing purposes, since it reduces overhead and establishes a pairwise electrode relation.

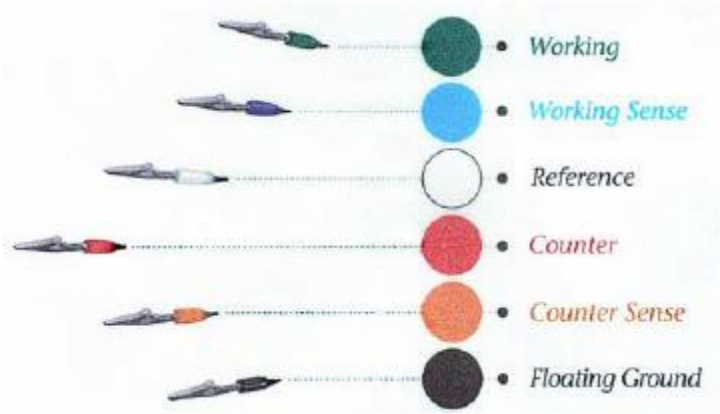


Figure 5-4 — Gamry colour coded leads, extracted from (Gamry Instruments, Inc., 2011).

The three-electrode setup is quite common, adding a separate reference electrode (generally close to the working electrode). Referring once more to Figure 5-3, the reference electrode would be represented by position B. The advantage is that the effects of the counter electrode are not considered within the measurement; due to the potential difference considered between points A and B (a negligible amount of current is considered to enter the reference electrode, therefore $I_{A-B} \approx I_{A-E}$).

Finally, the four-electrode setup, as seen in Figure 5-5, utilizes two reference electrodes. In this scenario the working sense and reference electrodes would be represented by positions B and D in Figure 5-3. The advantage of such arrangement is that is does not include the influence of the electrodes themselves, leaving only the target cell; considering of course, negligible amounts of current going towards the working sense and reference electrodes.

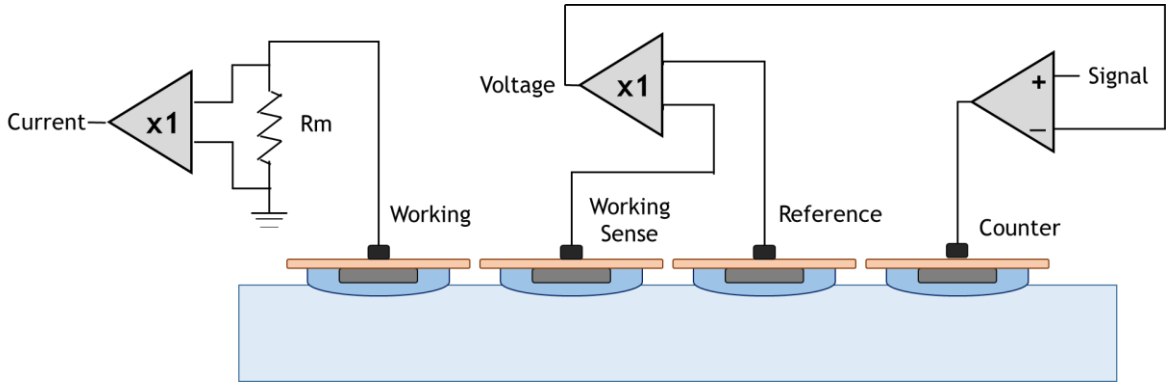


Figure 5-5 — Four-electrode setup.

All three setups where utilized in the following described experiments, each with specific measurement targets.

5.1.2 *Electrode-Agar Experiments*

A number of electrode-Agar experiments were undertaken in order to better understand the electrodes variability, without unknown factors introduced by the human skin. These

experiments followed similar procedures as those used by Dr. Tallgren's group in their experiments; in particular, the Agar-gel preparation conforms to the specifications described within the referenced article (Tallgren, Vanhatalo, Kaila, & Voipio, 2005).

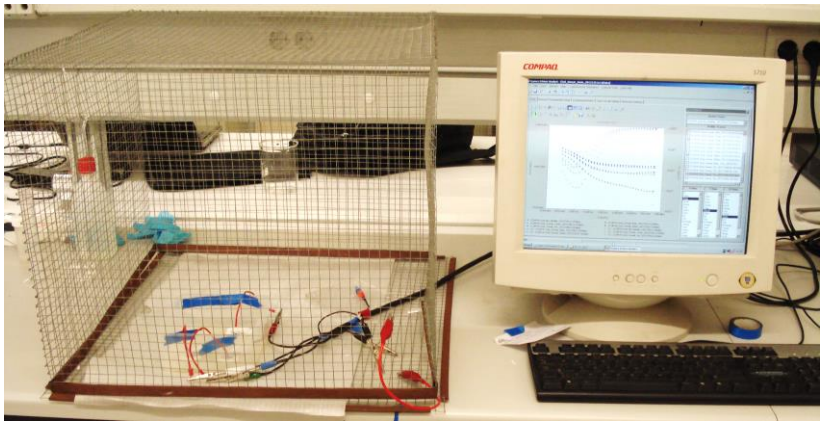


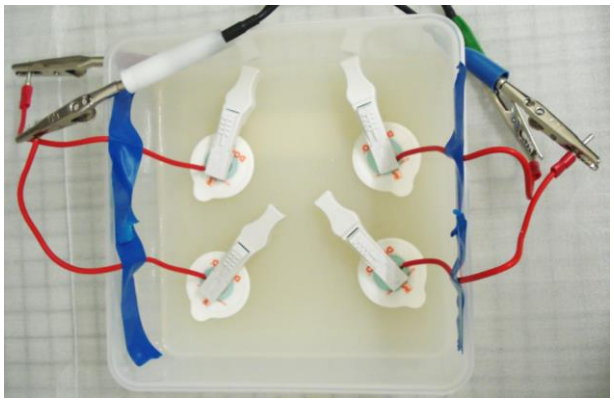
Figure 5-6 — Electrode-Agar experimental setup. Left side: Faraday cage and agar-gel container with Gamry G-300 leads. Right side: monitor with acquisition software displaying time-lapsed magnitude/phase measurements.

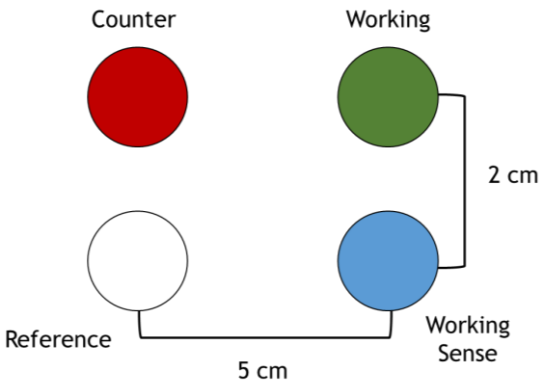
For the Agar-gel a solution of NaCl was dissolved in distilled water (150 mM) and heated until boiling point. Agar powder (3% w/v) was added slowly while stirring and the result placed in a container and left to solidify and stabilize for at least one hour. The resulting Agar-gel was then measured using a four-electrode arrangement as to determine the impedance characteristics of the gel without influence of the electrodes, in order to insure a reduced impedance (as to not influence the experiment's objective). The measured impedance was consistently between 18 – 22 Ω with less than 0.1 degrees mean and less than 0.15 degrees average deviation in the 0.1 – 100 Hz region. Special electrode clamps were utilized to insure a proper connection with the Gamry system's leads, while a Faraday cage surrounded the experiment as to reduce noise sources; the complete setup can be observed in Figure 5-6, while Figure 5-7 presents a close-up of the four-electrode arrangement for an electrode-Agar measurement and a colour coded diagram of the setup (colours relating to the Gamry's lead coding).

Once the characteristics of the gel were verified, experiments relating to the electrode-Agar interface were undertaken utilizing a three-electrode arrangement, as seen in Figure 5-8. All experiments were performed in the same controlled laboratory environment (regulated temperature and humidity), which included:

- Electrode-Agar characterization under normal conditions.
- Electrode-Agar characterization under normal conditions with electrode containing factory permitted imperfections, i.e., air bubbles within the electrode's gel.
- Electrode-Agar time-lapsed characterization during prolong period (+8 hours).
- Electrode-Agar characterization with partially blocked electrode.

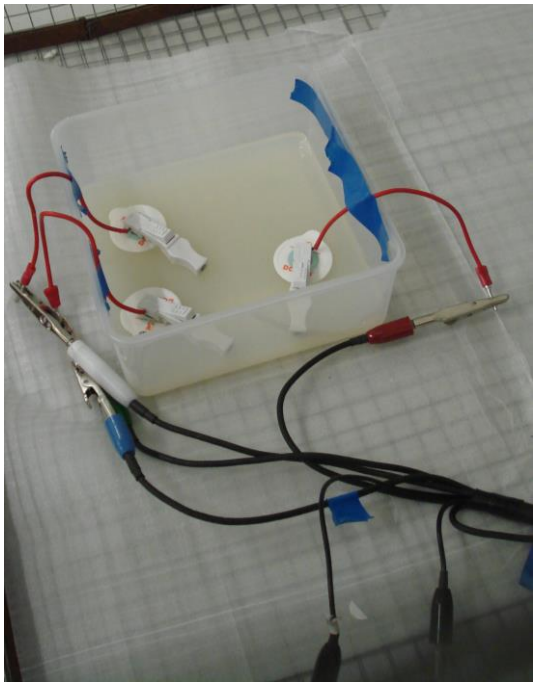
Additional experiments were also performed to gain a sense of different elements effects to the electrode-Agar characterization which included: electrode exposure to differing temperatures, pressure, exposure to artificial sweat, and electrical damage. The before-mentioned additional experiments will be summarized towards the end of the section.

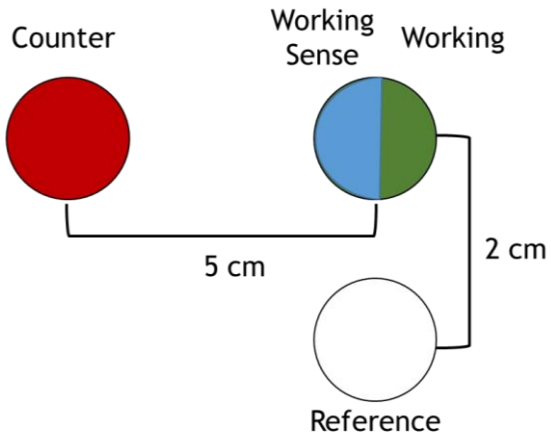




(a) (b)

Figure 5-7 — Four-electrode arrangement for agar-gel impedance measurement. (a) Experimental setup. (b) Colour coded diagram.





(b)

Figure 5-8 — Three-electrode arrangement for electrode-agar-gel impedance measurement. (a) Experimental setup. (b) Colour coded diagram.

Electrode-Agar characterization under normal conditions

Utilizing the three-electrode arrangement presented in Figure 5-8, five electrodes were characterized (as working electrodes) under similar environmental (laboratory climate control) conditions, allowed to stabilize for 5 minutes and using exact acquisition apparatus settings for galvanostatic operation:

- Starting frequency: 0.1 Hz.
- End frequency: 100 kHz.
- Points per decade: 10.
- Current: 50 μA AC, 0 DC component.

The results can be seen in Figure 5-9, where one can observe that even for similar conditions a fluctuation of the measurements exists, with an average deviation of 57 Ω for the magnitude

and 1.6 degree for the phase in the frequency region of interest (two outliners points were removed from consideration in the 1 Hz to 10 Hz region, since they presented consistently random deviations associated with the measurement equipment's mechanics). Such fluctuations can be easily explained through the introduction of surface contact variations, pressure of the electrode-Agar interface, among other factors, overall the deviation for the magnitude were mostly uniformly distributed; however, such is not the case for the phase, which has a peak average deviation at the 1 Hz mark with 4.8 degrees. The 1 Hz mark is of particular significance in this scenario due to its proximity to the negative peak of the phase, making such region of increase variability in the phase perspective.

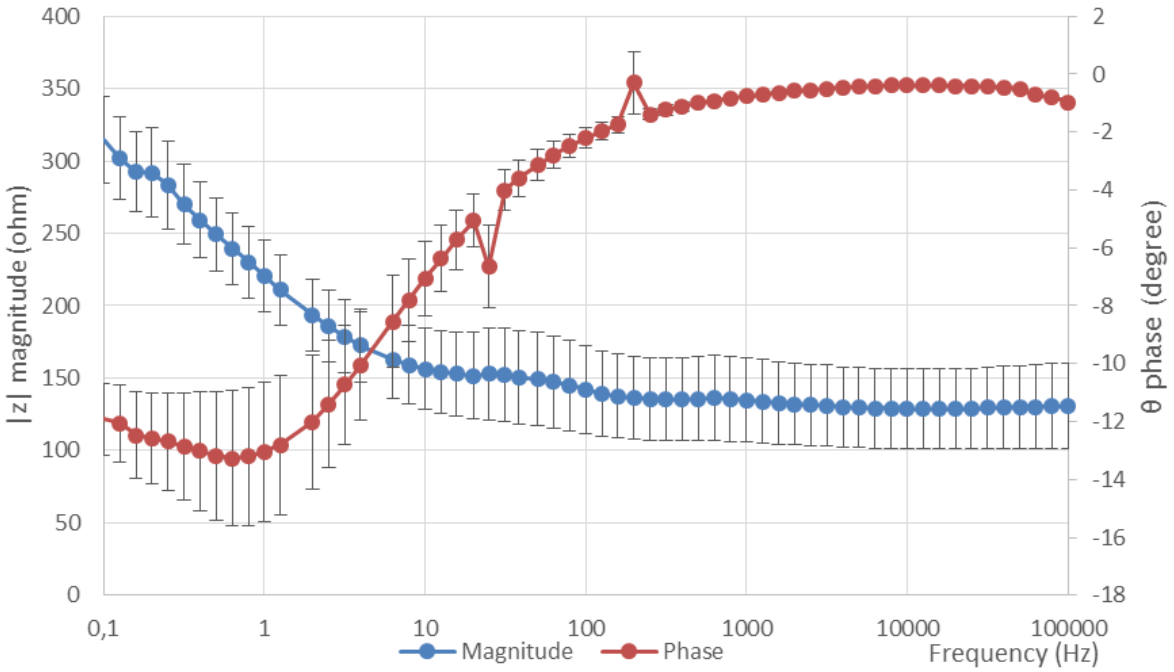


Figure 5-9 — Three-electrode arrangement for Ag-AgCl to agar-gel measurement in normal conditions.

The resulting tendencies of magnitude and phase are in accordance with the electrode-skin impedance response reported in literature, as well as the measurement presented by (Tallgren, Vanhatalo, Kaila, & Voipio, 2005). The difference observed is in the presence of a shift of the curves towards the low frequencies, marking the difference of the Agar-gel with actual skin. That consideration aside, the response proved appropriate for the experimental process at hand. The 57 Ω average deviation reveals a sensitivity that might prove challenging for conventional fault detection methodologies, since conservative analogue fault methods seek the measurement of well-defined components with specific tolerances. In this scenario, the electrodes present a deviation that although relatively small in the scale electrode-skin impedance measurements (which can vary from the MΩ to the tens of kΩ), is relatively significant for measurements such as bioimpedance (in the hundreds of Ω); therefore complicating modelling and associated fault tasks.

Electrode-Agar characterization with electrode containing factory imperfections

Factory imperfections refers to the number of inadequacies that can be observed on the gel of an electrode found within a factory sealed package (disposable Ag-AgCl electrodes conventionally come in packages of fifty). Such imperfections are seldom noticed or considered by healthcare personnel, or by electrode standards themselves for that matter, since the focus lies mostly on their electrical characteristics. Such small imperfections inside the gel introduce small measurement deviations. In order to ascertain the effect of such imperfections, a group of 5 electrodes that presented varying sizes of air bubbles trapped within their gel were characterized following the same methodology as the previously presented experiment. Only the electrode target for characterization presented the air bubble factory imperfection. Three examples of electrodes with air bubbles can be seen in Figure 5-10 (a), (b) and (c).

(a) (b) (c)

Figure 5-10 — (a) Electrode with small air bubble. (b) Electrode with medium air bubble. (c) Electrode with air bubble over the metal section.

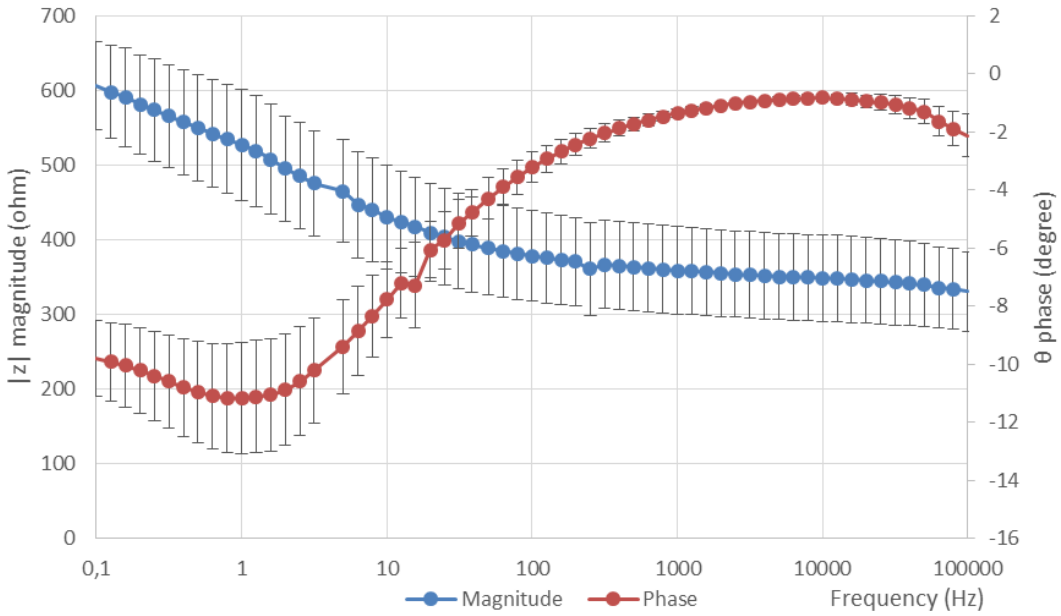


Figure 5-11 — Three-electrode arrangement for Ag-AgCl to agar-gel measurement in normal conditions with electrodes that contain factory imperfections, i.e., air bubbles.

The results seen in Figure 5-11 reveal an increased overall magnitude and an apparent shift of the negative peak of the phase. The mean average deviation is 124 Ω and 1.7 degrees, for the magnitude and phase respectively, with the same increased deviation observed in the 1 Hz region for the phase.

Electrode-Agar time-lapsed characterization

Long-term measurements require the placement of electrodes for prolong periods, however a number of factors come into play regarding the electrode-skin relation that might affect the impedance of the connection. In order to ascertain some of the effects of prolonged usage, electrodes, in three-electrode arrangements, were characterized in 30 minute intervals for at least eight hours.

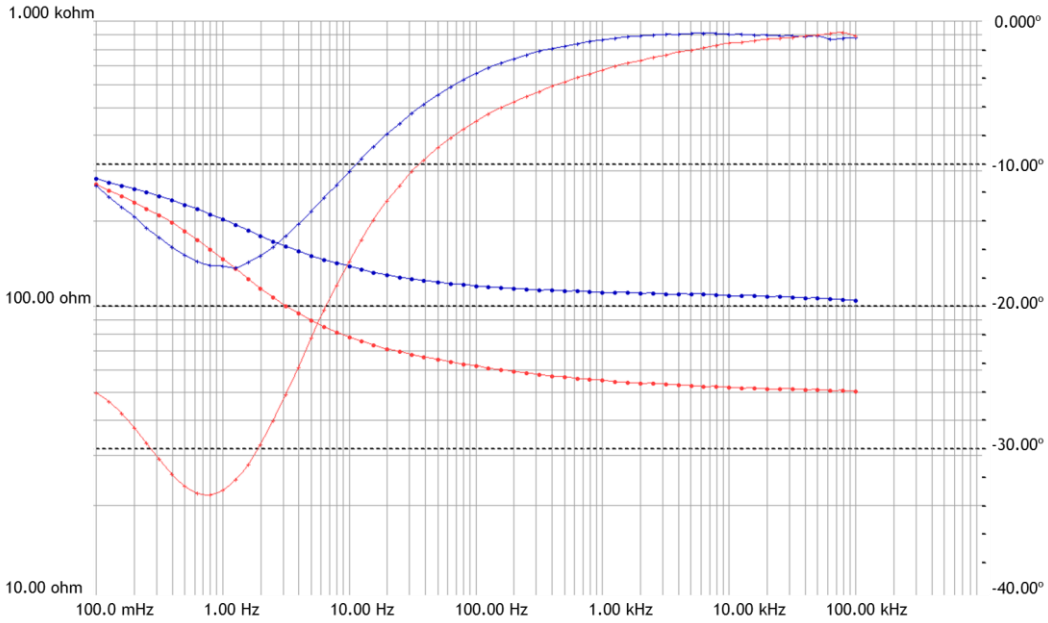


Figure 5-12 — Electrode-agar impedance characterization 12 hours apart.

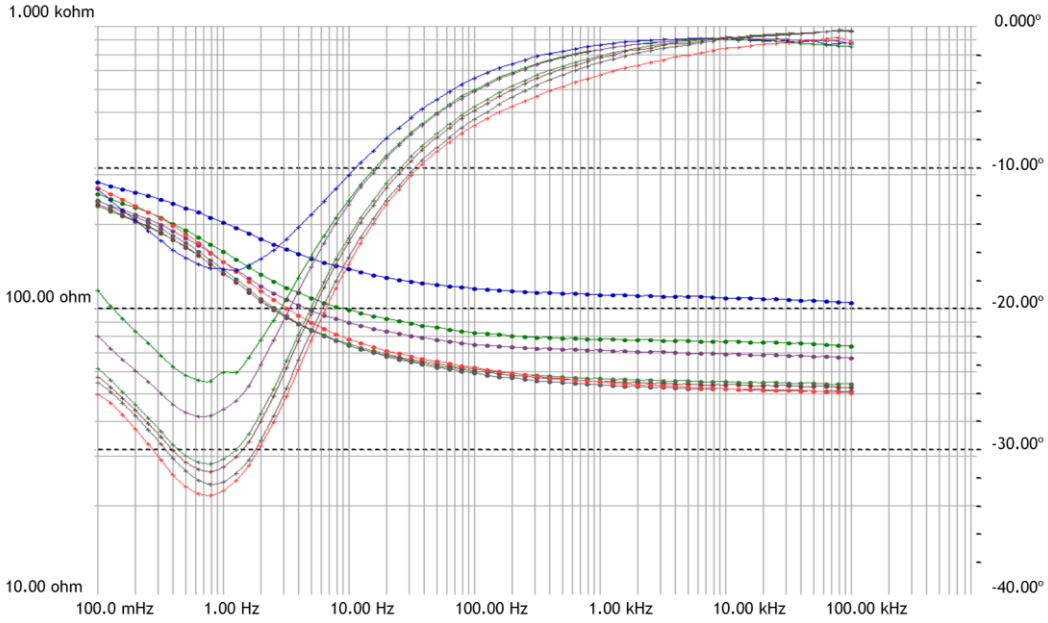


Figure 5-13 — Electrode-Agar impedance characterization first 6 measurements, 30 minutes apart and the 12 hours measurement in red.

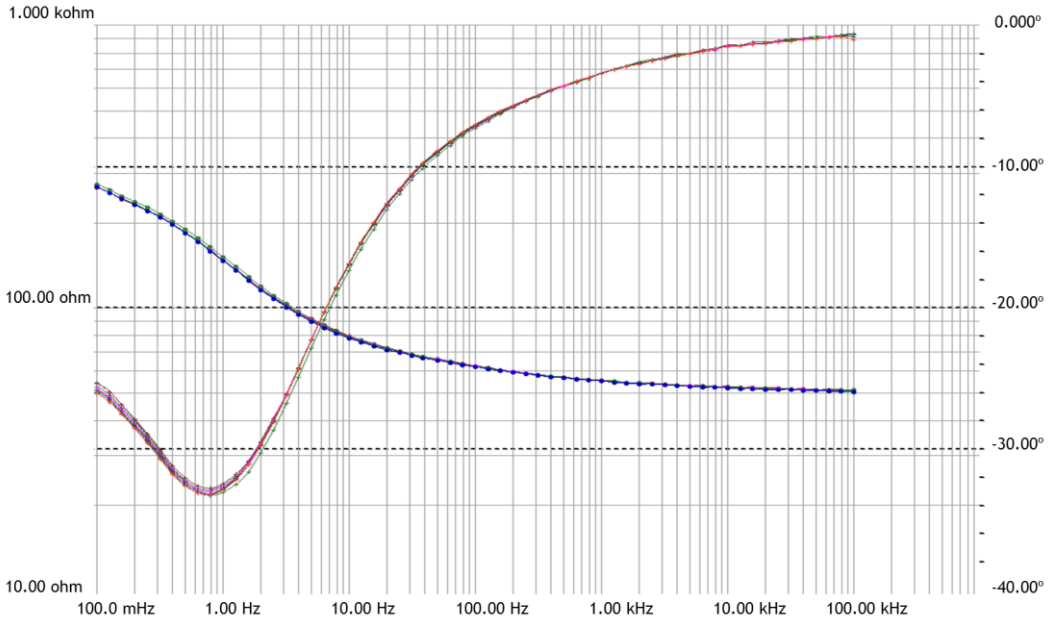


Figure 5-14 — Electrode-agar impedance characterization showing 6 measurements 30 minutes apart starting at the 6th hour.

Figure 5-12 presents two measurements twelve hours apart for the same electrode-Agar experiment. As can be noted, a significant difference on the measured phase can be observed towards the lower frequencies, with a peak difference of ~16 degrees near the 1 Hz mark. In contrast, the magnitude seems to follow an opposing pattern, with the difference becoming accentuated towards the higher frequencies with a peak 51 Ω difference. The observed variation can be explained due to the hydrophilic properties of the electrode's gel, which causes the gel to increase in volume during the experiment, thus increasing the area of contact and lowering the resistance; additionally, temperature equilibration between the two interacting elements takes place. The before mentioned process stabilizes in approximately 6 hours, as can be seen in Figure 5-13. After the stabilization stage, repeated measurements are very consistent in magnitude and phase as seen in Figure 5-14; similar to the effect reported on the electrode-skin interface (Rogers, 2003).

Electrode-Agar characterization with partially blocked electrode.

Occasionally an electrode's adhesive could wear out due to a number of factors such as sweat or friction. This causes the contact area between the electrode and the skin to be reduced, thus affecting the electrode-skin impedance. In order to gain perspective of such scenarios a number of electrodes were partially covered with isolating material, as to limit the contact area between the electrode and the Agar-gel. The resulting measurements can be observed in Figure 5-15, where predictively the reduction of contact area affected the relative electrode-Agar impedance, effectively doubling the impedance magnitude in the lower frequencies and almost quadrupling towards the higher frequencies, between the 75% blockage electrodes and the no blockage electrodes. A noticeable difference between the negative peak phases is also noted, of approximately 5 degrees per scenario.

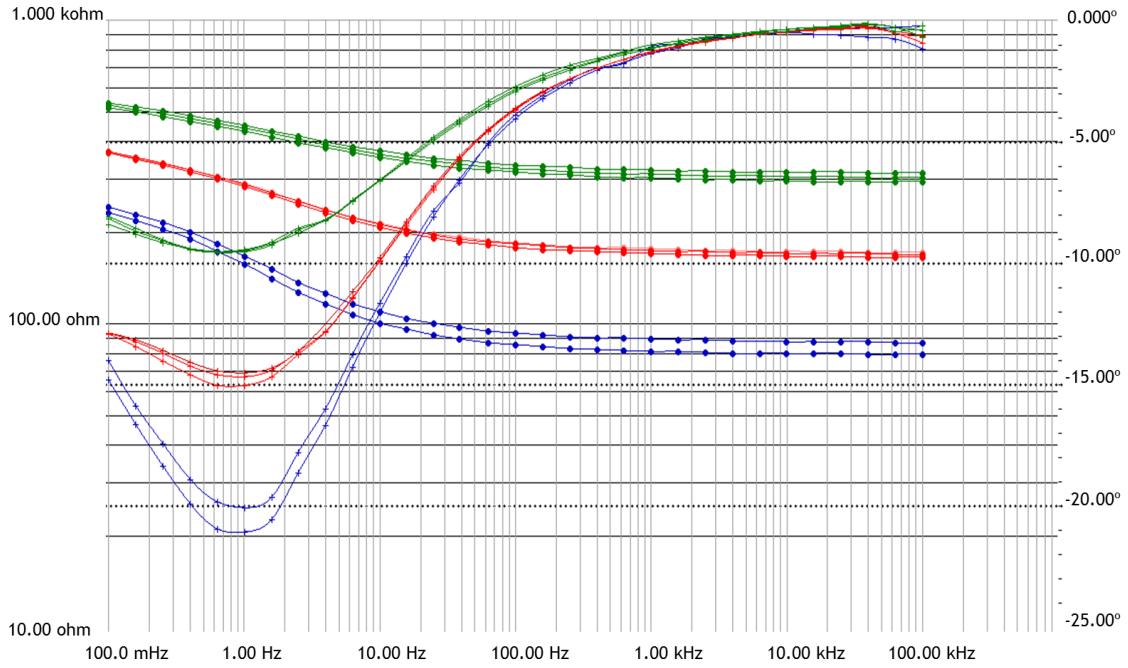


Figure 5-15 — Electrode-Agar impedance characterization for normal scenario in blue, 50% blockage in red and 75% blockage in green.

Summary of additional experiments and conclusions of electrode-Agar experiments

A number of experiments with varying temperatures, electrical damage and even the use of artificial sweat were performed which had no real conclusive results, however offer some insight into possible tendencies. For instance, a number of electrodes were placed in an oven at 70 ºC centigrade for a period of 1 hour, while another group was placed in a -20 ºC freezer for the same period; the electrodes were then allowed to rest for an additional hour at room temperature. The experiment aimed to mimic possible inadequate storage conditions electrodes might experience (although admittedly -20 ºC is an unlikely scenario). Some of the measurements can be seen in Figure 5-16, where the frozen electrodes seem to present higher electrode-Agar impedance, while the oven exposed electrodes present lower impedance in the same range as non-exposed electrodes.

Another experiment exposed electrodes to artificial sweat for varying periods of time from 5 minutes to 1 hour, some of the measurements can be seen in Figure 5-17, and although overall the magnitude seems to have reduced, most likely thanks to the additional Cl^- ions, there seems to be no relation with regards to the duration of the exposure.

Based on the data collected, it can be observed that the electrode-Agar impedance is sensitive to a wide number of variables, some of them cannot be effectively managed, even under controlled conditions such as a laboratory environment. An important finding was that the period of stabilization is much longer than the 5 minutes most healthcare personnel await prior to measurements. That said, electrodes that are to be used for an extended period of time are at times left to stabilize for a larger period of time, such as the case of surgery scenarios, where the personnel allocated the appropriate electrodes with an extended period prior to the surgery; however, if there is a need to replace such electrodes during the event, how is the stabilization

managed for such scenario? This evidences the need for continuous monitoring of the electrode-skin impedance.

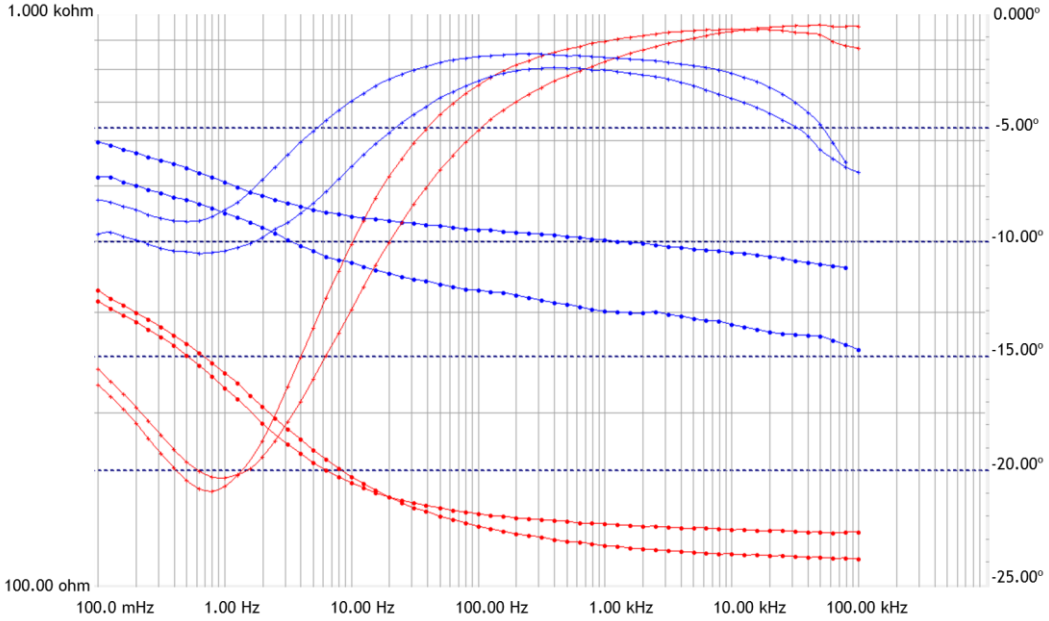


Figure 5-16 — Electrode-agar impedance characterization for 1 hour 70º degree exposed electrodes in red and 1 hour -20 degrees in blue.

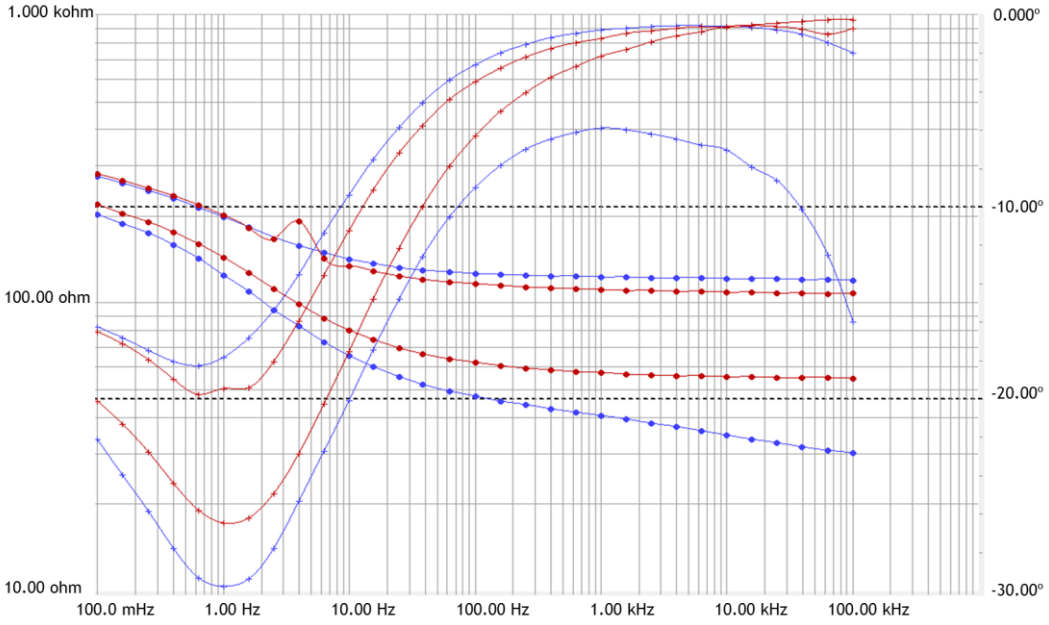


Figure 5-17 — Electrode-agar impedance characterization for 5 minutes (red) and 1 hour (blue) artificial sweat exposed electrodes.

5.1.3 *Electrode-Skin Experiments with Gamry G-300*

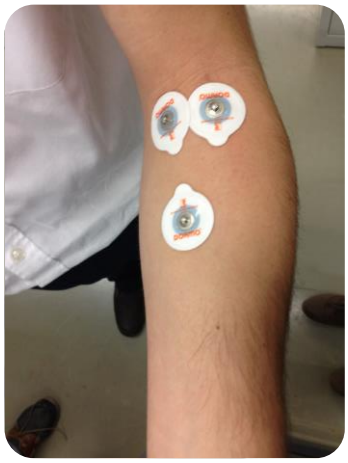
In order to gain insight into the variability of the electrode-skin impedance, a number of measurements were performed on volunteer students of the University of Porto, with the following characteristics:

- Age: mean 22.6 ± 1 years.
- Weight: mean 76.6 ± 14.1 kg.

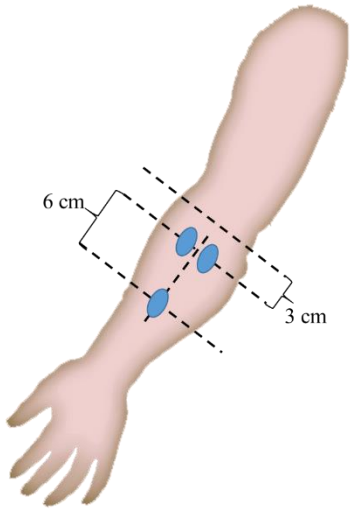
- Height: mean 1.74 ± 0.08 meters.

The skin was prepared with a straightforward technique, limited to light shaving (when required), degreased with alcohol, dead cells removed with a soft brush, later cleansed with soap and water, and the skin allowed to recover for 10 minutes, as seen in Figure 5-18 (a). Disposable paediatric Ag/AgCl foam electrodes, of 1 cm of diameter core and 3 cm of diameter (DORMO, ref SX-30), were placed at the anterior side of the radialis region of the left arm, chosen for its reduced follicle density and electromyographic interference, as seen in Figure 5-18 (b) and (c).

(a)



(b)

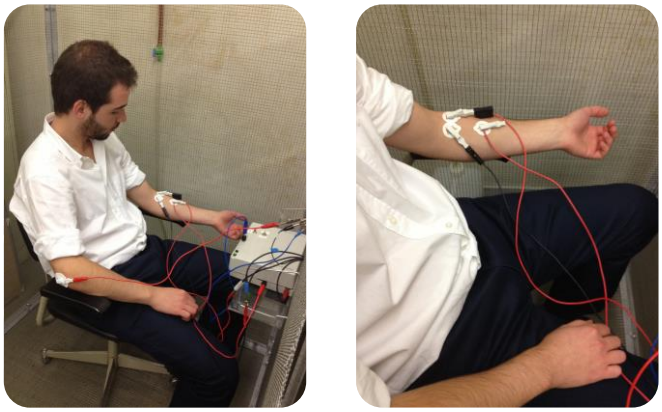


(c)

Figure 5-18 — (a) Skin preparation for electrode-skin impedance measurement. (b) Electrode placement for human electrode-skin impedance measurement. (c) Electrode placement diagram for electrode-skin impedance measurement.

(b)

Figure 5-19 — Electrode characterization setup. (a) Faraday cage view, (b) Current limiter and Gamry characterization equipment view.



(b)

(c)

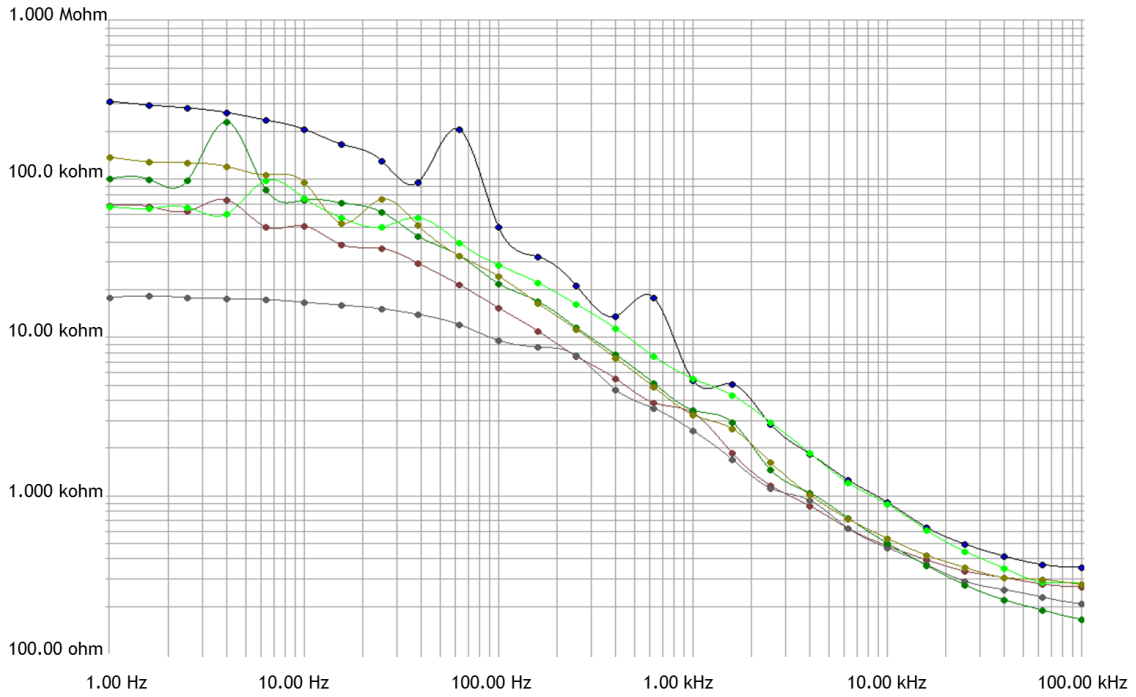
Figure 5-20 — (a) Close-up of volunteer within Faraday cage during electrode-skin impedance measurement. (b) Close-up of arm of a volunteer during an electrode-skin impedance measurement. (c) Volunteer inside Faraday cage during electrode-skin impedance measurement.

A three-electrode arrangement was placed, with the target electrode and its reference roughly 3 cm proximal to the elbow and the signal injection electrode roughly 6 cm from the centre point of the target-reference electrode line, proximal to the forearm mid-point (all measurements where considered from the centre of the electrodes), as observed in Figure 5-18

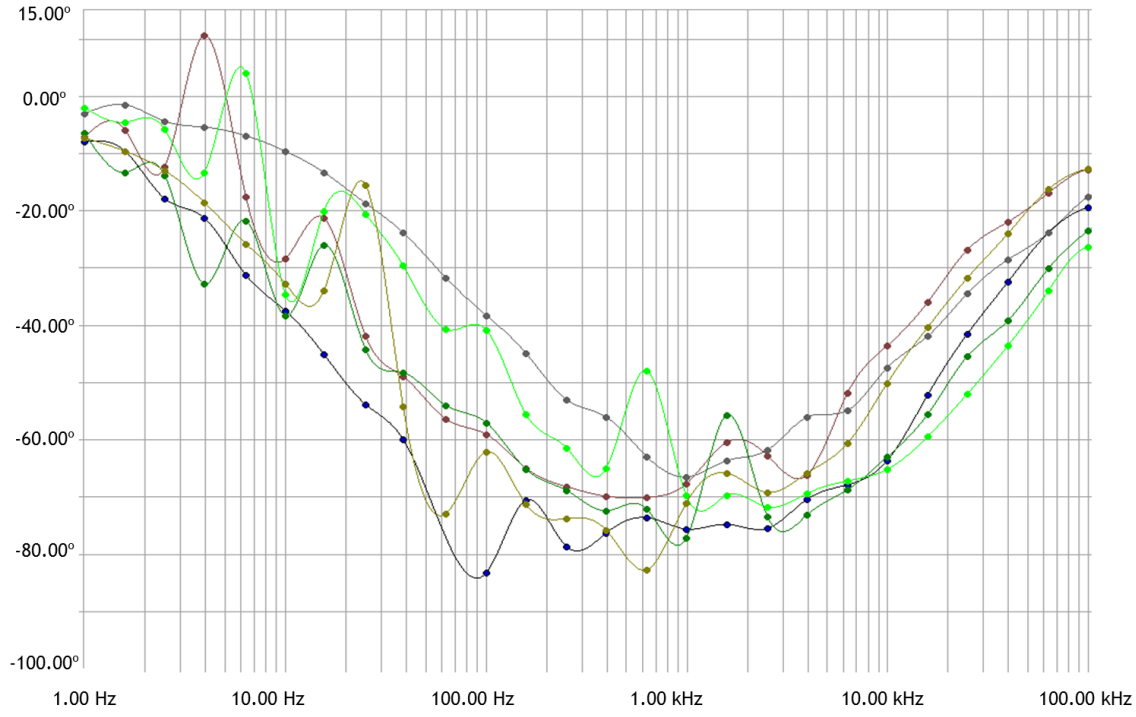
(c) (the ground electrode was located at the contralateral posterior side elbow). The subjects were then placed within a Faraday cage (seen in Figure 5-19 (a) and (b)), in order to reduce electromagnetic noise, in a sitting position with the left forearm resting horizontally (as can be seen in Figure 5-20 (a), (b), and (c)). A GAMRY Series G-300 Potentiostat/Galvanostat, in combination with a high-side overcurrent protection module (following IEC 60601-1 standards), was utilized for measuring the impedance in the 1 Hz to 100 KHz range. The frequency range was chosen taking into account that the electrode-electrolyte impedance dominates at low frequencies (< 1 Hz), the skin impedance dominates at intermediate frequencies (1 Hz < f < 10 KHz) and the underlying tissues impedance dominates at high frequencies (100 kHz < f < 10 MHz) (McAdams, Jossinet, Lackermeier, & Risacher, 1996). A five minute settling period was allowed prior to the first measurement, and the subjects were allowed to stand and move around between measurements; however, they were not allowed to eat/drink or perform any type of strenuous activity.

Figure 5-21 presents initial measurements for six individuals (4 male, blue, light and dark green and grey, and 2 female, yellow and red), from which one can appreciate the similarities and differences. The magnitudes presented in Figure 5-21 (a) all follow the same pattern, similar to the one exhibited by the electrode-Agar measurements. In this case the magnitude at frequency 1 Hz vary from roughly 300 kΩ to 18 kΩ, with most centred around 100 kΩ; such values are within the ones observed in literature (McAdams, Jossinet, Lackermeier, & Risacher, 1996), which can vary from 10 kΩ to 10 MΩ. For such reason healthcare personnel tend to follow a strict skin preparation regime, in order to lower the measured impedance in the lower frequencies under 10 kΩ. In the case of textile electrodes the problems are exacerbated, due to their sensitivity to pressure, fabric stretching, and motion artefacts (Puurtinen, Komulainen, Kauppinen, Malmivuo, & Hyttinen, 2006) (Marquez, Seoane, Valimaki, & Lindecrantz, 2009) (Beckmann, et al., 2010); however, such is outside the scope of the present work.

One can also observe that the phase for all volunteers has a negative peak in the 1 kHz regions, and in general do not present a smooth shape even under controlled conditions. Low frequency measurements tend to be susceptible to noise and random variations due to the prolonged duration and increased noised sources, in particular when compared to high frequency measurements. That said, the region of interest for biosignals is conventionally located under 1 kHz, complicating matters. The arithmetic average of the signals presented in Figure 5-21 can be found in Figure 5-22, with bars representing the average deviation. Overall the phase presents a mean average deviation of less than 4 degrees, peaking near the 50 Hz region. That might be explained by the electromagnetics properties of the human body and the ambient noise which typically presents a problem in the 50 Hz region. The magnitude variation on the other hand, seems to have proportionality towards the lower frequencies; where it can be argued that the particularities of the skin accentuate the electrode-skin dynamics.



(a)



(b)

Figure 5-21 — Electrode-skin impedance measurement for time 0 min of 4 male and 2 female student volunteer. (a) Magnitude. (b) Phase.

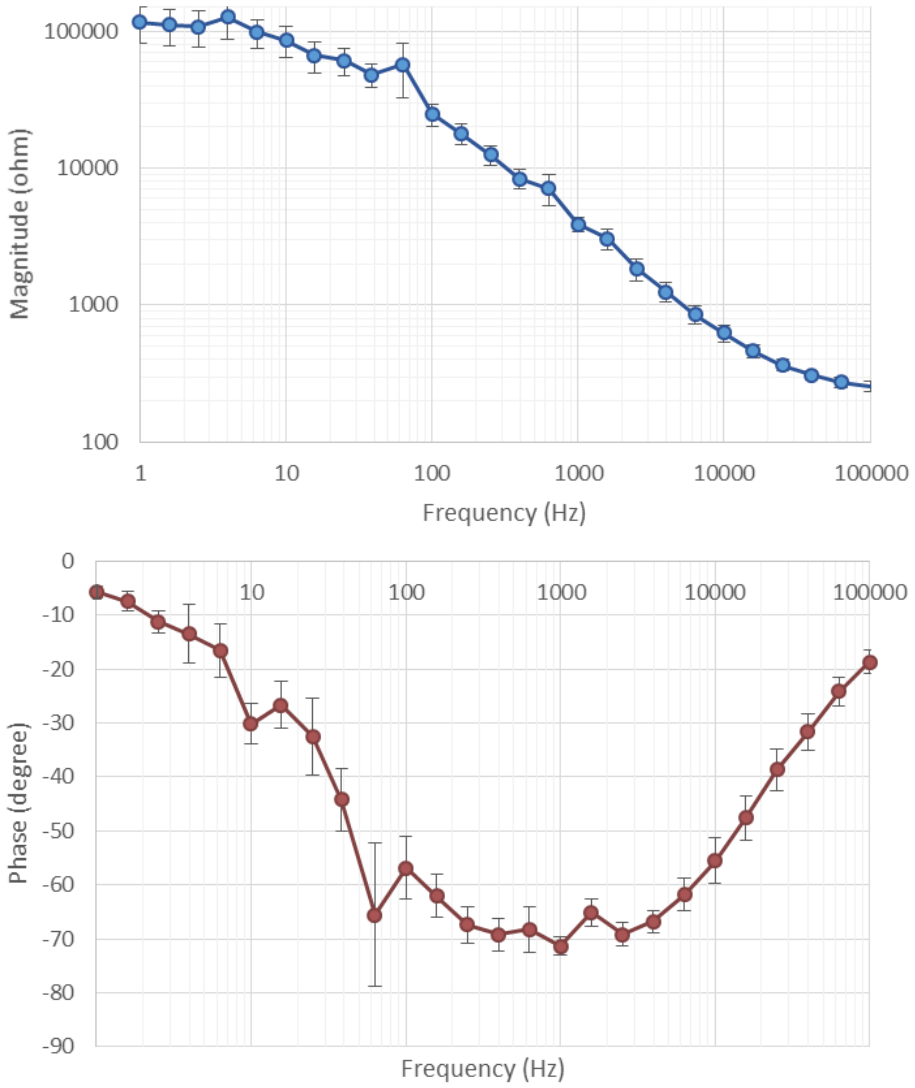


Figure 5-22 — Electrode-skin impedance measurement average with average deviation bars (top) magnitude. (Bottom) Phase.

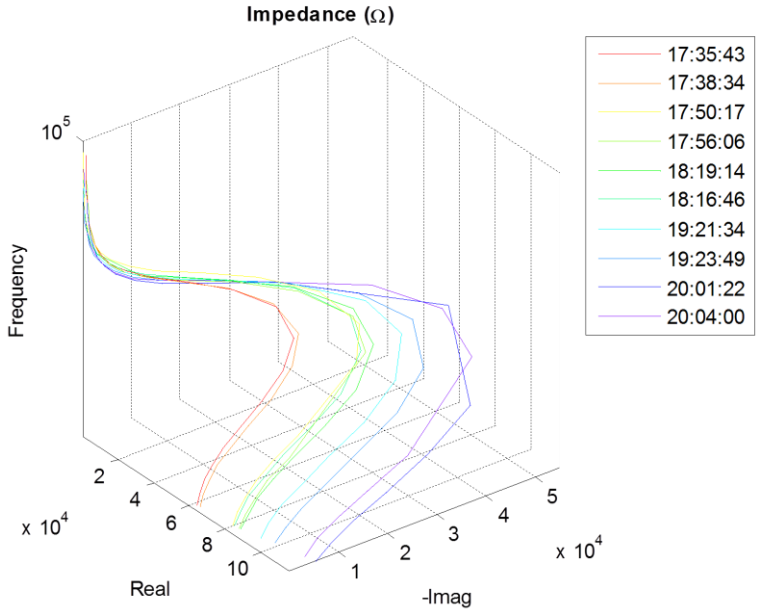


Figure 5-23 — Time lapsed three-electrode arrangement measurements on male subject.

Figure 5-23 summarizes the measurements of an electrode-skin impedance of a male volunteer. As can be observed, a similar stabilizing phenomenon occurred as in the case of the electrode-Agar. The same behaviour can be observed in Figure 5-24, in this case for a female volunteer with measurements performed up to 3 hours apart; and in Figure 5-25 for a different male volunteer. In this case the male volunteer presented low frequency impedance in the 3-4 MΩ range.

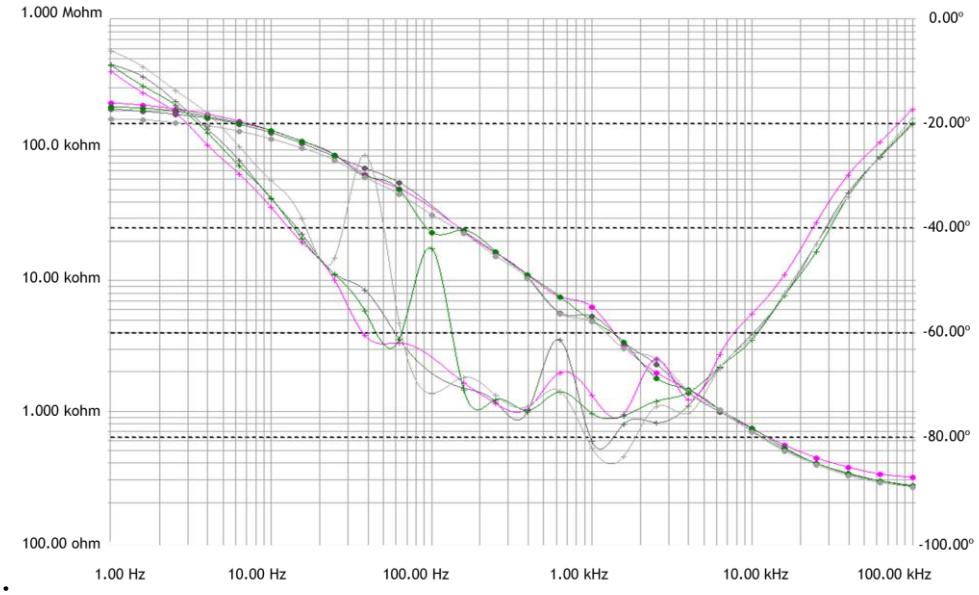


Figure 5-24 — Electrode-skin impedance for female volunteer: 0 min. (pink), 30 min. (green), 1 hours (light grey), and 3 hours (dark grey).

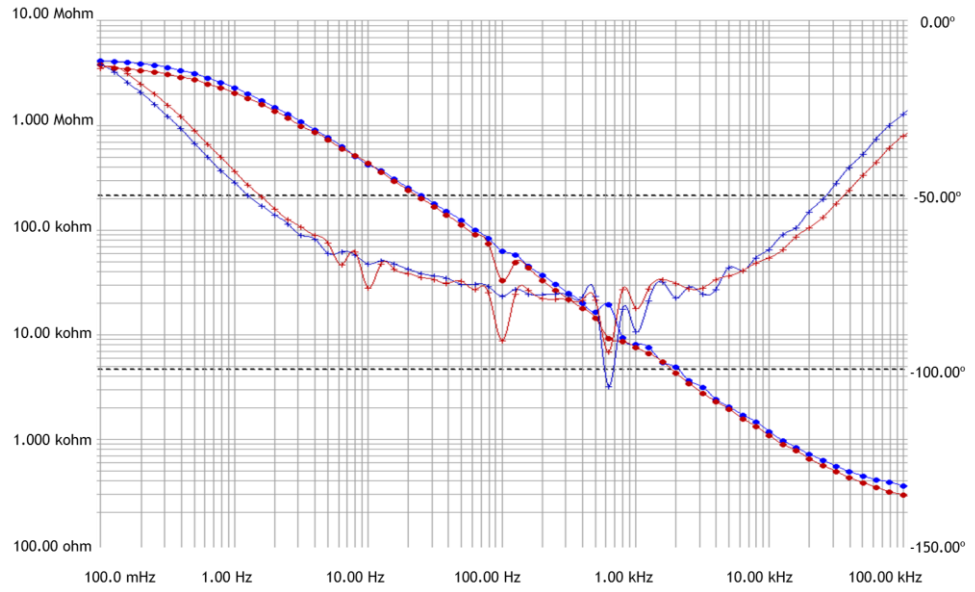


Figure 5-25 — Electrode-skin impedance for male volunteer: 0 min (blue), 2 hours (red).

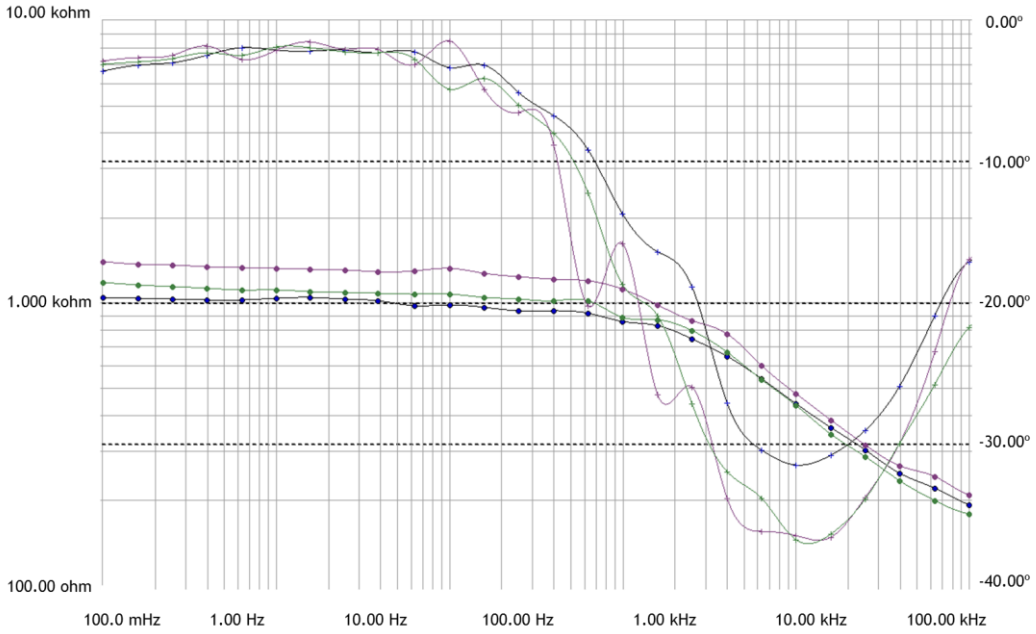


Figure 5-26 — Electrode-skin impedance for male volunteer: 0 min (purple), 1 hour (green), and 3 hours (blue).

In the case of Figure 5-26, one can observe an unusual case, where the low frequency impedance is near the 1 kΩ. As with the case of the volunteer presented in Figure 5-25, this extreme case scenario can present complications to a fault detection strategy based on traditional thresholds approach, since the connection might be discarded as faulty due to the unexpected low impedance.

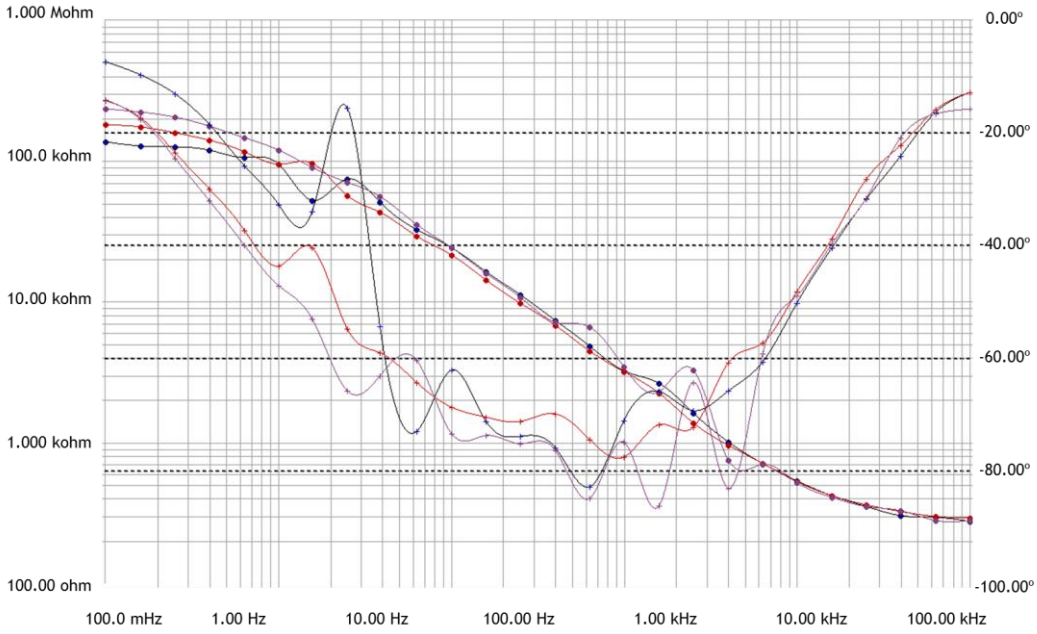


Figure 5-27 — Electrode-skin impedance for female volunteer: 0 min (blue), 15 min. (purple), and 2 hours (red).

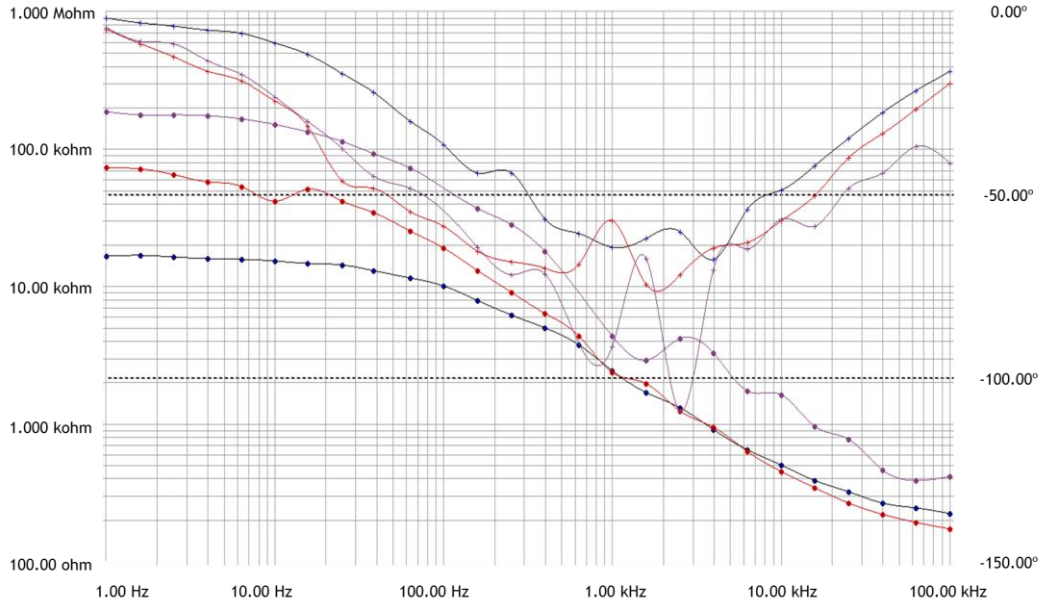


Figure 5-28 — Electrode-skin impedance for male volunteer: 0 min (blue), 15 min. (purple), and 3 hours (red).

Figure 5-27 and Figure 5-28 present two additional scenarios of concern. For instance, both volunteers experienced an increase of the electrode-skin impedance minutes after the initial measurements, and only after sometime that impedance decreased, however not under the initial measurements. A number of factors can occur to justify such behaviour: minor repositioning of the electrode caused by friction and arm movement, initial inflammation of the tissue as reaction to the electrode, white coat syndrome, among others (McAdams, Jossinet, Lackermeier, & Risacher, 1996). Also of note, is the difference in variation of the different volunteer, for instance in the case of Figure 5-28, one can observed changes from the low tens of kΩ to the low hundreds of kΩ, while for Figure 5-27 the variations are concentrated in the low hundreds of kΩ. All these factors need to be considered when selecting and/or designing the testing strategy and methodology.

5.2 Case study: Force Sensing Resistors

Force sensing resistors (FSR), or force sensitive resistor, are not as well studied as electrodes, however their entrance within the personal monitoring field is swiftly increasing their presence in literature. FSR's flexibility, thinness, durability and low cost, make them an ideal sensor for pressure related measurements, such as postural (Gopalai, Senanayake, & Gouwanda, 2011), gait (Huang, Chen, Shi, & Xu, 2007) (Jang, et al., 2010) (Khazraee, et al., 2013) and muscle activity (Orgis, Hreil, & Lukowicz, 2007) analysis. Such interest has driven a need for calibration, linearization, and compensation strategies for the FSR response conditioning (Hall, Desmoulin, & Milner, 2008) (Florez & Velasquez, 2010) (Barnea, Oprisan, & Olaru, 2012).

FSR present a continuous resistance change inversely proportional to the applied force, which can vary from ten grams to tens of kilograms; while having a thin profile (conventionally less than 0.5 mm), low cost, and are resistive to shock and environmental hazards. These variable

resistors can be manufactured in a wide variety of sizes, and in single or array configurations (some examples can be seen in Figure 5-29-left).

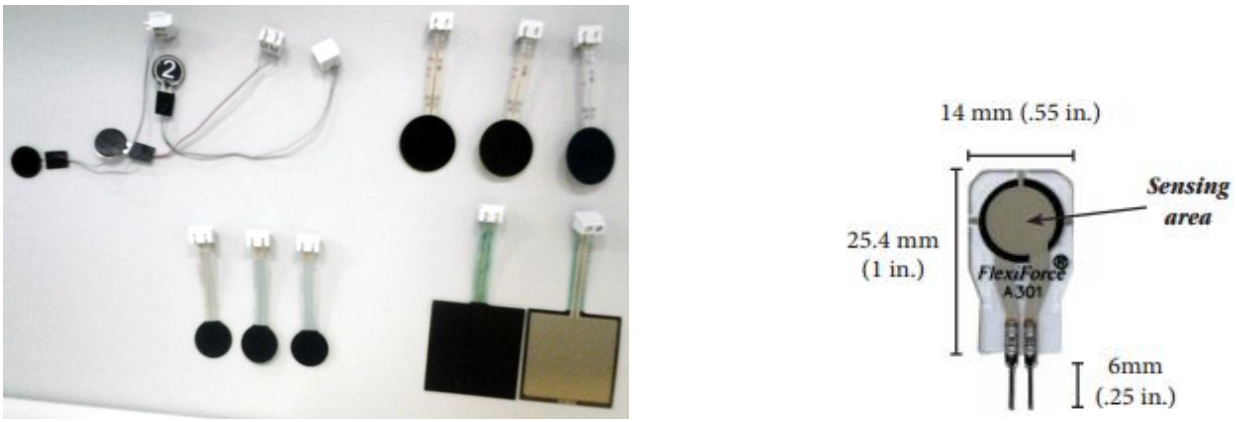


Figure 5-29 — Variety of FSR (left). FlexiForce model A301 actual size picture extracted from (Tekscan, 2014) (right).

Recent advances in FSR fabrication have greatly improved the thickness, linearity, repeatability, hysteresis and drift; as well as improving their durability. For example the FlexiForce model A301 from Tekscan® (a well-known manufacturer of commercially available FSR) presents the characteristics seen in Table 5-1 (Tekscan, 2014); the actual size A301 FSR can be seen in Figure 5-29 (right).

Table 5-1 FlexiForce model A301 specifications.

Property	Value
Thickness	0.203 mm
Length	25.4 mm
Width	14 mm
Sensing Area	9.53 mm diameter
Pin spacing	2.54 mm
Linearity	< ± 3 % (from 0 to 50% load)
Repeatability	< ± 2.5 % (80 % full force applied)
Hysteresis	< 4.5 3 % (80 % full force applied)
Drift	< 5 % constant load

The general structure of FSR can be seen In Figure 5-30, revealing the simplicity and elegance of their design; conventional variations have interdigitating electrodes instead of two pressure sensitive pads, generally based on a proprietary semi-conducting polymer, separated by spacers creating an air gap between them, such air gap is connected to an air duct which permits the flow of air into and out of the FSR.

From a circuital perspective a number of configurations can be utilized for interacting with a FSR, such as any number of current-to-voltage circuits, threshold switch setups, Schmitt trigger

oscillator or really any scheme that permits a quantifiable relation between a resistance and an output voltage/current; one such strategy can be seen in Figure 5-31. Direct consultation with manufacturer Tekscan® Inc., as well as preliminary analysis, revealed an expected capacitive component present within the FSR model; although a complete archetypal is seldom utilized by traditional methods, such characteristic proves useful for presence determination, since an FSR's no-load resistance tends to be higher than 1 MΩ, making them a hard target to identify. A general model of FSR can be seen in Figure 5-32.

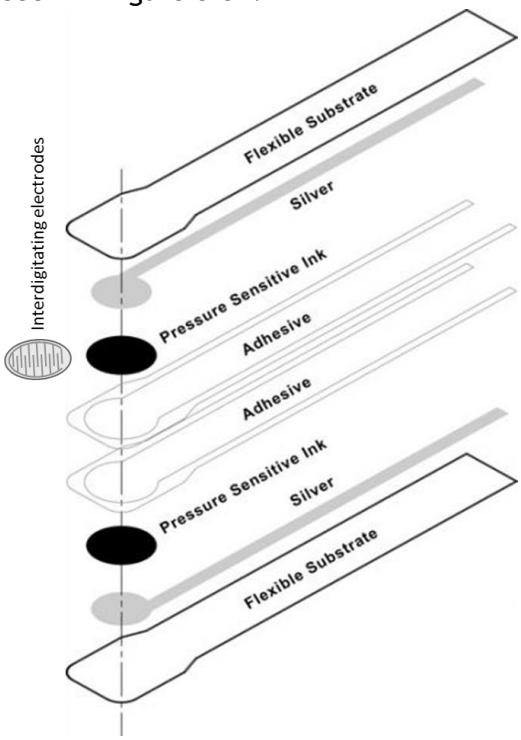


Figure 5-30 — FSR general structure, modified from (Tekscan, 2014).

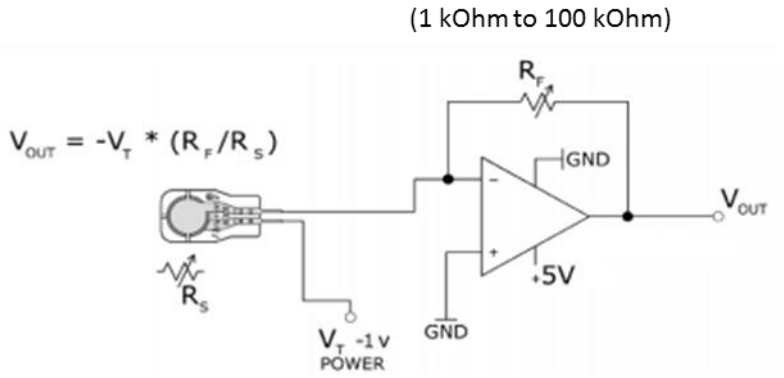


Figure 5-31 — Conventional electrical setup for FSR usage.

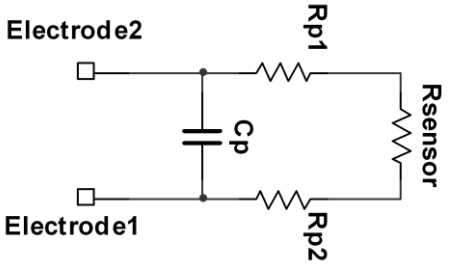


Figure 5-32 — Generic model for FSR, extracted from (IEE International Electronics and Engineer, 2007).

While fairly reliable, FSR are sensitive to pre-loading due to offset mounting, permanent loading signal drift, bending related pre-loading, broken connectors, and air duct blockage related issues; such concerns are related to the physical variations the structure of the FSR experiences. A setup was developed for FSR characterization, undergoing controlled pressure experimentation, utilizing the Tira Test 2705 tensile testing machine (seen in Figure 5-34), intended to establish controlled stimuli/response scenarios. Such experiments were managed in collaboration with the Department of Mechanical Engineering of FEUP, through Prof. José Esteves. Two arrangements were designed and specific parts were manufactured for repetitive pressure application, one for vertical even pressure and another for a 45 degree angle scenario for friction induction, as seen below in Figure 5-33. The intention of the before mentioned experiments was to produce controlled dynamic pressure and friction scenarios in order to generate characterization patterns profiles, using the PXI setup with the dual supply AFE previously described.

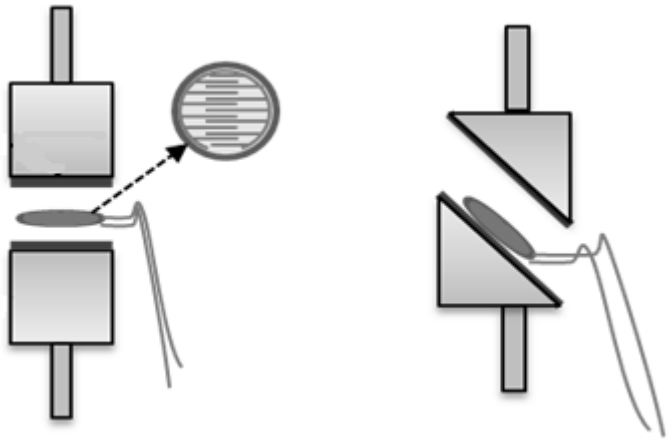
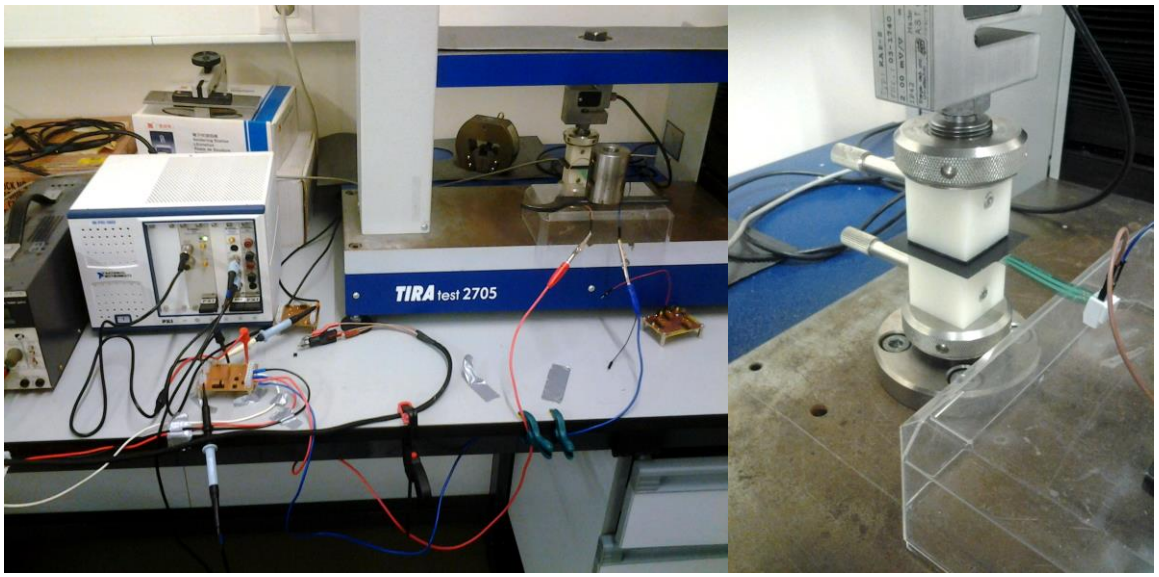


Figure 5-33 — Pressure application setups for FSR characterization.

(a)



(b) (c)

Figure 5-34 — Tira Test 2705 FSR characterization setup. (a) View of complete experimental setup. (b) Close-up of PXI AFE arrangement and TIRA test 2705 pressure arrangement. (c) Close-up of custom made pressure element and FSR.

5.2.1 *FSR characterization experiments with TIRA test 2705*

For these experiments the Interlink Electronics FSR Model 406 was utilized (purchased from Inmotion as INM-0038), a 1.5 inch or 3.81 cm FSR. Such component presents a square profile with a 1.5” by 1.5” (3.81 cm by 3.81 cm) active area and total length of 3.3” (8.38 cm), as seen in

Figure 5-35 and Figure 5-36. This FSR model is composed by a semiconductive layer, based on ultem resin 0.005" (0.13 cm) thick, a spacer layer and a conductive layer, as can be seen in Figure 5-37, with the characteristics present in Table 5-2.

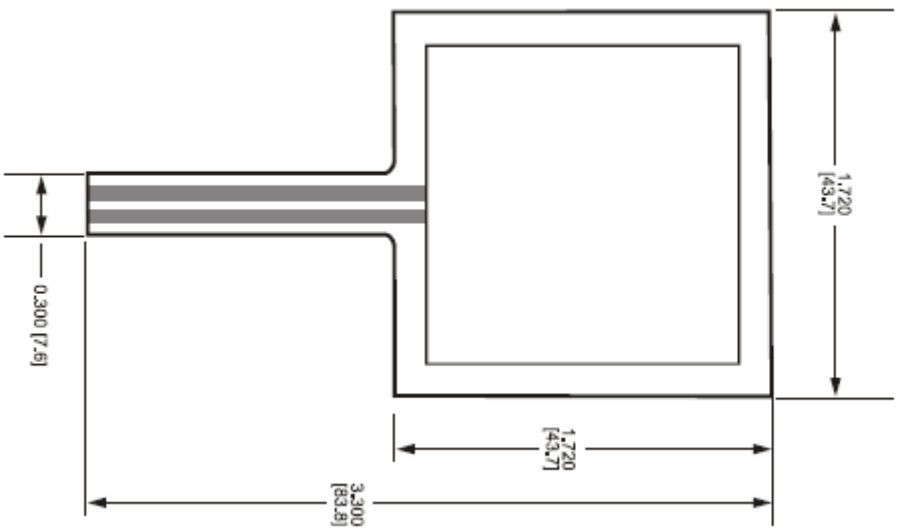
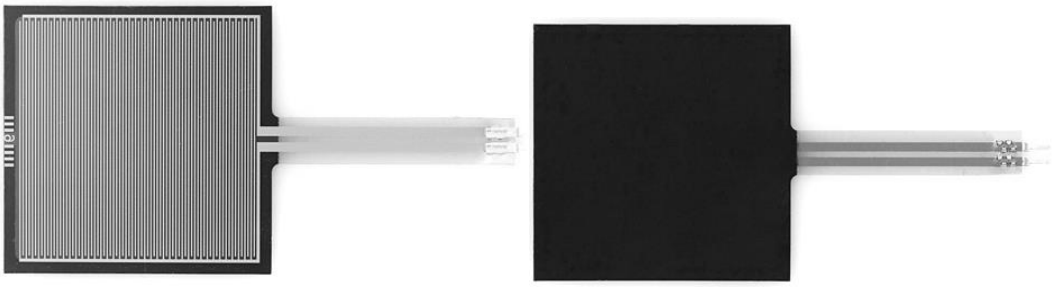


Figure 5-35 — FSR INM-0038 dimension diagram, extracted from (Interlink Electronics, 2010).



(a) **(b)**

Figure 5-36 — FSR INM-0038 (a) Front view. (b) Rear view. Extracted from (Inmotion Inc., 2010).

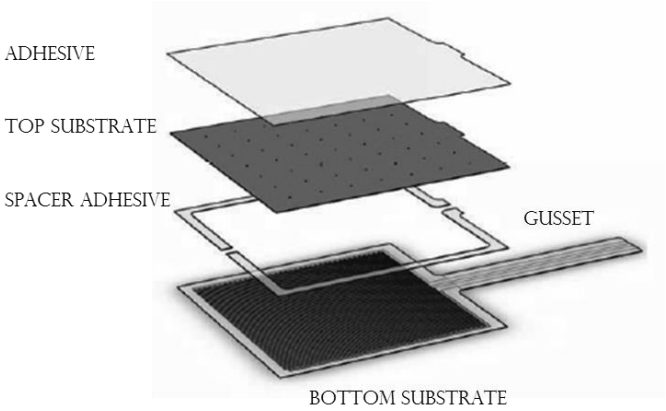


Figure 5-37 — FSR INM-0038 layer stack-up, extracted from (Interlink Electronics, 2013).

Table 5-2 FSR 400 series characteristics, extracted from (Interlink Electronics, 2013).

Property	Value
Actuation Force	~ 0.2 N minimal (typical value)
Force Sensivity range	~ 0.2 N – 20 N
Force Resolution	Continuous (analogue)
Force Repeatability	± 2 %
Non- Actuated Resistance	> 10 MΩ
Hysteresis	+ 10 % Average (RF+ - RF-)/RF+
Tap Durability	- 10% average resistance change (10 Million actuations, 1 kg, 4 Hz)
Standing Load Durability	- 5 % average resistance change (2.5 kg for 24 hours)

The experiments included the characterization of the FSR by continuous pressure measurements (equivalent to a dead-weight scenario), from now referred as TYPE-A measurement, and through stepped pressure changes from a minimal pressure to a maximum pressure, from now referred as TYPE-B measurement. The FSR were later exposed to a number of different performance affecting scenarios such as degradation through friction, bending and blockage of the air duct, among others; only a summary of the results is presented in continuation.

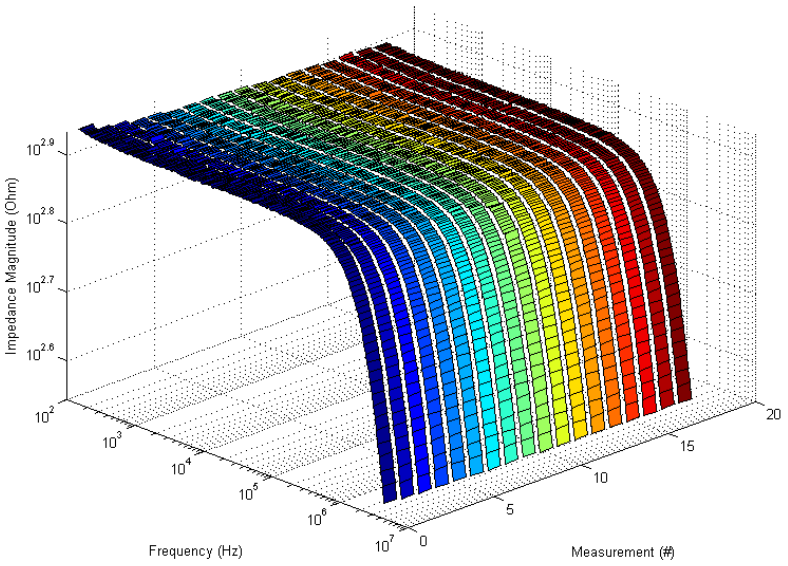
Figure 5-38 presents a set of measurements of the impedance magnitude of a FSR under constant pressure of 10 N performed one minute apart, from 100 Hz to 3 MHz, where one can note a drift effect. The arithmetic average for the 100 Hz to 100 kHz range of all measurements is 798.33 Ω with mean average deviation of 2.4 Ω, and the average cut-off frequency is located around 1.62 MHz (considering conventional $V_{out}/V_{in} = \sqrt[2]{1/2}$). The most significant drift occurs in the first minute with a 1.53 % difference (from ~839 Ω to ~826 Ω), and after 5 minutes the change lowers to less than 0.4 % (with reference to the initial measurement); in total a 7.2 % drift from initial measurement. The associated phase measurements presented in Figure 5-39 (a), reveals less than -1 degree phase for frequencies lower than ~20 kHz and around -59 degrees (average deviation 0.49 degrees) at the 3 MHz mark. Figure 5-39 (b) presents the capacitive reactance profile for the same measurements presented in capacitance units, calculated as:

$$C = \frac{1}{2\pi f \sin \emptyset |Z|} \qquad \text{Equation 5-3}$$

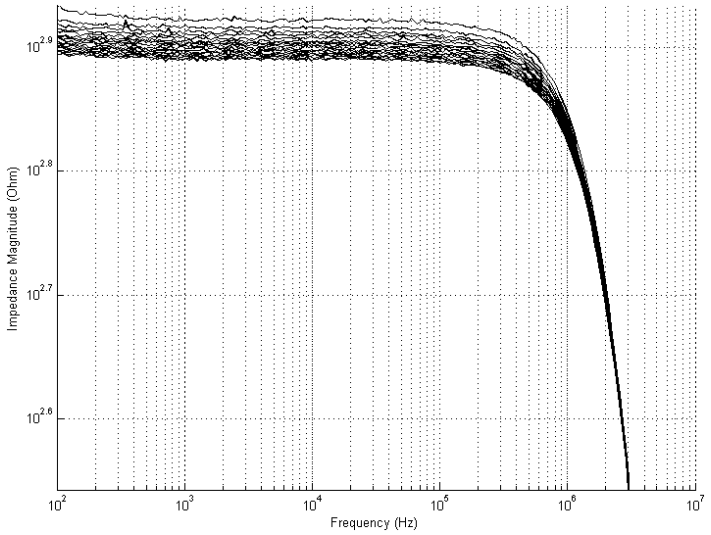
where the measured mean capacitance was 175 pF, with average deviation of 18 pF for the 3 MHz mark.

Figure 5-40 summarized the magnitude, phase and capacitance at 1 MHz frequency, where the drift trends can be observed. In general, the behaviour of the FSR to continuous pressure, behaves as expected of physical structure based on contact area, air displacement and pressure based resistive materials; the present drift is explained by the settling of the different layers, particularly marked by an increased drift towards the initial measurements.

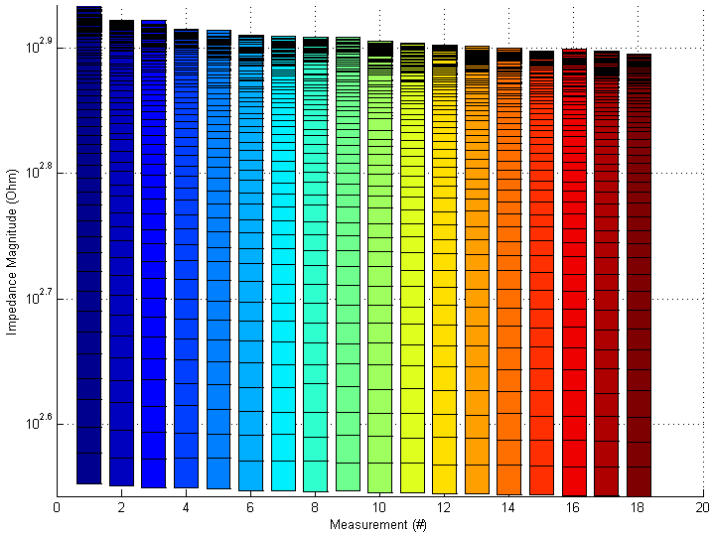
Figure 5-41 presents a set of TYPE-B measurements for the impedance magnitude, performed to the same FSR from the previous TYPE-A set. The measurements were performed in steps from 1 N to 50 N, distributed as follows: 1 N, 5 N, 10 N, 20 N, 30 N, 40 N, and 50 N. The range was swept twice from lower to higher pressure and back, allowing 1 minute settling time at each stage. There is a noted drift at the 1 N mark (expected by the continuous pressure presented on the target FSR) and an observable saturation after the 20 N marked (better seen in Figure 5-41b). The measured impedance ranges from roughly 12 kΩ (average for 1 N in < 100 kHz region for all three measures 12.37 kΩ with mean average deviation of 819 Ω) to roughly 290 Ω (for 50 N measurements in same region); a summary of the measurements can be found in Table 5-3. As can be observed both in Figure 5-41 (b) and Table 5-3, there is a significantly increased deviation at the 1 N pressure measurements representing 6.6 % of the average impedance magnitude, however for pressure over 5 N it drops to roughly 0.5 %, lowering with increased pressure. Such behaviour can be explained by the structural variations that occur at very low pressures, such as 1 N, and the mechanical instrumentation accuracy at such level (it is more challenging to maintain a steady pressure at the lower pressures due to external factors becoming more influential, such as vibrations).



(a)

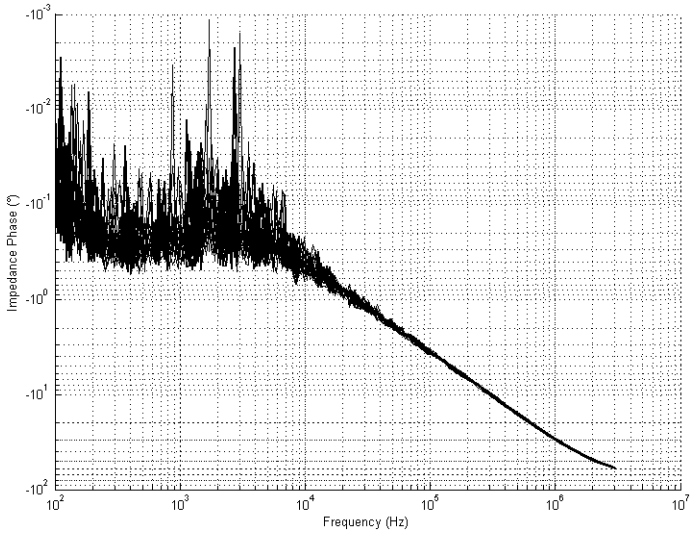


(b)

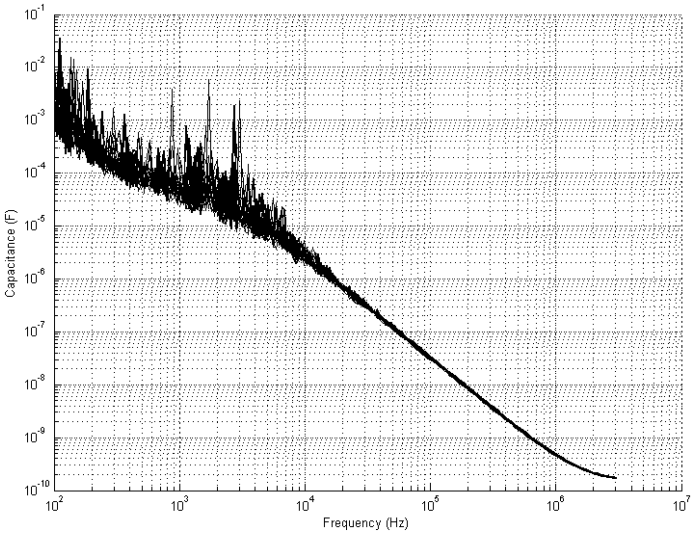


(c)

Figure 5-38 — FSR TYPE-A measurement (a) Measurements vs frequency vs magnitude. (b) Frequency vs magnitude, (c) Measurements vs magnitude.



(a)



(b)

Figure 5-39 — FSR TYPE-A measurement (a) Phase vs frequency. (b) Capacitance vs frequency.

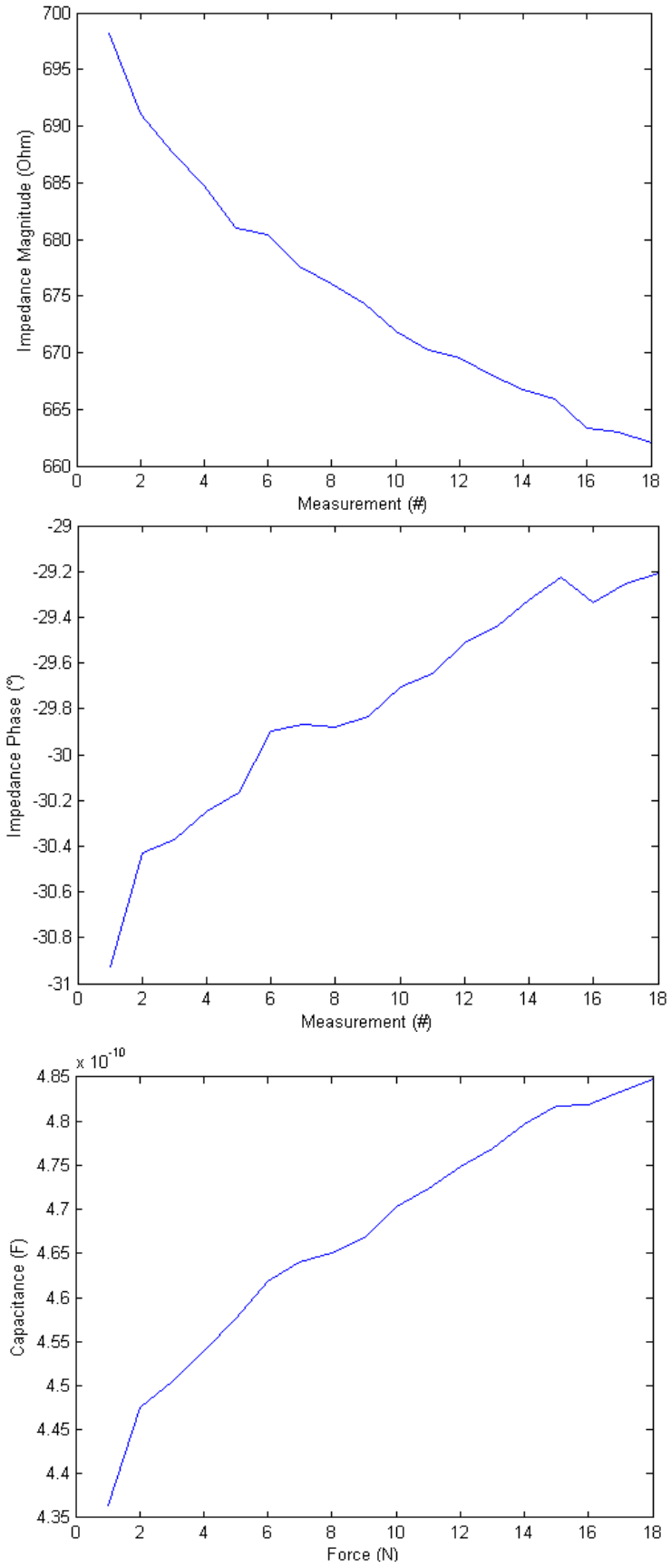
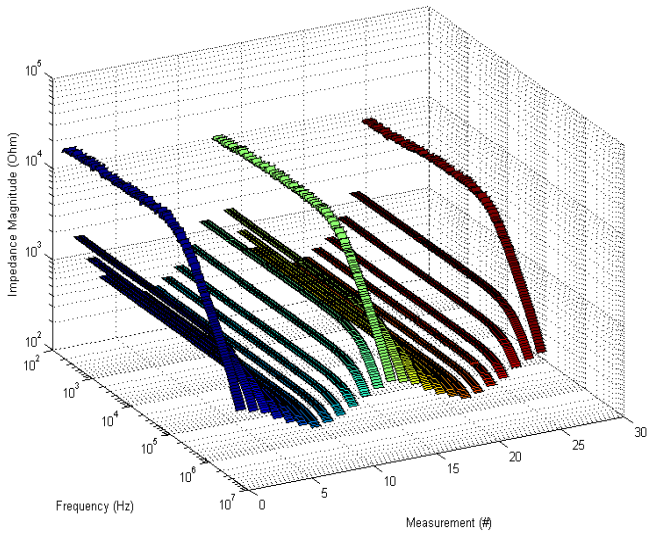
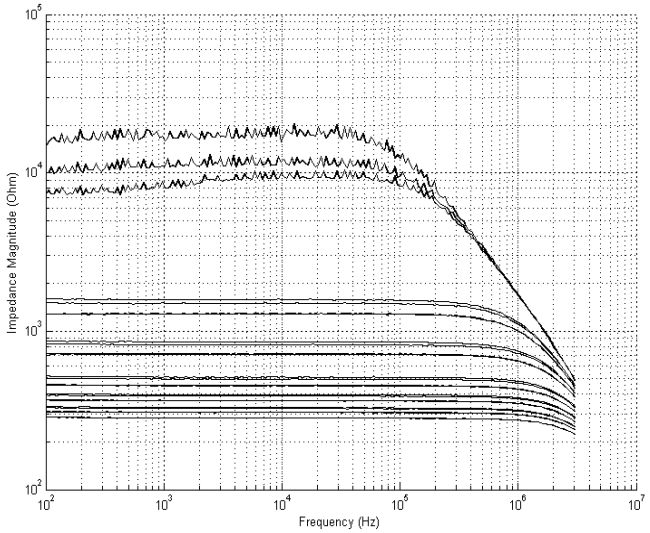


Figure 5-40 — FSR TYPE-A measurement for 1 MHz frequency. (Top) Magnitude. (Middle) Phase. (Bottom) Capacitance.



(a)



(b)

Figure 5-41 — FSR TYPE-B measurement (a) Measurements vs frequency vs magnitude. (b) Frequency vs magnitude.

Table 5-3 Summary of measurements for varying pressures for <100 kHz.

Pressure	Average	Mean Average Deviation
1 N	12.37 kΩ	819 Ω
5 N	1.41 kΩ	7.4 Ω
10 N	779 Ω	2.5 Ω
20 N	481 Ω	1.5 Ω
30 N	380 Ω	1.1 Ω
40 N	318 Ω	1 Ω
50 N	284 Ω	0.9 Ω

Considering the capacitive perspective, Figure 5-42 presents the measurements for the before mentioned TYPE-B measurement; where one observes hysteresis of ~8.4 % consistent with the specifications. The hysteresis was calculated based on delta of capacitance at force midpoint over capacitance extremes difference, following Eq. 5-4 and Eq. 5-5:

$$X_{midpoint} = \left(\frac{X_{max} - X_{min}}{2}\right) + X_{min} \quad \text{Equation 5-4}$$

$$Hysteresis = \frac{(Y_{midpoint\ negative} - Y_{midpoint\ positive})}{(Y_{max} - Y_{min})} x100\% \quad \text{Equation 5-5}$$

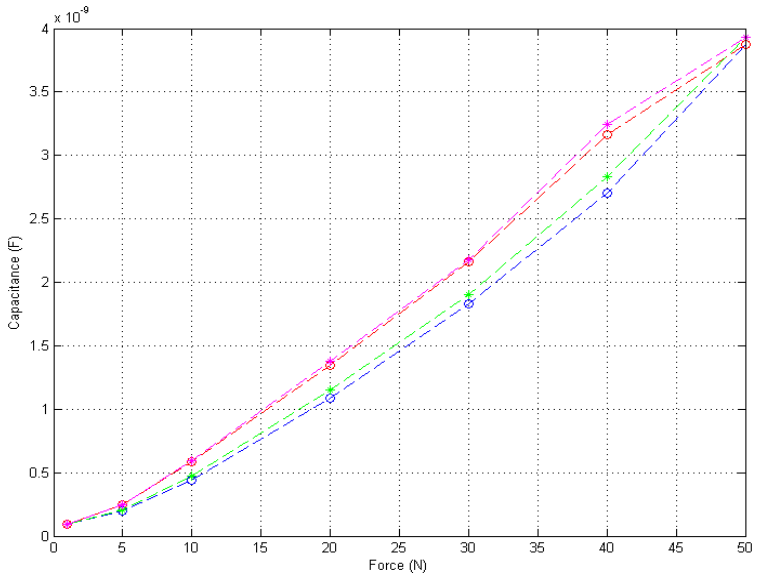


Figure 5-42 — FSR TYPE-B measurement capacitance for 1MHz frequency.

The FSR in question was then degraded through mechanical means through the use of a 45 degree inclined complementary parts for the TIRA Test 2705. A programmed sequence followed a pre-set pattern between 50 N to 4000 N with 10 seconds holds at each extreme and with a speed of 1 mm/s (equivalent stabilized change between extreme forces in under 2 seconds), for 10 hours. Figure 5-43 presents no-load capacitance, measured at 1 MHz, after consecutive degradation sequences and a minimal one hour recovery (the first measurement was performed prior to the degradation sequences). One notes a decreasing capacitance from 68 pF (measurement prior to degradation) to roughly 60 pF. A more noticeable change can be observed on the measurements impedance magnitudes, summarized in Figure 5-44 and Table 5-4. A 68 % decrease is observed for the 1 N measurements (for frequencies under 100 kHz), with average 42% decrease for the remaining pressure measurements.

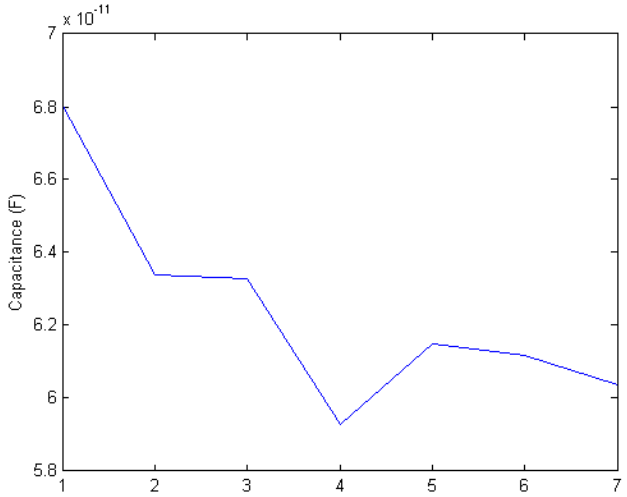


Figure 5-43 — No-load capacitance at 1MHz measurement between degradation session (10 hours of continuous 50 N to 4000 N 10 second holds, with 1 mm/s speed).

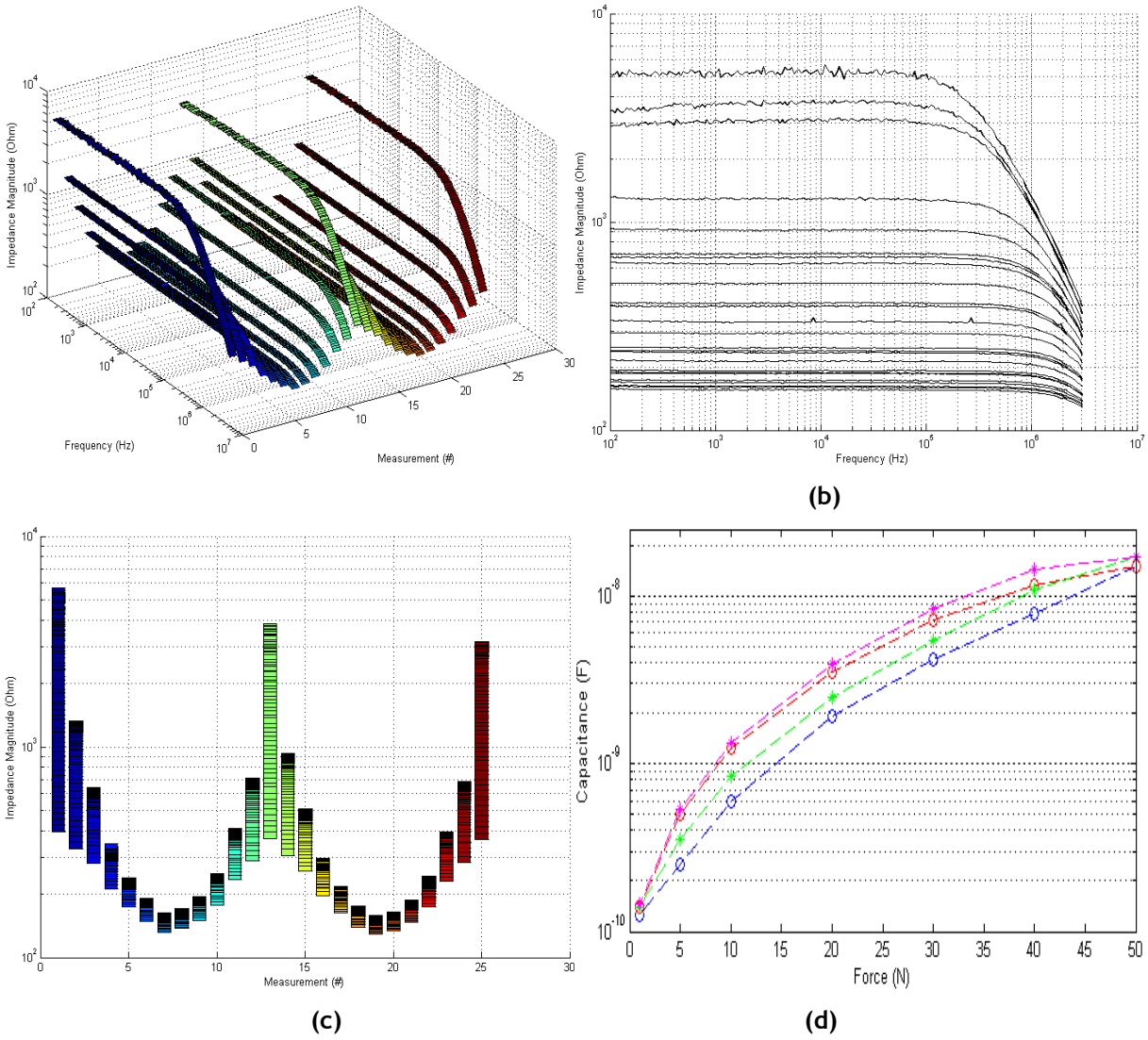


Figure 5-44 — TYPE-B measurement after six 10 hours degradation sessions. (a) Measurements vs frequency vs magnitude. (b) Frequency vs magnitude. (c) Measurements vs magnitude. (d) Force vs capacitance.

Table 5-4 Summary of measurements for varying pressures for > 100 kHz after degradation.

Pressure	Average	Mean Average Deviation
1 N	3.97 kΩ	84.2 Ω
5 N	897 Ω	4.2 Ω
10 N	486 Ω	1.4 Ω
20 N	279 Ω	0.8 Ω
30 N	208 Ω	0.6 Ω
40 N	174 Ω	0.4 Ω
50 N	159 Ω	0.4 Ω

In another experiment the FSR was purposely bent (different from the one utilized on the previous presented degradation experiments), altering the structure. The resulting measures are

presented in Figure 5-45 and Table 5-5, were the value are far lower than those presented in Table 5-3 for reference FSR (66% drop for 1 N down to 41 % for 50 N).

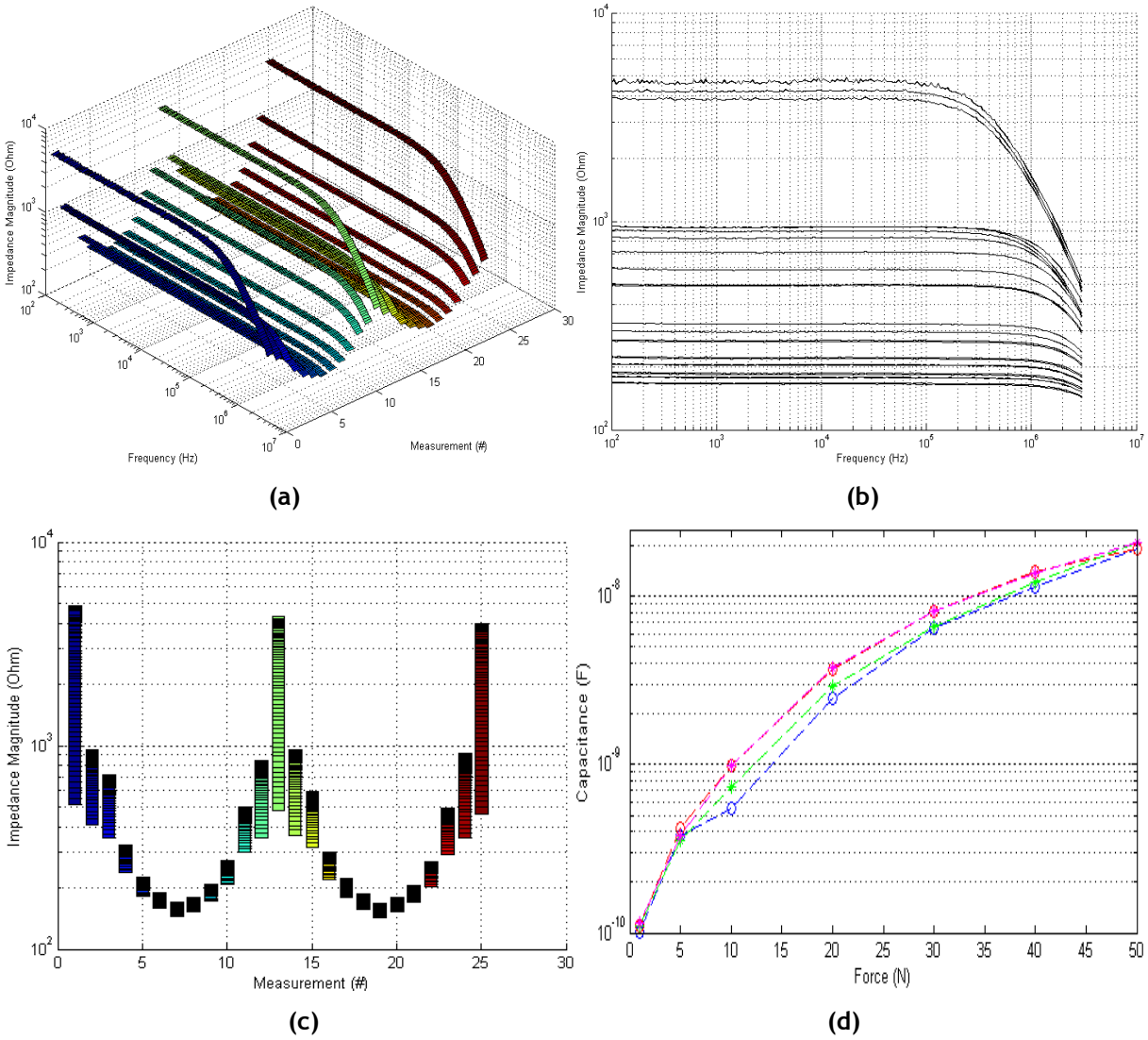


Figure 5-45 — TYPE-B measurement after bending. (a) Measurements vs frequency vs magnitude. (b) Frequency vs magnitude. (c) Measurements vs magnitude. (d) Force vs capacitance.

Table 5-5 Summary of measurements for varying pressures for <100 kHz after FSR bending.

Pressure	Average	Mean Average Deviation
1 N	4.24 kΩ	41.2 Ω
5 N	628 Ω	1.8 Ω
10 N	385 Ω	0.9 Ω
20 N	238 Ω	0.6 Ω
30 N	191 Ω	0.5 Ω
40 N	172 Ω	0.4 Ω
50 N	168 Ω	0.4 Ω

In another experiment the FSR was degraded to the point of breakdown, where it no longer responded to pressure; Figure 5-46 presents resulting capacitance measurements. It can be

noted that the measured capacitance no longer correlates to a specified pressure and is significantly lower with an average 15.3 pF with 0.75 average deviation.

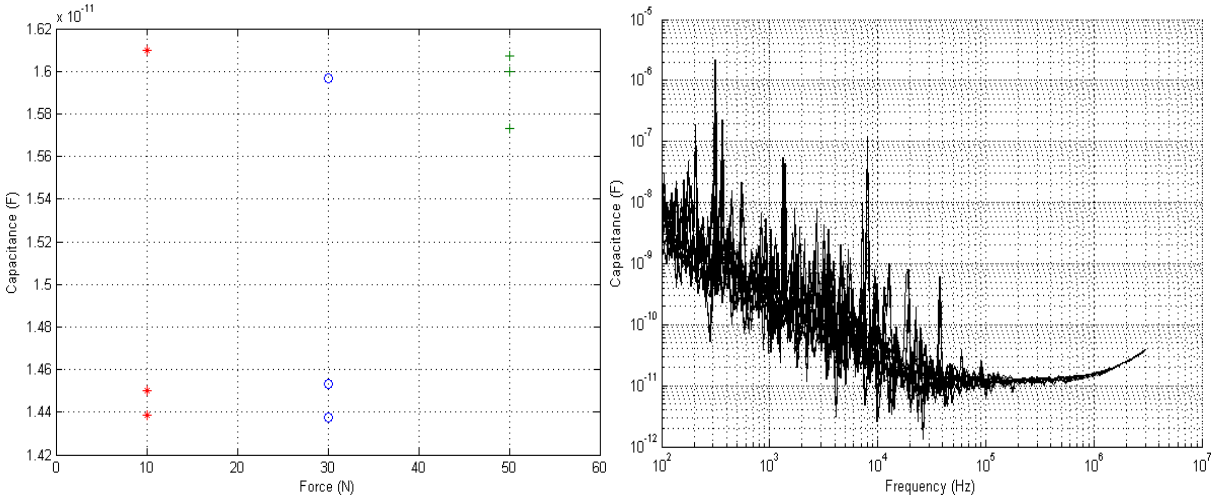


Figure 5-46 — Capacitance measurements after FSR breakdown for multiple forces. (Right) Capacitance vs frequency of all measurements. (Left) Capacitance vs force for all measurements.

Chapter 6

Case Studies SCPS Methodology

The knowledge gained through the experiments presented in the previous chapter permitted the development of SCPS based methodologies for sensor testing, in each of the specific cases. The resulting setups and procedures for the disposable electrode and FSR follow.

6.1 Electrode-skin Impedance SCPS Fault Detection Approach

A number of strategies can be used for monitoring the electrode-skin impedance, where considerations include: current limitation for safety, stability, bandwidth; and although compromises can be made at this early stage of personal monitoring technology, future technologies will have to include operation mode contact impedance verification and compensation strategies such as the ones presented by (Degen & Jäckel, 2008) (Harth & Lischinsky, 2011). Several approaches have been implemented through the years for the measurement and monitoring of the electrode-skin impedance, such as the ones presented in (Zepeda-Carapia, Márquez-Espinoza, & Alvarado-Serrano, 2005) (Grimbergen, VanRijn, & Peper, 1992) (Spinelli, Mayosky, & Pallas-Areny, 2006) (Kim, et al., 2010) (Hewson, Druchêne, & Hogrel, 2001).

Although electrodes serve a passive role during biopotential acquisitions (traditionally setup as a high impedance element), for the electrode-skin impedance characterization it is necessary to inject a stimulus; and although it is quite convenient to use an impedance analyser or electrochemical impedance spectroscopy system, portable systems would seldom benefit from such instrumentation, so more efficient strategies are required. Conventional methods include the use of voltage controlled current sources, such as the Howland configuration (and its variations), used, e.g., in impedance tomography systems (Ross, Saulnier, Newell, & Isaacson, 2003). Such approach provides good stability, although limited in range due to saturation effects, and not readily adaptable to single supply configurations (which are more readily compatible with battery-based systems). Another approach takes advantage of the common mode compensation feedback encountered (e.g., right leg drive) in biosignal acquisition setups and injects a signal outside the frequency of interest so that it can be later filtered and analysed in contrast (Degen & Jäckel, 2008); while others go a different way with the use of power line setups (Spinelli, Mayosky, & Pallas-Areny, 2006).

An electrode-skin impedance verification circuit was developed following a straightforward approach, based on the injection of a low amplitude stimulus current (less than 10 μA) in order to ascertain an electrode-pair impedance, as seen in Figure 6-1, based on the single-supply PXI

analogue front-end presented in Chapter 4, Section 4.3.2. The circuit counts with a calibration resistance, which contributes to limit the upper impedance range and avoids open circuit connections, while the reference resistance contributes to regulate the current. The management of the switching structures is left to the SCPS structures, based on the user-defined parameters. In this scenario, each electrode was assumed to have its own SCPS module and switching structure; admittedly somewhat unrealistic, however it serves as a conceptual demonstration. A more efficient approach would have all the electrodes switching structures controlled by the same SCPS module, serving as an array handler.

For the present scenario, a two-electrode arrangement was utilized, requiring multiple measurements in order to isolate a specific electrode fault; that said, most biosignal measurements are performed with electrode pairs, augmenting the electrode pair-wise analysis relevance. The default calibration resistance considered was of 100 kΩ, based on the observations of the electrode-skin experiments. Figure 6-2 (a) presents two measurements on a male volunteer, performed one after the other, from 100 Hz to 100 kHz. Even though attention was paid to minimized movement and external agents influence, minor deviations can be noted. In order to ascertain the difference of a regular measurement with conventional error inducing situations, Figure 6-2 (b) and (c) present two fault scenarios, motion artefact and loose connector. The volunteer was asked to move his arm during the measurement seen in Figure 6-2 (b), as to cause tension on the connectors themselves. As can be seen, both the phase and the magnitude deviate from the reference (in blue) towards the high frequencies. For Figure 6-2 (c) one of the electrode connectors was loosely placed, allowing for a less than secure connection, which introduced alterations of the magnitude towards the higher frequencies.

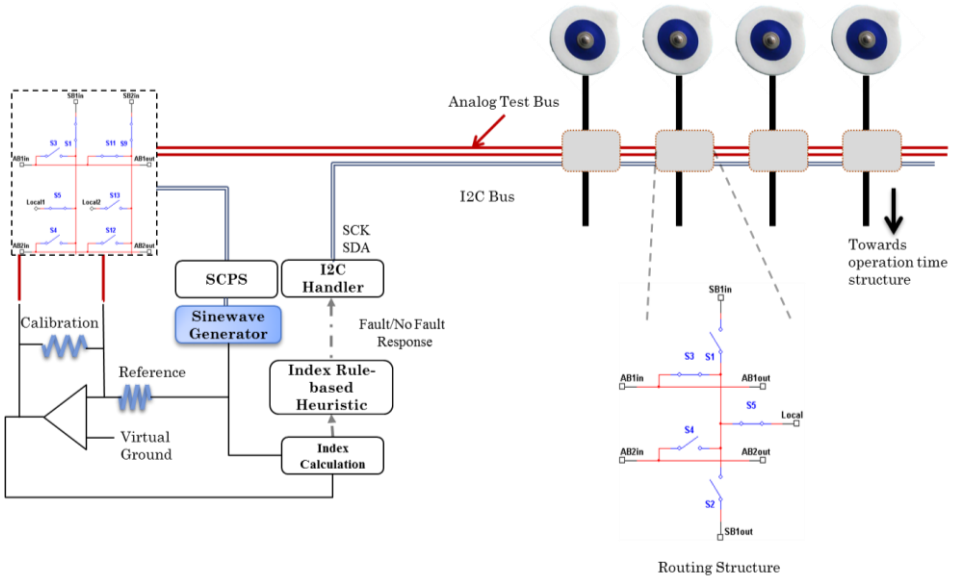
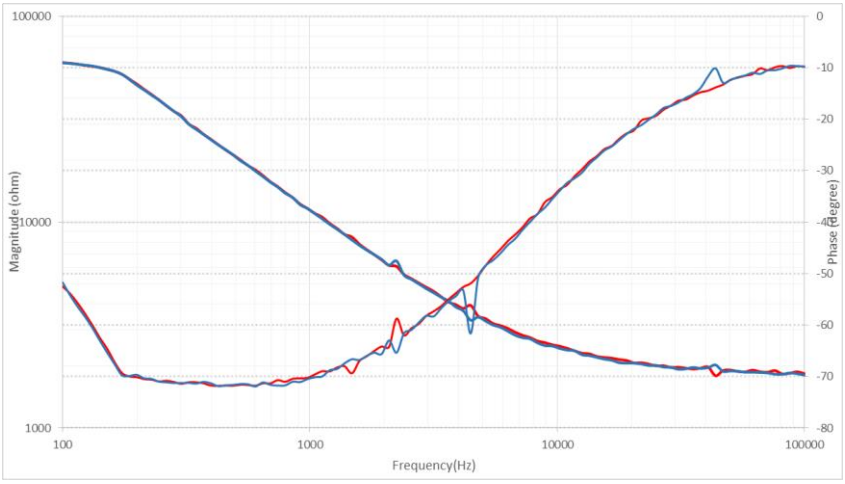


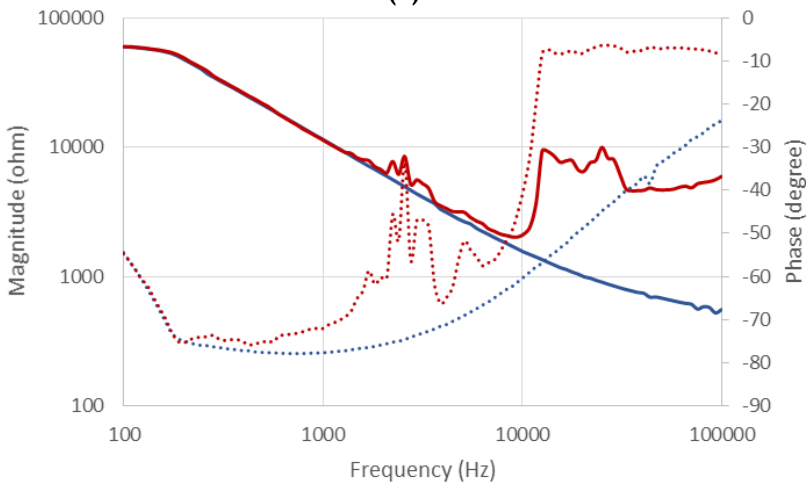
Figure 6-1 — A SCPS based approach for electrode fault detection.

A second male volunteer's measurements are present in Figure 6-3; in this case the variations between the measurements are more evident. For Figure 6-3 (b) an electrode was purposely disconnected, and although towards the lower frequencies the signal behaviour is as one would

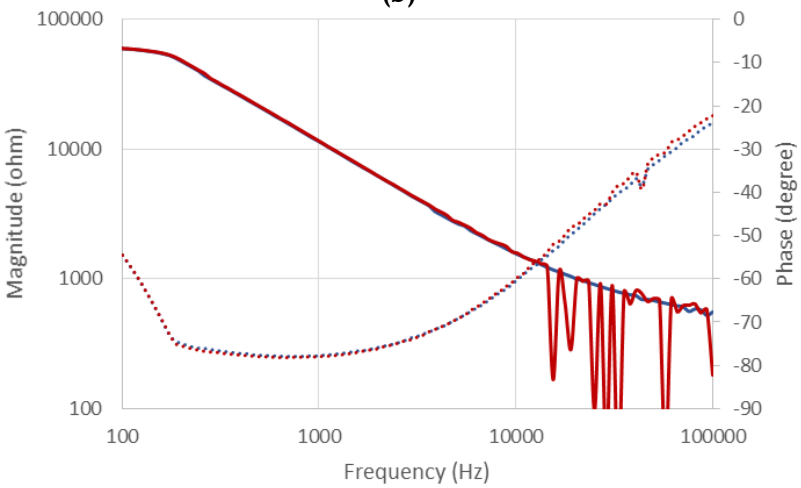
expect (saturated), towards the higher frequencies one encounters a dip on the magnitude and phase, caused by the presence of parasitic elements.



(a)

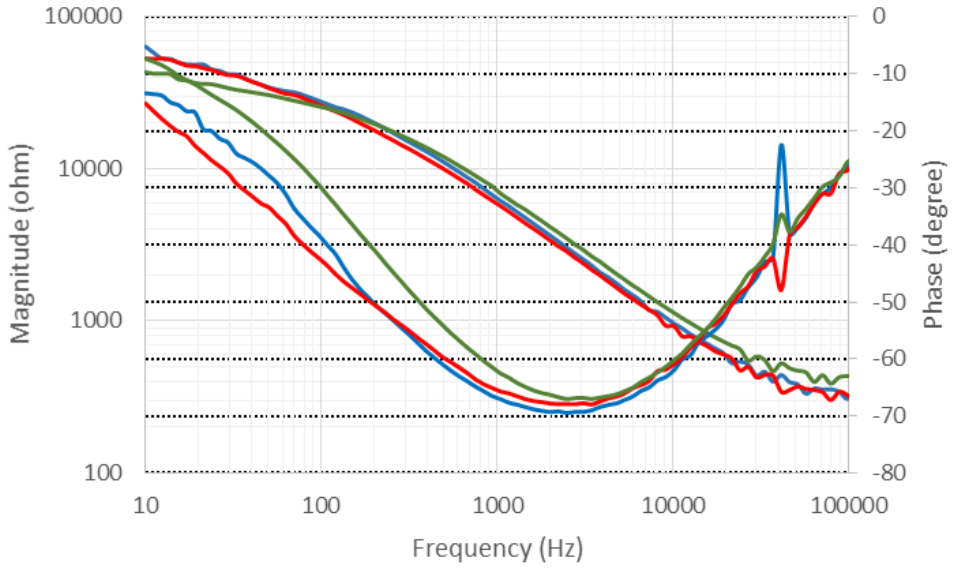


(b)

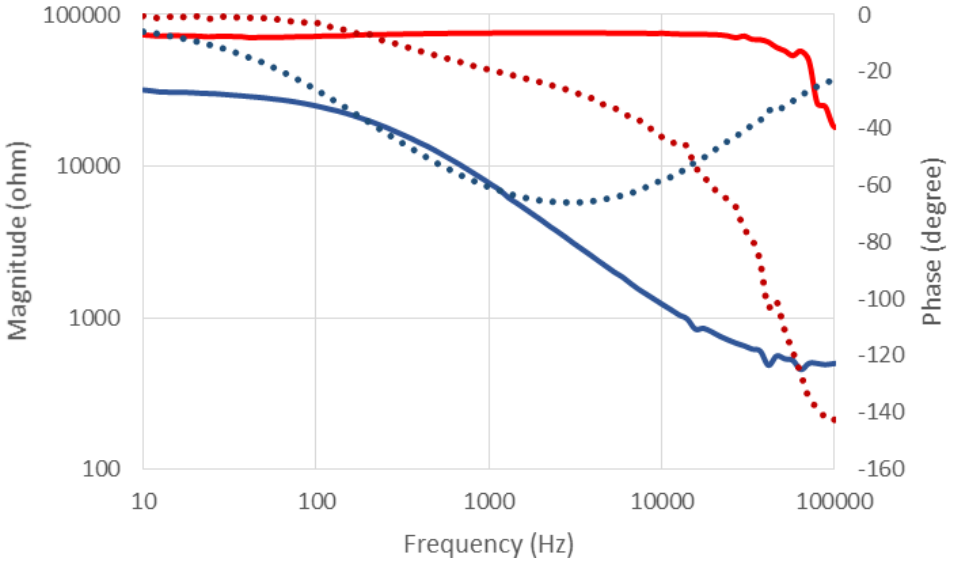


(c)

Figure 6-2 — Electrode-skin impedance two-electrode arrangement for male volunteer (a) Back to back measurements (b) Motion artefact (c) Loose connector. Initial measurement in blue, secondary measurement in red.



(a)



(b)

Figure 6-3 — Electrode-skin impedance two-electrode arrangement on male volunteer (a) Three back to back measurements (b) Bad connection. Initial measurement in blue, secondary measurement in red. In case of (a) initial measurement in green.

6.1.1*SCPS Electrode Fault Detection Methodology*

Complementary to the hardware elements, a methodological flow is required. In the case of electrode pairs, in order to pinpoint a specific faulty electrode (or at least causing measurement deviations), it is required that each electrode is covered by at least two measurements. In such scenario a faulty electrode would cause an abnormal measurement with every electrode it is paired with, therefore if it is paired with at least two electrodes that can be confirmed to have been part of a proper measurement, then the faulty electrode can be segregated. A pseudo-code for the described approach can be seen in Figure 6-4.

```
    FOR pair i, j from (E1, E2, … , En)
     {
        FOR frequency k from (at least one low frequency, ~10Hz, and one higher
frequency, ~100 kHz)
        {
           Standby setup (where Ei,j electrode pair is connected to analogue bus)
           Perform measurement
           Calculate impedance (stimulus/response ratio)
        }
        Calculate index (relation between measurements)
        Transfer result to pair Ei,j
     }
     Determine state (threshold based or as complex as required) by
     processing results at the module level (group process):
     any electrode with all faults is faulty
     any electrode with multiple faults could be tagged as warning.
       actions taken accordingly:
         LOCK faulty, BLOCK pair formation with faulty electrode.
```

Figure 6-4 — Pseudo-code for three electrode pair measurements.

Let us consider the SCPS instruction set and corresponding switching module states required to undertaken the before described flow. In first place, the electrodes as a set need to be configured to a known state that isolates connectivity with the subject, after which specific electrode pairs need to be properly routed and stimulated. Finally, the collection of measurements need to be processed and a decision regarding the state of the electrode needs to be taken, reflected on isolation of the module or at least the setting of a fault flag; Table 6-1 and Table 6-2 present one, of a number of different applicable flows, where Table 6-1 describe the actions for the first measurement and Table 6-2 presents the instructions for consecutive measurement sequences. All instructions and their specifiers are explained in detailed within Chapter 4 for the present I2C implementation, and in a generalized perspective in Chapter 3.

Figure 6-5 presents a number of possible switching states for a four-module scenario (each module controlling an electrode's switching structure). In the present scenario the regular operation scenario can be seen in Figure 6-5 (a), while the isolation arrangement can be seen in Figure 6-5 (b). Non-participating electrodes are arranged as seen in the ISOLATION setup. Variations of the flow can include multiple measurements for the same electrode pair, which can include line verification. For instance, after a pair-wise measurement such as the one in Figure 6-5 (c) and additional measurement with arrangement Figure 6-5 (d) permits a close-loop towards a source/sink instrument covering analogue bus verification. Such arrangement can be setup through inclusion in the user defined arrangement sequence accessed by Nxt-STBY pre-set states.

Table 6-1 SCPS instructions for electrode-pair verification flow.

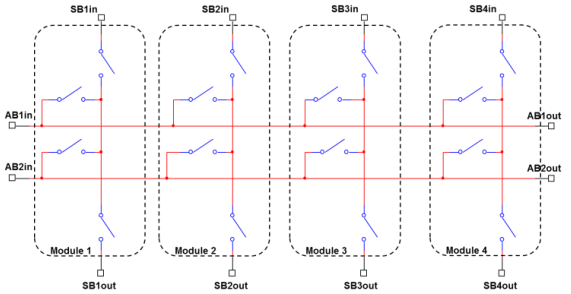
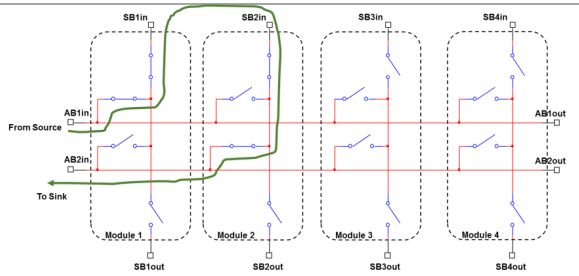
Instruction	Type	Instruction	Description	Switching Arrangement
SCPS General RESET	GLOBAL	• S = I2C Start Event • 0x00 = General Call (Software) • 0x800 = SCPS General RESET	All counter, pointers and flags are reset. The token is released and the switching modules are taken to a default position, i.e., ISOLATION	
Resource Request	GLOBAL	• ReStart • 0x00 = General Call (Soft.) • 0xD0 = Token Request • 0x01 = Remaining 10-bit Addr.	Token availability verification, if available the request continues and the token is taken by target group	Remains in last state
STBY-Default	CAPTURE	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. • 0x48 = STBY-Dflt	All Target group members follow user defined parameters for default stand-by setup. This includes signal generation activation as to stabilize stimuli if required. In this scenario it refers to the connection of the first electrode-pair, and provides the opportunity for the cell stabilization.	
CAPT-D	CAPTURE	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. • 0x4C = CAPT-D	All target group members set their capture and routing configuration on user defined parameter or UDP, based on the current standby associated capture. This includes capturing the measurement and writing to the associated register.	Remains in last state
SRT	SCAN	• ReStart • 0xF3 = SRT • STATUS register sent from Module 1st in DFTL list • ACK from MASTER signifies additional STATUS from next Module in DFTL list	SCPS READ transaction. I2C READ operation for STATUS register retrieval from SOURCE module. CAPTURE status reflected on STATUS register. Re-start event and new SRA for repeat STATUS verification. This provides a venue for capture “ready” assertion.	Remains in last state

Table 6-2 Continuation of SCPS instructions for electrode-pair verification flow.

Instruction		Type	Description	Instruction
Repeat as Needed	**Nxt-STBY**	CAPTURE	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. • 0x49 = Nxt-STBY (next standby setup in the UDP)	All Target group members follow UDP for next stand-by setup, i.e., the next electrode-pair is connected.
	SRT	SCAN	• ReStart • 0xF3 = SRT • STATUS register sent from Module 1st in DFTL list • ACK from MASTER signifies additional STATUS from next Module in DFTL list	Quick Transfer from SOURCE to TARGET Module of CAPTURE results, i.e., based on the current STBY state the UDP can declare which module and register is the source of the transfer information and which module and target is the receiver. This contributes to a streamlined transfer of the previous capture data.
	CAPT-D	CAPTURE	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. • 0x4C = CAPT-D	All Target group members follow UDP for current stand-by associated capture. Once more the electrode pair is stimulated and the response captured.
	SRT	SCAN	• ReStart • 0xF3 = SRT • STATUS register sent from Module 1st in DFTL list • ACK from MASTER signifies additional STATUS from next Module in DFTL list	SCPS READ transaction. I2C READ operation for STATUS register retrieval from SOURCE module. CAPTURE status reflected on STATUS register. Re-start event and new SRA for repeat STATUS verification, as described in Table 6-1 SCPS instructions for electrode-pair verification flow.
END-CAPT		CAPTURE	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. • 0x4D = END-CAPT	Release TOKEN (possible post-capture procedure activation). Once the sequence is over the TOKEN is released and the modules can be set to a default switching position, such as BYPASS.
PSET		PROCESS	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. • 0x28 = PSET	Follow default PROCESS setup. Fault flag updated, i.e., each individual module activates the processing procedure instantiated within and the results can flag a FAULT conditions, which can be associated with LOCK states.

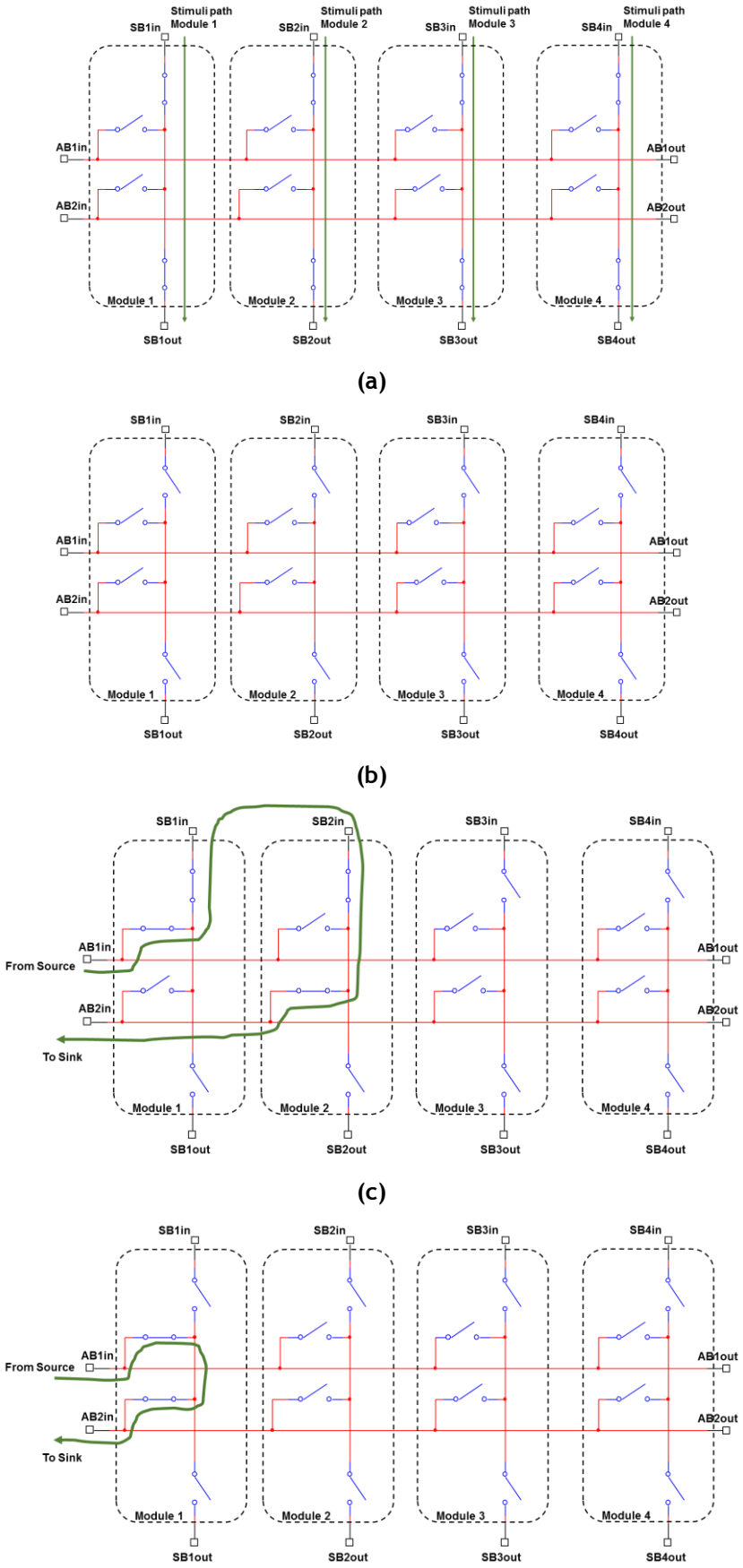


Figure 6-5 — Switching states for a four-electrode scenario. (a) BYPASS state. (b) ISOLATE state. (c) Electrode-pair connection (electrode 1 with electrode 3). (d) Line verification state.

6.2 FSR SCPS Fault Detection Approach

FSR offer a quite different testing scenario when compared to electrodes, not requiring pairing or subject to that same unpredictable variability related to an organic factor in their equation; that said, FSR present challenges by themselves. Although the FSR structure is not as sensitive to current as the human body, attention should be paid to the specifications of the manufacturer in order to avoid electrical or physical stress, thus producing deteriorating effects. Figure 6-6 presents an analogue bus based arrangement for FSR utilizing SCPS controlled switching structures.

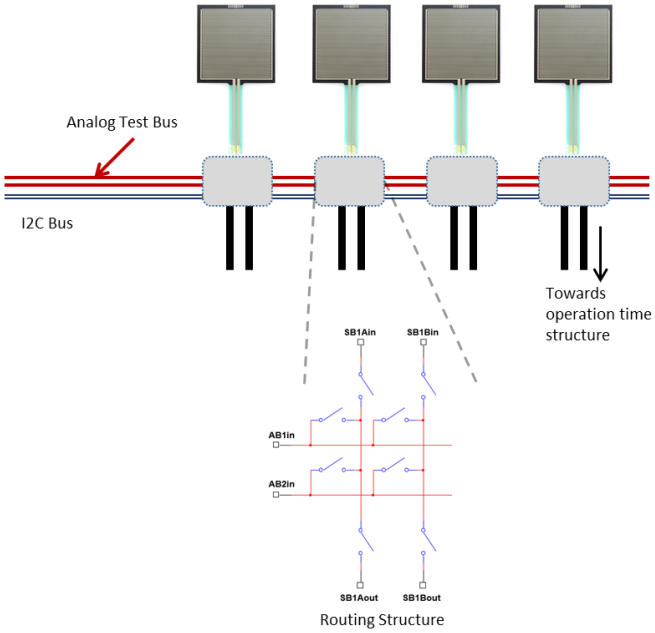


Figure 6-6 — A SCPS based arrangement for FSR.

The same single-supply AFE and switching modules that were utilized in the electrode-skin impedance setup were used for the present scenario, demonstrating the reusability of testing elements. Figure 6-7 presents three repetition measurements performed for no-load, minimal load (base structure for weights), 250 grams, 500 grams and 1 kilogram. As can be seen in Table 6-3, there is a wide variability of measurements for the no-load and minimal load in the range under 100 kHz, which dramatically decreases for weight as small as 250 grams; these measurements are consistent to the high impedance presented by the FSR under no load conditions, that said a stabilizing effect can be noted towards the higher frequencies.

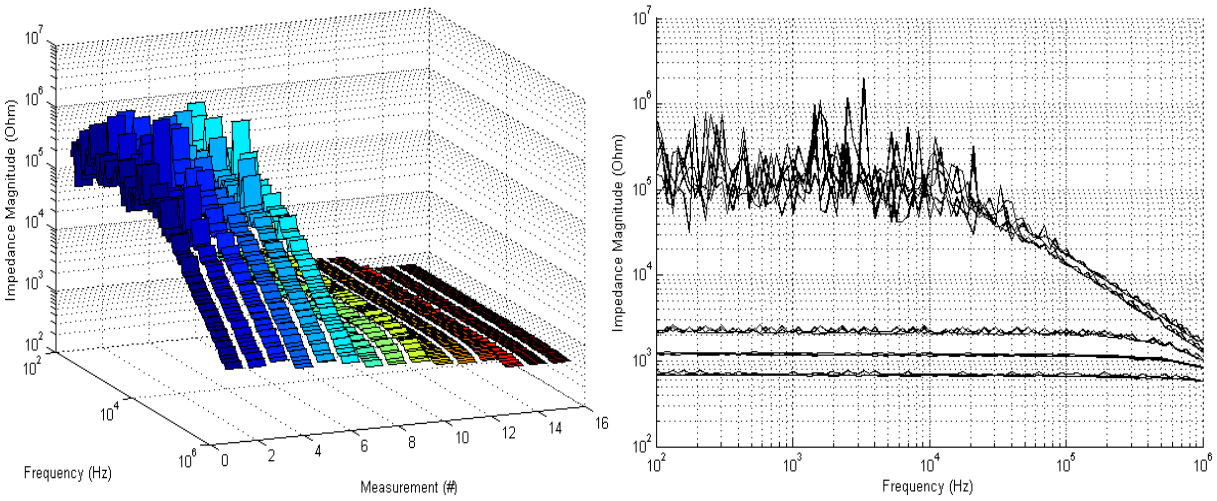


Figure 6-7 — TYPE B measurement using single-supply AFE for multiple repetition of no-load, minimal load, 250 grams, 500 grams and 1 kilogram. (Left) Measurements vs frequency vs impedance magnitude. (Right) Frequency vs impedance magnitude.

Table 6-3 Summary of measurements for varying pressures for < 100 kHz with single-supply setup.

Pressure	Average	Mean Average Deviation
No-load	171 kΩ	113 kΩ
Minimal	112 kΩ	71 kΩ
250 grams	2.22 kΩ	118 Ω
500 grams	1.20 kΩ	17 Ω
1 kg	690 Ω	11 Ω

Figure 6-8 presents capacitance measurements for the previously described load scenarios for different FSR: no-alteration or “normal”, obstructed air duct, damaged and broken; as can be observed, all four FSR present different profiles which are readily identifiable. The “obstructed” presents altered readings caused by the trapping of the air inside the FSR causing a cushioning effect to the pressure, such effect is more evident for small pressures as observed by the 250 grams measurements (middle group seen in Figure 6-8 (b)). The “damaged” FSR was perforated, reflected on its profile shift towards no-load scenarios and lowering of the no-load capacitance. Lastly, the breakdown scenario presents no response to pressure as well as a lower capacitance overall in the higher frequencies.

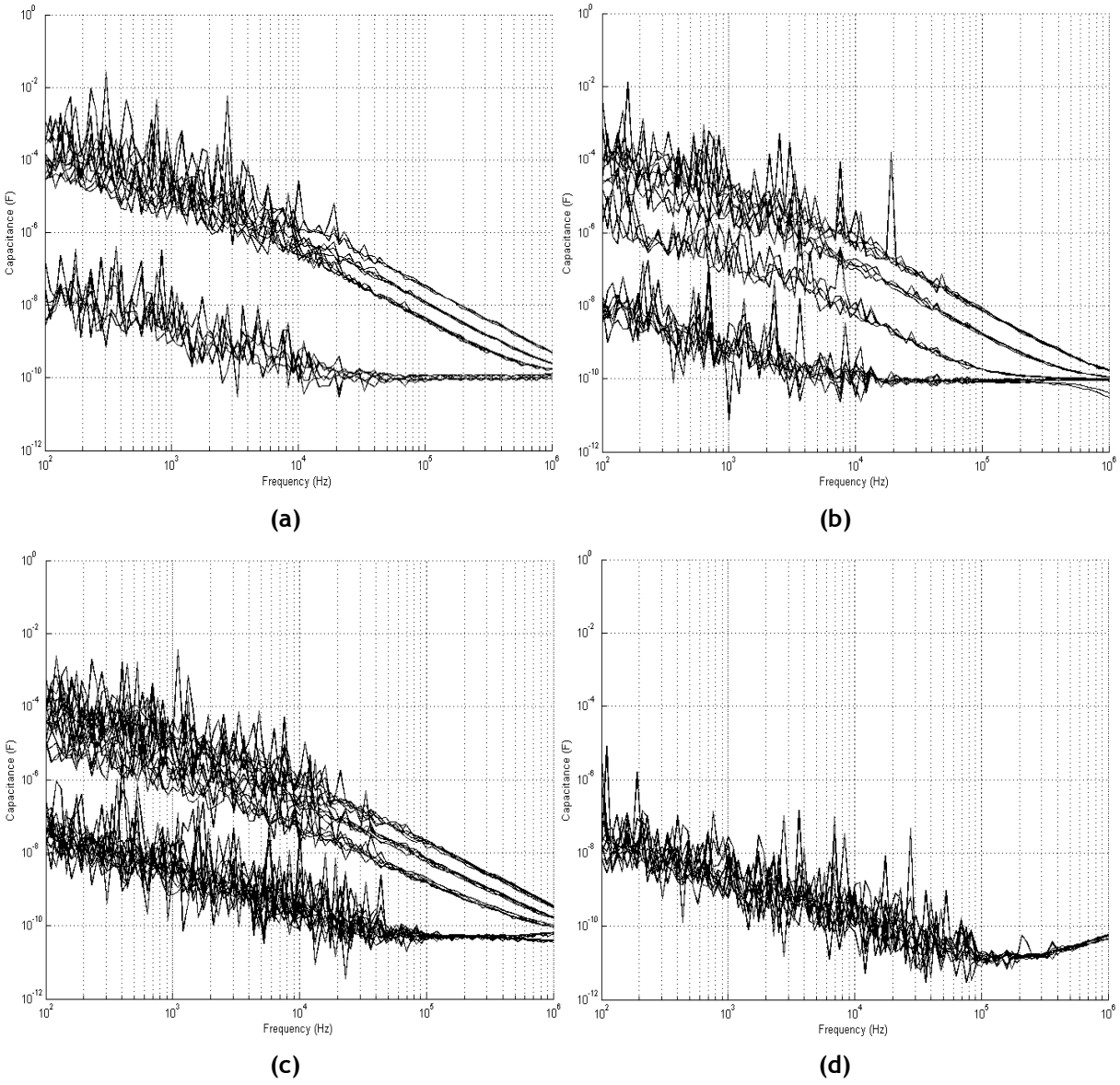


Figure 6-8 — TYPE B measurement of capacitance for multiple FSR scenarios: (a) Normal. (b) Obstructed. (c) Damaged. (d) Breakdown.

6.2.1 *SCPS FSR Fault Detection Methodology*

Complementary to the hardware elements, a methodological flow is required. In the case of FSR, a faulty or altered FSR can be established through a single measurement at a reference frequency, for instance 100 kHz (due to the observed variations). Figure 6-9 summarizes the pseudo-code for the FSR measurements. In this scenario is it not necessary to isolate the FSR since electrical interaction among them can only occur through the analogue bus and not by external venues (discounting an extreme failure scenario where the FSR become electrically connected to each other). Thus online measurements can take place, which permit the characterization of the response to external pressure, while measuring the associated capacitance useful for FSR state determination; i.e., every measurement can have a dual role for testing and for operation functionality. Thus, a simple flow suffices, where the analogue bus can serve as a resource minimizing strategy for FSR interaction or limited to testing functionality. The proposed flow can be seen in Figure 6-9:

```
FOR module from (FSR1, FSR2, … , FSRn)
{
   FOR frequency k (i.e. 100 kHz)
   {
         Standby setup (where FSRi is connected to analogue bus)
         Perform measurement
         Calculate impedance (stimulus/response ratio)
   }
   Calculate index (relation between measurements)
   Transfer result to FSRi
}
Determine state (threshold based or as complex as required) by
processing results at the module level (group process):
 any FSR outside a predetermined range is considered faulty
   actions taken accordingly:
     LOCK faulty.
```

Figure 6-9 — Pseudo-code for FSR measurement.

Let us consider the SCPS instruction set and corresponding switching module states required to undertaken the described flow. Table 6-4 and Table 6-5 contain one alternative to the before mentioned flow of events. Figure 6-10 presents switching states associated to the flow where the FSR are isolated from its operation flow connections and line verification is preform as part of the FSR state determination. Interestingly enough the instructions and SCPS flow are compatible between the FSR and the electrode pair scenario. For both sensors the same instructions sequence can be utilized, given that the particularities of the switching module response are contained within the UDP; this permits code reusability.

Table 6-4 SCPS instructions for FSR verification flow.

Instruction	Type	Instruction	Description
SCPS General RESET	GLOBAL	• S = I2C Start Event • 0x00 = General Call (Software) • 0x800 = SCPS General RESET	All counter, pointers and flags are reset. The token is released and the switching modules are taken to a default position, i.e., ISOLATION
Resource Request	GLOBAL	• ReStart • 0x00 = General Call (Soft.) • 0xD0 = Token Request • 0x01 = Remaining 10-bit Addr.	Token availability verification, if available the request continues and the token is taken by target group
STBY-Default	CAPTURE	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. • 0x48 = STBY-Dflt	All Target group members follow user defined parameters for default stand-by setup. This includes signal generation activation as to stabilize stimuli if required. In this scenario it refers to the connection of the FSR, and provides the opportunity for the cell stabilization.
CAPT-D	CAPTURE	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. • 0x4C = CAPT-D	All target group members follow UDP for current standby associated capture. This includes capturing the measurement and writing to the associated register.
SRT	SCAN	• ReStart • 0xF3 = SRT • STATUS register sent from Module 1st in DFTL list • ACK from MASTER signifies additional STATUS from next Module in DFTL list	SCPS READ transaction. I2C READ operation for STATUS register retrieval from SOURCE module. CAPTURE status reflected on STATUS register. Re-start event and new SRA for repeat STATUS verification. This provides a venue for capture “ready” assertion.

Table 6-5 Continuation of SCPS instructions for FSR verification flow.

Instruction		Type	Description	Instruction
Repeat as Needed	**Nxt-STBY**	CAPTURE	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. • 0x49 = Nxt-STBY (next standby setup in the UDP)	All Target group members follow UDP for next stand-by setup, i.e., the next electrode-pair is connected.
	SRT	SCAN	• ReStart • 0xF3 = SRT • STATUS register sent from Module 1st in DFTL list • ACK from MASTER signifies additional STATUS from next Module in DFTL list	Quick Transfer from SOURCE to TARGET Module of CAPTURE results, i.e., based on the current STBY state the UDP can declare which module and register is the source of the transfer information and which module and target is the receiver. This contributes to a streamlined transfer of the previous capture data.
	CAPT-D	CAPTURE	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. • 0x4C = CAPT-D	All Target group members follow UDP for current stand-by associated capture. Once more a FSR is stimulated and the response captured.
	SRT	SCAN	• ReStart • 0xF3 = SRT • STATUS register sent from Module 1st in DFTL list • ACK from MASTER signifies additional STATUS from next Module in DFTL list	SCPS READ transaction. I2C READ operation for STATUS register retrieval from SOURCE module. CAPTURE status reflected on STATUS register. Re-start event and new SRA for repeat STATUS verification, as described in
END-CAPT		CAPTURE	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. • 0x4D = END-CAPT	Release TOKEN (possible post-capture procedure activation). Once the sequence is over the TOKEN is released and the modules can be set to a default switching position, such as BYPASS.
PSET		PROCESS	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. • 0x28 = PSET	Follow default PROCESS setup. Fault flag updated, i.e., each individual module activates the processing procedure instantiated within and the results can flag a FAULT conditions, which can be associated with LOCK states.

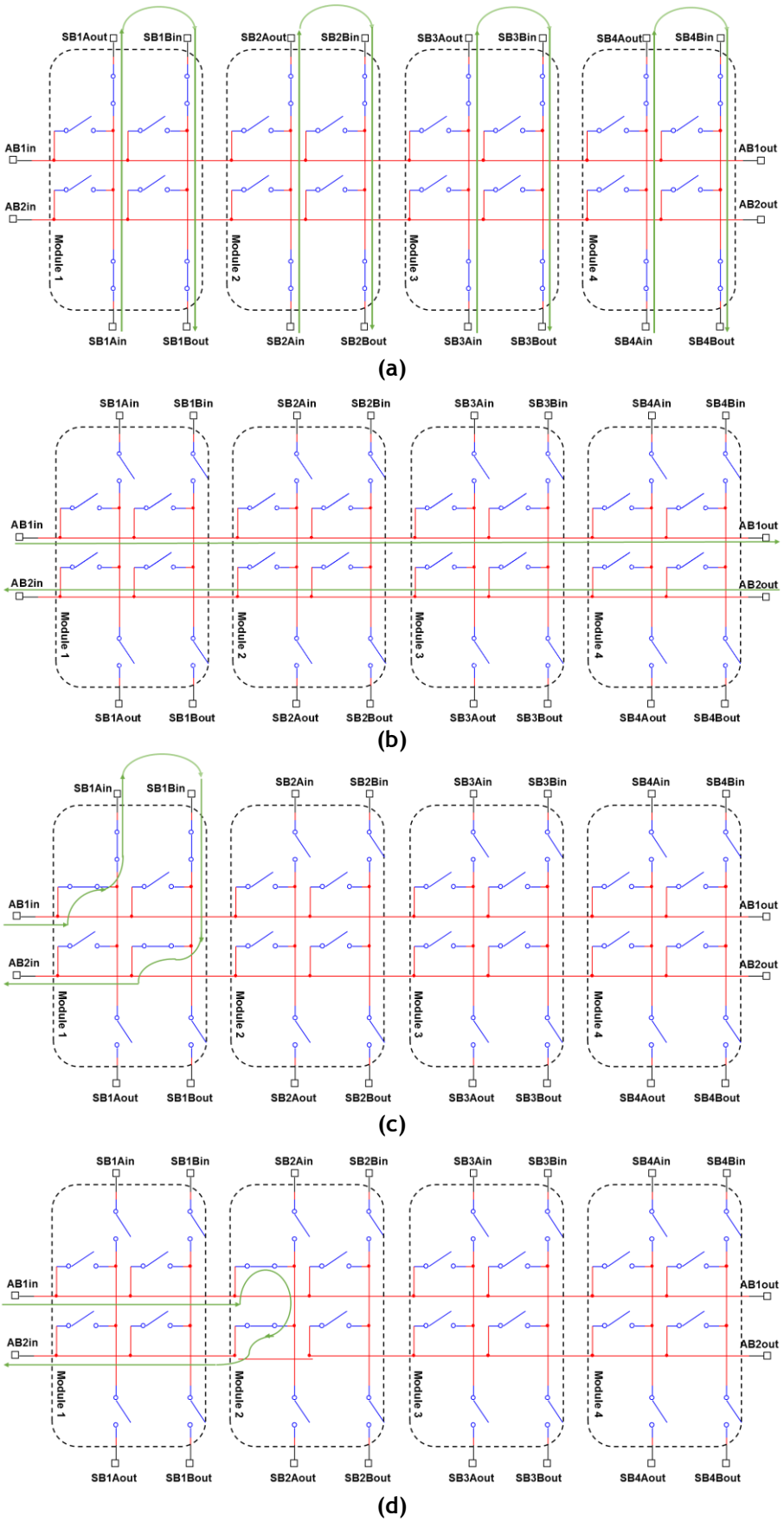


Figure 6-10 — Switching states for a four-FSR scenario. (a) Regular operation state. (b) BYPASS state. (c) FSR module 1 connection. (d) Line verification state.

As mentioned previously, a number of different flows can be implemented, including "on-the-fly" instructions that provide the different modules state associated instructions which are presented with the instruction instead on relying on pre-set user definitions; Table 6-6 presents the instructions for an "on-the-fly" approach. In this scenario the CAPT-S instruction can be used to pass specific switching arrangement information to the target modules. For instance if one considers the arrangements seen in Figure 6-10, each of the switches can be assigned a bit on the 8-bit switching state specifier, thus providing direct control. Alternatively, the switching state can be used to access a look-up-table with pre-set switching setups, useful for scenarios where the number of switches to control is impractically large to be set individually.

Table 6-6 SCPS instructions for FSR verification flow using "on-the-fly" instructions.

Instruction		Type	Description	Instruction
STBY-Dflt		CAPTURE	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. • 0x48 = STBY-Dftl	All Target group members follow user defined parameters for default stand-by setup. This stage is used in order to arrange all group members in a default state.
Repeat as Needed	**CAPT-S**	CAPTURE	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. • 0x4F = CAPT-S • Depending on target modules follows: - Target Member e.g. 0x01 - Switching State e.g. 0xAC	Only access members change their state, so it is expected for the additional members of the group that were not accessed to be set an appropriate state. Through this instruction a specific FSR can be setup for a measurement without the need for pre-set parameters. In this case the switching state can be used to assert and deassert specific switches of the arrangement.
	STBY-Dflt	CAPTURE	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. - 0x48 = STBY-Dftl	All Target group members follow user defined parameters for default stand-by setup. All members are returned to a default state and a quick transfer can follow.
	SRT	SCAN	• ReStart • 0xF3 = SRT • STATUS register sent from Module 1st in DFTL list • ACK from MASTER signifies additional STATUS from next Module in DFTL list	Quick Transfer from SOURCE to TARGET Module of CAPTURE results, i.e., based on the current STBY state the UDP can declare which module and register is the source of the transfer information and which module and target is the receiver. This contributes to a streamlined transfer of the previous capture data.
END-CAPT		CAPTURE	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. • 0x4D = END-CAPT	Release TOKEN (possible post-capture procedure activation). Once the sequence is over the TOKEN is released and the modules can be set to a default switching position, such as BYPASS.
PSET		PROCESS	• ReStart • 0xF2 = SWT • 0x01 = Remaining 10-bit Addr. • 0x28 = PSET	Follow default PROCESS setup. Fault flag updated, i.e., each individual module activates the processing procedure instantiated within and the results can flag a FAULT conditions, which can be associated with LOCK states.

6.3 SCPS ProLIMB EMG Module Fault Detection Approach

The SCPS framework has been shown up to this point as a management mechanism for multi-sensor scenarios; although it was conceived for a number of flexible setups that include intra-modular resource management. As a contrasting example, the following section describes the inclusion of the SCPS framework and methodologies to an ECG module of a wearable system intended for gait analysis produce by the ProLIMB project researchers of the Faculty of Engineering of the University of Porto.

6.3.1 *Wearable Data Acquisition System for Gait Analysis*

Current instrumentation and methods for gait analysis are still expensive and complex, difficult to setup by healthcare staff, hard to operate and uncomfortable for the patient, while requiring a very high level of expertise for data gathering, analysis and interpretation. A new instrument infrastructure specifically dedicated to capturing locomotion data was developed by members of the FEUP's ProLIMB project. The ProLIMB system includes, in a single infrastructure, the means to capture inertial and surface electromyography signals (sEMG) of the lower limbs. It is presented as a network of sensor nodes interconnected through textile-conductive yarns and provides the measurement of kinematic variables, as well as the EMG signals that are most important for locomotion. Each node comprises an EMG sensor, an accelerometer, and a gyroscope, as well as an operation managing microcontroller responsible also for routing data in the established mesh network. EMG electrodes and the interconnections among sensor nodes are sewed on the leggings using yarns made with twisted filaments, each one a polymeric filament covered by a very thin layer of silver. Aggregated information is sent to a personal computer through a Bluetooth wireless link from a central processing module (CPM), as seen in Figure 6-11(a), while Figure 6-11(b) and (c) show an early prototype and the textile embedded wires and electrodes respectively. The system allows the measurement of typical kinematic variables of the lower limbs, namely linear and angular movement of thighs and shanks, as well as the myoelectric signals of strategic muscles for locomotion analysis, as seen in Figure 6-12, following recommendations from the Surface ElectroMyoGraphy for the Non-Invasive Assessment of Muscles (SENIAM) project (Hermens, et al., 1999) and a team of physiotherapists and specialists in gait analysis from the *Escola Superior de Tecnologia da Saúde do Porto* - IPP.

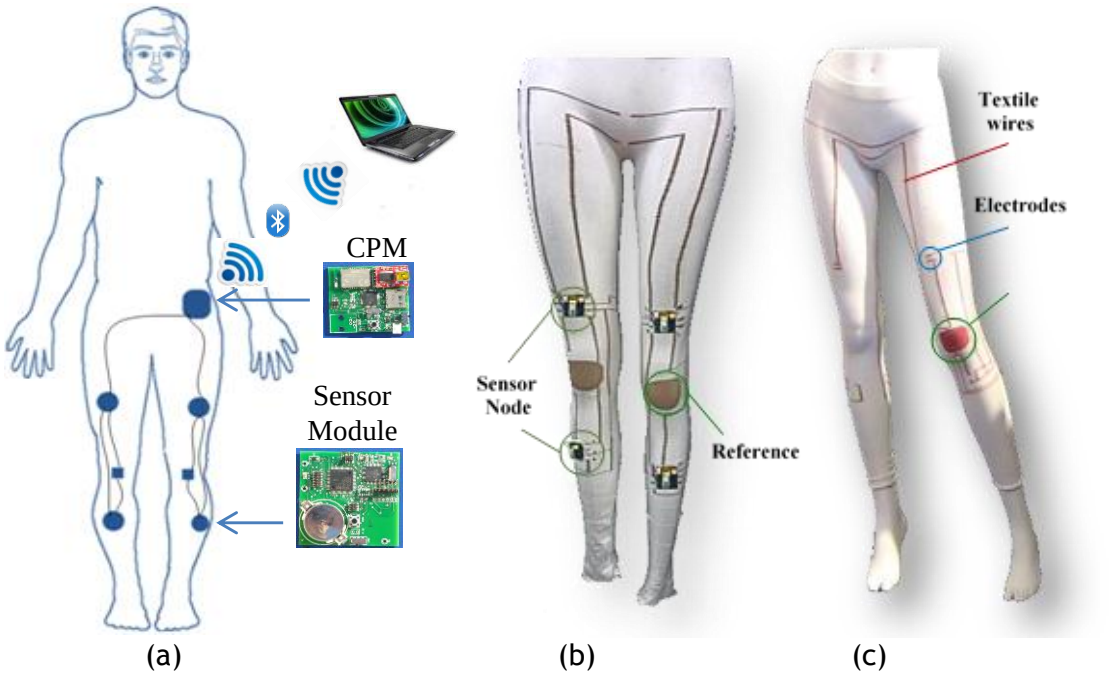


Figure 6-11 — (a) Gait analysis infrastructure (b) Early prototype of gait analysis system (c) Textile embedded wires and electrodes.

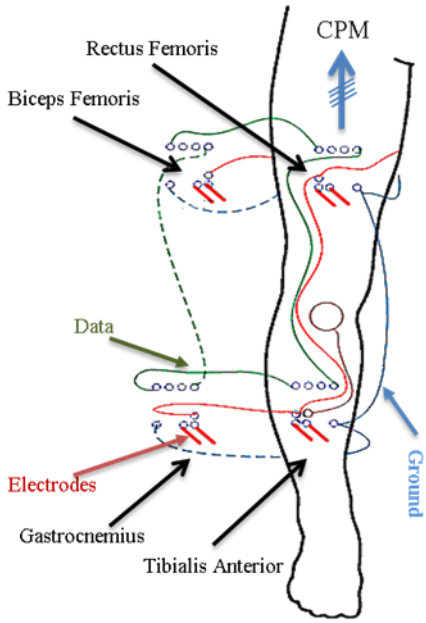


Figure 6-12 — Gait analysis structure detailed view.

The EMG module contained within each sensor node, shown in Figure 6-13, can be divided in two main sections: the electrodes and the signal conditioning circuitry. The electrodes are grouped in sets of two acquisition electrodes per targeted muscle plus a reference electrode per leg placed on the knee. The SCC comprises the following stages: an instrumentation amplifier, drift removal, filtering, gain adjustment, and a body reference drive feedback connected to the reference electrode. These stages have a predictable behaviour established by their configuration and/or combination of elements such as resistors and capacitors, which

show an acceptable dispersion of values among them, maintaining the proper functioning of the system. However, variations in the components' manufacturing process, different life-time degradations, electrical faults (shorts and open circuits), or environmental issues such as, humidity, pressure or temperature, can alter such balance of values. Therefore, it is important to ensure that the system is operating within the defined limits before and during its usage, in order to insure the reliability of the captured data.

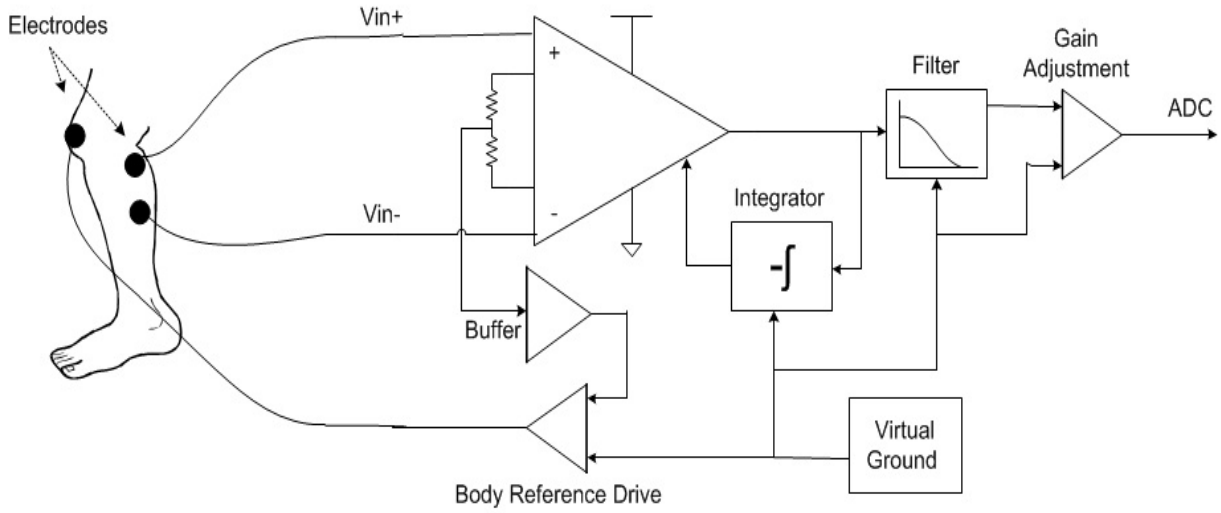


Figure 6-13 — EMG signal conditioning module structure.

Built-in self-testing/calibration (BISTC) strategies have traditionally focused on performing detection, diagnosis and repair actions of a specific module, section, component, or IP core core (Zaki, Tahar, & Bois, 2008) (Burns & Roberts, 2011). Communication and area overhead, increased complexity and resources, or energy expenditure are just a few factors that limit traditional approaches. In order to address some of the aforementioned limitations, a BIST structure was proposed, which reduces implementation overhead, in terms of design time, pin-count and board area, through the reuse of the I2C bus (already used for connecting the accelerometer and the gyroscope) for testing management purposes as seen in Figure 6-14; where the embedded instrument refers to the EMG module previously described. Additional resource reutilization and component count minimization was achieved, through the reuse of the I2Cbus as a stimuli/response transport. In this test case scenario the SCPS is used as a module management mechanism as opposed to targeting specific sensors; thus, proving its flexibility and versatility. The approach seeks to integrate within the module elements required for testing of the different aspects, such as the electrode-skin impedance for proper sensor contact verification, as well as the signal conditioning circuitry functional response. In such setup, a switching matrix manages signals routing, with special consideration to active operation time synchronization, i.e., meaning that safety considerations are also in play due to the nature of the electrode-skin interface and possible shock. Figure 6-15 presents an overview of the strategy applicable to the described scenario.

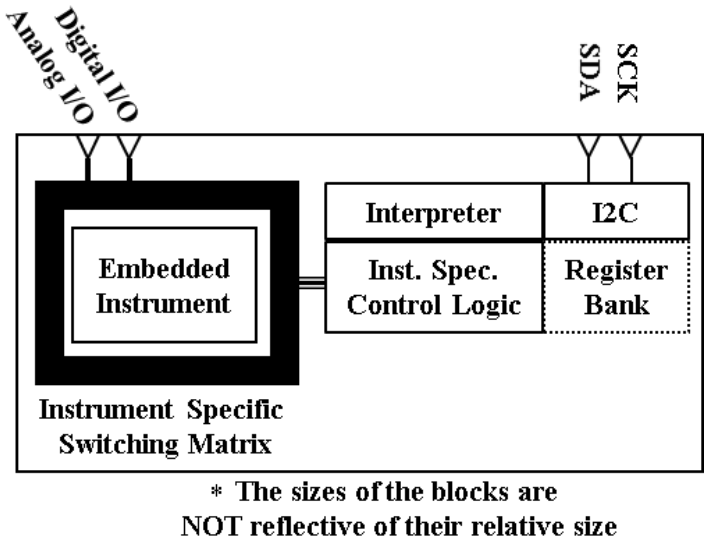


Figure 6-14 — Overview of generic embedded instrument with proposed infrastructure.

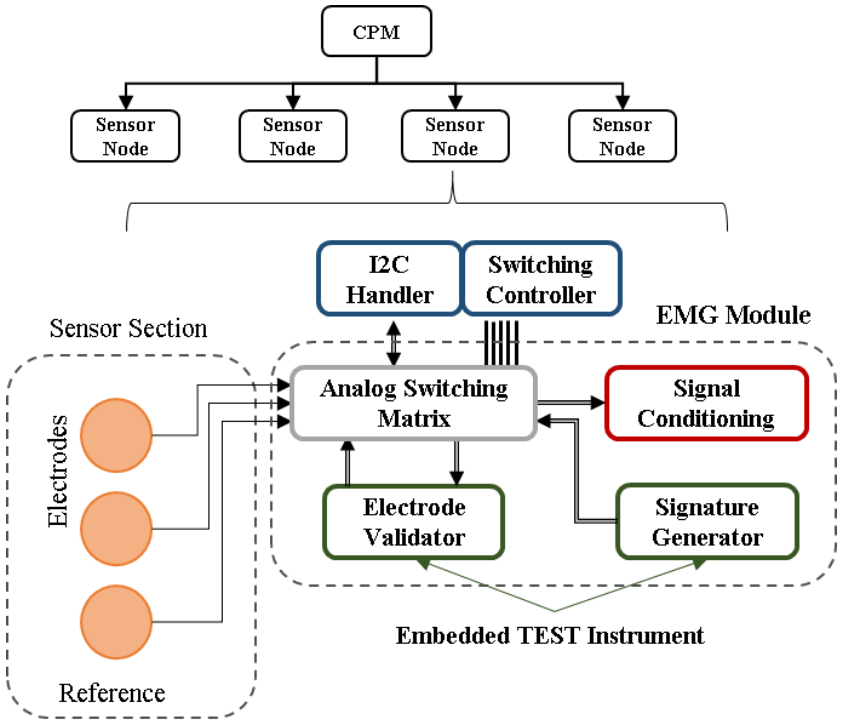


Figure 6-15 — EMG module BIST structure.

The electrode-skin impedance verification circuit was developed following a straight forward approach, based on the injection of a small current (lower than 10μA) in order to ascertain an electrode pair target load. Individual electrode-skin interface strategies generally utilize a three electrodes approach (one electrode-skin contact target and two others for sinking and voltage reference respectively); however, an electrode pair-wise verification was preferred in this case, in order to maintain simplicity. A single-supply current to voltage converter was used as observed in Figure 6-16, which includes a calibration resistor in parallel with the target load in order to control threshold limits and avoid open feedback

scenarios. The stimulating current being introduced to the body is a paramount consideration, in order to comply with IEC60601-1 standard, thus the presence of a limiting reference resistor. A local DC reference can be applied as stimulus in addition to a virtual ground compensated square wave signal sent through the I2C bus.

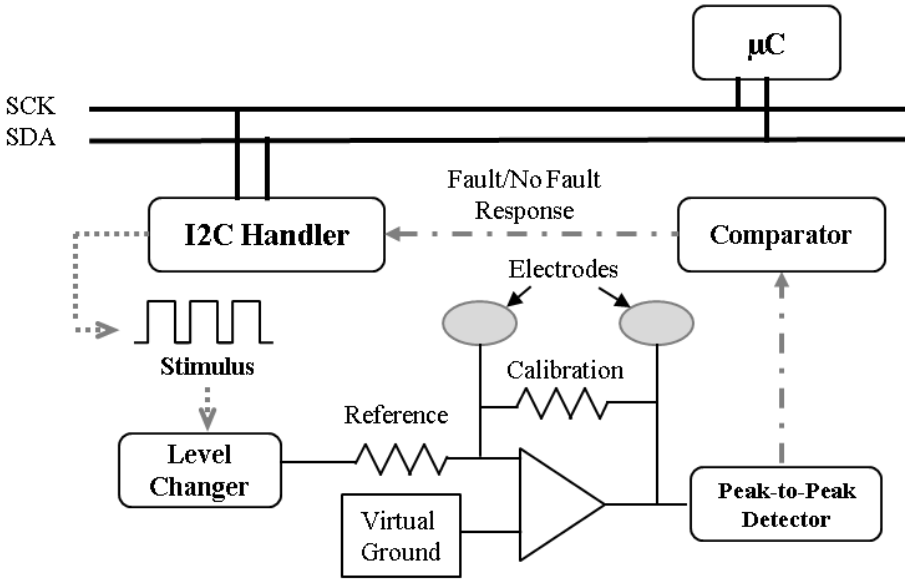


Figure 6-16 — Electrode-skin verification structure.

Common-mode rejection, amplification and filtering are regular stages of any electrode based signal conditioning circuit (Webster J. G., 2009). Such conditioning is performed in order to reduce the effects of common-mode potentials, random noise, motion and power-line artifacts, as well as to effectively retrieving the components of interest of the measured signal. Amplification factors and cut-off frequencies are dependent on the signal type (Webster J. G., 2009), and deviation can cause unwanted elements to be introduced into the conditioned signal.

The test of the signal conditioning circuit was achieved by means of the injection of an impulse stimulus at the input, fusion of the response of targeted nodes, and the collection of the final response in the form of a digital signature that can be compared against a response table. Such response table is composed by a set of signatures corresponding to the tolerance determined by acceptable components variations.

A delta-sigma (ΔΣ; or sigma-delta, ΣΔ) like modulator was used to convert the signal conditioning circuit response into a bit stream, being the I2C bus used for stimuli generation and response capture purposes (Figure 6-17). An I2C bus driven stimulus was preferred over a locally generated one, in order to reduce local sources of noise (such as clocks), gain increased stimulus shaped flexibility, and reuse of existing resources. The target observation nodes were determined through a sensitivity analysis after a SPICE simulation, which established that the low-pass filter output and the ADC input are the nodes that best reflect variations within the components of the signal conditioning circuit, seen in Figure 6-18. The signal conditioning circuit test impulse is designed in order to stimulate the signal

conditioning circuit frequency bandwidth and amplitude full range. The observation of different analogue nodes and their compression into a single bit stream improves observability and saves test response resources and time. This way the need for an analogue test bus line, the inclusion of a complex analogue to digital converter and the multiplexed test response acquisition are avoided.

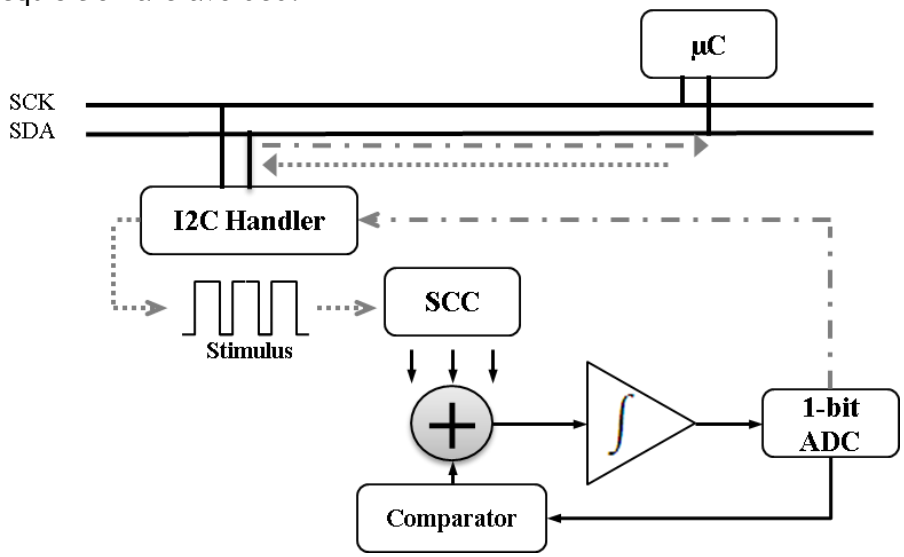


Figure 6-17 — Signal conditioning circuit test infrastructure.

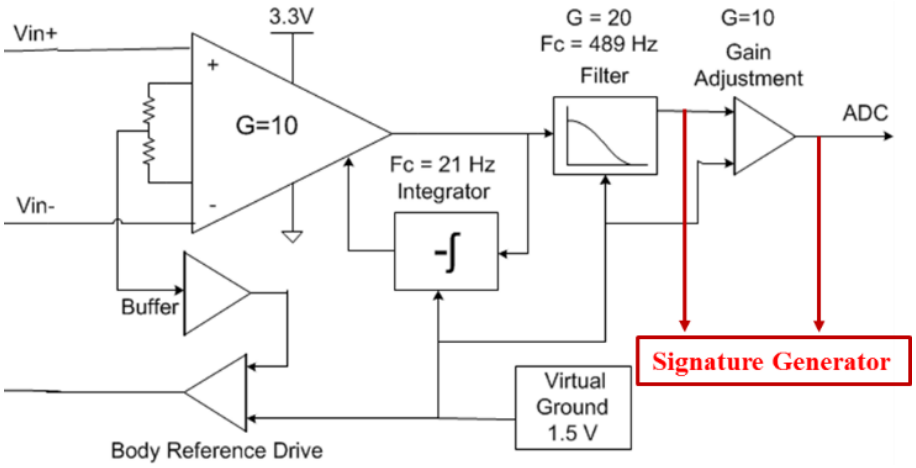


Figure 6-18 — Signal conditioning circuit test nodes.

In order to reduce noise along the communication lines, complexity and total area of the test circuit, it was decided to differ from traditional delta-sigma modulators, by eliminating the flip-flops generally present between comparators. The output of the signature generator was kept in a non-ground state through the use of a pull-up resistor until the test stimulus forces the first '0', to ensure a known initial condition and thus a predictable start sequence, compatible with I2C as well. After such start event, the signal is captured every 10 µs during 1.05 ms generating a 105-bit signature.

The resulting signature is acquired through the I2C bus by the local processing module, which applies a window bit density filtering and Ziv-Lempel based lossless compression algorithm (Ziv & Lempel, 1977). As the signal conditioning circuit test response presents

variations due to the acceptable tolerances of its components, the golden signature is actually a set comprising the signatures of the different admissible responses. The Ziv-Lempel based lossless compression algorithm replaces repetitive bit sequences by a shorter code, as observed in Figure 6-19.

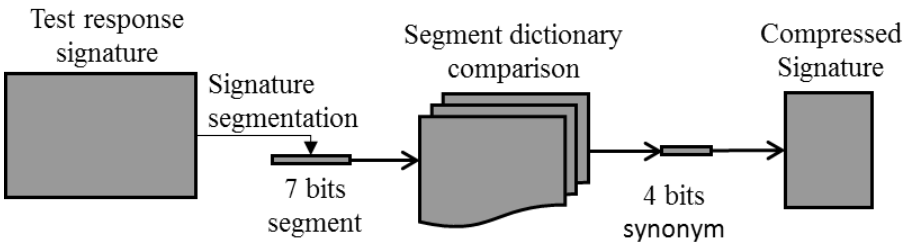


Figure 6-19 — Compression algorithm overview.

In order to manage the previously mentioned testing sequences, the SCPS framework compatible approach was established. In the present case, a simplified command set served for event identification, utilized for routing elements configuration. On-the-fly stimuli configurability (when a stimulus was expected from an external source) was achieved through an event sequence compatible with I2C, which permits the transporting the stimulus and response to and from the target module as described in Figure 6-20.

The sequence sets up the appropriate routing configuration through acknowledgement of a test command and uses the next two SCK low for stimulus and response transport. In order to avoid start/stop events from occurring, the master element insures a low state of the SDA prior to SCK high. A re-start or stop event can then be used at the event of the sequence to finalize the action.

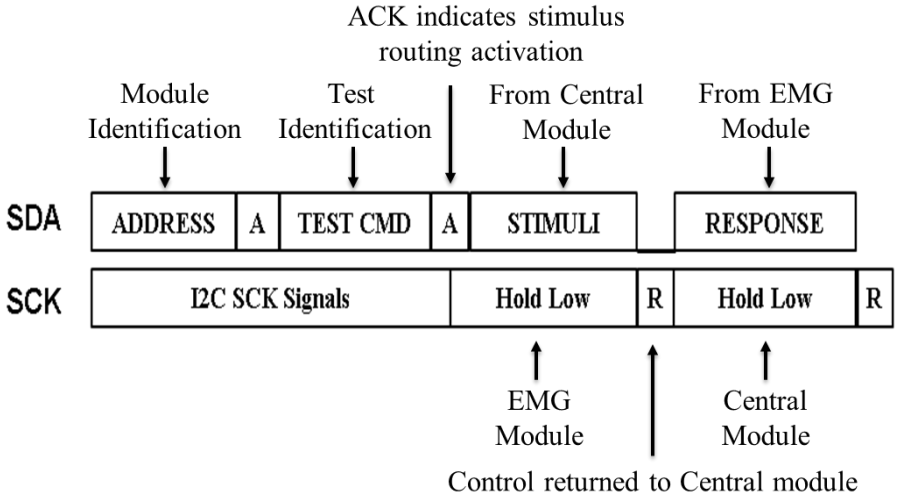


Figure 6-20 — SCPS/I2C compatible sequence for stimulus/response transport.

Chapter 7 Conclusion and Recommendations

Mixed-signal, analogue and sensor testing represents one of the most complex challenges of electronics production, in no small part due to the approach that analogue design has undertaken within the electronic community. The digital world has benefitted greatly of standardization, some say at the loss of flexibility and creativity, due to the use of design automation strategies and instruments; however, the gains clearly outweigh the loss evidenced by the well-established methodologies of testing, design for testability, design automation and the number of time proven methods and strategies that serve digital electronics in general.

Although there is evidence that analogue electronics and sensors do not share the modelling simplicity of their digital counterparts, it is necessary to pursue a common syntax simplification in order to achieve a point of industry/academy reinforced progress. Such efforts are palpable through international agreements and joint action tasks, where communication and physical layers seems to benefit the most with cases such as DFI, MIDI, HDMI, to name a few; however, broader projects such as Nanotest, TOETS and ELESIS aim for higher ground.

The present work is a contribution to the area of mixed-signal, analogue and sensor testing in general; although initially thought for wearable monitoring technology. It represents a consolidation of numerous preceding efforts and strategies, benefitting of their wisdom. In a way, it represents a methodology for analogue syntax translation into the digital domain, by presenting a digitally controlled and managed structure for mixed-signal, analogue and sensor test and measurement. Additionally, the introduction of the concept of groups, not new by any means (however novel in a way in this particular area), facilitates the re-utilization of resources and permits a different approach from the ones that seem to dominate up to this moment. Such strategy was only conceivable due to the multi-disciplinary context in which the work was realized, and the specific condition a wearable monitoring system introduces, revealing the importance of a multi-perspective approach and consideration of practical scenarios.

The author is the first to admit that by no means this work is a final solution to the overwhelming technological issue of analogue mixed-signal field, and should be only considered a step in this research area, hopefully in the right direction. The introduction of a group approach permits the reutilization of resources and the simplification of communication and synchronization strategies overhead; key aspects in the complex multi-core scenarios of SoC, BSN and other sensor and core driven strategies. Within wearable monitoring systems, the approach solves an issue of active operation testing management, necessary for continuous sensor state monitoring and calibration given the case. Standard methods such as

the 1149.X, provide core independent schemes; however, the complexity and style of the communication structure are incompatible with their mapping to *in-situ* managed setups, making them dependent on ATE. That said, ATE based strategies serve a valuable role at the production phase, nonetheless present limitations beyond such point. The increasing number of cores, analogue and sensor elements being incorporated within modern technology benefits of interdependence at the local level; nevertheless, core privacy need to be maintained. The SCPS methodology permits such interdependence without the loss of core construction disclosure, by defining a functional mapping of common actions. Such mapping, reflected within the defined setup, capture, process and scan functions, combined with granular addressability (for individual, group and global addressing), offer designers flexibility at the implementation level, while standardizing the syntax and actions, thus permitting the share of behavioural information for testing/measurement specific actions without compromising on design specifications.

One must admit that, although group addressing simplifies the access and control of multiple elements the methodology would benefit of a more automated addressing scheme that permits locally reprogrammable assignable identification, though such was left as a challenge for a future investigation. Some would also argue that element independence is lost through the use of the SCPS framework, moreover that the methodology suggest an inter-module coordination that would be seldom practical at industry level. Although such concern is shared by the author, evidence of industry level cooperation and compromise has been seen on the past decades and seems to be only gaining strength. Inter-modular collaboration should not be seen as a limitation; on the contrary, it is a path for reliability assurance through inter-module checks, balance and support.

The introduction of industry level standardized instruments will only reinforce the work presented within this thesis, and it is the strong recommendation of the author that their continuous exploration be continue, in particular within the field of wearable monitoring systems, due to their unique inherit inter-disciplinary requirements which benefits from collaborative methodologies at both processing and measurement level.

References

IEEE Std 1149.7-2009. (2009). IEEE Standard for reduced-pin and enhanced-functionality test access port and boundary-scan architecture. IEEE Standards.

IEEE Std 1500-2005 IDAMS 3.5 test. (2012). IEEE standard testability method for embedded core-based integrated circuits IDAMS 3.5. IEEE Standard. DOI:10.1109/IEEESTD.2012.6311551.

AAMI. (2000). ANSI/AAMI EC12:2000 Disposable ECG electrodes. AAMI Reaffirmation 2010. AAMI.

Agilent Technologies. (2009). Agilent impedance measurement handbook: A guide to measurement technology and techniques. Agilent Technologies.

Akyildiz, I. F., Su, W., Sankarasubramaniam, Y., & Cayirci, E. (2002, March 15). Wireless sensor networks: A survey. Computer Networks, 38(4), 393-422. DOI:10.1016/S1389-1286(01)00302-4.

Albus, Z., Valenzuela, A., & Buccini, M. (2009, October). Ultra-low power comparison: MSP430 vs. Microchip XLP Tech Brief.

Al-Obaidi, A. A., & Meribout, M. (2011). A new enhanced Howland voltage controlled current source circuit for EIT applications. IEEE GCC Conf. and Exhibition. Dubai, United Arab Emirates: IEEE Proceedings.

Altera Corporation. (2010). Stratix Series FPGA low power consumption features. (Altera Corporation) Retrieved 2010, from FPGA, CPLD and ASIC from Altera: http://www.altera.com/products/devices/stratix-fpgas/stratix-iv/overview/power/stxiv-power.html?GSA_pos=1&WT.oss_r=1&WT.oss=low power fpga

Analog Devices. (2011). ADXL345 digital accelerometer datasheet Rev. C s1. Analog Devices.

Analog Devices. (2013). Low cost CMOS, high speed, rail-to-rail amplifiers. Analog Devices. Retrieved from http://www.analog.com/static/imported-files/data_sheets/ADA4891-1_4891-2_4891-3_4891-4.PDF

Analog Devices Inc. (2011). ADG711/ADG712/ADG713: CMOS low voltage 4 Ω SPST switches. Rev. B. Analog Devices. Retrieved from www.analog.com

Analog Devices, Inc. (2012). AD5934: 250 kSPS, 12-bit impedance converter, network analyzer: Rev. C. Analog Devices. Retrieved from www.analog.com

Andlauer, R., & Vu, P. (2002, May 27). Analog test bus grows in importance. EDN Network. Retrieved www.edn.com

Annus, P., Krivoshei, A., Min, M., & Parve, T. (2008). Excitation current source for bioimpedance measurement applications: analysis and design. IEEE Int. Instrumentation and Measurement Technology Conf. Victoria, Canada: IEEE Proceedings.

ANSI. (2005). IEC 60601-1-3: Medical electrical equipment - Part 1: General requirements for basic safety and essential performance. (3.0 ed.). ANSI.

Arabi, K., & Kaminska, B. (1996). Oscillation-test strategy for analog and mixed-signal integrated circuits. Proceedings VLSI Test Symposium (pp. 476-482). Princeton, NJ: IEEE. DOI:10.1109/VTEST.1996.510896.

Arabi, K., & Kaminska, B. (1997). Oscillation built-in self-test (OBIST) scheme for functional and structural testing of analog and mixed-signal integrated circuits. Proceedings of International Test Conference (pp. 786-795). IEEE. DOI:10.1109/TEST.1997.639692.

Arbet, D., Stopjakova, V., Majer, L., Gyepes, G., & Nagy, G. (2013). New OBIST Using on-chip compensation of process variations toward increasing fault detectability in analog ICs. IEEE Transactions on Nanotechnology, 12(4), 486-497. DOI:10.1109/TNANO.2013.2251656.

Aroom, K. R., Harting, M. T., Cox, C. S., Radharkrishnan, R. S., Smith, C., & Gill, B. S. (2009). Bioimepdance analysis: A guide to simple design and implementation. Journal of Surgical Research, 153, 23-30.

Assambo, C., Baba, A., Dozio, R., & Burke, M. J. (2007). Determination of the parameters of the electrode-skin impedance model for ECG measurements. Proceedings of the 6th WSEAS Int. Conf. on Electronics, (pp. 90-95). Corfu, Greece.

Avci, A., Bosch, S., Marin-Perianu, M., Marin-Perianu, R., & Havinga, P. (2010). Activity recognition using inertial sensing for healthcare, wellbeing and sports applications: a survey. Proceedings of International Conference in Architecture of Computing Systems (ARCS) (pp. 1-19). Hannover, Germany: IEEE.

AVR XMEGA; Rev. 7925C-AVR-10/08/10M. (2008).

Azais, F., Bernard, S., Betrand, Y., & Renovell, M. (2000). Towards an ADC BIST scheme using the histogram test technique. European Test Workshop, 2000. Proceedings. IEEE.

Azimane, M. (2012). Reducing test cost for mixed signal circuits: from TOETS to ELESIS. Proceedings 17th IEEE European Test Symposium (ETS). Annecy, France: IEEE. DOI:10.1109/ETS.2012.6233051.

Aziz, O., Lo, B., Darzi, A., & Yang, G.-Z. (2006). Introduction. In G.-Z. Yang (Ed.), Body Sensor Networks. London: Springer Verlag.

Bächlin, M., Föster, K., & Tröster, G. (2009). SwimMaster: a wearable assistant for swimmer. Proceedings of 11th International Conference on Ubiquitous Computing, (pp. 215-224). DOI:10.1145/1620545.1620578.

Baker, B. (2000). AN682: using single supply operational amplifiers in embedded systems. Microchip. Retrieved ww1.microchip.com

Baker, K., Richardson, A. M., & Dorey, A. P. (2002). Mixed signal test: techniques, applications and demands. IEE Proceedings Circuits, Devices and Systems, 143(6), 358-365. DOI:10.1049/ip-cds:19960904.

Barnea, A., Oprisan, C., & Olaru, D. (2012). Force sensitive resistors calibration for use in gripping devices. Mechanical testing and diagnosis, 3, 18-27.

Barragán, M. J., Vásquez, D., Rueda, A., & Huertas, J. L. (2010). Guidelines for the efficient design of sinewave generators for analog/mixed-signal BIST. 16th International Mixed-Signals, Sensors and Systems Test Workshop. Seville, Spain: IEEE Proceedings.

Basio, W., & Prasad, A. (2006). Analysis of skin-electrode impedance using concentric ring electrode. Conference Proceedings IEEE Engineering in Medicine and Biology Society (pp. 6414-6417). IEEE.

Beckmann, L., Neuhaus, C., Medrano, G., Junqbecker, N., Walter, M., Gries, T., & Leonhardt, S. (2010). Characterization of textile electrodes and conductors using standardized measurement setups. Physiological Measurements, 31(2), 233-247. DOI:10.1088/0967-3334/31/2/009. Epub 2010 Jan 20.

Bennetts, R. G. (2007). IEEE 1149.1 JTAG and boundary scan tutorial. Technical paper. ASSET.

Bilas, V., Santic, A., Lackovic, I., & Ambrus, D. (2001). A low.power wireless interface for human gait assessment. Proceedings of the 18th IEEE Instrumentation and Measurement Technology Conference (pp. 614-618). IEEE. DOI:10.1109/IMTC.2001.928891

Bleecker, J., Bolas, M., Carter, W., Hoberman, P., & Meyers, A. (2007). Mobzombies: A wearable sensor for a playground style electronic game. 11th IEEE International Symposium on Wearable Computers. Boston, MA, USA: IEEE.

Bonato, P. (2005). Advances in wearable technology and application in physical medicine and rehabilitation. Journal in NeuroEngineering Rehabilitation, 2, 2.

Bonato, P., De Rossi, D., Dittmar, A., Jayaraman, S., Korhonen, I., Lymberis, A., Yuan-Ting, Z. (2006). IEEE EMBS Technical Committee on wearable biomedical sensors & systems: Position paper. Proceedings of the International Workshop on Wearable and Implantable Body Sensor Networks (BSN'06). 0-7695-2547-4/06. Boston, USA: IEEE. DOI:10.1109/BSN.2006.28.

Borges, L. M., Barroca, N., Velez, F. J., & Lebres, A. S. (2009). Smart-clothing wireless flex sensor belt network for foetal health monitoring. 3rd International Conference on Pervasive Computing Technologies for Healthcare 2009. London, UK: IEEE.

Borges, L. M., Rente, A., Velez, F. J., Salvado, L. R., Lebres, A. S., Oliveira, J. M., Ferro, J. (2008). Overview of progress in smart-clothing project for health monitoring and sport applications. First International Symposium on Applied Sciences in Biomedical and Communication Technologies. Aalborg, Denmark: IEEE.

Bourdenas, T., & Sloman, M. (2009). Towards self-healing in wireless sensor networks. Proceedings of Wearable and Implantable Body Sensor Networks (pp. 15-20). IEEE. DOI:10.1109/BSN.2009.14.

Bourke, P. (1999, December). Interpolation methods. Retrieved 2010, from http://local.wasp.uwa.edu.au/~pbourke/

Boverman, G., Kim, B. S., Isaacson, D., & Newell, J. C. (2007). The complete electrode model for imaging and electrode contact compensation in electrical impedance tomography. Proc. 29th IEEE EMBS. IEEE Proceedings.

Braga, J. A., Da Silva, J., Alves, J. C., & Matos, J. S. (2004). A wrapper for testing analogue to digital converters cores in SoCs. Proceedings of IEEE European Test Symposium (pp. 170-175). IEEE.

Brown, J. Q., Srivastava, R., & McShane, M. J. (2005). Encapsulation of glucose oxidase and an oxygen-quenched flurophore in polyelectrolyte-coated calcium alginate microspheres as optical glucose sensor systems. Biosensors and Bioelectronics, 21(1).

Buis, A. W., & Convery, P. (1997). Calibration problems encountered while monitoring stump/socket interface pressures with force sensing resistors: techniques adopted to minimise inaccuracies. Prosthetics and Orthotics International, 21(3), 179-182.

Bushnell, M., & Agrawal, V. (2000). Model-based analog and mixed-signal test. In M. Bushnell, & V. Agrawal, Essentials of electronic testing for digital, memory and mixed signal VLSI circuits (pp. 385-416). Springer. DOI:10.1007/0-306-47040-3_11.

Bychkovskiy, V., Megerian, S., Estrin, D., & Potkonjak, M. (2003). Colibration: a collaborative approach to in-place sensor calibration. Proceeding of the International Conference on Information Processing in Sensor Networks (pp. 301-316). Springer-Verlag.

Charles, H. K., & Cain, R. P. (2009). Ultra-thin and flexible physiological monitoring system. Proceedings on IEEE Sensors Applications Symposium (pp. 230-235). New Orleans, USA: IEEE. DOI:10.1109/SAS.2009.4801806.

Chen, H.-k., Wang, C.-h., & Su, C.-c. (2002). A self-calibrated ADC BIST methodology. Proceedings of the 20 th IEEE VLSI Test Symposium (VTS'02).

Cheng, K. S., Isaacson, D., Newell, J. C., & Gisser, D. G. (1989). Electrode models for electrical current computed tomography. IEEE Transactions on Biomedical Engineering, 36(9).

Cheng, L., & Haile, S. (2008). Managed exercise monitoring: a novel application of wireless on-body inertial sensing. 5th International Summer School and Symposium on Medical Devices and Biosensors. IEEE.

Cheng, L., & Hailes, S. (2008). Analysis of wireless inertial sensing for athlete coaching support. IEEE Global Telecommunications Conference. IEEE.

Chi, E. H. (2005). Introducing wearable force sensors in martial arts. IEEE Pervasive Computing, 4(3), 47-53.

Collete, M., Humeau, A., & Abraham, P. (2008). Time and spatial invariance of impedance signals in limbs of healthy subjects by time-frequency analysis. Annals of Biomedical Engineering, 36(3), 444–451.

Connaghan, D., Hughes, S., May, G., Kelly, P., Conaire, C., O'Connor, N., Moyna, N. (2009). A sensing platform for physiological and contextual feedback to tennis athletes. Sixth International Workshop on Wearable and Implantable Body Sensor Networks, IEEE Conferences.

CORDIS. (2010, January 27). CORDIS: The DIAMOND project. Retrieved August 21, 2013, from European Commission: http://cordis.europa.eu/fetch?CALLER=EN_NEWS&ACTION=D&SESSION=&RCN=31703

Coyle, S., Lau, K.-T., Moyna, N., & al., e. (2010, March). BIOTEX: biosensing textiles for personalised healthcare management. IEEE Transactions on Information Technology in Biomedicine, 14(2), 364-370. DOI:10.1109/TITB.2009.2038484.

Crouch, A. (2011). IEEE P1687 Internal JTAG (IJTAG) tutorial. ASSET InterTech, Inc.

Cumming, D. R., Hammond, P. A., Wang, L., Cooper, J. M., & Johannessen, E. A. (2006). Wireless sensor microsystem design: Practical perspective. In G.-Z. Yang (Ed.), Body Sensor Networks. London, UK: Springer-Verlag.

Cunha, J. P., Cunha, B., Pereira, A. S., Xavier, W., Ferreira, N., & Meireles, L. (2010). Vital-Jacket®: A wearable wireless vital signs monitor for patients' mobility in cardiology and sports. 4th International Conference on Pervasive Computing Technologies for Healthcare (PervasiveHealth). IEEE.

CWAV Inc. (2013). USBEE ZX PC and USB logic analyzer, signal generator, protocol decoder and analyzer. Retrieved JUne 10, 2014, from http://www.usbee.com/zx.html.

da Silva, E., Costa, F., Behrens, F., Kickhofel, R., & Maltione, R. (2009). Analog test bus architecture for small die size and limited pin count devices with internal IPs testability emphasis. 10th Latin American Test Workshop.

da Silva, J. M. (2014). ProLimb Webpage. Retrieved July 28, 2014, from http://paginas.fe.up.pt/~jms/prolimb/prolimb.html#results.

Das, S. R., Zakizadeh, J., Biswas, S., Assaf, M. H., Nayak, A. R., Petriu, E. M., . . . Sahinoglu, M. (2007). Testing analog and mixed-signal circuits with built-in hardware— A new approach. IEEE Transaction on Instrumentation and Measurement, 840-855. DOI:10.1109/TIM.2007.894223.

DaSilva, F., Zorian, Y., Whetsel, L., Arabi, K., & Kapur, R. (2003). Overview of the IEEE P1500 standard. Proceedings of Test Conference (pp. 988,997). IEEE. DOI:10.1109/TEST.2003.1271086.

Datasheet: Linear technology. (n.d.). LTC1407-1/LTC1407A-1. Serial 12-Bit/14-Bit, 3Msps simultaneous sampling ADCs with shutdown.

Datasheet: Linear technology. (n.d.). LTC6912 dual programmable gain amplifiers with serial digital interface.

Degen, T., & Jackel, H. (2008). Continuous monitoring of electrode-skin impedance mismatch during bioelectric recordings. IEEE Transactions on Biomedical Engineering, 55(6), 1711-1715.

Degen, T., & Loeliger, T. (2007). An improved method to continuously monitor the electrode-skin impedance during bioelectric measurements. 29th IEEE EMBS. IEEE Proceedings.

Dewei, J., & Jing, L. (2009). Human power-based energy harvesting strategies for mobile electronic devices. Frontiers of Energy and Power Engineering in China, 3(1).

Digikey. (2014). DV1-100 Tech Tools | DV1-100 ND | Digikey. Retrieved June 10, 2014, from http://www.digikey.pt/product-detail/en/DV1-100/DV1-100-ND/565870.

Dillard, W., Narayanan, K., Trent, V., & Greene, M. (2008). Issues in wearable biomechanical inertial sensor systems. IEEE/ION Position, Location and Navigation Symposium. IEEE Conferences.

Donno, M., Palange, E., Di Nicola, F., Bucci, G., & Ciancetta, F. (2007). A flexible optical fibre goniometer for dynamic angular measurements. IEEE Instrumentation and Measurement Technology Conference Proceedings (pp. 1-5). IEEE.

Duan, J., Chen, D., & Geiger, R. (2009). Cost effective signal generators for ADC BIST. Circuits and Systems, 2009. ISCAS 2009.

Dufort, B., & Roberts, G. W. (1999). On-chip analog signal generation for mixed-signal built-in self-test. 34, No 3.

Duzevik, I. (Oct 2003). Design and implementation of IEEE 1149.6. Test Conference, 2003. Proceedings. ITC 2003. International, (pp. pp. 87-95 Vol.2).

Eklow, B. (2005). An Update on IEEE 1149.6 - Successes and issues. Test Conference, 2005. Proceedings. ITC 2005. IEEE International, (p. 7).

Eklow, B., Barnhart, C., Ricchetti, M., & Borroz, T. (Oct. 2003). IEEE 1149.6 - a practical perspective. Test Conference, 2003. Proceedings. ITC 2003. International, (pp. pp. 70-78 Vol.2).

Eklow, B., Parker, K., & Barnhart, C. (Oct. 2003). IEEE 1149.6: a boundary-scan standard for advanced digital networks. Design & Test of Computers, IEEE, (pp. vol.20, no.5, pp. 76-83).

EMBS. (2008). Technical Committee on Wearable Biomedical Sensors and Systems: Home. (Engineering in Medicine and Biology Society) Retrieved 03 24, 2010, from Technical Committee on Wearable Biomedical Sensors and Systems: http://tc-wearable-sensors.embs.org/index.html.

ENIAC. (2013). ELESIS: European library-based flow of embedded silicon test instruments. ENIAC.

Ermes, M., Parkka, J., Mantyjarvi, J., & Korhonen, I. (2008). Detection of Daily Activities and Sports With Wearable Sensors in Controlled and Uncontrolled Conditions. IEEE Transactions on Information Technology in Biomedicine, 12(1).

Evers, S. M., Struijs, J. N., Ament, A. J., van Genugten, M. L., Jager, J. H., & van den Bos, G. A. (2004, April 8). International comparison of stroke cost studies. Stroke, 35(5), 1209-1215. DOI: 10.1161/01.STR.0000125860.48180.48.

Fatang, C., & Linyu, Y. (2011). The design and application of I2C Bus in the TD-LTE Comprehensive Test Instrument. Proc. of Int. Conf. on Business Comp. and Global Informatization. IEEE Computer Society.

Fefer, D., Drnovsek, J., & Jeglic, A. (1993). Comparative analysis of digital sinewave generation. Proceedings IMTC93 (pp. 668-669). Irvine, CA, USA: IEEE. DOI:10.1109/IMTC.1993.382560.

Feng, J., Qu, G., & Potkonjak, M. (2004). Sensor calibration using nonparametric statistical characterization of error models. Proceedings of IEEE Sensors (pp. 1456-1459). IEEE. DOI:10.1109/ICSENS.2004.1426461.

Ferreira, J., Seoane, F., & Lindecrantz, K. (2011). AD5933-based electrical bioimpedance spectrometer. Towards textile-enabled applications. Proceedings of EMBC 2011 (pp. 3282-3285). IEEE. DOI:10.1109/IEMBS.2011.6090891.

Florez, J. A., & Velasquez, A. (2010). Calibration of force sensing resistors (FSR) for static and dynamic applications. ANDESCON (pp. 1-6). IEEE. DOI:10.1109/ANDESCON.2010.5633120.

Föster, K., Brem, P., Rogen, D., & Tröster, G. (2009). Unsupervised classifier self-calibration through repeated context occurrences: Is there robustness against sensor displacement to Gain? Proc. 13th IEEE Int. Symposium on Wearable Computers (pp. 77-84). IEEE.

Franks, W., Schenker, I., Schmutz, P., & Hierlemann, A. (2005, July). Impedance characterization and modelling of electrodes for biomedical applications. IEEE Transactions on Biomedical Engineering, 52(7), 1295-1302.

Gamry Instruments Inc. (2010). Application note: Potentiostat fundamentals. Rev. 2.0 8/25/2011. Warminster, PA, USA. Gamry Instruments.

Gamry Instruments, Inc. (2011). Two-, three-, and four-electrode experiments. Tech Note, Rev. 3.0. USA: Gamry Instruments, Inc.

Garrault, P., & Philofsky, B. (2006). HDL coding practices to accelerate design performance. XILINX. White Paper: Virtex-4, Spartan-3/3L, and Spartan-3E FPGAs.

Glaros, C., Fotiadis, D. I., Likas, A., & Stafylopatis, A. (2003). A wearable intelligent system for monitoring health condition and rehabilitation of running athletes. 4th Annual IEEE Conference on Information Technology Application in Biomedicine. UK: IEEE.

Gopalai, A. A., Senanayake, A., & Gouwanda, D. (2011). Determining level of postural control in young adults using force sensing resistors. IEEE Transactions on Information Technology in Biomedicine, 15(4), 608-6014. DOI:10.1109/TITB.2011.2140378.

Grillet, A., Barco, N. V., Kinet, D., Witt, J., Schukar, M., Krebber, K., Depre, A. (2008, July). Optical fiber sensors embedded into medical textiles for healthcare monitoring. IEEE Sensors, 8(7), 1215-1222. DOI:10.1109/JSEN.2008.926518.

Grimbergen, C. A., VanRijn, A. C., & Peper, A. (1992). A method for the measurement of the properties of individual electrode-skin interfaces and the implications of the electrode properties for preamplifier design. International Conference of the IEEE Engineering in Medicine and Biology Society. 6, pp. 2382-2383. Paris, France: IEEE. DOI:10.1109/IEMBS.1992.5761414.

Grimnes, S. (2006). Bioimpedance. In Wiley Encyclopedia of Biomedical Engineering. John Wiley & Sons.

Griss, P., Tolvanen-Laakso, H. K., Meriläinen, P., & Stemme, G. (2002). Characterization of micro machined spiked biopotential electrodes. IEEE Transactions on Biomedical Engineering, 49(6).

Hall, R. S., Desmoulin, G. T., & Milner, T. E. (2008, December 5). A technique for conditioning and calibrating force-sensing resistors for repeatable and reliable measurement of compressive force. Journal of Biomechanics, 41(16), 3492-3495. DOI:10.1016/j.jbiomech.2008.09.031.

Hannu, J., Hakkinen, J., Voutilainen, J. V., Jantunen, H., & Moilanen, M. (2012). Current state of the mixed-signal test bus 1149.4. Journal Electron Test, 857-836. DOI:10.1007/s10836-012-5339-7.

Hao, Y., & Foster, R. (2008). Wireless body sensor networks for health-monitoring applications. Physiological Measurements, 29, 27-56.

Harth, Y., & Lischinsky, D. (2011). A novel method for real-time skin impedance measurement during radiofrequency skin tightening treatments. Journal of Cosmetic Dermatology, 10, 24-29.

Hary, D., Bekey, G. A., & Antonelli, D. J. (1987). Circuit models and simulation analysis of electromyographic signal sources - I: The impedance of EMG electrodes. IEEE TRANSACTIONS ON BIOMEDICAL ENGINEERING, BME-34(2).

Haslett, J. W., & Rao, M. K. (1979, June). A high quality controlled current source. IM-28(2), 132-140.

Heile, B. (2012, September 23). IEEE 802.15 Working group for WPAN. Retrieved September 1, 2013, from http://www.ieee802.org/15/.

Heinz, E. A., Kunze, K. S., Gruber, M., Bannach, D., & Lukowicz, P. (2006). Using wearable sensors for real-time recognition tasks in games of martial arts - An initial experiment. 2006 IEEE Symposium on Computational Intelligence and Games. Lake Tahoe, NV, USA: IEEE.

Henrey, M., Sheridan, C., Khokhar, Z. O., & Menon, C. (2009). Towards the development of a wearable rehabilitation device for stroke survivors. Proceedings IEEE International Conference Science and Technology for Humanity (TIC-STH) (pp. 12-17). Toronto, Canada: IEEE. DOI:10.1109/TIC-STH.2009.5444522

Hermens, H. J., Freriks, B., Merletti, R., Stegeman, D., Blok, J., Rau, G., Hägg, G. (1999). European recommendations for surface electromyography. Enschede, the Netherlands: Roessingh Research and Development. Retrieved from http://www.seniam.org/

Hewson, D. J., Duchene, J., & Hogrel, J. Y. (2001). Changes in impedance at the electrode-skin interface of surface EMG electrodes during long-term EMG recordings. Proceedings of the 23rd Annual International Conference of the IEEE Engineering in Medicine and Biology Society. 4, pp. 3345-3348. IEEE. DOI:10.1109/IEMBS.2001.1019543.

Higgins, H. (2006). Wireless Communication. In G.-Z. Yang (Ed.), Body sensor networks. London, UK: Springer-Verlag.

Higgins, M., MacNamee, C., & Mullane, B. (2008). IEEE 1500 wrapper control using an IEEE 1149.1 test access port. Proceedings IET Signals and Systems Conf. Galway, Ireland: IEEE.

Hoffman, K. P., Ruff, R., & Poppendieck, W. (2006). Lon-term characterization of electrode materials for surface electrodes in biopotential recording. Proc. 28th IEEE EMBS. IEEE Proceedings.

Holleczek, T., Zysset, C., Arnrich, B., Roggen, D., & Troster, G. (2009). Towards an interactive snowboarding assistance system. International Symposium on Wearable Computers. IEEE Conferences.

Hosticka, B. J. (2007). Analog circuits for sensors. Proceedings of Solid State Circuits Conference (pp. 97-102). IEEE.

Huang, B., Chen; Shi, X., & Xu, Y. (2007). Gait event detection with intelligent shoes. International Conference on Information Acquisition. Jeju City, Korea: IEEE. DOI:10.1109/ICIA.2007.4295799

Huang, J. J., & Cheng, K. S. (1998). The effect of electrode-skin interface model in electrical impedance imaging. Proc. Int. Conf. on Image Processing. IEEE Proceedings.

Huigen, E., Peper, A., & Grimbergen, C. A. (2002). Investigation into the origin of the noise of surface electrodes. Medical and Biological Engineering and Computing, 40(3), 332-338. DOI:10.1007/BF02344216.

I2C-bus.org. (n.d.). I2C Bus: Addressing. Retrieved 04 07, 2014, from http://www.i2c-bus.org/addressing/.

I2C-bus.org. (n.d.). Typical I2C bus setup. Retrieved 04 07, 2014, from http://www.i2c-bus.org/typical-i2c-bus-setup/.

IEE International Electronics and Engineer. (2007). Specification sheet for standard single sensors: Pressure sensitive single sensor, Rev. 6. IEE.

IEEE 1149.4-1999. (2000). IEEE standard for a mixed-signal test bus. IEEE Standards.

IEEE Std. 1149.1-1990. (1990). IEEE standard test access port and boundary-scan architecture. IEEE Standard. DOI:10.1109/IEEESTD.1990.114395.

IEEE Std. 1149.1-2001. (2001). IEEE standard test access port and boundary-scan architecture. IEEE Standards.

IEEE Std. 1149.1-2013. (2013). IEEE standard for test access port and boundary-scan architecture. IEEE Standards. DOI:10.1109/IEEESTD.2013.6515989.

IEEE Std. 1149.4-2010. (2011). IEEE standard for a mixed-signal test bus. IEEE Standards.

IEEE Std. 1149.6-2003. (2003). IEEE standard for boundary-scan testing of advanced digital networks. IEEE Standards.

IEEE Std. 1149.7-2009. (2010). IEEE standard for reduced-pin and enhanced-functionality test Access Port and Boundary-Scan Architecture. IEEE Standards.

Imote2: High-performance Wireless Sensor Network Node. (n.d.). 6020-0117-02 Rev A.

Inmotion Inc. (2010). Inmotion: 1-5-3-81cm-force-sensing-resistor. Retrieved July 5, 2014, from http://www.inmotion.pt/store/1-5-3-81cm-force-sensing-resistor.

Interlink Electronics. (2010, June 9). Model: INM-0038 1.5" (3.81 cm) Force Sensing Resistor. Retrieved July 5, 2014, from http://www.inmotion.pt/store/1-5-3-81cm-force-sensing-resistor.

Interlink Electronics. (2013). FSR 400 Series data sheet. Retrieved July 5, 2014, from http://www.interlinkelectronics.com/FSR406.php#

International Electrochemical Commission. (2005). International Standard 6060 - 1. (3er Ed.). International Electrochemical Commission.

International Technology Roadmap for Semiconductor. (2011). Test and test equipment. Retrieved from http://www.itrs.net/Links/2012ITRS/Home2012.htm

IRIS: Wireless measurement system. (n.d.). 6020-0124-01 Rev A. Datasheet. MEMSIC.

Jang, E. H., Cho, Y. J., Chi, S. Y., Lee, J. Y., Kang, S. S., & Chun, B. T. (2010). Recognition of walking intention using multiple bio/kinaesthetic sensors for lower limb exoskeletons. International Conference on Control, Automation and Systems. Gyeonggi-do, Korea: IEEE.

Jensen, J., Li, J., & Sigel, G. (1989). A fiber optic angular sensor for biomedical applications. Proceedings of the Annual International Conference of the IEEE Engineering in Engineering in Medicine and Biology Society. 4, pp. 1118-1119. IEEE.

Jette, A. M. (2005, December). The post-stroke rehabilitation outcomes project. Archives of Physical Medicine and Rehabilitation, 86(12), 124-125. DOI:10.1016/j.apmr.2005.09.015

Jiang, W., & Agrawal, V. D. (2008). Built-in self-calibration of on-chip DAC and ADC. Test Conference, 2008. ITC 2008.

Johnson, H., & Graham, M. (1993). High-speed digital design: A handbook of black magic. Upper Saddle River, New Jersey, USA: Prentice Hall.

Jones, D. L. (2004, June 29). PCB design tutorial. Retrieved from Alternatezone.

Kaminska, B., & Arabi, K. (2003). Mixed signal DFT: A concise overview. ICCAD, (pp. 672-679).

Kappenman, E. S., & Luck, S. J. (2010). The effects of electrode impedance on data quality and statistical significance in ERP recordings. Psychophysiology, 888-904. DOI:10.1111/j.1469-8986.2010.01009.x

Keithley Instruments Incorporated. (2011). Making precision voltage and low resistance measurements.

Kephart, J., & Chess, D. (2003). The vision of autonomic computing. Computer, 36(1).

Khan, Q., & Bang, S. (2009, April 9). Energy harvesting for self-powered wearable health monitoring system. Retrieved 2010, from EE Times Europe Analog: http://www.analog-europe.com/en/energy-harvesting-for-self-powered-wearable-health-monitoring-system.html?cmp_id=7&news_id=221901075.

Khazraee, M., Zamani, A. R., Hallajian, M., Ehsani, H. A., Moghaddam, H. A., Parsafar, A., & Shabany, M. (2013). A novel hardware implementation for joint heart rate, respiration rate, and gait analysis applied to body area networks. International Symposium on Circuits and Systems (pp. 1889-1892). IEEE. DOI:10.1109/ISCAS.2013.6572235.

Kilgore, K. L., Peckham, P. H., Keith, M. W., & Thrope, G. B. (1990). Electrode characterization for functional application to upper extremity FNS. 17(1).

Kim, B. C., Byrd, T., Toledo, F., Wokhlu, S., Beskar, E., Rousselin, R., Kendall, G. (2008). Low cost automatic mixed-signal board test using IEEE 1149.4. IEEE International Test Conference. IEEE Conferences.

Kim, D. J., & Prabhakaran, B. (2011). Motion fault detection and isolation in body sensor networks. Pervasive and Mobile Computing, 727-745.

Kim, S., Tazicioglu, R. F., Torfs, T., Dilpreet, B., Julien, P., & Van Hoof, C. (2010). A 2.4 uA continuous-time electrode-skin impedance measurement circuit for motion artifact monitoring in ECG acquisition systems. IEEE Symposium on VLSI Circuits (pp. 219-220). IEEE.

Knight, J. H., Schwirtz, A., Psomadelis, F., Baber, C., Bristow, H. W., & Arvanitis, T. N. (2005). The design of the SensVest. Pervasive Ubiquitous Computing 9: 6–19.

Knorr, B., Hughes, R., Sherrill, D., Stein, J., Akay, M., & Bonato, P. (2005). Quantitative measures of functional upper limb movement in persons after stroke. International IEEE EMBS Conference on Neural Engineering (pp. 252-255). IEEE. DOI:10.1109/CNE.2005.1419604.

Koukourlis, C. S., & Voulgaris, N. C. (1989). A digital method for sinewave generation. Archiv für Elektrotechnik, 72(5), 327-331.

Koushanfar, F., Potkonjak, M., & Sangiovanni-Vicentelli, A. (2003). On-line fault detection of sensor measurements. Proceedings of IEEE Sensors (pp. 974-979). IEEE. DOI:10.1109/ICSENS.2003.1279088.

Krohn, D. (2000). Fiber optic sensors: Fundamentals and application. USA: Instrument Society of America.

Kulla, J. (2013). Detection, identification, and quantification of sensor fault in a sensor network. Mechanical Systems and Signal Processing, 40(1), 208-221.

Kyle, U. G., Bosaeus, I., De Lorenzo, A. D., Deurenberg, P., Elia, M., Gomez, M. J., & Lilienthal, H. B. (2004). Bioelectrical impedance analysis - part II: utilization in clinical practice. Clinical Nutrition, 23(6), 1430-1453.

Lampasi, D. A., Moschitta, A., & Carbone, P. (2008). Accurate digital synthesis of sinewaves. IEEE Transaction on Instrumentation and Measurement, 57(3), 522-529. DOI:10.1109/TIM.2007.911583.

Lara, O. D., & Labrador, M. A. (2013). A survey on human activity recognition using wearable sensors. IEEE Communications surveys and tutorials, 1192-1209. DOI:10.1109/SURV.2012.110112.00192.

Lee, D. D. (2006). Development of an impedance method based wireless sensor node for monitoring of bolted joint preload. University of California, San Diego.

Lee, J. W., Oh, T. I., Paek, S. M., Lee, J. S., & Woo, E. J. (2003). Precision constant current source for electrical impedance tomography. 25th Int. Conf. of the IEEE EMBS. Cancun, Mexico: IEEE Proceedings.

Lee, K. J. (2006). Boundary scan and core-based testing. In L. T. Wang, C. W. Wu, & X. Wen (Eds.), VLSI Test Principles and Architectures (pp. 557-617). Elsevier.

Lee, N. C. (1993). Practical considerations for mixed-signal test bus. Proc. Int. Test Conference (pp. 591 - 592). Baltimore, MD, USA. IEEE. DOI:10.1109/TEST.1993.470649

Ley, A. (2009). DOIng more with less - An IEEE 1149.7 embedded tutorial: Standard for reduced-pin and enhanced-functionality test access port and boundary-scan architecture. International Test Conference. IEEE Conferences.

Ley, A. (2011). IEEE P1687 Internal JTAG (IJTAG) taps into embedded instrumentation. ASSET InterTech, Inc.

Li, R., Hu, X. L., & Tong, K. Y. (2008). Combined EMG-driven system with functional electrical stimulation for post stroke rehabilitation. Proc. 2nd EMBS and Conf. on Biomedical Robotics and Biomechatronics. IEEE Proceedings.

Li, Z., He, Z., Wang, W., & Ren, C. (2008). Measurement system for electrical impedance and EGG. Proc. 5th Int. Conf. on Information Tech. & Application on Biomedicine.

Liu, H., & Liu, W. D. (2010). Low-power and portable design of bioelectrical impedance measurement system. Proceedings of ICIE 2010 (pp. 38-41). IEEE. DOI:10.1109/IEMBS.2011.6090891.

Liu, Q., Hay, J., & Andrews, J. (1993). Body rolls and hand path in freestyle swimming: an experimental study. Journal of Applied Biomechanics, 238-253.

Lo, B. P., & Yang, G.-Z. (2007). Body sensor networks - Research challenges and opportunities. IET Seminar on Antennas and Propagation for Body-Centric Wireless Communications (pp. 26-32). IEEE.

Lo, B., & Yang, G. Z. (2005). Architecture for body sensor networks. Perspectives in Pervasive Computing (pp. 23-28). London, UK: IEEE.

Lo, B., & Yang, G. Z. (2005). Key technical challenges and current implementations of body sensor networks. 2nd International Workshop on Body Sensor Networks. London, UK: IEE Proceedings.

Lo, B., & Yang, G. Z. (2006). Body sensor networks: infrastructure for life science sensing research. Proceedings of IEEE Life Science Systems and Applications Workshop (pp. 1-2). IEEE. DOI:10.1109/LSSA.2006.250376.

Lo, B., & Yang, G.-Z. (2006). Body sensor networks: Infrastructure for life science sensing research. IEEE/NLM Life Science Systems and Applications Workshop. IEEE Conferences.

Lo, B., Deligianni, F., & Yang, G. Z. (2006). Source recovery for body sensor network. Proceedings of IEEE Body Sensor Networks (pp. 202-206). IEEE. DOI: 10.1109/BSN.2006.51

Lopez, A. D., Mathers, C. D., Ezzati, M., Jamison, D. T., & Murray, C. (2006, May 27). Global and regional burden of disease and risk factors, 2001: systematic analysis of population health data. The Lancet, 367(9524), 1747 - 1757. DOI: 10.1016/S0140-6736(06)68770-9.

Lorinxz, K., Kuris, B., Ayer, S., Patek, S., Bonato, P., & Welsh, M. (2007). Wearable wireless sensor network to assess clinical status in patients with neurological disorders. International Conference on Information Processing in Sensor Networks. Cambridge, MA, USA.

Lu, A. K., & Roberts, G. W. (1994). An analog multi-tone signal generator for built-in-self-test applications. International Test Conference.

Lu, A. K., Roberts, G. W., & Johns, D. A. (1994). A high-quality analog oscillator using oversampling D/A conversion techniques. 41, No 7.

Lubaszewski, M., Mir, S., & Pulz, L. (1997). ABILBO: Analog built-in block observer. Proc. Int. Cong. on Computer Aided Design.

Lukowicz, P. (2007). Bodynet architectures: the meaning of wearability. Proceeding of the ICST 2nd international conference on Body Area Networks. Brussels, Belgium.

Madhavan, R. (n.d.). Quick reference for Verilog HDL. Automata Publishing Company.

Madni, J. A., & Lee, J.-Y. (2009). Processing biometric data of game players using body sensors. IEEE Sensors Applications Symposium. New Orleans, USA: IEEE Conference.

Mahapatro, A., & Khilar, P. M. (2011). Online fault detection and recovery in body sensor networks. Proceedings WICT (pp. 407-412). IEEE. DOI:10.1109/WICT.2011.6141280.

Maher, M. P., Pine, J., Wright, J., & Tai, Y. C. (1999). The neurochip: a new multielectrode device for stimulating and recording from cultured neurons. Journal of Neuroscience Methods, 87(7).

Maher, M., Wright, J., Pine, J., & Tai, Y. C. (1998). A microstructure for interfacing with neurons: the neurochip. Proceedings of IEE Engineering in Medicine and Biology Society (EMBC) (pp. 1698-1702). Hong Kong\: IEEE. DOI:10.1109/IEMBS.1998.746911.

Mancini, R. (2000). Design of op amp sine wave oscillators. Analog and Mixed-Signal Products.

Mancini, R., & Palmer, R. (2001). Sine-wave oscillator. Texas Instruments Incorporated.

Mao, W., Gulati, R. K., Goel, D. K., & Ciletti, M. D. (1990). QUIETEST: a quiescent current testing methodology for detecting leakage faults. IEEE Computer Aided Design (pp. 280-283). IEEE. DOI:10.1109/ICCAD.1990.129902.

Margo, C., Katrib, J., Nadi, M., & Rouane, A. (2013). Four electrode embedded bioimpedance measurement system. Proceedings FTFC 2013. IEEE. DOI:10.1109/FTFC.2013.6577773.

Marquez, J. C., Seoane, F., Valimaki, E., & Lindecrantz, K. (2009). Textile electrodes in electrical bioimpedance measurements - a comparison with conventional Ag/AgCl electrodes. (pp. 4816-4819). Minneapolis, USA: IEEE. DOI:10.1109/IEMBS.2009.5332631.

Mars, P. (2010, 06 07). Managing the power in wireless sensor networks powered by energy-harvesting circuitry. (RF Designline) Retrieved 2010, from RF Designline: http://www.rfdesignline.com/howto/225400098.

Matsushita, S., Shiba, A., & Nagashima, K. (2006). A wearable fatigue monitoring system - Application of human-computer interaction evaluation. Seventh Australasian User Interface Conference. Conferences in Research and Practice in Information Technology, Vol. 50. Hobart, Australia.

Mc Adams, E. (2006). Bioelectrodes. In Encyclopaedia of Medical Devices Instrumentation (2 ed., Vol. 1). John Wiley & Sons.

McAdams, E. T., Jossinet, J., Lackermeier, A., & Risacher, F. (1996). Factors affecting electrode-gel-skin interface impedance in electrical impedance tomography. Medical and Biological Engineering and Computer, 34(6), 394-408. DOI: 10.1007/BF02523842.

McClelland, C. (2012). FPGALink user manual. Retrieved June 8, 2014, from http://www.swaton.ukfsn.org/docs/fpgalink/verilog_paper.pdf

McClelland, C. (2014). Dynamic illusions. Retrieved June 8, 2014, from http://www.makestuff.eu/wordpress/

McGinney, K. (2011, October 14). PXI modular instrument implementation of an impedance analyzer. Retrieved June 9, 2014, from https://decibel.ni.com/content/docs/DOC-18804

MICAz: Wireless Measure System. (n.d.). 6020-0060-04 Rev A.

Michahelles, F., & Schiele, B. (2005, July-September). Sensing and monitoring professional skiers. Pervasive Computing, 4(3), 40-46.

Miclea, L., Enyedi, S., Toderean, G., & Prinetto, P. (2004). Towards micro agent based DBIST/DBISR. International Test Conference 2004, (pp. 867 - 874).

Miclea, L., Szilárd, E., & Benso, A. (2002). Intelligent agents and BIST/BISR - Working together in distributed systems. Proceedings of ITC International Test Conference.

Microchip technology Inc. (2005). Analog sensor conditioning circuits. Microchip technology Inc.

Milor, L. S. (1998). A tutorial introduction to research on analog and mixed-signal circuit testing. IEEE Transaction on Circuits and Systems, 45(10), 1389-1407.

Mir, S., Lubaszeweki, M., Liberali, V., & Courtois, B. (1995). Built-in self-test approaches for analogue and mixed-signal integrated circuits. Proceedings, Proc. 38th Symp. on Circuits and Syst. (pp. 1145 - 1150). Rio de Janeiro: IEEE.

Mitchell, M. (2004, June). Choosing an Ultralow-Power MCU. Application Report.

Morris, D., Schazmann, B., Wu, Y., Coyle, S., Brady, S., Hayes, J., Diamond, D. (2008). Wearable sensors for monitoring sports performance and training. 5th International Summer School and Symposium on Medical Devices and Biosensors. IEEE Conferences.

Mundt, C., Montgomery, K., Udoh, U., & al., e. (2005, September). A multiparameter wearable physiologic monitoring system for space and terrestrial applications. IEEE Transactions on Information Technology in Biomedicine, 9(3), 382-391. DOI:10.1109/TITB.2005.854509.

NanoWatt XLP eXtreme Low Power MCUs. (2009, November).

NASA. (1975). SP-368 biomedical results of Apollo. Washington, USA: Scientific and Technical Information Office, National Aeronautics and Space Administration. Retrieved 01 16, 2014, from http://history.nasa.gov/SP-368/s6ch3.htm

National Semiconductor. (2004). Mixed signal testing using the IEEE 1149.4 STA400.

National Semiconductor. (2005, March). SCAN90CP02 Design for test features. Application Note 1313.

National Semiconductor. (2006, February). Leadless lead frame package (LLP) Application Note 1187.

National Semiconductor. (2008). LVDS owner's manual: Including high-speed CML and Signal Conditioning.

National Semiconductor. (2008, October 17). SCAN90004 4-channel LVDS buffer/repeater with pre-emphasis and IEEE 1149.6.

National Semiconductor. (2009, March 9). SCAN90CP02 1.5 Gbps 2x2 LVDS crosspoint switch with pre-emphasis and IEEE 1149.6.

Neuman, M. R. (1998). Biopotential electrodes. In Medical instrumentation - Application and design. John Wiley & Sons.

Niazmand, K., Tonn, K., Kalaras, K., Fietzek, U. M., Mehrkens, J. H., & Lueth, T. C. (2011). Quantitative evaluation of Parkinson's disease using sensor based smart glove. International Symposium on Computer-Based Medical Systems (CBMS), (pp. 1-8). DOI:10.1109/CBMS.2011.5999113

NXP. (2014, April 4). UM10204 I2C-bus specification and user manual version 6. NXP Semiconductor.

Ohletz, M. J. (1991). Hybrid built-in self-test for mixed analog/digital integrated circuits. Proceedings of European Test Conference, (pp. 307-316).

Orgis, G., Hreil, M., & Lukowicz, P. (2007). Using FSR based muscle activity monitoring to recognize manipulative arm gestures. International Symposium on Wearable Computer. IEEE. DOI:10.1109/ISWC.2007.4373776.

Overly, T. G. (2007). Development and integration of hardware and software for active-sensors in structural health monitoring. University of Cincinnati.

Pansiot, J., King, R. C., Mcllwraith, D. G., Lo, B., & Yang, G. Z. (2008). ClimBSN: climber performance monitoring with BSN. Proceedings of Symposium on Medical Devices and Biosensors (pp. 33-36). Hong Kong: IEEE. DOI:10.1109/ISSMDBS.2008.4575009.

Pansiot, J., Lo, B., & Yang, G. Z. (2010). Swimming stroke kinematic analysis with BSN, (pp. 153-158).

Pantelopoulus, A., & Bourbakis, N. G. (2010). A survey on wearable sensor-based systems for health monitoring and prognosis. IEEE transactions on systems, man, and cybernetics, 40(1), 1-12. DOI:10.1109/TSMCC.2009.2032660.

Paradiso, R., Longa, G., & Taccini, N. (2005). A wearable health care system based on knitted integrated sensors. IEEE Transactions on Information Technology in Biomedicine, 337-344. DOI:10.1109/TITB.2005.854512.

Parker, K. (1998). The boundary-scan handbook: Analog and digital (Vol. 2nd rev.). Kluwer Academic Press.

Patel, B. A., Anastassiou, C. A., & O'Hare, D. (2006). Biosensor Design and Interfacing. In G. Z. Yang (Ed.), Body Sensor Networks (pp. 41-82). London, UK: Springer.

Patel, S., Park, H., Bonato, P., Chan, L., & Rodgers, M. (2012, April 20). A review of wearable sensors and systems with application in rehabilitation. Journal Neuroengineering Rehabilitation, 9-21. DOI: 10.1186/1743-0003-9-2.

Peng, Y., Xia, Y., & Wang, S. (2009). Design of a high precision current source. The Ninth Int. Con. on Electronic Measurement & Instruments. IEEE Proceedings.

Pistoia, G. (2009). Baterry operated Devices and Systems. Amsterdam, Netherlands: Elsevier B.V.

Posse, K., Crouch, A., Rearick, J., Eklow, B., Laisne, M., Bennetts, B., Cote, J. F. (2006). IEEE P1687: Towards standardised access of embedded instrumentation. Proceedings of IEEE International Test Conference (p. 8). Santa Clara, CA: IEEE. DOI:10.1109/TEST.2006.297744.

Powell, H. C., Hanson, M. A., & Lach, J. (2007). A wearable inertial sensing technology for clinical assessment of tremor. Biomedical Circuit and Systems Conference BIOCAS 2007 (pp. 9-12). IEEE. DOI:10.1109/BIOCAS.2007.4463296.

Puurtinen, M. M., Komulainen, S. M., Kauppinen, P. K., Malmivuo, J. A., & Hyttinen, J. A. (2006). Measurement of noise and impedance of dry and wet textile electrodes, and textile electrodes with hydrogel. 28th International Conference of Engineering in Medicine and Biology Society (pp. 6012-6015). New York, USA: IEEE. DOI:10.1109/IEMBS.2006.260155.

Sutherland, S. Verilog HDL quick reference card. 2001. Retrieved in: http://www.sutherland-hdl.com/online_verilog_ref_guide/verilog_2001_ref_guide.pdf

Raeifi-Naein, M. (2008). Low-noise current excitation sub-system for medical EIT. Physiological Measurement, 29(1), 173-184.

Rahal, M., Khor, J. M., Demosthenous, A., Tozzard, A., & Bayford, R. (2009). A comparison study of electrodes for neonate electrical impedance tomography. Physiological Measurement, 30, s73-s84.

Rajsuman, R. (2000). Iddq Testing for CMOS VLSI. Proceedings of the IEEE, 544-568. DOI:10.1109/5.843000.

Rearick, J. (2006). What do embedded instruments look like? Agilent Technologies. Retrieved from http://grouper.ieee.org/groups/1687/instruments_sdd06.pdf

Rehman, A., Mustafa, M., Javaid, N., Qasim, U., & Khan, Z. A. (2012). Analytical survey of wearable sensors. Proceedings of International Conference on Broadband, wireless computing, communications and applications (BWCCA) (pp. 408-413). IEEE. DOI:10.1109/BWCCA.2012.73.

Righetti, X., & Thalmann, D. (2010). Proposition of a modular I2C-based wearable architecture. (pp. 802-805). IEEE Proceedings.

Roberts, G. (1996). Metrics, techniques and recent developments in mixed-signal testing. Proc. of the IEEE/ACM Int. Conf. on Computer Aided Design (pp. 1-8). San Jose, CA: IEEE.

Rocha, L., & Correia, J. (2006). Wearable sensor network for body kinematics monitoring. 10th IEEE International Symposium on Wearable Computers. IEEE Conferences.

Rogers, S. (2003). Sensor noise fault detection. Proceedings of American Control Conference. 5, pp. 4267-4268. IEEE. DOI:10.1109/ACC.2003.1240506.

Rosell, J., Colominas, J., Riu, P., Pallas-Areny, R., & Webster, J. G. (1988). Skin impedance from 1 Hz to 1MHz. IEEE Transactions on Biomedical Engineering, 649-651. DOI:0018-9294/88/0800-064.

Ross, A. S., Saulnier, G. J., Newell, J. C., & Isaacson, D. (2003). Current source design for electrical impedance tomography. Physiological Measurements, 21(2), 509. DOI:10.1088/0967-3334/24/2/361.

Salazar, A. J., & Bravo, R. J. (2006). Managing EMG signals for control strategies for a multi-functional interface for patients with severe motor disabilities. The International Special Topic Conference on Information Technology in Biomedicine. Ioannina, Greece.

Salazar, A. J., Bahubalindruno, G., Locharla, G. R., Mendonça, H. S., Alves, J. C., & Da Silva, J. M. (2011). A comparison of look-up table based sine wave generation implementations. Proceedings REC2011. Porto, Portugal.

Salazar, A. J., Bravo, R. J., & Ponticelli, D. (2005). Hybrid multi-source, multi-function patient adaptable system for assistive technology control applications. 3rd European Medical and Biological Engineering Conference. European Conference on Biomedical Engineering. Prague, Czech Republic: IFMBE Proceedings.

Salazar, A. J., Mendes, B., Machado, J., & Correia, M. (2014). Built-in self-testing methodology and infrastructure for an EMG monitoring sensor module. International Journal in Advances in Systems and Measurements, 7(1&2), 68-79.

Salazar, A. J., Silva, A., Silva, C., Borges, C. M., Correia, M. V., Santos, R. S., & Vilas-Boas, J. P. (2013, March). Low-cost wearable data acquisition for stroke rehabilitation: A proof

of concept study on accelerometry for functional task assessment. Topics in Stroke Rehabilitation.

San-Um, W. (2010). Developments of built-in self-test and calibration of analog mixed-signal LSI for catastrophic failures and parametric variations. Kochi University of Technology.

Schmid, T., Shea, R. S., Friedman, J., & Scrivastava, M. B. (2007). Movement analysis in Rock-climbers. International Conference in Information Processing in Sensor Networks. Cambridge, MA, USA: ACM.

Schmitt, O. H., & Almasi, J. J. (1970). Electrode impedance and voltage offset as they affect efficacy and accuracy of VCG and ECG measurements. International Vectorcardiography Symposium, (pp. 245-253).

Shaikh, Saghir A; (2004). IEEE Std. 1149.6 Implementation for a XAUI-to-Serial 10-Gbps Transceiver. ITC INTERNATIONAL TEST CONFERENCE (pp. 543-550). Charlotte, NC, USA: IEEE.

Sharma, A. B., Golubchik, L., & Govindan, R. (2010). Sensor faults: detection methods and prevalence in real-world datasets. ACM transactions on Sensor networks, 6(3), 1-34. DOI:10.1145/1754414.1754419

Silva, A. S., Salazar, A. J., Borges, C. M., & Correia, M. V. (2013). Wearable monitoring unit for swimming performance analysis. Biomedical Engineering Systems and Technologies, Communications in Computer and Information Science, 273, 80-93. DOI: 10.1007/978-3-642-29752-6_7

Silva, M., Caratino, A., Carvalho, H., Montagna, G., Monteiro, J., & Rocha, A. (2009). Study of vital sign monitoring with textile sensors in swimming pool environment. Proceedings of IEEE Industrial Electroncs Society Conference. Porto, Portugal.

Silva, M., Catarino, A., Carvalho, H., Rocha, A., Monteiro, J., & Montagna, G. (2009). Textile sensors for ECG adn respiratory frequency on swimsuits. Intelligent Textiles and Mass Customisation International Conference Proceedings, (pp. 301-310). Casablanca, Morocco.

Slamani, M., & Kaminska, B. (1993). T-BIST: a built-in self-test for analog circuits based on parameter translation. Proceedings of Asian Test Symposium, (pp. 172-177).

Slamani, M., Kaminska, B., Courtois, B., & Lubaszewski, M. (1995). Frequency-based BIST for analog circuit testing. Proc. VLSI Test Symp. (pp. 54-59).

Soma, M. (1995). Structure and concepts for current-based analog scan. Proceedings of CICC, (pp. 517-520).

Spach, M. S., Barr, R. C., Havstad, J. W., & Long, E. C. (1966). Skin-electrode impedance and its effect on recording cardiac potentials. Circulation, 34, 649-656. DOI:10.1161/01.CIR.34.4.649

Spinelli, E. M., Mayosky, M. A., & Pallas-Areny, R. (2006). A practical approach to electrode-skin impedance unbalance measurement. IEEE Transactions on Biomedical Engineering, 53(7), 1451-1453. DOI:10.1109/TBME.2006.875714

Strong, K., Mathers, C., & Bonita, R. (2007). Preventing stroke: saving lives around the world. Lancet Neurol., 6(2), 182-187.

Stroud, C. E. (2012). A designer's guide to built-in self-test. Kluwer Academic Publishers.

Sunter, S. (2004). Implementing and Using a Mixed-Signal Test Bus. Retrieved September 2013, 18, from IEEE 1149.4 Mixed-Signal Test Bus Working Group: http://grouper.ieee.org/groups/1149/4/Sunter_1149.4_Tutorial.pdf

Sunter, S. (2011, July 19). Essential principles for practical analog BIST. Retrieved September 15, 2013, from http://www.eetimes.com/document.asp?doc_id=1278936

Sunter, S., & Roy, A. (2011). A mixed-signal test bus and analog BIST with 'unlimited' time and voltage resolution. Procedings of 16th IEEE European Test Symposium (pp. 81-86). IEEE Computer Society.

Surapa, T., Benny, L., & Guang-Zhong, Y. (2005). Perspective in pervasive computing. IEE Proceedings of the Perspective in Pervasive Computing. IEE Conferences.

Swanson, D. K., & Webster, J. G. (1974). A model for skin-electrode impedance. In Biomedical electrode technology: theory and practice (pp. 117-128). Academic Press.

Tallgren, P., Vanhatalo, S., Kaila, K., & Voipio, J. (2005). Evaluation of commercially available electrodes and gels for recording of slow EEG potentials. Clinical Neurophysiology, 1(16), 799-806.

Technical Committee on Wearable Biomedical Sensors and Systems: Home. (2008). (Engineering in Medicine and Biology Society) Retrieved 08 30, 2013, from Technical Committee on Wearable Biomedical Sensors and Systems: http://tc-wearable-sensors.embs.org/index.html

Tekscan. (2014). FlexiForce Force Sensors. Retrieved July 5, 2014, from http://www.tekscan.com/flexible-force-sensors?utm_source=google&utm_medium=cpc&utm_term=force+sensitive+resistor&utm_content=ad2&utm_campaign=flexiforce&gclid=COnApazqrb8CFWjJtAodtQ0A4w

Tekscan. (2014, July 5). FLX-A301 force sensor, Rev. E_9.30.13. Retrieved July 5, 2014, from http://www.tekscan.com/pdf/FLX-A301-force-sensor.pdf

Telgenkamp, I. (2012). Testing the reliability of the WalkinSense: a system for plantar pressure measurements. Faculty of Health, Medicine and Life Sciences, Maastricht University.

TELOSB: TELOSB mote platform. (n.d.). 6020-0094-01 Rev B.

Tesconi, M., Tognetti, A., Pasquale Scilingo, E., Zupone, G., Carbonaro, N., De Rossi, D., Marella, M. (2007). Wearable sensorized system for analyzing the lower limb movement during rowing activity. IEEE International Symposium on Industrial Electronics. Vigo, Spain: IEEE.

Texas Instrument. (2007). Low power RF protocols - ZigBee- CC2420 - TI.com. (Texas Instruments) Retrieved 2010, from Analog, Embedded Processing, Semiconductor Company, Texas Instruments: http://focus.ti.com/docs/prod/folders/print/cc2420.html

Texas Instrument. (2007 Rev. 2008). I2C Bus Extender. Datasheet.

Texas Instrument. (2013). SNOS986D – LMH6622 Dual Wideband, Low Noise, 160MHz, Operational Amplifiers. Texas Instruments. Retrieved from http://www.ti.com.cn/cn/lit/ds/symlink/lmh6622.pdf

Texas Instrument Inc. (2005 Rev. 2008). 4-Channel I2C and SMBus multiplexer with interrupt logic.

Thankler, H. R., & Kanoun, O. (2001). Recent advances in sensor technology. Proceedings of IEEE Instrumentation and Measurement Technology Conference (IMTC) (pp. 309-316). Budapest, Turkey: IEEE. DOI:10.1109/IMTC.2001.928831.

Thiemjarus, S., Lo, B., & Yang, G. Z. (2005). Context aware sensing: what is the significance? Proceedings of the Perspective in Pervasive Computing. (pp. 163-170).

Tisdale, E. (1999). Measuring an Unknown, a laboratory problem for basic electronics. Journal of Industrial Technology, 16(1).

TOETS. (n.d.). Retrieved August 21, 2013, from TOETS: Towards One European Test Solution: http://www.lirmm.fr/w3mic/TOETS/

Tollefson, J., Voroniouk, M., & Jakubiak, A. (2011, 09 20). Designing smarter: single battery applications. Retrieved 09 28, 2011, from EEtimes: www.eetimes.com

Tommorrow Options Microelectronics. (2010). Walkinsense. (Tomorrow Options Microelectronics) Retrieved July 6, 2011, from www.tomorrow-options.com/pt/products

Tomorrow Options. (2012). WalkinSense: features. Retrieved September 3, 2013, from http://www.tomorrow-options.com/walkinsense_features/

Tränkler, H.-R., & Kanoun, O. (2001). Recent advances in sensor technology. Proceedings of IEEE Instrumentation and Measurement Technology Conference, (p. 8). Budapest, Hungary.

Tufail, F., & Islam, M. H. (2009). Wearable wireless body area networks. International conference on Information management and engineering (ICIME) (pp. 656-660). IEEE. DOI:10.1109/ICIME.2009.142

Turcato, A., & Ramat, S. (2011). A computational framework for the standardization of motion analysis exploiting wearable interial sensors. IEEE Engineering in Medicine and Biology Society Conference (EMBC) (pp. 4963-4966). IEEE. DOI:10.1109/IEMBS.2011.6091230

Van Laerhoven, K., Lo, B., Ng, J., Thiemjarus, S., King, R., Kwn, S., Yang, G. Z. (2004). Medical healthcare monitoring with wearable and implantable sensors. Proc. of the 3rd International Workshop on Ubiquitous Computing for Healthcare Applications.

Vauhkonen, P. J., Vauhkonen, M., Savolainen, T., & Kaipio, J. P. (1999). Three-Dimensional electrical impedance tomography based on the complete electrode model. IEEE Transactions on Biomedical Engineering, 46(9).

Venkatasubramanian, K., & Gupta, S. K. (2008). Ayushman: a secure, usable pervasive health monitoring system. Proceedings of the 2nd International Workshop on Systems and Networking Support for Health Care and Assisted Living Environments (pp. 12:1--12:3). ACM. DOI:10.1145/1515747.1515763.

Virk, M. H. (2013). Design and implementation of a multi-purpose wireless body area network. University of OULU.

Vuorela, T., Vanhala, J., Seppa, V., & Hyttinen, J. (2008). Two portable long-term measurement devices for ECG and bioimpedance. 2nd Int. Conf. PervasiveHealth. IEEE Proceedings.

Waller, R. (n.d.). Scanning Solutions: Embedded instrumentation illuminates the future of validation and test. Retrieved 02 07, 2014, from http://fplreflib.findlay.co.uk/articles/29543/P29-30.pdf

Wang, L. T., Wu, C. W., & Wen, X. (2006). VLSI Test principles and architectures: design for testability. (pp. 619-678). Elsevier.

Wang, Y.-s., Wang, J.-x., Lai, F.-c., & Ye, Y.-z. (2005). Optimal schemes for ADC BIST based on histogram. Proceedings of the 14th Asian Test Symposium (ATS '05).

Warneke, B., Atwood, B., & Pister, K. S. (2001). Smart dust mote forerunners. 14th IEEE International Conference on Micro Electro Mechanical Systems (pp. 357-360). Interlaken, Switzerland: IEEE. DOI:10.1109/MEMSYS.2001.906552

Warneke, B., Last, M., Liebowitz, B., & Pister, K. (2001). Smart Dust: communicating with a cubic-millimeter computer. Computer, 34(1), 44-51. DOI:10.1109/2.895117

Warriach, E. U., Tei, K., Nguyen, T. A., & Aiello, M. (2012). Fault detection in wireless sensor networks: a hybrid approach. Proceedings of IPSN, (pp. 87-88).

Webster, J. (Ed.). (2009). Medical instrumentation: Application and Design (4th Ed.). Wiley and Sons.

Welch, J., Guilak, F., & Baker, S. D. (2004). A wireless ECG smart sensor for broad application in life threatening event detection. Proc. 26th IEEE EMBS, (pp. 3447-3449).

Wenzel, T., & Ehrenberg, H. (2012). Embedded system access (ESA): changing the paradigm of electrical test. White paper. Retrieved 08 15, 2013, from http://files.iccmedia.com/pdf/goepel130204.pdf

Wey, C. L. (1990). Built-in self-test (BIST) structure for analog circuit fault. IEEE Transaction on Instrumentation Measurement, 517-521.

Wey, C. L., & Krishnan, S. (1992). Built-in self-test (BIST) structure for analog circuit fault diagnosis with current test data. IEEE Transaction on Instrumentation Measurements, 41(4), 535-539. DOI:10.1109/19.155921

Wiese, S. R., Anheier, P., Connemara, R. D., Mollner, A. T., Neils, T. F., Kahn, J. A., & Webster, J. G. (2005). Electrocardiographic motion artefact versus electrode impedance. IEEE Transaction in Biomedical Engineering, 52(1), 136-139.

Williams, T. W., & Parker, K. P. (1983). Design for testability - A survey. Proceedings of the IEEE (pp. 97-112). IEEE. DOI:10.1109/PROC.1983.12531

XILINX. (n.d.). Retrieved 6/26/2009, from Design performance and runtime strategies for FPGAs : http://www.xilinx.com/itp/xilinx9/help/iseguide/html/ise_imp_strategies.htm

XILINX. (2005). Using block RAM in Spartan-3 generation FPGAs. Application Note: Spartan-3 FPGA Family.

XILINX. (2006). Spartan-3E starter kit board user guide.

XILINX. (2008). Spartan-3 FPGA family data sheet. Product Specification.

XILINX. (2008). Spartan-3E FPGA family: Complete data sheet. Product Specification.

XILINX. (2009). ChipScope Pro 11.1 software and cores user guide.

Xilinx Inc. (2010). Power solutions: Information and tools for conquering the key challenges of power consumption. (Xilinx Inc.) Retrieved 2010, from FPGA solutions from Xilinx, Inc.: http://www.xilinx.com/products/design_resources/power_central/

Xing, Y., & Fang, L. (2010). Design-for-test of digitally-assisted analog IPs for automotive SoCs. Proceedings of IEEE Asian Test Symposium (pp. 185-191). IEEE.

Yang, G. Z., & Hu, X. (2006). Multi-sensor fusion. In G. Z. Yang (Ed.), Body sensor networks (pp. 239-302). Springer.

Yang, G. Z., Lo, B., & Thiemjarus, S. (2006). Autonomic Sensing. In Body sensor networks (pp. 333-366). London, UK: Springer.

Yang, G.-Z. (Ed.). (2006). Body sensor networks. Springer.

Yang, G.-Z. (2008). Sports body sensor networks. International Summer School and Symposium on Medical Devices and Biosensors. Hong Kong: IEEE.

Yang, G.-Z., Lo, B., & Thiemjarus, S. (2006). Autonomic sensing. In G.-Z. Yang (Ed.), Body Sensor Networks. Springer-Verlag.

Yang, L., & Shouqian, S. (2006). Smart sport underwear design. 7th International Conference on Computer-Aided Industrial Design and Conceptual Design. Hangzhou, China: IEEE.

Yi-Zhi, W., Jia-Xin, S., Long-Fei, L., Yong-Sheng, D., & Hong-An, X. (2010). Performance evaluation of a novel cloth electrode. 4th Int. Conf. on Bioinformatics and Biomedical Eng. (pp. 1-5). IEEE Proceedings.

Yuan, J. (2012). Built-in self-test techniques for data converter in analog and mixed-signal circuits. Kochi University of Technology.

Yunfei, H. (2009). Development of a bioimpedance based human machine interface. Prince of Songkla University, Electrical Engineering Department.

Zambrano, A., Derogarian, F., Dias, R., Abreu, M. J., Catarino, A., Rocha, A. M., da Silva, J. M., Canas, J. F., Tavares, J. G., Correia, M. V. (2012). A wearable sensor network for human locomotion data capture. Studies in Health Technology and Informatics, 177 (pp. 216-223).

Zepeda-Carapia, I., Márquez-Espinoza, A., & Alvarado-Serrano, C. (2005). Measurement of skin-electrode impedance for a 12-lead electrocardiogram. 2nd Int. Conf. on Elec. and Electr. Eng,. IEEE Proceedings.

Zephyr Technology Corporation. (2012). Bioharness 3: wireless professional heart monitor and physiological monitor with bluetooth. Retrieved September 3, 2013, from http://www.zephyranywhere.com/products/bioharness-3/

Zivkovic, V., van der Heyden, F., Gronthoud, G., & de Jong, F. (2008). Analog test bus infrastructure for FR/AMS modules in core-based design. Proc. of European Test Symp. (pp. 27-32).