Bachelor final project

MICROCHANNEL FABRICATION

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ABSTRACT

In this project, we have studied a new microchannel fabrication based on the idea of the transference of a thin layer of Si_3N_4 onto a full of string chip, also made of Si_3N_4.

In order to do so, we have created two different wafers. The first of them was a silicon wafer with channels. We have covered this wafer of Si_3N_4 and cut it into chips. The other one was a Si wafer covered with Si_3N_4 in one of its sides. We have diced it until it was a thin layer and cut it into chips. Both processes have been carried out at a clean room.

The next steps have taken place in a laboratory. In this environment, we have etched the Si from the Si_3N_4 wafer until we had a thin layer of Si_3N_4 and transfer this layer on the top of the channel chips.

After analyzing the complete microchannel chips with the microscope, we have concluded that this process can be a good alternative of fabrication.

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INTRODUCTION

This project presents a fabrication system of microchannels. The development of microfluidic technology and the increasing of their applications have augmented the need of developing new fabrication methods faster and cheaper than traditional ones.

Microchannels are defined as flow passages that have hydraulic diameters in the range of 1 to 100 micrometres [1] or from 10 until 200 micrometres [2]. They are basic components in many silicon related technologies. They have a lot of importance in some ambits as physics, chemistry, biologics and medicine. They are the main part of MEMS devices [3] [4].

The classical fabrication of microchannel chips is a complex process based on the idea of a sacrificed layer (typically made with polysilicon) that must be etched. This process is not optimal. First of all, using a material as a support and then deleting it costs an amount of money that could be avoided. On the other hand, the etching of this layer often takes more than 24 hours. During this etching, several parts of the chip can be damaged. [5][6]

We have done a research based on the idea of improving this fabrication system, deleting the sacrificed layer and following a faster and easier procedure.

The method that we present is the transference of a silicon nitride lid on the top of a silicon chip. Both two parts concern basic fabrication methods as lithography, spin coating, etching and dicing.

To do this investigation, we have tried different procedures for each part of the process and then they have been analyzed and compared. According to the results, we have found new processes to improve them.

FABRICATION: CLEAN ROOM

The process of fabrication for each wafer has been completely different so we will explain them separately. The detail of every step and the recipes of the process flow are in the Appendix 1 and 2.

CHIPS WITH CHANNELS

This correspond to the chips covered with channels.

PATTERN

We have designed a basic pattern to test the effectivity of the process, this design is represented in Figure 1 [7].

As we can see, we have channels of different sizes from $2\ \mu m$ to $100\ \mu m$.

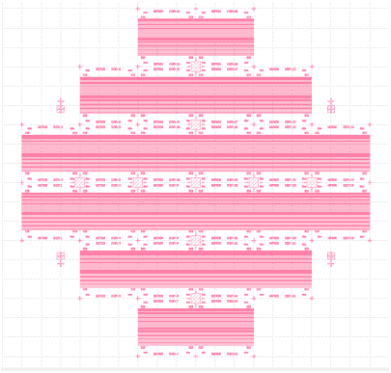


Figure 1: Pattern designed by Tom Larsen.

PROCESS FLOW

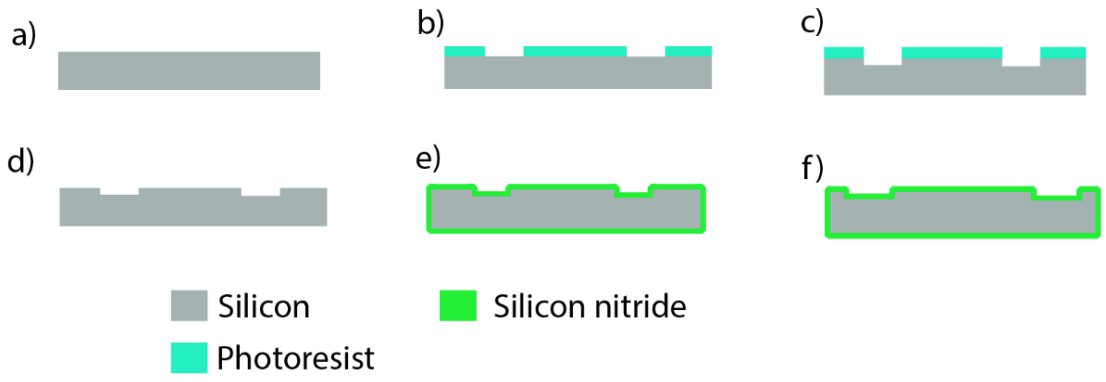


Figure 2: a) Original silicon wafer, b) wafer with a photoresist pattern layer after photolithography, c) wafer after etching 10 or 30 μm, d) wafer after cleaning the photoresist, e) wafer with silicon nitride in both sides, f) chips of silicon and cover by silicon nitride.

As illustrated in the figure, the fabrication starts with two 525 µm silicon wafers, single side polished. This wafer is spin coated with 2 µm photoresist layer (Bis(trimethylsilyl)amine) with the machine

ACS200. To finish the photolithography process, they have been exposed and the photoresist have been eliminated according to the design. For this process, we used the machine MLA150.

The next step has been a deep reactive-ion etching (DRIE). In this procedure, the parts that have not been covered with the photoresist have been etched. The etching has been different for each wafer. The wafer 39 has been etched approximately 30 µm and the wafer 40 has been etched 10 µm. The etching has not been very precise due to the different width in the pattern. Regions with bigger channels have been more exposed to reactive-ion than regions with smaller ones.

After etching, we have cleaned the silicon wafer of photoresist using the machine TEPLA, which is a plasma stripper, and the machine UFT remover, which is a photoresist remover.

Then, we have covered these wafers with silicon nitride with a low pressure chemical vapor deposition. The slide of silicon nitride has a thickness of 100 nm.

Finally, the wafers have been cut into 10x10 mm chips. To do so, we have used a protection of 5 µm of photoresist (same photoresist as before: Bis(trimethylsilyl)amine) with the machine ACS200. After the dicing with the machine Disco, we have cleaned all the rest of photoresist of the wafer (machine UFT remover).

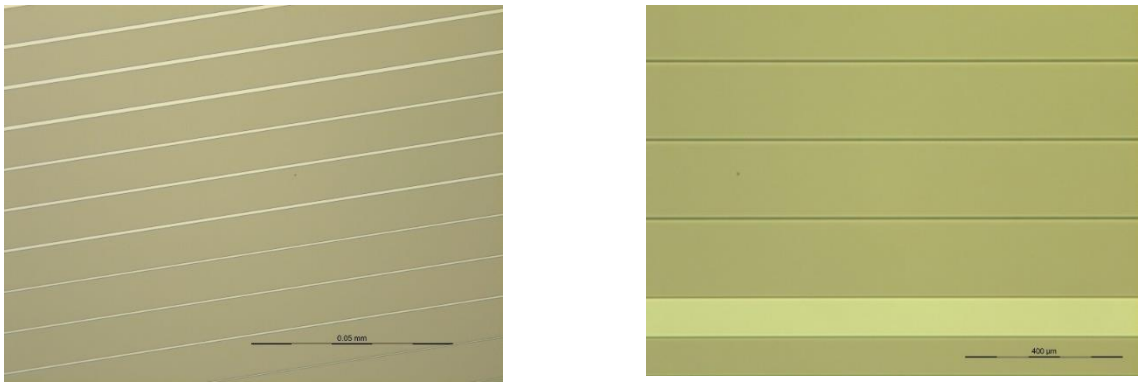


Figure 3: Detail of the channels chips. Left image represents the wafer 40 and it has been taken with a Nikon 5x lens. Right picture is the wafer 39, taken with Nikon 10x lens.

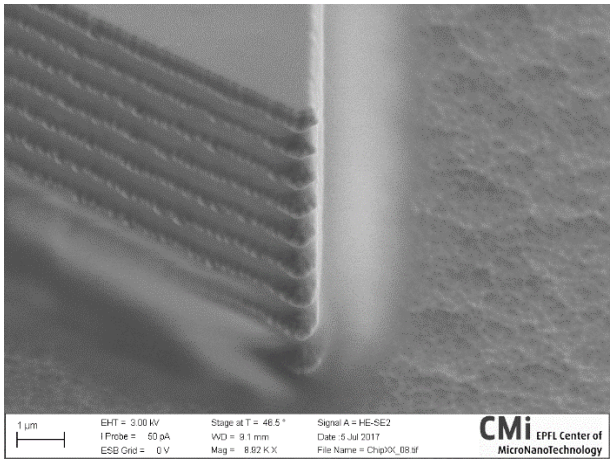


Figure 4: Detail of the deep reactive-ion etching (DRIE). In the picture, we can see the undulating sidewall of the silicon structure.

PROCESSFLOW

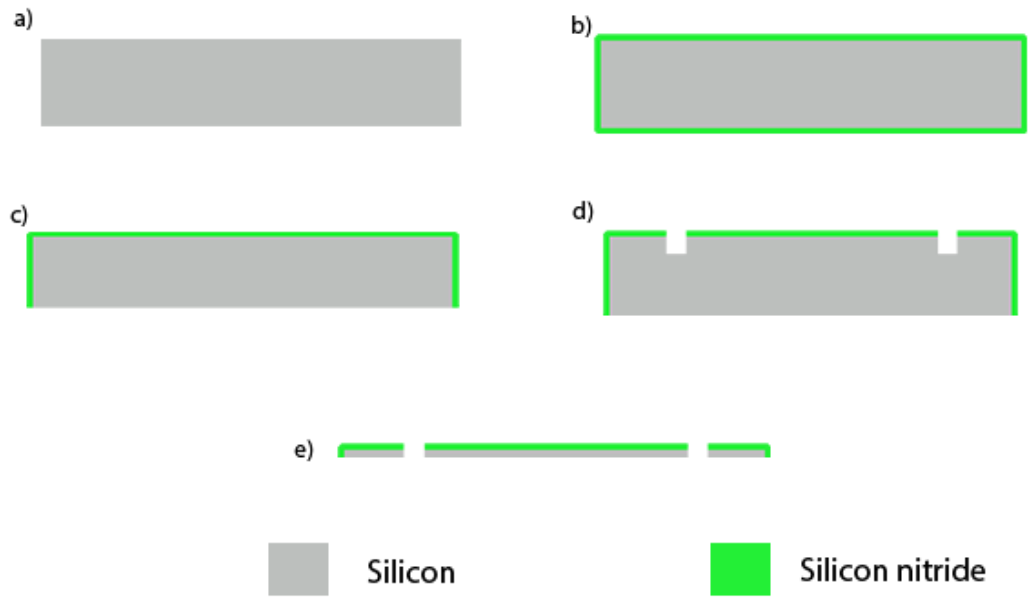
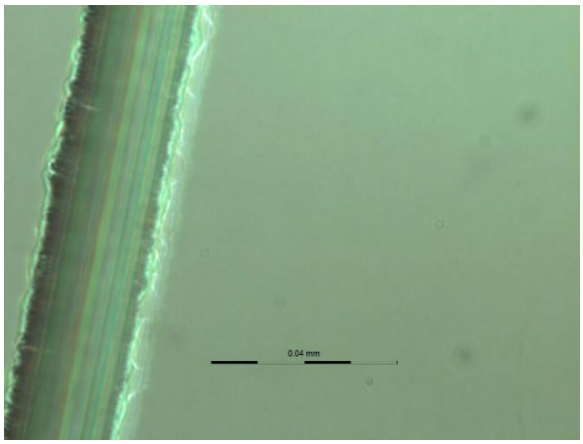


Figure 5: a) Original silicon wafer, b) wafer cover with silicon nitride in both sides, c) wafer after cleaning back side of silicon nitride (etching) d) wafer diced before grinding e) wafer grinded.

As illustrated in the figure, we have taken a 525 µm silicon wafer single side polished, as in the previous process. Using the machine LPCVD Nitride we have covered it with 100 nm of silicon nitride. After that, the silicon nitride of the backside has been etched using the plasma etching machine SPTS APS.

Then, the wafer was subjected to a dicing before a grinding process. The chips size has been 10x10 mm and the dicing has been about 150 µm depth. As in the silicon nitride channel chips, we have used the machine Disco.

Finally, the silicon part of the wafer has been grinded until a final thickness of 50µm. As result, we had 49,9 µm silicon chips covered with 100 nm silicon nitride.



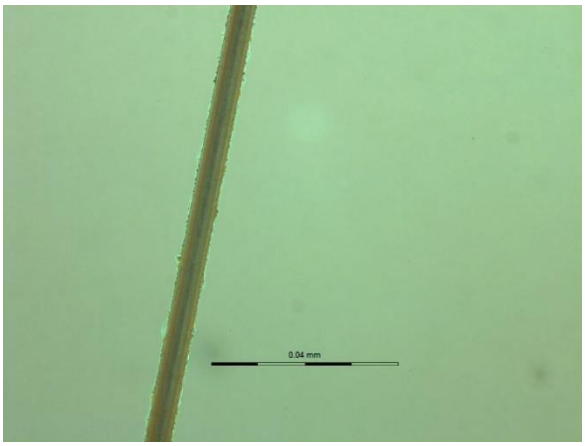
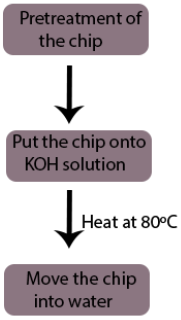


Figure 6: Detail of the wafer results after dicing.

FABRICATION: LABORATORY

SILICON NITRIDE LIDS: ETCHING



This process has been characterized by three main steps. The first of them is a pretreatment of the chip, which has differed from one test to other, then we have the real etching process and finally a change of the chip into water.

The etching of silicon can be done with a KOH solution. Comparing different KOH solutions and the etching speed of each one, we have considered that this process would be done with 25% KOH solution at 80 ºC [8].

FIRST TRY

Figure 7: Chips prepared in KOH solution to be etched. Hot plate temperature 80ºC.

As we can see in the figure, at the first attempt we have tried to etch the silicon just adding it to the top of the solution.

As the density is very small because of the size of the chip, we thought that it would not be necessary to use an extra element to assure the floating.

However, after a few hours, the chip was sunk. The silicon nitride lid was impossible to fish.

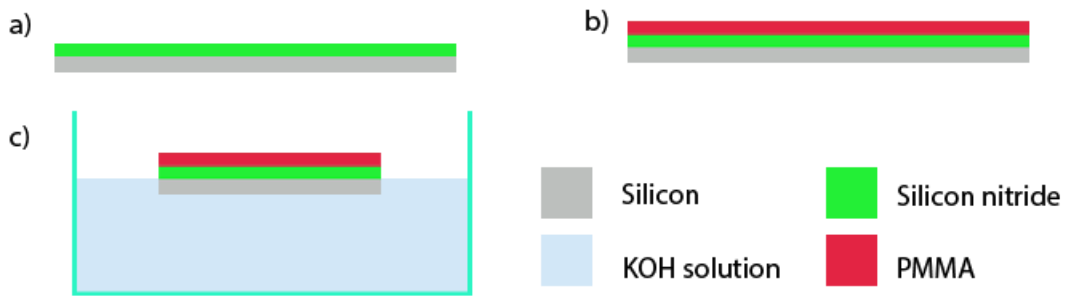


Figure 8: Pretreatment of chips in the second try. We have spin coated 300 nm of PMMA on the top of the silicon nitride.

In the second try, we have put approximately 300 nm of PMMA on the top of the silicon nitride as protective coating and to make it float.

The problem was that the film of PMMA and silicon nitride supported too much stress during the etching.

The result is a deformation of the lid.

Figure 9: Result of the etching with PMMA on the top. We can see that the structure is not flat, there is a deformation.

THIRD TRY

We have added 300 nm of PMMA and on the top a block of PDMS to protect the chip from the stress. The result was that the union of silicon nitride and PMMA got separated of the PDMS during the etching.

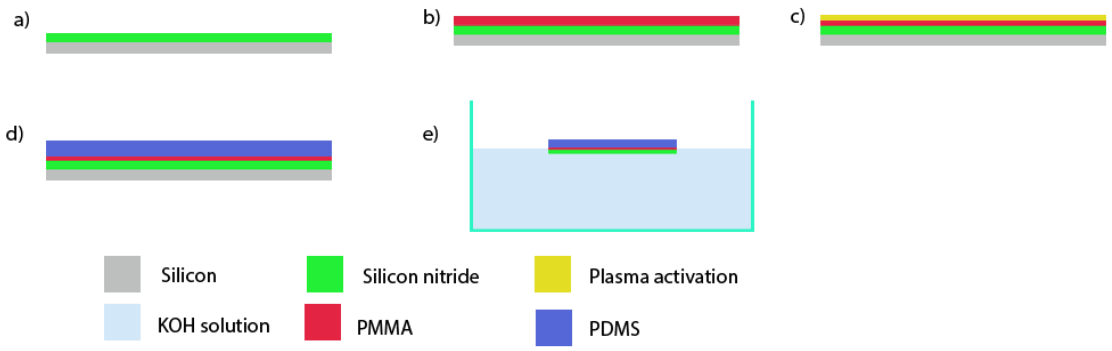


Figure 10: Detail of the process a) Chip with silicon nitride on the top, b) spin coating of 300 nm of PMMA, c) plasma activation at 100W for 0.1s, d) adding the PDMS, e) etching

FOURTH TRY

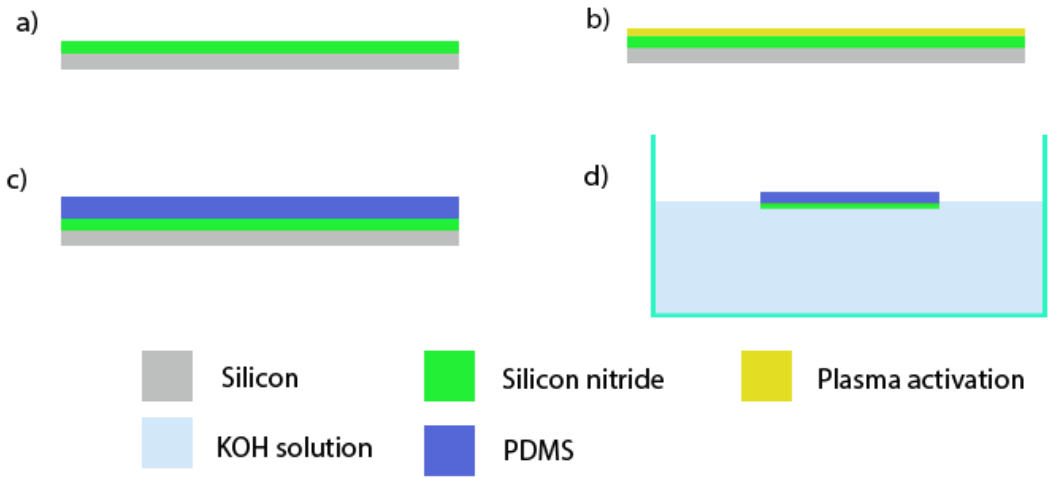


Figure 11: Detail of the process a) Chip with silicon nitride on the top b) Plasma activation at 100W for 0.1s c) Adding the PDMS, e) etching

As we saw that the block of PDMS and PMMA did not work, we tried to omit the PMMA. We put directly the PDMS on the top of the silicon nitride.

After the etching, the silicon nitride was delaminated from PDMS.

FIFTH TRY

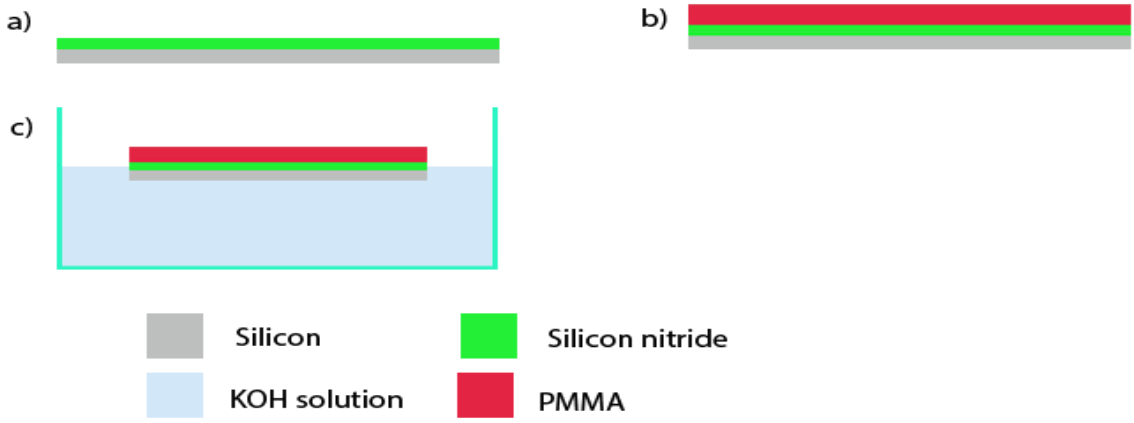


Figure 12: Detail of the process a) silicon nitride chip, b) spin coating of PMMA 1.5 µm, c) etching

In this case, we increased the amount of PMMA till 1.75 µm. The result was acceptable, the silicon nitride floated and it was slightly deformed but the fishing was difficult.

SIXTH TRY

Figure 13: Detail of the process a) Silicon nitride chip b) spin coating of PMMA 1.5 µm, c) plasma activation at 100 W for 0.1 s, d) adding of PDMS, e) etching

We have spin coated approximately 1.5 µm of PMMA on the top. We have done a O_2 treatment of PDMS block to assure the permanence of the PMMA and the PDMA together during the etching. We found out that it is difficult to separate both blocks after the transference.

We have done the same as sixth try but we have cut the PDMS in the center as the right-side pattern. As we can see in the pictures, we have eliminated the tension and the part that is not covered with PMMA can be transferred without problems.

This idea has been inspired in some transferring methods of graphene [5].

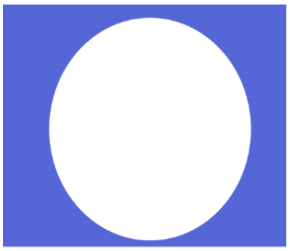


Figure 14: PDMS pattern

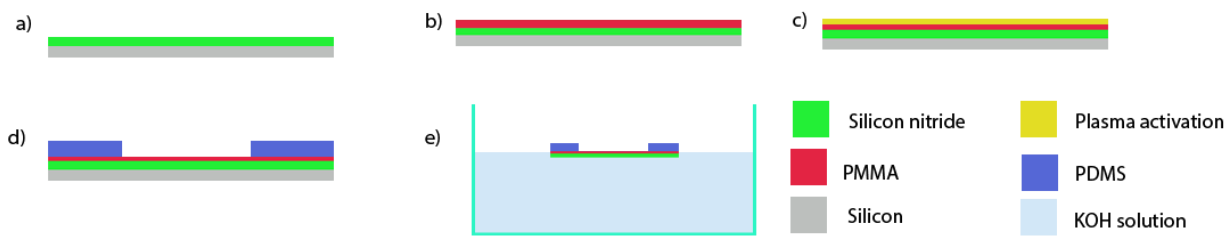


Figure 15: All the steps detailed of the two channel wafers from left to right. a) Original silicon nitrate chip, b) silicon nitrate chip covered with PMMA on the top side, c) plasma activation, d) chip with PDMS on the top, d) chip etched.

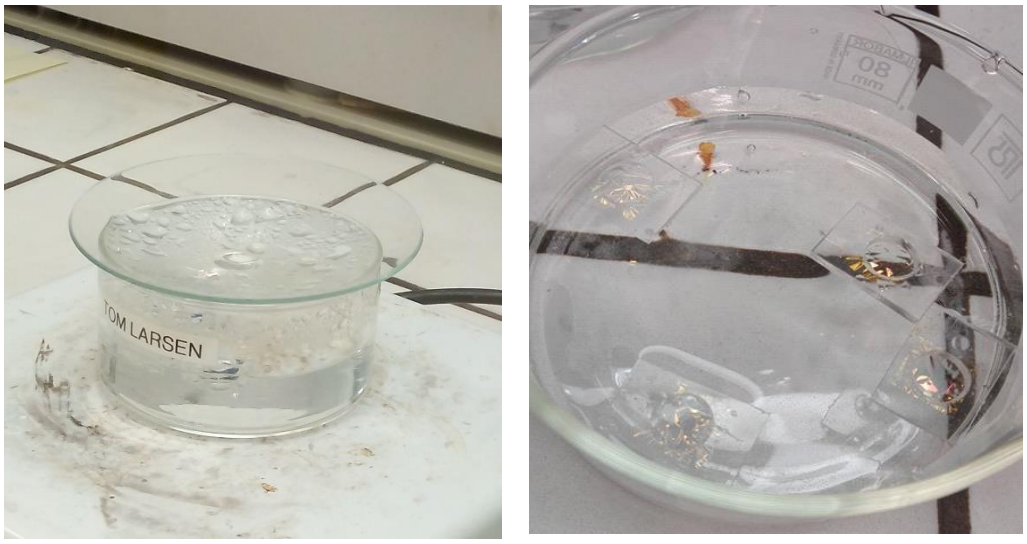


Figure 16: The picture of the left side represents the etching process. The chips are on KOH solution, the temperature is 80ºC and we can see the formation of some bubbles around the silicon. At the picture on the right we have the result, the chips are on water.

TRANSFERENCE

In the transference of the silicon nitride lid on the top of the channel chip, we have made several checks as well. These tests have been differentiated first by the pretreatment of the chip and then by the temperature used. In all cases we did a cleaning in acetone of the trench chips before the transference to avoid dust and a cleaning again after the deposition, in acetone and in ISA.

All these tests used the PDMS with hole-PMMA-silicon nitride-block.

DRY TRANSFERENCE

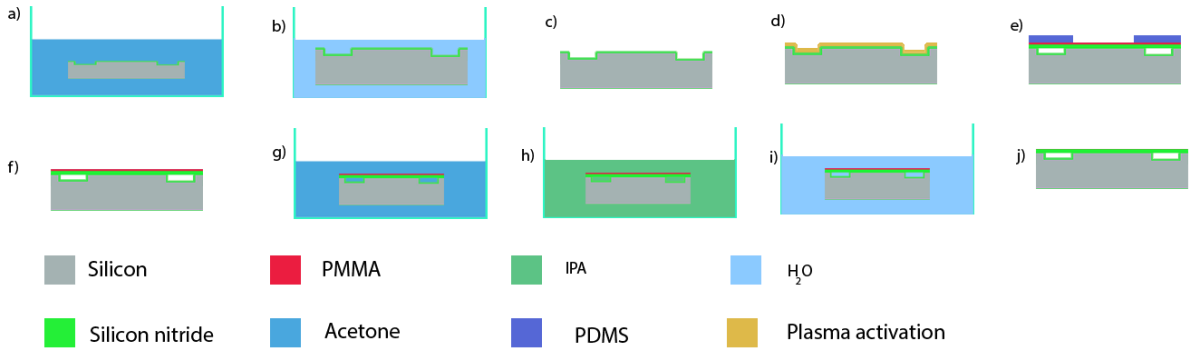
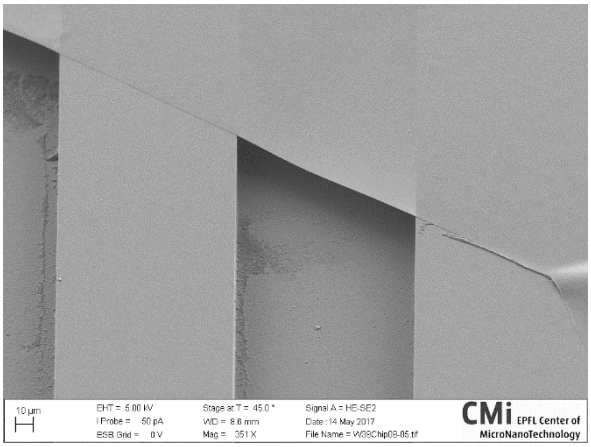


Figure 17: a) Channel chips cleaning in acetone, b) channels chips in water, c) drying of the chip, d) plasma activation of the surface at 100W for 1 minute, e) transferring of the silicon nitride block at 150º C, f) elimination of the PDMS, g) cleaning in acetone to dissolve the PMMA, h) cleaning in IPA, i) moving to water, j) final chip.

This trial has been characterized by the transference of the silicon film onto the chip after drying both parts and applying a plasma activation.

We have applied an O_2 treatment to the channel chips and then put on the top of them the silicon nitride block. After that, the PDMS was taken out and, after the submersion of the chip in acetone to delete the PMMA, we obtained the final chip.



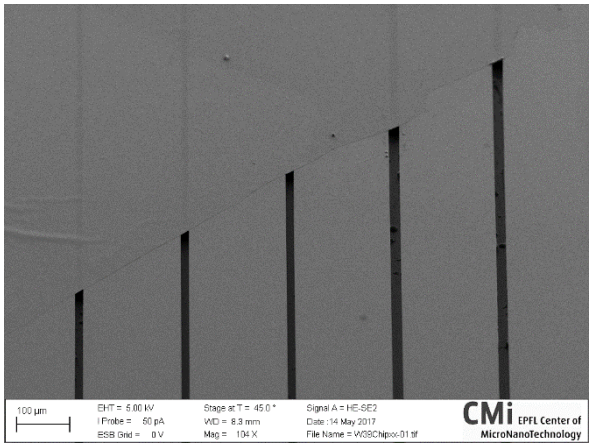


Figure 18: Results of the chip fabrication shown with an electron microscope. We can see in both images that there are some folds on the longer width trenches. The silicon nitride lid is also cracked in some parts.

WET TRANSFERENCE

We have tried to improve the results obtained in the dry transference by doing it with wet chips. The process will mainly follow the same steps but the transfer temperatures have changed in each of them. This process is similar to the dry transfer but we have deleted the plasma activation and the chips are wet when we start the transference.

FIRST TRY

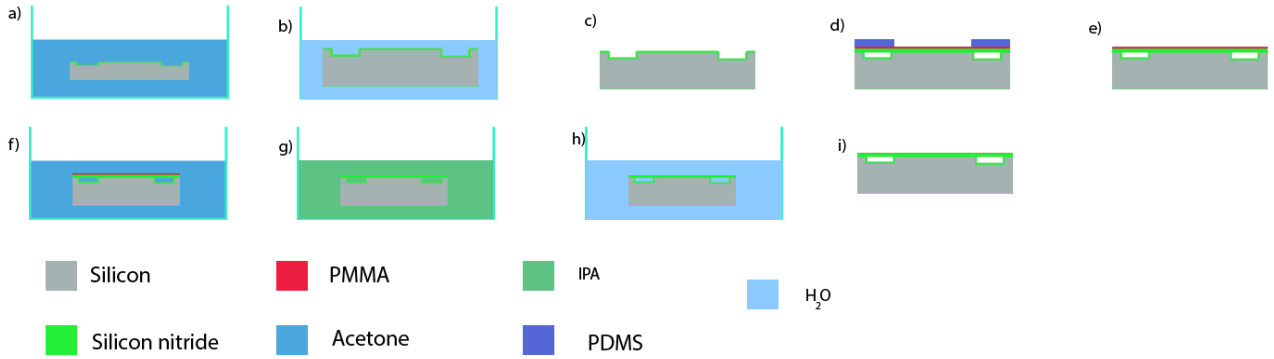


Figure 19: From left to right we have the following steps a) channel chips cleaning in acetone, b) chips in water, c) cleaned chip, c) transferring the silicon nitride block at 60º C to dry and changing the temperature to 150º C to do the deposition, d) cleaning in acetone to dissolve the PMMA and lift-off the PDMS, h) cleaning in IPA, e) resulting chip.

We have done the transference on a hot plate at 60ºC. The temperature has been maintained until water evaporation and then, it was heated at 150ºC i.e. deposition temperature of silicon nitride.

To eliminate the PMMA and the PDMS in this case we have taken out the PDMS before introducing the chip into acetone. After the cleaning process with the acetone (removal of PMMA) and IPA, the chips have been changed to water and heated at 60º to evaporate the rest of water. The elimination of the PDMS block before introducing it in acetone has damaged the silicon nitride surface.

SECOND TRY

This process has been performed at the same temperatures as the previous one.

The complete block has been introduced into acetone. The PDMS have been rubbed out subsequently of the PMMA dissolution. The chips have been moved into water and heated at 60º C to be dried again.

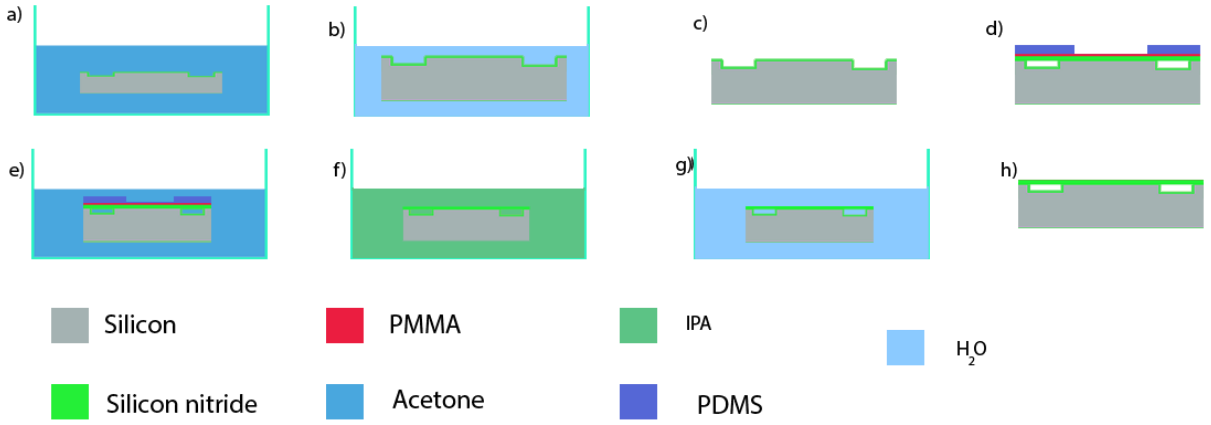


Figure 20: From the left to the right we have a) cleaning in acetone of the chip, b) moving to water, c) channel chips, d) transference of the lid at 60º C to dry, change to 150º to do the transference, e) moving of the complete block into acetone, f) moving of the final chip into IPA to finish the cleaning, g) changing to water, h) final chip.

We have obtained the following results:

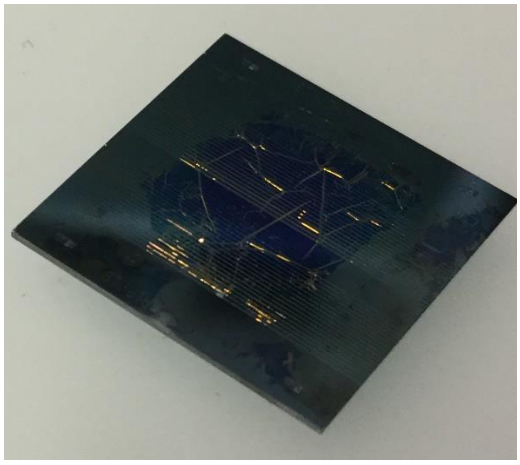


Figure 21: Pictures of the resulting transference. We can see the existence of some folds (gold lines) and some scratched parts that have not been covered with silicon nitride.

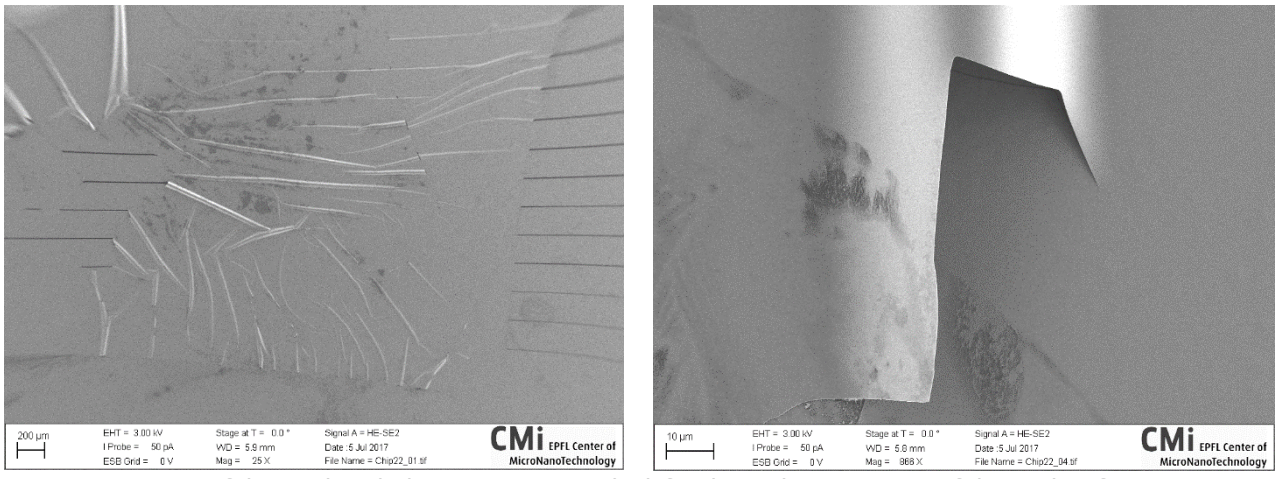


Figure 22: Pictures of the result with the microscope. At the left side, we have a picture of the total surface. We can see the existence of big flat parts but many long folds too. At the right side, a picture of a detail of one of the folds. We can see in both pictures that the silicon nitride layer is resistant - there are only some parts fractured and a lot of folds.

THIRD TRY

In this case, we have repeated the process already explained in the second try but doing the transference in the inverse position, PDMS-PMMA-silicon nitride structure on the button and then the trenches wafer on the top.

Using this process, we wanted to improve the lid and create bigger flat parts, assuming that one of the main reasons of the folds could be the weight of the water before the evaporation.

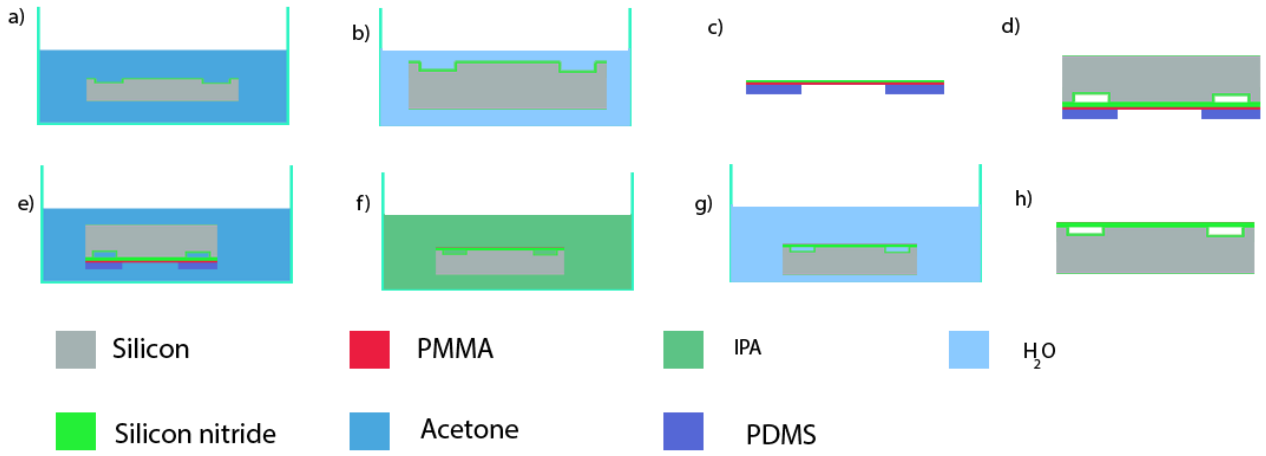


Figure 23: From the left to the right we have a) cleaning in acetone of the chip, b) moving to water, c) silicon nitride block, d) transference, heating of the block at 60ºC and, after the evaporation of the surface, increasing the temperature until 150ºC, e) moving the complete block into acetone, f) moving the final chip into IPA, g) changing to water, h) final chip.

We have obtained the following results:

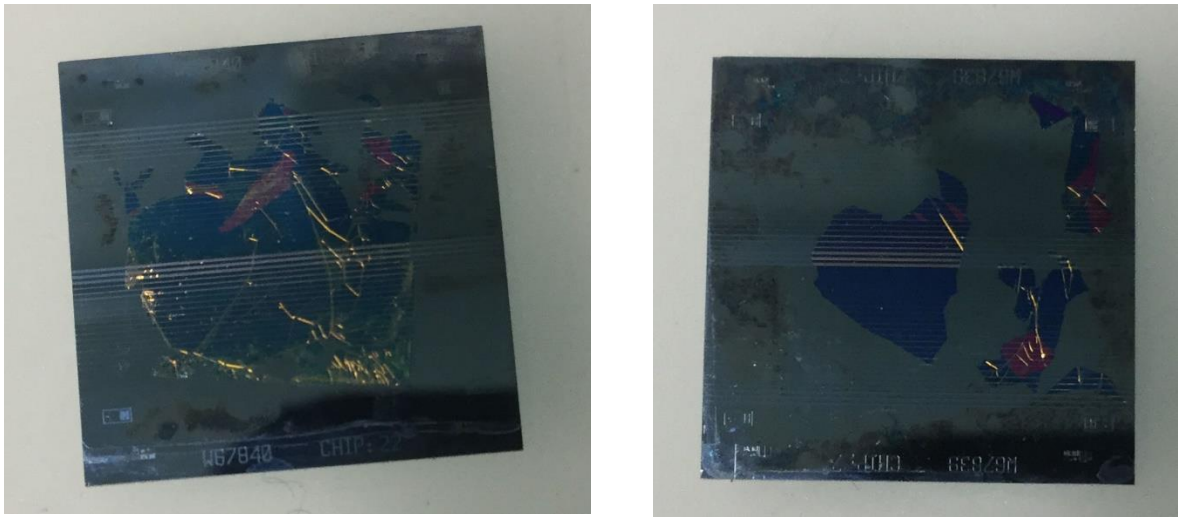


Figure 24: Pictures of the backside transference result. At left side, we have a chip with less folds than the second try. At the right side, we have a test without folds and bigger flat parts (the microscope images demonstrated that this test was not so efficient).

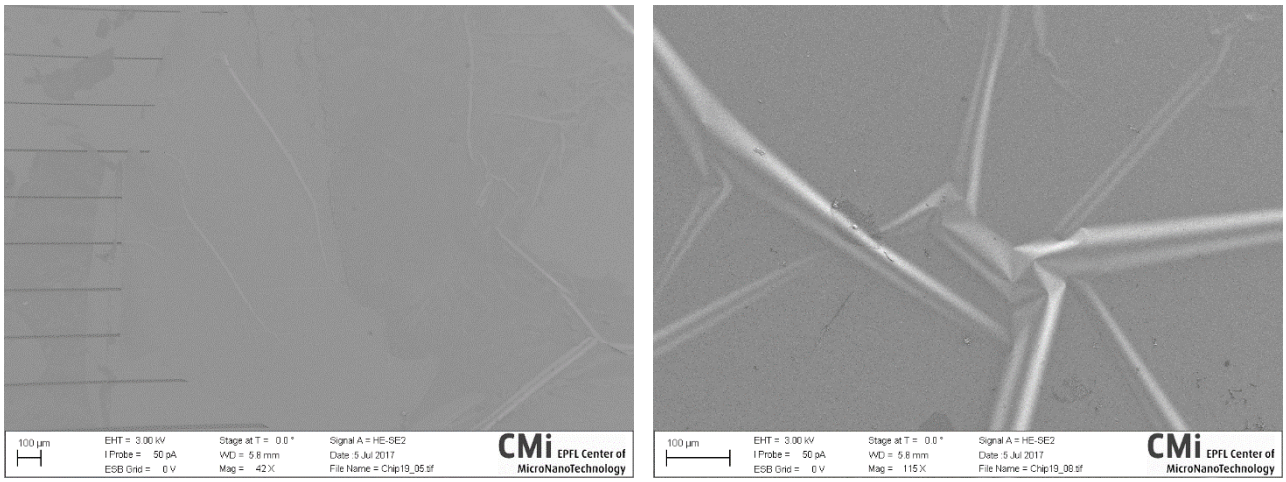


Figure 25: Pictures from electron microscope correspond with left chip of figure 24. At the left side, we can see a big flat part. At the left side, we have a detail of the union of some folds, demonstrating the strength and quality of the silicon nitride lid.

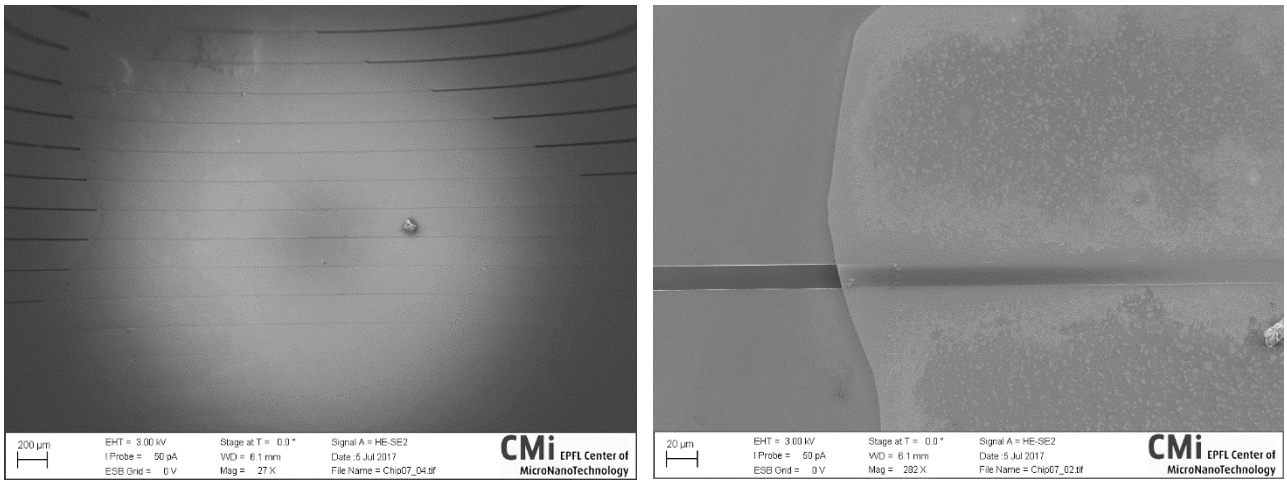


Figure 26: Pictures from electron microscope, chip at the right-side in figure 22. At the left, this picture shows a big flat layer without folds, the detail of the picture (right side) shows the existence of water behind the silicon nitride layer.

FOURTH TRY

After an investigation about this subject, we have found the following document [8].

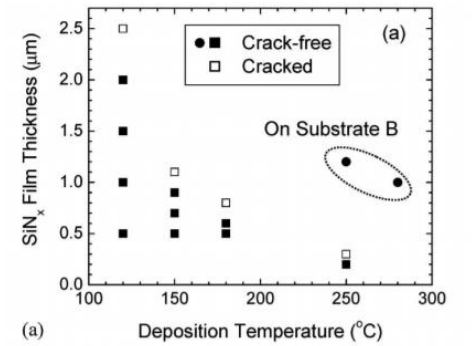


Figure 27: Deposition temperature dependence of thickness. [8]

According to our film thickness, the deposition temperature should be around 300º C to have a flawless behavior.

We have tried to heat the transistor to 60º for the water evaporation and then 300º for the deposition. This test has been done using the normal and the backside transference.

We have found that a part of the chip was damaged and burned.

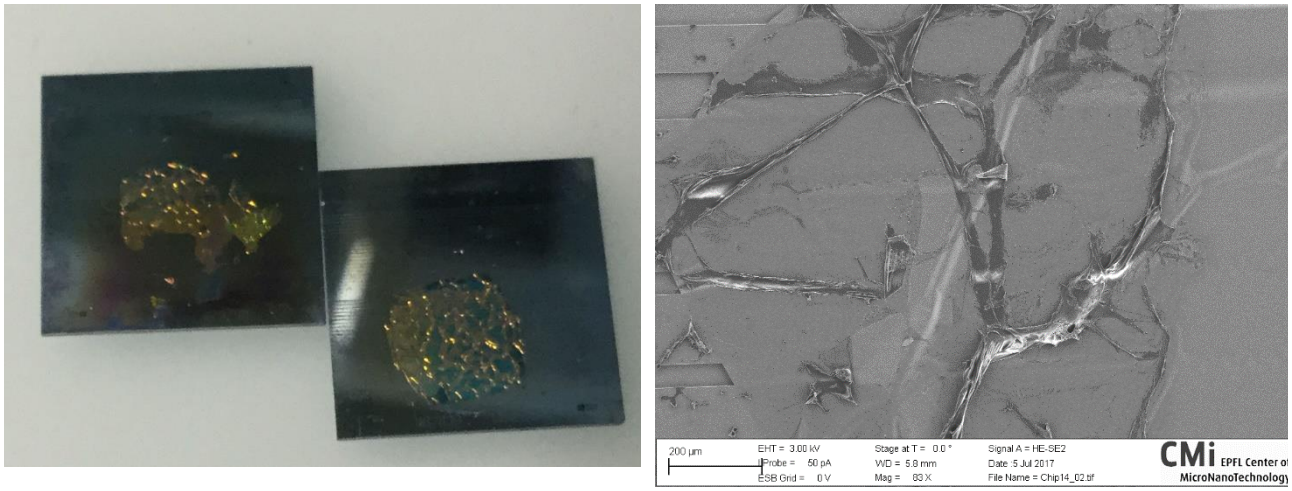


Figure 28: Results of the test at 300ºC. At the left side we have two chips, the first one was made with the normal transference and the second one with backside transference. We can see that the burned zones are bigger in the left one. At the right side, a picture from the electron microscope. We can see plastic burned (PMMA) on the silicon nitride layer but behind it the existence of big flat surfaces.

FIFTH TRY

In this attempt, we have tried to use higher temperatures [8], avoiding the problem of damaged surfaces. To do so, we have taken out the PDMS block before starting to apply the temperatures, expecting that this would implied the elimination of the PMMA (burned element in previous test). We have heated the chip at 60º again for the water evaporation and then at 300º for 5 minutes. After that we have moved to 150º to finish the transference.

The result is that the chip surface is still damaged and the transferring surface is smaller.

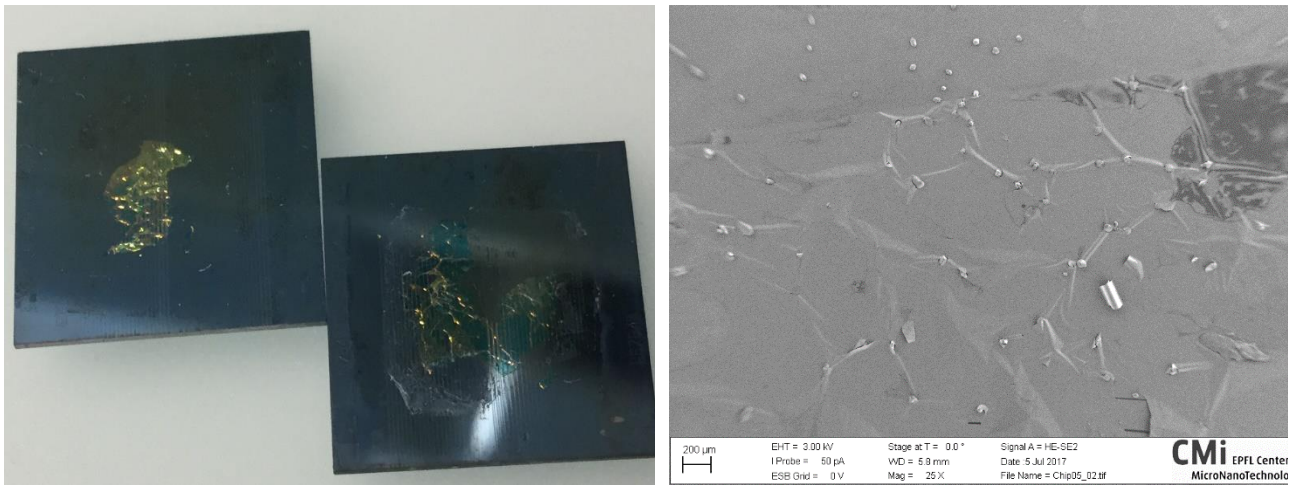


Figure 29: Pictures of the test at 300ºC and 150ºC. Left side: We can see that as we took out the PMDS and PMMA block before the transfer, trying to avoid the burning of the PMMA, there is just a small part of the silicon nitride that has been transferred. Right side: Picture with microscope. We can see that the transference has been damaged, a lot of folds appear and some burned zones. We can see dust in the picture too.

RESULTS

The results can be presented clearly in the following diagram:

Dry transference

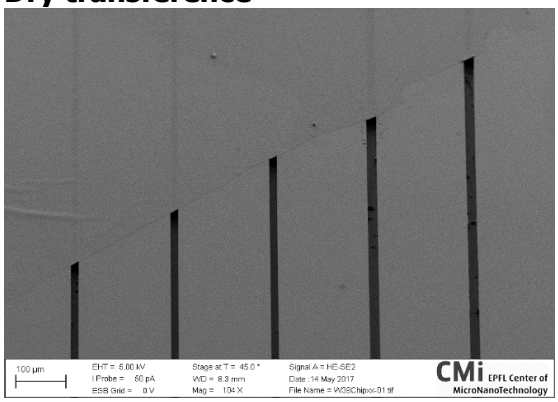


Figure 30: Dry transference channels detail.

Dry transference demonstrated to be a good option but it requires more steps than wet transference and the quality of the silicon nitride layer is worse.

In this process, we saw the existence of some fractures in the silicon nitride layer while in wet transference we did not find them.

Wet transference

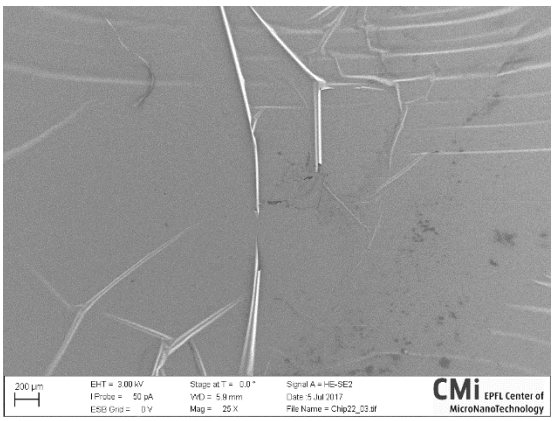


Figure 31: 60-150ºC wet transference.

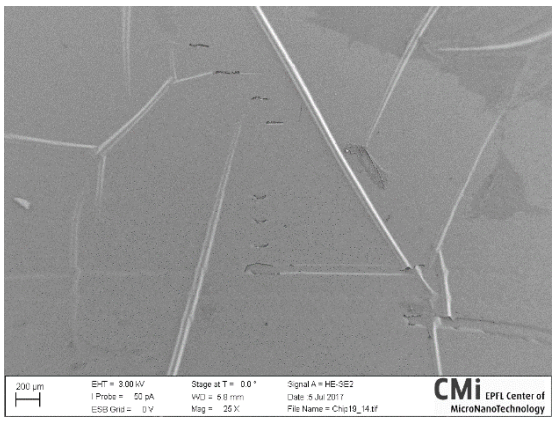


Figure 32: 60-150ºC wet backside transference

Comparing these processes, we can see in both the existence of long folds and flat surfaces of big quality. The results of both processes are similar.

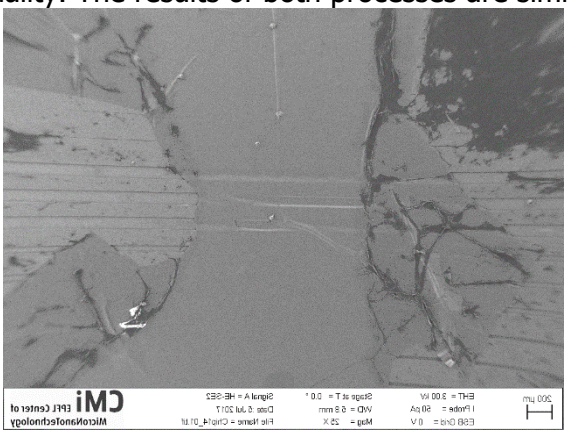


Figure 33: 60-300ºC wet transference

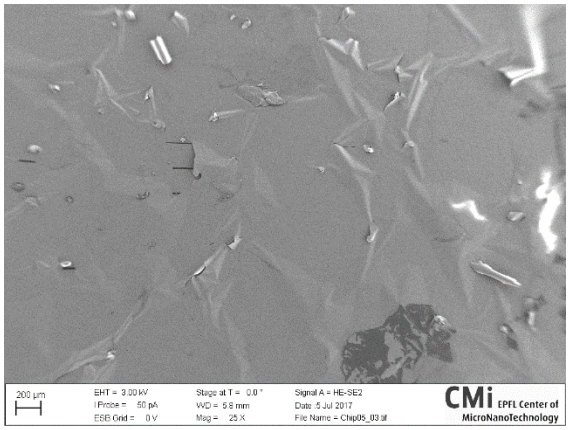


Figure 34: 60-300-150ºC wet transference

Comparing these two process we have that in both exist burned parts of PMMA. The left one presents better flat surfaces than the right one but in the right one the burned parts are smaller.

As we can see, there are some common factors:

- All the test present flat surface parts of big dimensions, which can demonstrate that the system could replace the traditional system.
- There are many folds.

And there are some differences too:

- The quantity of folds varies from one test to other.
- Heating at 300º degrees has as consequence burned PMMA regions.

After the analysis of this results, we can conclude that our research has been successful.

PERSPECTIVES

This project constitutes the first step of further researches that can improve this method to finally have a better microchannel fabrication process than the current one.

To improve this system, next researches should focus on deleting the folds or try to reduce them, because they are one of the main problems of this system. We think that a good idea to make it could be the division of the silicon layer surfaces in smaller regions so if a fold appears, its propagation would be more complicated.

It would be necessary to analyse the final material composition of each layer as well. In the microscope analysis, we can see that there are different colours, which can mean that there are different materials.

CONCLUSION

In this paper, we have been studying a new microchannel fabrication process. This process pretends to improve the classical one, eliminating the damage that some chip parts suffer. The system is based on the idea of creating a chip with a pattern and a lid of silicon nitride on the top.

First, we have created two different chips models. We have applied a pattern to the first of them (process of lithography and etching), covered it with silicon nitride and diced. The second one has been covered with silicon nitride, diced and grinded. These processes have taken place in a clean room.

Then, to create our silicon nitride lid we have analysed different etching process of silicon in KOH solution. Based in diverse experimental procedures, we have concluded that the best option to have a good quality film was to spin coating 1.5 μm of PMA and cover it with a layer of PDMS with a hole in the middle.

The final step has been the deposition of the silicon nitride layer on the top of the patterned chip. First, we have done the process drying both surfaces and, after the application of a plasma activation, we have glued them at a deposition temperature of 150ºC. This process implies some cracks in the silicon nitride surface. We have tried then to do a transference without drying the elements applying first a temperature of 60ºC to evaporate the water and then 150ºC to do the deposition. The conclusion of this scheme is that we have found a good method for the creation of good quality microchannel chips.

The main problem that we have found in this research is the existence of folds. It could be a good idea to focus the next experiments and researches on finding a technique to avoid this perturbances and to assure bigger flat parts.

In addition, this project has provided me, as electronic engineering student, the opportunity of experiment the fabrication of microelectromechanical system, learning the clean room process, putting in practice my knowledges of physics and chemistry and discovering a field that I love.

My special greetings to my director of project, Guillermo Villanueva, who helps me to find a project that could give me access to fabrication systems and specially to Dr. Tom Larsen who has been helping me since the beginning, treating me with a lot of patience and explaining me all the things that I did not understand.

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APPENDIX 1: PROCESS FLOW CHIPS WITH CHANNELS

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CMi EPFL Center of MicroNanoTechnology

☐ Semestral Project ☐ Master Project ☐ Thesis ☑ Other

Project Name

Description

Fabrication of silicon chips with channels

Technologies used			
Spin coating, direct laser writing, development, deep reactive ion etching, resist stripping, wafer dicing, low pressure chemical deposition.			
Photolith masks			
MASK #	**Critical** DIMENSION	CRITICAL ALIGNMENT	REMARKS
1	2UM	FIRST MASK	SILICON ETCH
Substrate Type			
Silicon <100>, Ø100mm, 525um thick, Single Side polished, Test wafer			

Process outline

Step	Process description	Cross-section after process
01	*Photolith* Spincoating: ***ACS200*** PR : *AZ ECI 3027 – 2 um*	

	Exposure : ***MLA150*** Mask : *CD = 2um* Development : *ACS200*	
02*	*DRIE* Machine: ***AMS200*** Process name: *SOI_sharp* Etch depth: *10 um and 30 um*	
03	*Resist strip* Machine: ***Tepla*** Process name: High_2min Machine: ***UFT remover*** Process name: *Standard*	
04	*LPCVD silicon nitride* Machine: *LPCVD Nitride* Process name: *Low stress* Target thickness: *100 nm*	
05	*Dicing* Protection: Machine: *ACS200* Process name: *5 um resist* Dicing: Machine: *Disco* Chip clean: Machine: *UFT remover* Process name: *Standard*	

*10 um on one wafer and 30 um on another.

APPENDIX 2: PROCESS FLOW SILICON NITRIDE LIDS

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CMi EPFL Center of MicroNanoTechnology

☐ Semestral Project ☐ Master Project ☐ Thesis ☑ Other

Project Name

Description

Fabrication of thin Si chips with SiN frontside coverage.

Technologies used
Low pressure chemical vapour deposition, reactive ion etching, dicing, griding.
Substrate Type
Silicon <100>, Ø100mm, 525um thick, Single Side polished, Test wafer

Process outline

Step	Process description	Cross-section after process
01	*LPCVD silicon nitride* Machine: *LPCVD Nitride* Process name: *Low stress* Target thickness: *100 nm*	

02	*Removal of backside SiN* Machine: ***SPTS APS*** Process name: *SiN etch*	
03	*Dicing before grinding* Machine: *Disco* Cut depth: *150 um*	
03	*Grinding* Machine: *DAG810* Final thickness : *50 um*	

APPENDIX 3: DATES

CHIPS WITH CHANNELS

Projet: Chips with channels

Operator: Castillo Moreno, Claudia

Created: 2017.27.03

Substrates: Silicon <100>, Ø100mm, 525um thick, Single Side polished, Test wafer

Step N°	Description	Equipement	Program / Parameters	Target	Actual	Remarks	Si wafer 39	Si wafer 40
1	**Photolithography -First litho**							
2	300 nm oxide	-	-	300 nm		CMi staff		
3	Oxide thickness	Nanospec		300 nm		With Tom	300 nm	300 nm
4	Rinsing of wafers					With Tom		
	PHOTOLITHOGRAPHY -							
5	Spincoating	ACS200	Recipe n 0126: CMi.4in.ECI 3027 2um0.HMDS.topEC				Y	Y
6	Exposure	MLA150					Dose: 215 Defoc 2	Dose: 230 Defoc: -1
7	Developing	ACS200	Recipe n 0926: CMiDev.4in.ECI 3027 2um0				YY	YY
8	Inspection	Microscope	Pictures already taken					
2	**Etching**							
9	Silicom- Dry etching	AMS200	SOI_ACCURATE ++				3 min + 1.5 min (30um)	1.5 min (10 um)
3	**Resist strip**							
10	Dry- oxygen plasma	Tepla 300	5 min				Y	Y
11	Wet-Solvent	UFT Resist					Y	Y
12	Inspection	Microscope					OK	OK
4	**LPCVD Silicon nitride**							
13	Spincoating	LPCVD Nitride	Low stress				Y	Y
14	Inspection	Microscope	Chech exposure grids				OK	OK
5	**Dicing**							
15	Protection	ACS200	Recipe n 0129: CMi.4in.ECI.3027 5um0.HMDS.topEC				Y	Y
16	Dicing	Disco						
17	Chip clean	UFT Resist						

SILICON NITRIDE LIDS

Projet : Silicon nitride lids

Operator : Castillo Moreno, Claudia

Created : 2017.27.03

Substrates : Silicon <100>, Ø100mm, 525um thick, Single Side polished, Test wafer

Step N°	Description	Equipement	Program / Parameters	Target	Actual	Remarks	Si wafer 41	Si wafer 67843
1	**LP silicon nitride**							
2	100 nm	LPCVD Nitride	low stress			CMi staff		
	Removal of backside SiN							
5	Etching	SPTS APS	SiO2 PR3:1 time: 1 min				Y	**Y**
	PMMA cover: Clean room							**Y**
	2	**Dicing before grinding**						
9	Dicing		150 um				Y	**Y**
10	Clining	UFT resist					Y	**Y**
	3	**Grinding**						
11	Grinding	DAG810	50 um				Y	