An Eight-Lane 7-Gb/s/pin Source Synchronous Single-Ended RX With Equalization and Far-End Crosstalk Cancellation for Backplane Channels

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***Abstract*— This paper presents a versatile crosstalk cancellation scheme for single-ended multi-lane backplane links. System-level investigations show that a scheme, which combines analog filters and decision-feedback crosstalk compensation on the receiver (RX) side only, can efficiently remove crosstalk patterns in straight channels as well as boards with reflections due to via stubs. An eight-lane single-ended RX has been manufactured in 32-nm SOI CMOS to validate our findings. A CTLE and eight-tap decision feedback equalizer equalize the channel without transmitter feedforward equalizer. A continuous time crosstalk canceller reduces precursors by nearest neighbors, while the residual postcursors from all aggressors are suppressed by direct feedback 7 × 8-tap decision-feedback crosstalk canceller (DFXC). Measurements with flip-chip packaged RX show that the RX macro can equalize both a 30-dB insertion loss single-ended channel with 0-dB signal-to-crosstalk at Nyquist and a channel with 28-dB attenuation with the signal-to-crosstalk ratio of 6 dB combined with reflections due to via stubs. The RX operates up to 7 Gb/s/pin with PRBS11 data at bit error rate (BER) $<10^{-12}$, and occupies 300 × 350 μm^2 with an energy efficiency of 5.9 mW/Gb/s from 1-V supply.**

***Index Terms*— Continuous time linear equalizer, decision-feedback equalizer, far-end crosstalk (FEXT), inter-symbol interference (ISI), source-synchronous architecture.**

I. Introduction

ADVANCES in CMOS process technologies have led to an exponential increase in the digital processing power of high-performance microprocessor units, leading to an increment of the data transfer bandwidth between local chips.

Manuscript received July 7, 2017; revised October 11, 2017 and December 1, 2017; accepted December 2, 2017. This paper was approved by Guest Editor Jack Kenney. This work was supported in part by the European Commission through the ERC Future Proof and ERC Time-Data Tradeoffs and in part by the Swiss Science Foundation under Grant SNF 200021-146750 and Grant SNF CRSII2-147633. *(Cosimo Aprile and Alessandro Cevrero contributed equally to this work.) (Corresponding author: Cosimo Aprile.)*

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Digital Object Identifier 10.1109/JSSC.2017.2783679

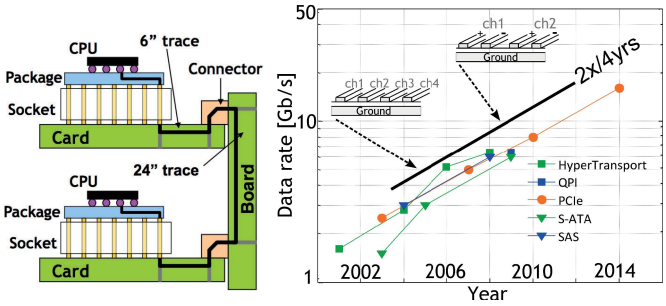


Fig. 1. (a) Backplane link, SE 4.8 Gb/s [3]. (b) Pin data rate evolution across most common I/O standards [1].

Over the past years, the data rate required for each pin has almost doubled every four years across different I/O standards, as depicted in Fig. 1 [1]. However, due to packaging constraints as well as chip size limitation, the number of package pins is increasing only slightly, while the number of transistors served by one I/O approximately doubles every new CMOS technology node [2]. At the same time, low power consumption is a first-order design constraint for I/O circuits. ITRS assumes that high-performance serial transceivers can consume a maximum of 10% of the chip power and I/O links should occupy maximum 20% of the entire chip area.

In combination with innovative circuits techniques, adopting single-ended signaling technology doubles the performance (bandwidth per pin) with respect to similar channel boards operating with differential lines per signal, such as *Quick Pack Interconnect* by Intel [4] and Hypertransport by AMD [5]. The main limitation of using single-ended printed circuit board (PCB) traces comes from the increase in crosstalk (XTC) noise due to electromagnetic coupling because of increased wire density. As data rate increases, crosstalk becomes then the most significant noise source in single-ended parallel links.

Crosstalk is the combination of far-end and near-end electromagnetic coupling. *near-end crosstalk* does not affect the signal integrity in unidirectional links [6], while *far-end crosstalk* (FEXT) heavily affects single-ended PCB traces. Conventionally, board-level techniques allow to handle FEXT,

increasing, for instance, the distance between channels, or including shielding techniques [7], [8]. However, these techniques require additional space on PCB and are rarely implemented in high-density and high-speed links. On the circuit side, there is a lack of crosstalk cancellation schemes that simultaneously handle a multichannel board. Most previous works focus on crosstalk compensation circuits for memory channels. Crosstalk-induced timing distortion is reduced by means of the timing-delay adjustment of data transition versus the state of the data [9]. However, the challenge is in knowing the correct timing compensation, which is also dependent on the process variation [10]. Crosstalk in the memory interface has also been addressed by Bae *et al.* [11], where it limits the maximum number of transitioning lanes, but does not compensate for the distorted signals. Other approaches to compensate for crosstalk noise include the use of staggered I/Os combined with a glitch suppression scheme to improve vertical eye opening or a slew rate control driver on transmitter (TX). Sham *et al.* [12] proposed to cancel FEXT injected by neighboring aggressor lanes by using *finite impulse response* at the TX. Nazari and Emami-Neyestanak [13] used a switched capacitor technique linearly combining two analog signals to reduce crosstalk, where the amount of FEXT is controlled attenuating a passive filter output.

All of the previous designs do not address the multiple crosstalk lane sources per channel bundle. To the best of our knowledge, for the first time, Oh and Harjani [14] adequately addressed crosstalk issues considering a minimum of four lanes for single-ended channels. The receiver (RX) macro proposed by Oh and Harjani [14] is power efficient and can be extended to an infinite number of lanes. However, it trades FEXT compensation by the increase of wire spacing every two lanes to minimize residual error terms. In addition, the channel used for measurement has a relatively low insertion loss (-11 dB at Nyquist frequency) and does not requires power hungry decision feedback equalizer (DFE) function. All of the proposed schemes have poor adaptability to different FEXT environments or result large circuit complexity or significant power consumption.

In this paper, we propose a versatile RX circuit capable of coping with large insertion loss and can minimize crosstalk with multiple channels having the identical lane spacing and important channel attenuation of 28 and 30 dB at Nyquist frequency. This paper extends our previous work [15], by considering different crosstalk reduction methodologies tailored with the channel board characteristics (see Section II-B). Furthermore, we provide more electrical characterizations (see Section IV), which are aligned with the system-level analysis (see Section II) and demonstrate the inter-symbol interference (ISI) equalization and crosstalk reduction strength of the overall RX circuit. This paper is organized as follows. The system-level analysis is discussed in Section II, while the RX macroarchitecture and its functional units are described in Section III. Section IV gives the electrical measurements and Section V discusses the results and concludes this paper.

II. System-Level Analysis

In high-loss single-ended communication links, the main signal path needs to be equalized to cope with ISI noise.

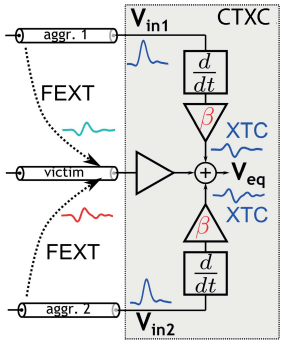


Fig. 2. Crosstalk cancellation using CTXC front end on three-lane channel.

Moreover, the precursors, cursor, and postcursors FEXT components need to be minimized to improve the signal integrity.

In this section, we first discuss the crosstalk cancellation strategy we adopt on the RX macro (see Section II-A), and then, we present the different channel board characteristics used to test the chip (see Section II-B). The mathematical paragraph (see Section II-C) discusses the crosstalk reduction in ideally coupled lanes, highlighting its limitations. Section II-D shows the system-level simulations of a continuous time crosstalk canceller (CTXC) and a decision feedback-based crosstalk canceller (DFXC) blocks, highlighting how their coexistence has to be tailored depending on the channel board characteristics. The last part of this section (see Section II-E) analyses the crosstalk cancellation techniques proposed in this paper, in case of skewed board lanes.

A. Crosstalk Cancellation Considerations

Analog filters can be used at the RX side to remove crosstalk components. The compensation scheme relies on the fact that, in ideally coupled lanes, FEXT is proportional to the derivative of the crosstalk source signal. A differentiation (easily implemented with analog filters), with appropriate gain β, can then reproduce FEXT and subtract it to the forward signal component to effectively remove FEXT [16]. It is possible to replace the RX analog filters with a feedforward equalizer at the transmitter (TX) side. However, such architecture is unable to prevent jitter amplification in the transmitted signal and imposes stringent linearity specifications in the output drivers.

For these motivations, in the proposed I/O link, the received data from adjacent lanes are processed in the analog domain by means of a CTXC,[1] to generate precursors and cursor FEXT cancellation signals [14], [15], [17]. The CTXC concept for three-lane channel is shown in Fig. 2, where a passive differentiator block is used to emulate the FEXT signal.

In presence of an eight-lane single-ended bus, the extension of the scheme introduced for three-lane system would differentiate the received signals from the seven aggressors (the crosstalk sources) and add them to the forward signal lane with appropriate gain. However, processing the received signal from all aggressor lanes to remove FEXT in a defined victim lane (the crosstalk recipient) is not a practical solution,

[1] Named XCTLE in [15].

TABLE I
KEY PARAMETERS OF THE CROSSTALK BOARD

Name	Extensions & Stubs	Length	Geometry
Ch1	none	995 mm	s=1.5×w=142 μm
Ch2	2 via stubs	720 mm	s=1.5×w=142 μm

since it would enlarge the capacitance at the summation node, limiting the bandwidth of the overall system.

Based on these motivations, our CTXC implementation receives the signals from the two adjacent channels only, which have the greatest impact on the signal integrity over the victim lane. By doing so, large FEXT cursor and precursor components can be reduced.

The residual crosstalk noise is then treated and effectively removed by means of a decision-feedback based block, cross-connected between each lane of the channel board [15], [17]. The analog correction of such DFXC,[2] is based on the switch-cap approach proposed in [18]. As a result, the transmitted signal over each lane is corrected by CTLE and DFE for the ISI distortion, while CTXC and seven DFXCs minimize the crosstalk noise.

The CTXC and DFXC systems dovetail and ensure the crosstalk cancellation completely on the RX side, thereby coupling the RX circuit with TXs sourced by different vendors.

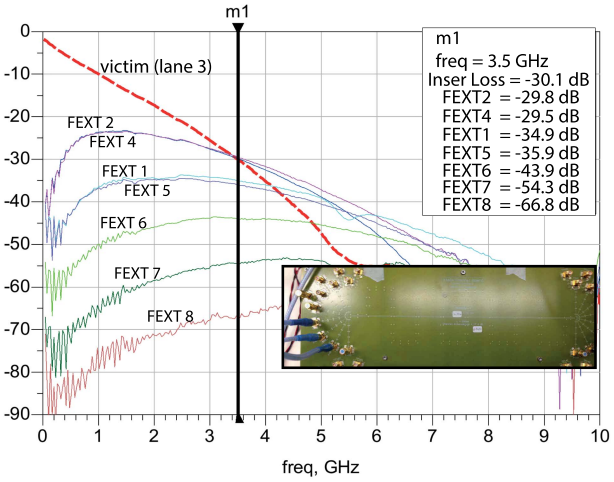
B. Boards Characteristics

In this paper, two different boards have been used to emulate multi-lane single-ended legacy channels for servers' applications. For consistency, we consider two complementary cases, (their main parameters are in highlighted in Table I), labeled Ch1 and Ch2, which are defined as follows.

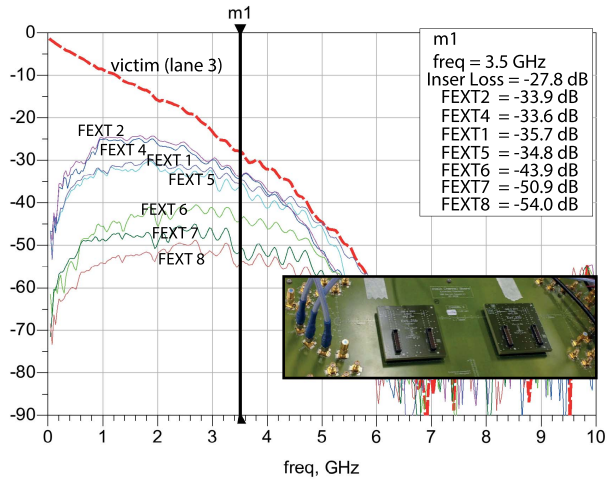
1) Ch1 Board: The crosstalk board Ch1 consists of a Rogers-PCB mother card, which hosts eight clean channels (no notches in the frequency response) due to the absence of extension boards, vias, and connectors. The signal travels for 995 mm on the mother card, in a lane defined by its trace width $w = 95\ \mu$m and lane-to-lane spacing $s = 142\ \mu$m. Ch1 is an example of large attenuation channel, -30 dB at Nyquist frequency, and important FEXT contribution. Fig. 3(a) displays the S-parameters (insertion loss and FEXT from all switching lanes) with respect to lane 3, in each channel bundle.

2) Ch2 Board: Channel Ch2 consists of a 720-mm Rogers-PCB mother card with extension Rogers-PCB board mounted on top with two Erni MicroSpeed connectors. The signal travels for 100 mm on the mother card, then goes to the first extension board, travels back to the mother card for 100 mm, travels in the second extension board, and finally arrives to the RX. In this channel, $s = 1.5 \times w = 142\ \mu$m. Board Ch2 FEXT does not follow the ideal derivative model, due to the presence of connectors and via arrays in the signal path. With respect to Ch1, Ch2 results as a more severe board channel, with an important channel attenuation around 28 dB and a more severe FEXT contribution. Fig. 3(b) displays the S-parameters for lane 3 in each channel bundle.

[2]Named XDFE in [15].



(a)



(b)

Fig. 3. Forward and FEXT frequency responses (magnitude) for (a) Ch1 and (b) Ch2 PCB board.

C. Mathematical Formulation for Ideally Coupled Lanes

This section provides an overview of the crosstalk contribution within N ideally coupled lanes (e.g., Ch1 board), where the FEXT follows the derivative model [16].

The frequency-domain representation of the received vector signal $\mathbf{Z} \in \mathbb{R}^N$ is given by $\mathbf{Z} = \mathbf{G} \cdot \mathbf{H} \cdot \mathbf{X}$ [14], where $\mathbf{G} \in \mathbb{R}^{N \times N}$ is given by the CTXC contribution, $\mathbf{H} \in \mathbb{R}^{N \times N}$ is the frequency channel response matrix, and $\mathbf{X} \in \mathbb{R}^N$ is the input signal vector.

As addressed in [14], the setting that ensures zero crosstalk contribution from the nearest neighbor is $G_x = \beta G_0$, where G_x and G_0 define the CTXC analog gain for the crosstalk cancellation component and forward received strength, respectively. Under this scenario, the multiplication between the channel response matrix $\mathbf{H}$ and the CTXC matrix $\mathbf{G}$ shows the additional reused crosstalk energy $(2\omega^2\beta^2)G_0H$. Nonetheless, it also shows an error contribution at each lane from the second neighbors and reveals the presence of additional uncompensated noise terms $\omega^2\beta^2 G_0 H$. In [14], it is proposed to solve this issue by pairing up every two lanes and maintaining sufficient distance between the bundle, thereby trading board

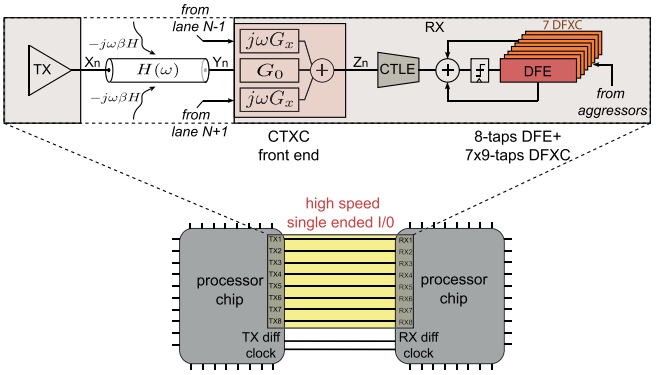


Fig. 4. Single-lane transceiver block diagram with crosstalk compensation scheme combining CTXC on the front end.

area for residual error term. However, this reduces the PCB area efficiency, and it may not even be possible in applications where dense PCB routing is required. It should be noticed that using such an analog front end, residual errors' terms can never be forced to zero.

In this paper, instead of zero forcing the FEXT from adjacent lanes (setting $G_x = \beta G_0$) and trying to minimize the error term by increased board spacing, we optimize the gain settings G_x and G_0 in the CTXC with the goal of maximizing the vertical and horizontal eye opening. Paragraph II-D1 discusses this crosstalk reduction technique, applied for channel Ch1, where CTXC is sufficient to open the eye diagram in each lane.

However, if the board presents connectors and via arrays in the signal path (e.g., Ch2 board), the crosstalk patterns will be more intricate and will not follow the ideal coupled lanes model. Therefore, the CTXC only would not be sufficient to ensure operations at BER $= 10^{-12}$, and necessitates the DFXC to reduce the FEXT postcursors. Such a crosstalk cancellation technique is addressed in Section II-D2.

D. System-Level Simulations

A system-level analysis is performed to investigate the optimized crosstalk cancellation strategies for the channels described in Section II-B.

Fig. 4 highlights one of the eight single-ended lanes within the channel bundle. The eight-lane channel bundle frequency-domain data (forward and FEXT response) have been collected in a 16-port S-parameter file, which models the interconnect. On the RX side, each lane features a CTXC followed by a CTLE, 8-tap DFE and 7 × 8-tap DFXC. In the eight-lane topology, it is assumed that data patterns of different lanes are uncorrelated.

1) Ch1 Board Crosstalk Reduction: In this section, the crosstalk reduction technique applied for Ch1 board (described in Section II-B1) is addressed.

The calibration is performed over R, C, G_x, G_o, and CTLE settings. Due to large channel attenuation, both CTLE and DFE are required to effectively remove ISI. The simulation results are presented in Fig. 5. All simulations include a 5-ps TX random uncorrelated jitter (roughly 3.5% UI for 7-Gb/s

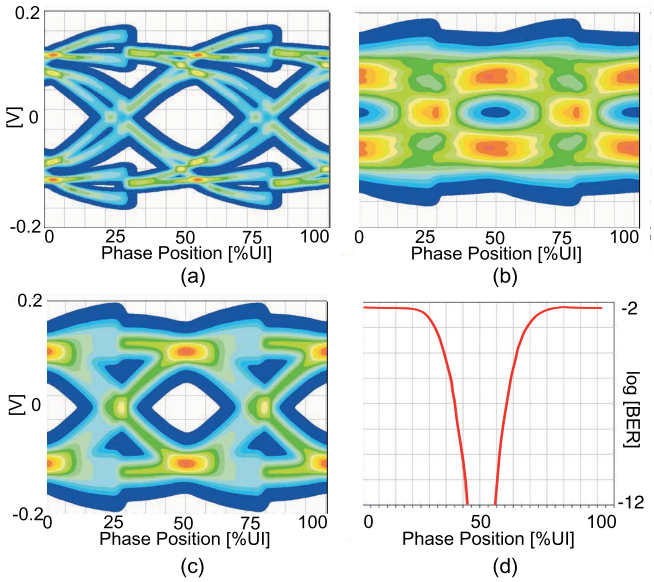


Fig. 5. Simulated RX data eye for Ch1 board, with all aggressors (a) switched off and (b) switched on without crosstalk compensation scheme (CTLE and DFE on, in both cases). (c) Data eye and (d) bathtub plot with optimally calibrated CTXC front end. All aggressors are transmitting.

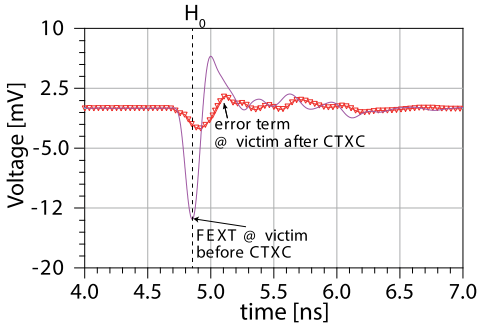


Fig. 6. FEXT pulse response from the aggressor to victim lane before and after CTXC.

data rate). The data eye is completely closed when all aggressors are transmitting. The CTXC front end is able to open a closed data eye with 35% UI eye width and 75-mV eye height. Fig. 6 shows the FEXT pulse response between the aggressor and victim at 7 Gb/s, before and after the crosstalk compensation scheme (with optimal filter setting's calibration). Such an analysis highlights that the CTXC makes the system less sensitive to jitter noise, since it flattens the derivative of the crosstalk pulse response.

2) Ch2 Board Crosstalk Reduction: This section discusses the crosstalk reduction technique addressed for channel board Ch2 (defined in Section II-B2). The limits of CTXC with this particular board are evinced in Fig. 7, which shows a completely closed eye for 7 Gb/s with only the two-nearest aggressor lane switching. Thus, a different crosstalk minimization technique is involved for this type of channel board. First, the CTXC-CTLE strength calibration targets the reduction of precursors and cursor crosstalk contribution. Then, the crosstalk terms are determined from detected bits in the aggressor lanes and its derived voltage is subtracted over the victim by means of the DFXC filters. A statistical

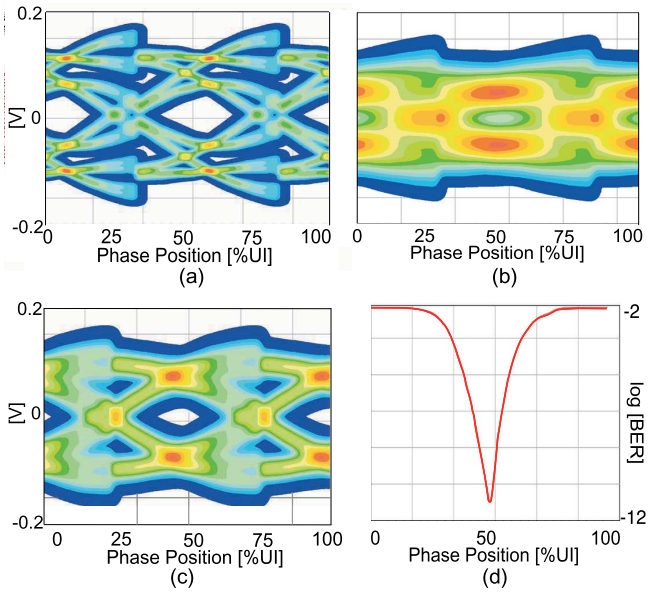


Fig. 7. Simulated RX data eye for Ch2 board, with all aggressors (a) switched off and (b) switched on without crosstalk compensation (CTLE and DFE on, in both cases). (c) Data eye and (d) bathtub plot with optimally calibrated CTXC front end with the two nearest aggressors transmitting.

analysis using MATLAB Software has been performed to validate the CTXC-DFXC effect. A *probability distribution function* (pdf) of the ISI and crosstalk pulse response spanned over all postcursor taps has been developed, where values have been found convolving the ISI and crosstalk terms. The crosstalk pdf allows to analyze all the possible combinations of postcursor ISI and the FEXT taps. Such an analysis is valid by assuming that the data over the victim and the aggressors are white and uncorrelated.

To perform such analysis, the pulse response on the victim lane (only the victim lane TX is transmitting, while all the aggressors are silent) is combined with the crosstalk pulse responses (only the aggressor transmits a pulse, while the victim TX is silent) of the aggressor lanes. During this phase, the CTLE is activated, while DFE is OFF. Given a sampling window $\mathcal{D} = \{x_1, \ldots, x_m\}$ of $m = 32$ sampling points in 1 UI, the optimal h_0 has been found by choosing the index of the sampling point in $\mathcal{D}$ that maximizes the eye aperture V_{eye}, which is defined as

$$V_{\text{eye}} = \text{Signal} - \text{CDF}_{\text{NIX}}^{-1} - \text{Sensitivity} \tag{1}$$

where Signal $= h_0 - \mid h_{-1} \mid$ is the signal amplitude given by the cursor h_0 minus the absolute value of the first of the precursors h_{-1} (which has the same polarity as the cursor value in these types of channels); $\text{CDF}_{\text{NIX}}^{-1}$ is the inverse of the *cumulative distribution function* (CDF) of the *noise, ISI, and crosstalk* (NIX) at BER $= 10^{-12}$. The CDF is computed convolving the ISI, crosstalk, and noise distributions, given by the pdf analysis. The input referred noise includes CTLE, comparator, and jitter noise. The term Sensitivity $= 5$ mV is the minimum comparator voltage sensitivity.

Using the precise pdf approach for analyzing ISI and crosstalk has been necessary, since using a simpler rms summation of ISI and crosstalk components was found to give

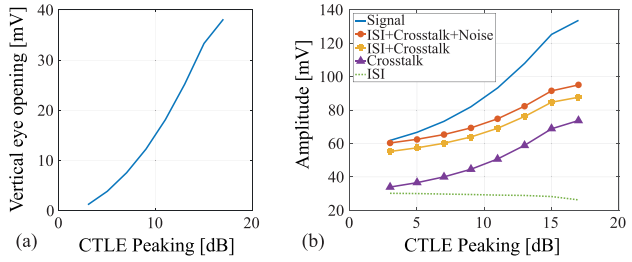


Fig. 8. Highlight of (a) vertical eye aperture and (b) *signal*, crosstalk, and ISI evolution for different CTLE peaking settings.

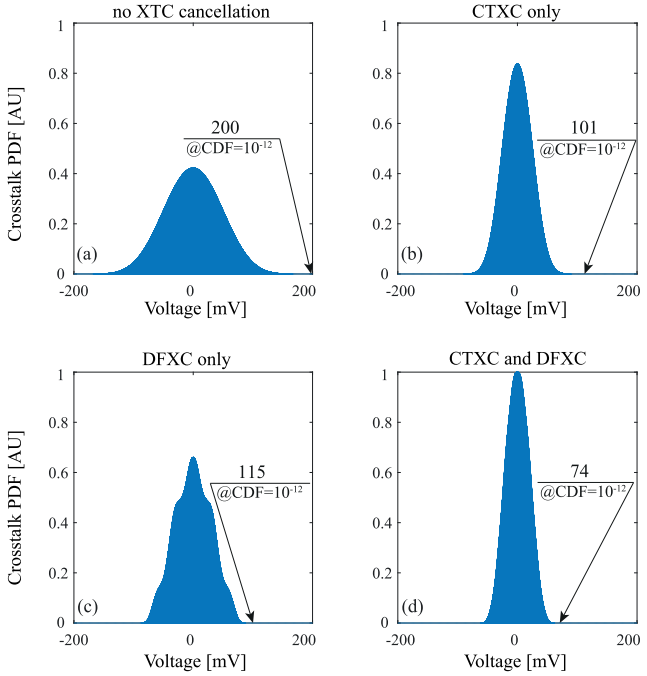


Fig. 9. PDF of the crosstalk pulse response spanned over all postcursor taps (a) without crosstalk cancellation, (b) with only CTXC on, (c) with CTXC off and DFXC on, and (d) with both CTXC-DFXC activated.

overly pessimistic results, which is due to the non-Gaussian nature of distributions for ISI and crosstalk.

Fig. 8(a) shows the vertical eye opening versus CTLE peaking settings, including 8-tap DFE equalization co-optimized with CTXC and 56-tap DFXC at BER $= 10^{-12}$. The trend reveals that high peaking settings provide the maximum vertical eye opening, even in the presence of crosstalk. This counter intuitive trend can be explained in Fig. 8(b), where the *signal*, ISI, and crosstalk contribution (derived by the pdf analysis) are plotted independently. Eventhough the CTLE peaking is generated by lowering the dc gain, larger CTLE peaking settings increase the *signal*. This is because lower peaking results in more ISI, which requires the CTLE output to be scaled to meet linearity requirements for DFE equalization. Moreover, crosstalk components increase with CTLE peaking, since the CTLE tends to amplify crosstalk. Overall, increasing the CTLE peaking, the *signal* grows faster than crosstalk does and ISI is reduced; then, the net eye opening is larger with high peaking settings.

The crosstalk pdf obtained with the statistical analysis is reported in Fig. 9 in four different scenarios, with the maximum CTLE peaking setting. In particular, Fig. 9(a) shows the

TABLE II
CROSSTALK CANCELLATION PERFORMANCES

Board Ch2				
$Signal = h_0 - h_{-1}$ [mV]	138			
Δ_{ISI} [mV]	26			
σ_{Noise} [mV]	4			
$Sensitivity$ [mV]	5			
CTXC	OFF	ON	OFF	ON
DFXC	OFF	OFF	ON	ON
Δ_{XTK} [mV]	200	101	115	74
$\Delta_{ISI+XTK}$ [mV]	211	114	126	88
$\Delta_{ISI+XTK+Noise}$ [mV]	214	121	131	95
V_{eye} [mV]	−105	−7	2	38

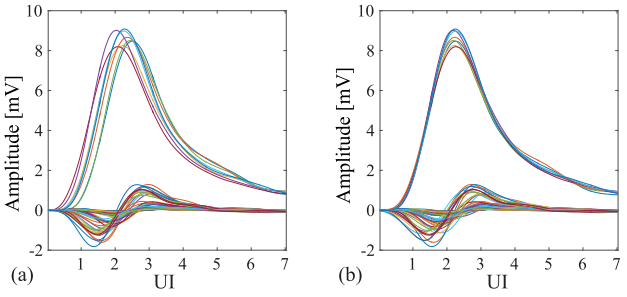


Fig. 10. (a) Skewed and (b) un-skewed impulse responses at the TX side.

crosstalk pdf with no FEXT cancellation, while in Fig. 9(b), only the CTXC is activated, reducing the crosstalk noise amplitude at BER $= 10^{-12}$ from 200 to 113 mV. The pdf distribution for the DFXC-only is reported in Fig. 9(c). When CTXC is combined with DFXC, as shown in Fig. 9(d), the crosstalk error term Δ_{XTK} at BER $= 10^{-12}$ is equal to 73.5 mV, showing a significant improvement in vertical eye opening. The results from the pdf analysis are reported in Table II, which highlights the crosstalk cancellation strength for all the CTXC-DFXC combinations. Without crosstalk reduction, the FEXT contribution overcomes the cursor h_0 amplitude, resulting to a closed eye. The vertical eye aperture is improved, once both the CTXC and the DFXC crosstalk canceller blocks are optimally calibrated, resulting in 38.7-mV vertical eye opening.

E. Crosstalk Cancellation Over Skewed Lanes

Some differences in the lane length, due to manufacturing tolerance, can be the cause of some skew experienced by the non return to zero (NRZ) signal traveling the channel bundle, both on the TX and the RX side. Fig. 10(a) shows the skewed impulse responses for all the eight single-ended lanes of channel board Ch2, once the signals are launched at the same time at the TX. Such an unwanted issue can be solved forcing delay adjustments on the TX side, resulting in aligned impulse responses, as depicted in Fig. 10(b).

However, the skew adjustment on the TX for each forward paths does not solve the crosstalk pulse responses skew issue on the RX side. Fig. 11(a) shows two signals traveling a multi-lane board with identical channel lengths. The crosstalk coupling from the aggressor to the victim lane is then perfectly corrected by the CTXC signal, given by $-\beta d/dt$ of the aggressor pulse response, at the time t_0.

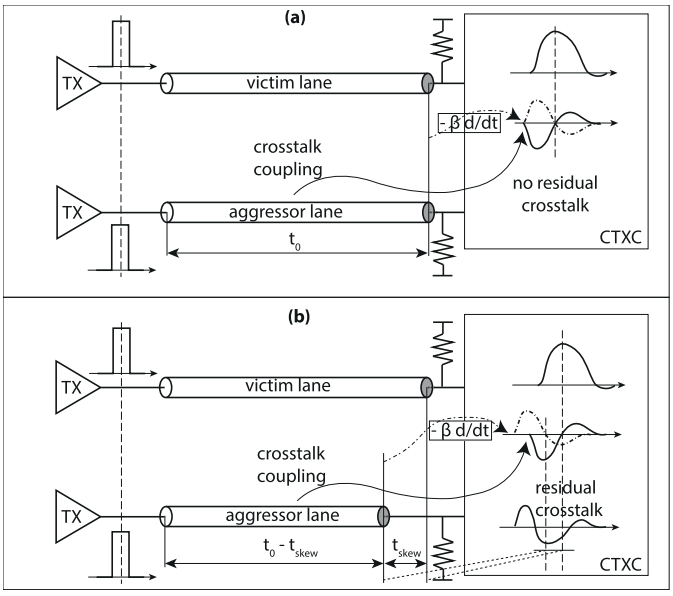


Fig. 11. Qualitative highlight of CTXC effects for (a) un-skewed and (b) skewed board lanes.

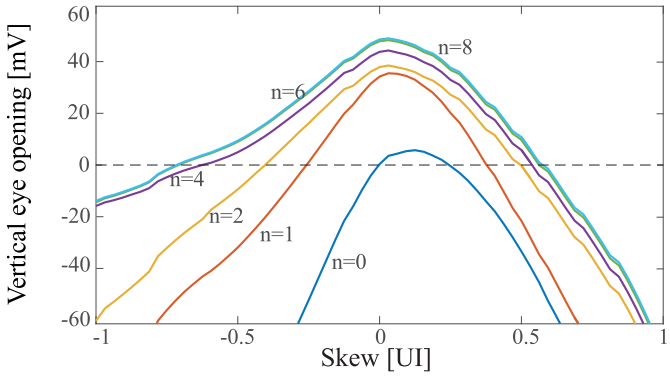


Fig. 12. Vertical eye aperture versus different lane skews at the RX side, with a different number n of taps activated on the DFXC. The simulations are performed with the Ch2 channel board.

In case of different channel lengths, the crosstalk coupling signal arrives to the RX terminal at a different instant with respect to its correction version because of the channel skew. Considering that the aggressor lane is shorter than the victim lane, as highlighted in Fig. 11(b), the XTC coupling arrives at time $t_0 - t_{\mathrm{skew}}$, while the FEXT cancellation signal, generated in the CTXC, is ready at time t_0. This produces a residual crosstalk signal, which might be partially reduced by the DFXC. For this reason, the CTXC of each lane has to be adapted accordingly.

An analysis is performed to verify how the DFXC system interacts with the RX system sensitivity. Fig. 12 shows the vertical eye aperture with different lane skews at the RX, with a different DFXC number of taps activated, over a single lane of Ch2 board. The DFXC contribution is already evident on the vertical eye aperture, from no crosstalk reduction (i.e., $n = 0$ curve) to tap-1 of the DFXC activated ($n = 1$ curve). Interestingly, it is important to evince how the DFXC reduces the sensitivity to the skew. For instance, considering in Fig. 12

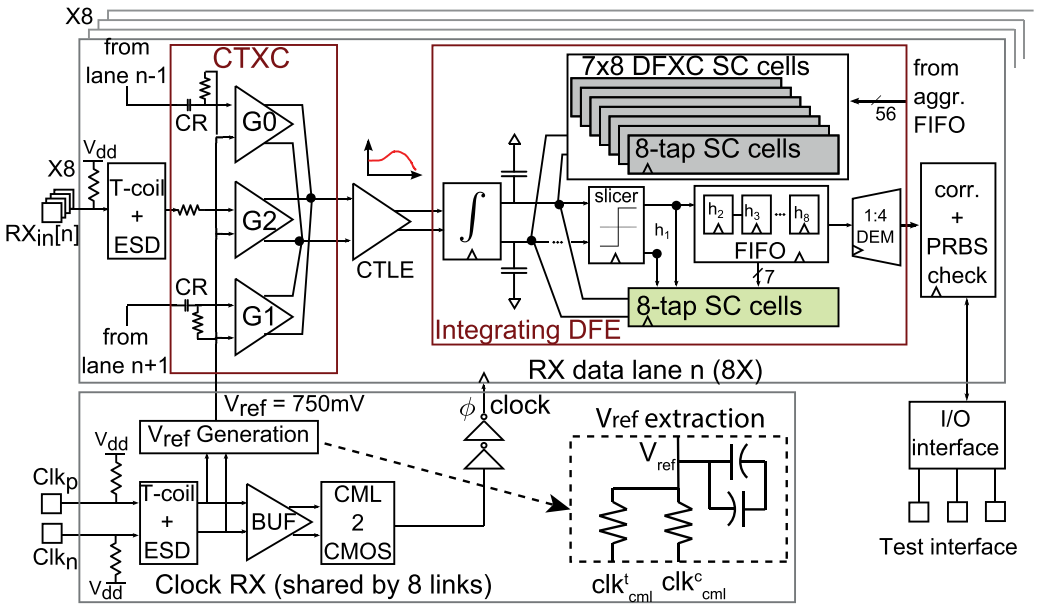


Fig. 13. Eight-lane single-ended RX architecture.

the curve with the first four taps activated (i.e., $n = 4$ curve), the vertical eye opening is flattened with respect to the one without DFXC contribution. Moreover, the DFXC contribution is limited to the first 2–4 taps, since only marginal crosstalk reduction is obtained with more taps activated.

III. Receiver Architecture and Circuits

The architecture of the source synchronous RX is shown in Fig. 13. It consists of eight single-ended data lanes and one shared differential clock lane. Each datapath starts with the termination front end, followed by a product-level electrostatic discharge (ESD) protection combined with T-COIL for bandwidth extension. The CTXC processes the input signal together with the nearest aggressor. The CTXC output goes to a two-stage CTLE followed by a direct feedback 8-tap DFE and 56-tap DFXC running at full rate. Equalized output at full rate is then deserialized to quarter rate and sampled by a digital engine, used for adaptation and BER check.

A. Clock Generation

A full rate clock supplied off chip with 1-V_{pp} swing and 750-mV CM is terminated differentially before being amplified by a CML buffer [19]. The reference voltage V_{ref} is extracted directly from the input clock common mode without the need of a dedicated pin as in many single-ended standards, such as DDRX. The buffered input clock is then converted to CMOS level and buffered to the local clock distribution within each lane.

B. CTXC and CTLE

The CTXC is located after the impedance matching network and presents an FEXT reduced signal to the CTLE. Fig. 14 shows the circuit implementation of the proposed CTXC circuit.

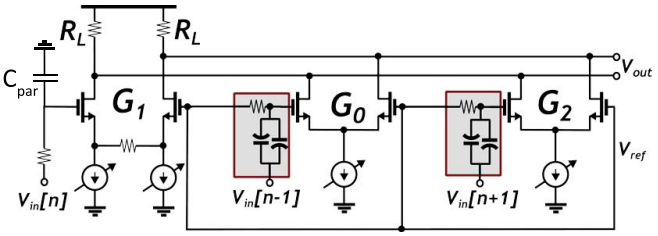


Fig. 14. CTXC stage with single-ended passive differentiator, variable gain amplifier, and current summation. The two high-pass *RC* differentiators are highlighted in the boxes.

The CTXC consists of two passive differentiators followed by a current domain adder. The differentiators produce a single-ended crosstalk cancellation signal from the two adjacent lanes. The values of $R = 972\ \Omega$ and $C = 30$ fF have been chosen to provide return loss below -10 dB up to 4 GHz at each of the broadband 50-Ω RX inputs. In [14], a resistor–capacitor replica circuit is added in the forward path to equalize phase delays between forward and crosstalk cancellation paths. In this way, the transfer function of the differentiator differs from the replica circuit by sRC, providing 90° phase shifts at all frequencies. However, this creates a parasitic pole on the main signal path. In this design, only the resistor is added in the main path, while the capacitor consists of the CTXC input stage loading directly. Circuit simulations across corners resulted in acceptable distortion with marginal impact on crosstalk cancellation.

A current domain adder with programmable gain combines the signals from the three paths. Three digitally programmed bias currents enable to adjust the gain of the forward and crosstalk cancellation paths independently. Variable gain amplifier (VGA) bias currents are binary weighted and can be adjusted with 4-bit resolution, enabling crosstalk cancellation over a wide range. The forward path uses a degenerated differential pair to improve linearity. Since the differentiated

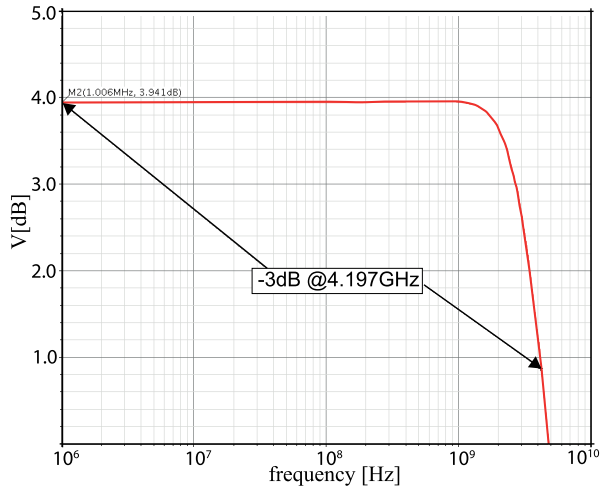


Fig. 15. Simulated ac response of main signal path VGA with maximum gain setting.

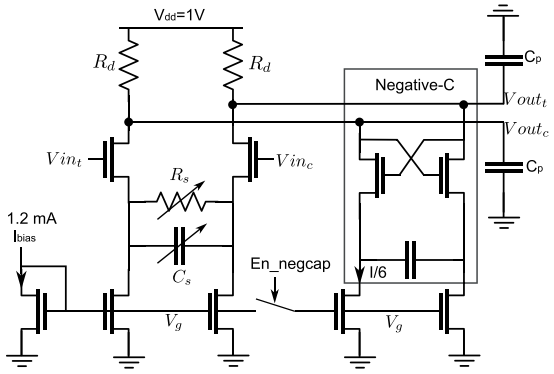


Fig. 16. CTLE stage with negative-C bandwidth enhancement. Reprinted from [18].

signals have a small amplitude, because FEXT is typically much smaller than the main signal component, there is no degeneration resistor in the crosstalk cancellation VGA. The single-ended to differential conversion is performed in the CTXC directly by connecting the VGA input differential pair to V_{ref} on one side and to the differentiator/ compensator on the other side.

Fig. 15 displays the simulated (after *RC* extraction) frequency response of the forward path VGA. The dc gain is 3.9 dB with a 3-dB bandwidth of 4.19 GHz. Bandwidth limitations come from the large capacitance at the current summation node, which corresponds to 16 fF. This is still acceptable for 7–8 Gb/s, and hence, no architecture change is needed.

The CTLE circuit, depicted in Fig. 16, is a differential buffer stage with programmable capacitive and resistive source degeneration [18]. A negative capacitance is in parallel with the differential pair and, if enabled, is used to enhance the bandwidth of the circuit. The programmable resistive degeneration is controlled with 9 thermometer coded steps, providing 17 settings in total. The degeneration capacitance is binary programmable with 4-bit resolution. Each capacitance step is implemented with two anti-parallel connected varactors. Two CTLE stages are cascaded to provide up to 17-dB peaking at 3.5 GHz with -3.7 dB dc gain.

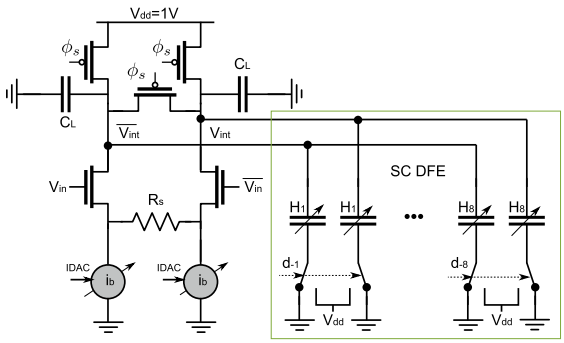


Fig. 17. Integrating DFE using SC feedback.

C. DFE and DFXC

The DFE core, shown in Fig 18, includes 8-tap DFE and 7×8 DFXC switched-capacitor cells. A current integrating stage amplifies the CTLE output for 1/2 UI. A track and hold stage is avoided to limit the kT/C noise with a cost of 0.9-dB loss due to half UI time window integration. The DFE core loop is based on a direct feedback full rate DFE, where the critical timing loop is for *tap-1* (h_1) equalization feedback. Digitally programmable *switched capacitor digital-analog converters* (SC-DAC) are implemented to add charge on the integration node. This approach enables a fast DFE feedback thanks to the instantaneous effect of the charge injection on the summation node and allows a relaxation of the DFE timing loop, compared with current summation DFE [18]. Each capacitive DAC is programmable with 6-bit resolution, with 1 LSB $=$ 250 aF ($C_{\text{max}} = 15.75$ fF) and is realized with metal M1 and M2 layers for the finger caps. Correction tap h_1 uses three SC cells connected in parallel, allowing a wider range correction. The less critical DFE taps h_2 to h_8 and the remaining 48-DFXC taps are driven by FIFO data. The implemented DFE, with a capacitance charge feedback, is shown in Fig. 17. A dynamic differential latch receives the digital data resolved by the strongARM data-latch [18], and samples them at the falling clock edge. The differential cascoded voltage switch (DCVS) and dynamic latch together implement the function of a flip-flop. The dynamic latch avoids charge injection, which occurs before the integration period. In fact, in an SC-DFE, no DFE correction is performed if the charge injection occurs during the reset phase. The data format is kept in pre-charged dynamic logic from the data-latch to each SC-DAC input. In this way, it is possible to close the DFE tap-1 timing with reasonable margin, since a conversion step to static CMOS logic is avoided.

Each lane includes an additional offset-programmable latch (amplitude path), shown in Fig. 18 (top), for RX internal eye measurement and DFE tap calibration. It consists of a DCVS latch with integrated voltage offset followed by a *set–reset* latch. The amplitude bit is fed into the digital calibration block, where the information is processed to find a correlation between the received amplitude samples and previous data bits indicating the presence of ISI or FEXT.

IV. Measurement Results

The layout of the fabricated circuit, whose RX macro measures 300×350 μm^2, is shown in Fig. 19. The chip, fabricated

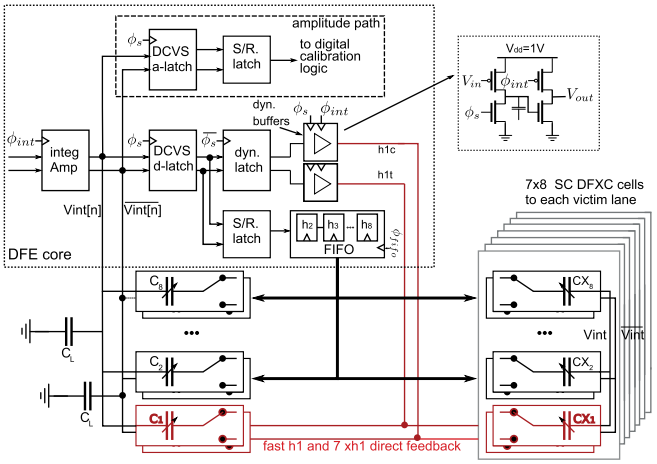


Fig. 18. DFE and DFXC core, with fast tap-1 feedback, including 8-tap DFE and 7 × 8 DFXC SC cells.

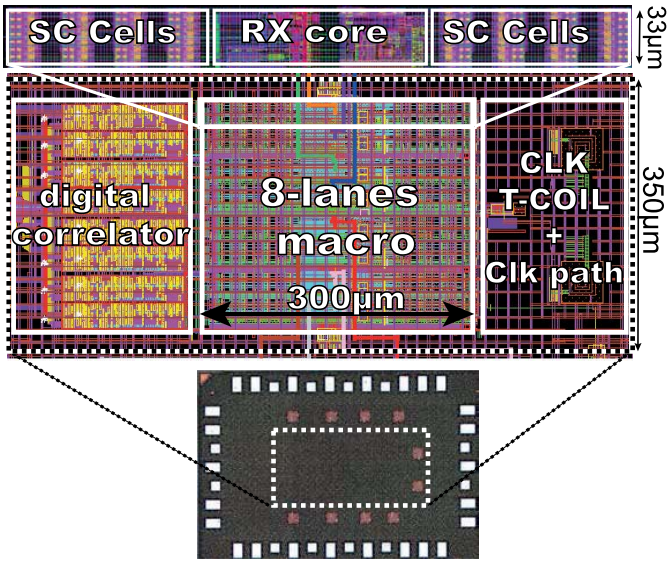


Fig. 19. Layout of RX macro (center), detail of the SC-DFE cells (top), and the die micrograph (bottom).

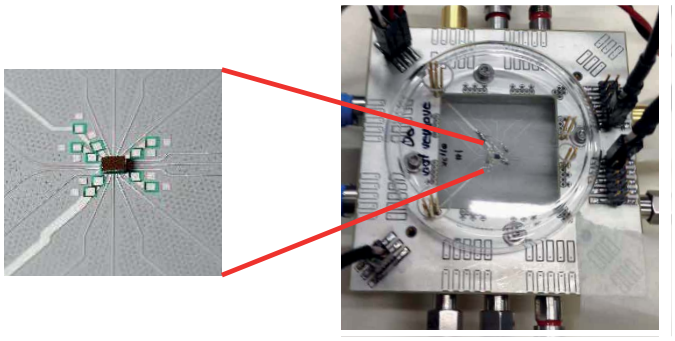


Fig. 20. Left: chip is flip-chip mounted on the LCP PCB. Right: LCP is packaged in a rigid metallic frame.

in 32-nm SOI CMOS, has been flip-chip mounted on a high-frequency, low-loss substrate, *liquid crystal polymer* (LCP) PCB, shown in Fig. 20 (left). The LCP itself is embedded in a rigid metallic frame, which includes impedance-matched high-frequency coaxial connectors, as shown in Fig. 20 (right).

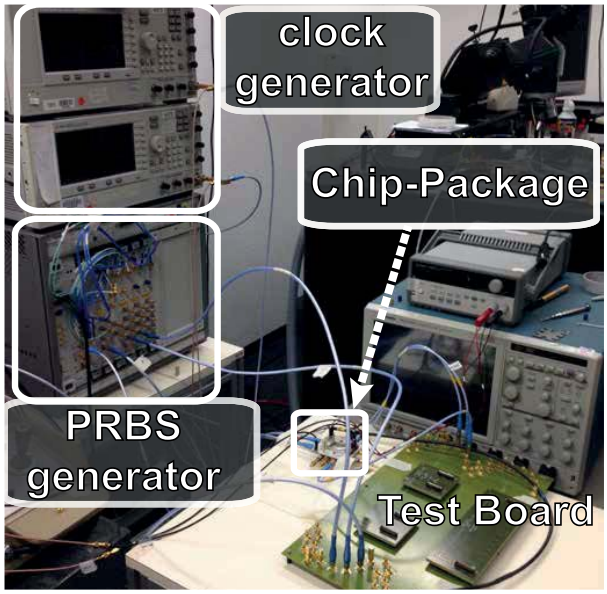


Fig. 21. Measurement setup: clock generators on top-left, PARBERT for PRBS generation on bottom-left, test board Ch2 on bottom-right, and the RX in the middle.

The RX performances have been tested with both the channels described in Section II-B. The characterization has been performed using high-frequency probing cables connected to an Agilent PARBERT. Fig. 21 shows the measurement setup. Read/write process has been performed thanks to a bidirectional digital interface, used to interface the RX chip with a PC. An on-chip error counter (PRBS checker) and correlator, running at quarter rate, has been exploited to run the electrical characterization for latch offset correction, timing adjustment, and CTXC-CTLE and DFXC-DFE coefficient tuning. A three-lane measurement was performed owing to the limitation of the measurement equipment. The data streams sent over the three adjacent lanes were PRBS7 on aggressors and PRBS11 on the victim, thus uncorrelated bit sequences.

A. Ch1 Measurement Results

The calibration of the internal registers has been addressed as follows: as first step, we calibrate the forward signal path only, switching off the aggressor TXs. The RX output, read by the on-chip amplitude path, is sent to the correlator and analyzed on a PC, using MATLAB tool. The new CTLE-DFE coefficients are written to the internal registers, in order to reduce the ISI. Following this step, we switch on one of the two nearest TX lanes, and we perform the CTXC parameters' sweep, through the PC. The same process is performed for tuning the other nearest aggressor lane, calibrating the second branch of the CTXC. Once the two CTXC set points have been defined, the forward signal calibration is repeated, to reduce the impact of the CTLE on the reduced crosstalk pulse responses, trading off the CTLE and CTXC contribution.

Fig. 22 shows the measured BER bathtub curves related to board Ch1, generated internally by doing a horizontal sweep of the data through the Agilent PARBERT phase generator (32-step UI). Once the aggressor lanes are transmitting, the

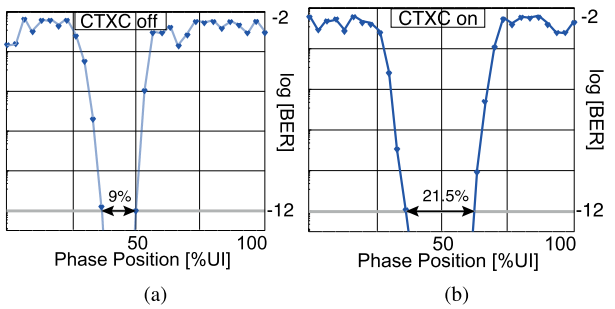


Fig. 22. Measured bathtub plots for Ch1 board with CTXC (a) switched off and (b) switched on, with the two nearest aggressor lanes transmitting.

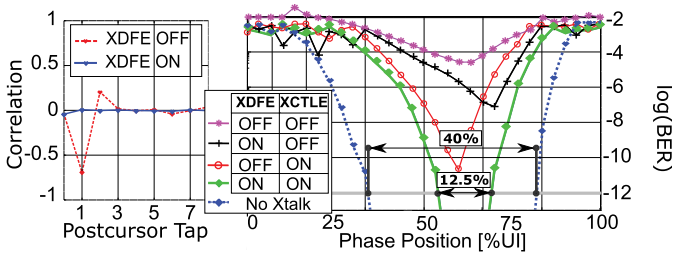


Fig. 23. Board-Ch2. Left: measured correlation with postcursor taps with and without DFXC. Right: measured bathtub plots.

bathtub curve shows a horizontal aperture of 12% UI, which rises to above 25% UI, once the CTXC is activated.

B. Ch2 Measurement Results

The correlation measurement between the two aggressors toward the victim postcursors is necessary for the DFXC taps tuning, over board Ch2. The correlation values were read through the on-chip amplitude path, by the PC and the updated coefficients rewritten to the circuit registers, driving the correlation with postcursor channel taps to zero [see Fig. 23 (left)]. The BER bathtub curves are shown in Fig. 23 (right). With silent aggressors, the RX eye is open with a horizontal margin of 40% UI at 10^{-12} BER. Once the two adjacent aggressor lanes are transmitting, the link does not operate error free, since the bathtub curve reaches only 10^{-4} BER. After switching on the crosstalk cancellation blocks, the eye is reasonably open with a 12.5% UI margin [highlighted in Fig. 24(d)], showing that both CTXC and DFXC are necessary to ensure errorfree operation of the RX. Fig. 24(a)–(c) displays the measured eye diagrams, generated internally by doing a horizontal sweep of the data through the Agilent PARBERT phase generator and vertically by sweeping the amplitude programmable latch offset. The measured vertical eye margins are 22.4 and 64 mV_{ppdiff} at 10^{-8} BER with and without crosstalk, respectively.

A power breakup for 7-Gb/s operation is shown in Table III, which reports the power consumed by one lane. The clock generation circuit is amortized by eight lanes. The DFE core datapath includes integrating amplifier, DCVS latches, dynamic datapath, and digital FIFO. The total power dissipation, once the CTLE, CTXC, 8-tap DFE, and 56-tap DFXC are active, amounts to 5.9 mW/Gb/s with 1-V supply at package,

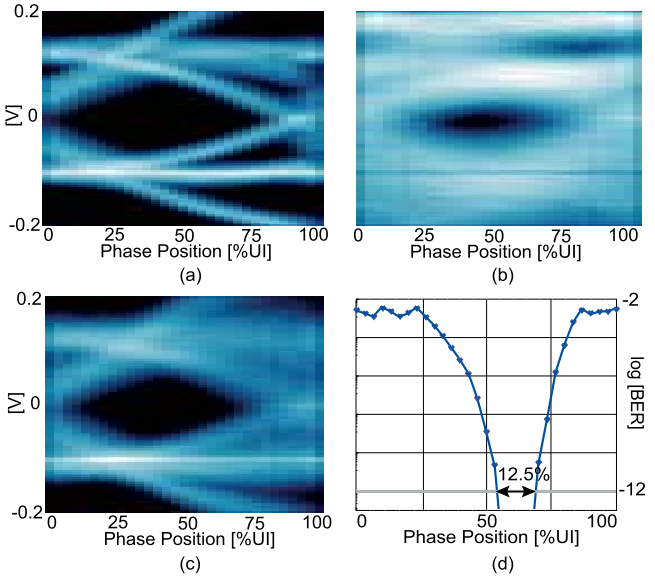


Fig. 24. Received eye diagrams with silent aggressors (top-left), crosstalk cancellation off (top-right), and crosstalk cancellation activated (bottom-left) with related bathtub plot (bottom-right).

TABLE III
RX POWER DISTRIBUTION

	μW/Gb/s
clk path (amortized by 8 lanes)	66
local clock distribution	260
CTLE-CTXC	1150
DFE-DFXC	3894
digital correlator	250
1:4 demux	280
Total	5900

from which 3.9 mW/Gb/s are used in the 64-tap DFE+DFXC SC cells and core datapath.

Table IV shows a comparison of the RX macro with prior art. The power overhead compared with the prior art mainly comes from the DFXC function. Moreover, the power number reported here includes the complete RX macro, including digital correlation logic. Finally, the proposed scheme results to be an extremely flexible FEXT compensation scheme, which can be adapted for different single-ended boards.

V. CONCLUSION

In this paper, we reported an eight-lane single-ended RX circuit for source-synchronous links for high-loss channels affected by FEXT. Each lane performs ISI equalization and FEXT cancellation based on a CTXC and 7×8-taps DFXC ensuring robust operation. Unlike the previous literature [13], [16], where crosstalk cancellation schemes were tested on channel with moderate insertion loss, the proposed RX macro can equalize both a 30-dB insertion loss single-ended channel with a signal-to-crosstalk ratio of 0 dB from the nearest lanes at Nyquist, and a channel with 28 dB attenuation and reflections due to via stubs with the signal-to-crosstalk ratio of 6 dB.

TABLE IV
COMPARISON OF EIGHT LANES × 7-Gb/s RX MACRO WITH PRIOR ART

Reference	[16]	[13]	[20]	[14]	**This work**	
XTC type	CTXC	Rx passive SC	TX FIR	CTXC	CTXC, 7x8 DFXC	
I/O type	Single-ended	Differential	Single-ended	Single-ended	Single-ended	
Multi-channel num.	2	2	2	4	8	
Data-rate (Gb/s)	6	15	7	12	7	
Channel Attenuation	9 dB	14.5 dB	N/A	11 dB	30 dB	28 dB
Signal-to-Crosstalk ratio	N/A	1 dB	N/A	0 dB	0 dB	6 dB
Eq. power (pJ/bit/lane)	2.4	0.033	N/A	0.96	8 (full RX)	
process node	130 nm	45 nm SOI	40 nm	65 nm	32 nm SOI	
area (mm^2/lane)	0.03	N/A	N/A	0.036	0.012	

The crosstalk reduction strategy can be used across a variety of channels with different crosstalk patterns, due to board geometry. This trend demonstrated with measurements showed good agreement with a system-level analysis. Interestingly, it has been shown how the vertical eye opening improves by increasing CTLE peaking even with severe crosstalk. Moreover, it has been demonstrated that the first 2–4 DFXC taps are sufficient to reduce the crosstalk even in the presence of skew between lanes in the channel bundle.

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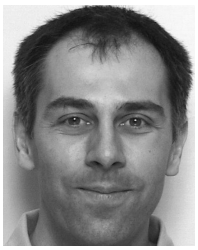

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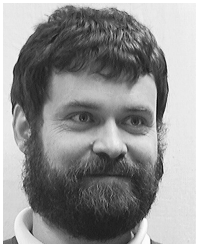

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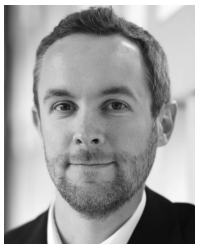

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