Analysis of Power Consumption in LC Oscillators based on the Inversion Coefficient

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***Abstract*—This paper carries out a power-driven performance analysis on the most widely used LC oscillators' topologies, by means of the Inversion Coefficient methodology. The aim is to investigate on the best trade-off for Internet-of-Things related applications, where power consumption shall be minimized. The analysis is based on the BSIM6 model targeting a 40nm CMOS technology to investigate the trade-offs related to each topology and comparing them with respect to output voltage amplitude, phase noise and power consumption. The comparison is based on a figure-of-merit highlighting the best biasing regions, in terms of Inversion Coefficient, for the target required performance.**

***Index Terms*—Internet of Things, LC oscillators, low-power, inversion coefficient**

I. Introduction

THE "Internet of Things" (IoT) has started to evolve from an abstract and appealing concept to a real and promising opportunity to set the biggest digital revolution after the introduction of the Internet. All portable devices will become the center of a network made of sensors and beacons spread in every other object which will allow to receive information or to control them remotely. In order to achieve this, it will be necessary to produce very power-efficient nodes, ideally able to work for years out of a coin battery cell or even less. In order to be able to communicate with the outside world, they will need ultra-low-power radios and specifically ultra-low-power frequency synthesizers.

The most power hungry block of such frequency synthesizers remains the Voltage-Controlled Oscillator (VCO), generally classified in two families: harmonic (i.e. LC-based) and relaxation oscillators (i.e. ring-based). In particular, during the last ten years, new LC-based topologies have been reported in the literature, where an increased voltage and/or current efficiency has been the result of the modifications, introduced on top of the basic structure.

In order to achieve a better efficiency, the basic LC oscillator has evolved employing differential transistors with different conduction angle or bias region. As a consequence, due to the similarities with some power amplifiers, the members of the family of harmonic oscillators have been categorized in classes as well.

In this context, this work focuses on the analysis of the basic version of three topologies, i.e. Class-B, Class-C, and Class-D (Fig. 1), since they are representative enough for understanding their pros and cons in terms of power consumption and phase noise, aiming at investigating the trade-offs and providing the best choice for IoT applications.

The paper has been organized as follows. In Section II the description of the three analyzed topologies is carried out. Section III details the conducted analysis showing the results in terms of power consumption, phase noise and comparing them by means of a figure-of-merit, followed by conclusions.

II. Description of the Topologies

A. Class-B oscillator

Fig. 1a shows a Class-B oscillator with an NMOS cross-coupled pair only, one of the best-known and widely employed topologies [1]. When the single-ended oscillation amplitude is lower than the supply voltage V_{DD} (theoretical limit), the oscillator operates in the so-called "current limited" regime. In this condition, the output differential voltage amplitude A_{diff} is set by the nonlinear characteristic of the active transistors, namely when the transconductance of the fundamental component $G_{\mathrm{m(1)}}$ matches G_{mcrit}, defined as the cross-coupled transistor's G_{m} for obtaining a zero amplitude oscillation [2]. Indeed, the fundamental component of the current is the only one not filtered out by the LC tank.

The bias current is steered from one branch to the other once per period, when the respective transistors are active: the larger the amplitude, the harder the current is steered. Since each transistor is active for approximately half a period, which means a conduction angle of 180°, this topology is called Class-B. When the amplitude reaches V_{DD}, it remains almost constant even if the bias current is increased further, making the oscillator working in the so-called "voltage limited" regime. Several variations have been studied for this topology, in order to improve the power consumption and the phase noise performance [3], [4].

B. Class-C oscillator

Fig. 1b shows a Class-C oscillator with an NMOS cross-coupled pair only. It is pretty similar to a Class-B, but it contains two essential modifications. First of all, a large capacitor C_{tail} is connected to the source of the cross-coupled pair in parallel to the bias transistor. Secondly, the cross-coupled transistors' gates are not anymore biased at V_{DD} but at a lower voltage, through a RC net (R_{bias} and C_{bias}) which enables AC coupling of the output signal. The role of C_{tail} is to allow a more efficient generation of the current first harmonic, so that a higher oscillation amplitude can be obtained out of the same

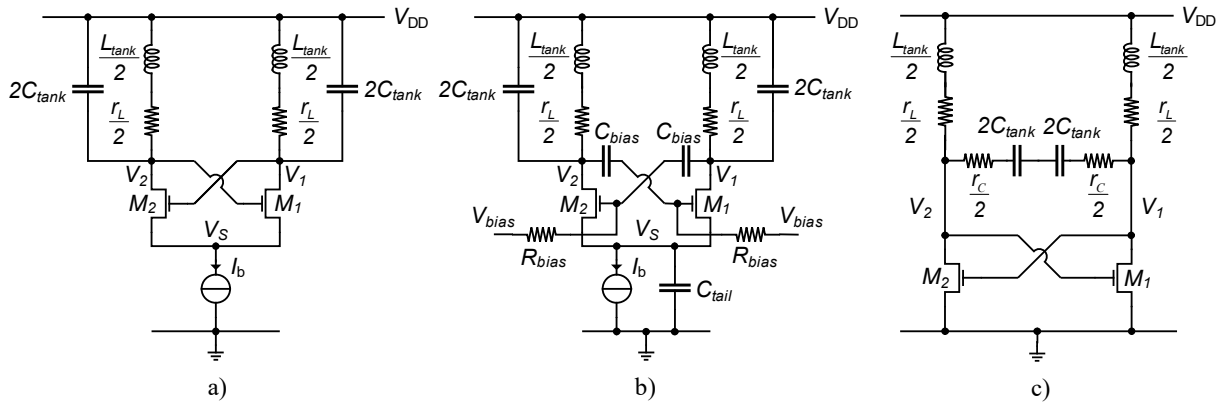

Fig. 1. Three topologies of LC oscillators: a) Class-B, b) Class-C, and c) Class-D oscillators.

bias current [5]. Indeed, it prevents the source node from swinging, providing sharp current spikes at the peak of voltage swing [6]. The current waveform doesn't look like a square wave anymore but it shows narrow and high pulses, since the active transistor conducts for less than half a period (conduction angle $< 180°$). This behavior gives the name to the topology. Moreover, it filters out noise at the second harmonic coming from the bias transistor, preventing it from contributing to phase noise after down-conversion around the fundamental.

$C_{\rm tail}$ alone is not enough for the oscillator to benefit from working in Class-C. As it can be observed also in Class-B, when the oscillation amplitude exceeds a given limit, the active transistor goes from saturation to triode region for a fraction of the semi-period. As a consequence, it loads the tank due to any capacitance at the source, increasing the phase noise. In Class-C this effect is even worse, because it either vanishes the benefits coming from Class-C operation or it affects the phase noise even more. In order to prevent it, the active transistor must not leave the saturation region or, at least, must not go in deep triode region. This is obtained by lowering its overdrive voltage, biasing the gate below $V_{\rm DD}$ and accepting a reduction of the maximum achievable differential oscillation amplitude $A_{\rm diff}$, which depends on the chosen bias voltage. Unfortunately, the implementation of Class-C oscillators suffers from a trade-off between start-up robustness and maximum oscillation amplitude in steady-state condition.

C. Class-D oscillator

Fig. 1c shows a Class-D oscillator, whose behavior is quite different from the previous two topologies, since it is even more nonlinear. Indeed, the bias transistor has been removed forcing the oscillator to work in the "voltage controlled" regime instead of the "current controlled". The oscillation amplitude is set by $V_{\rm DD}$ and it is allowed to peak well above boosting the voltage efficiency ($A_{\rm diff}/V_{\rm DD}$), while the current consumption depends either on $V_{\rm DD}$ or on the tank losses [7]. Moreover, the differential transistors don't work anymore as transconductors but as switches: when active they are in triode region, since their gate voltage is close to $V_{\rm DD}$ and the drain voltage falls to ground. Due to this behavior the oscillator has been classified as Class-D.

As a whole, the circuit is very simple and it can benefit a lot from device scaling due to improved switching performance. Since the output nodes are ideally shorted to ground during half of the oscillation period, the inductor and the capacitance are not in parallel for the same amount of time. For this reason, the tank has a time-variant nature, differently from the two previous topologies, and the oscillation frequency cannot be predicted by the standard tanks formula. Moreover, the oscillation frequency is different whether the capacitance is differential or single-ended. Finally, the equivalent parallel resistance approximation is not valid anymore, so the losses of the capacitor and of the inductor (r_C and r_L) have to be separately taken into account.

III. LC Oscillators Topologies Analysis

A. The Inversion Coefficient Methodology

In order to address the requirements imposed by IoT applications, especially in terms of power budget, in this paper the Inversion Coefficient (IC) has been used as the driving parameter for the forthcoming analysis. This is mainly due to the capability to investigate the performance of CMOS transistors in all the regions of operation, to be identified through the value of IC itself. Indeed, the definition of Weak, Moderate and Strong Inversion (WI, MI, SI respectively) is straightforward through IC, as described in [8]: WI corresponds to $IC \leq 0.1$, MI to $0.1 < IC < 10$ and SI to $IC \geq 10$.

Table I shows the parameters which have been kept constant throughout the analysis in order to get a fair comparison among the three topologies. A commercial 40 nm bulk CMOS technology has been chosen, whose model card for BSIM6 model has been extracted with ICCAP starting from DC, CV, RF and RF noise measurement data [9]. ADS has been used as simulator. The value of $C_{\rm tank}$ has been tuned by simulation to match 1 GHz precisely, in order to take into account the contribution of the parasitic capacitances of the differential transistors $C_{\rm par} = (4C_{GD} + C_{GS} + C_{GB})/2$, which change depending on their width and bias region.

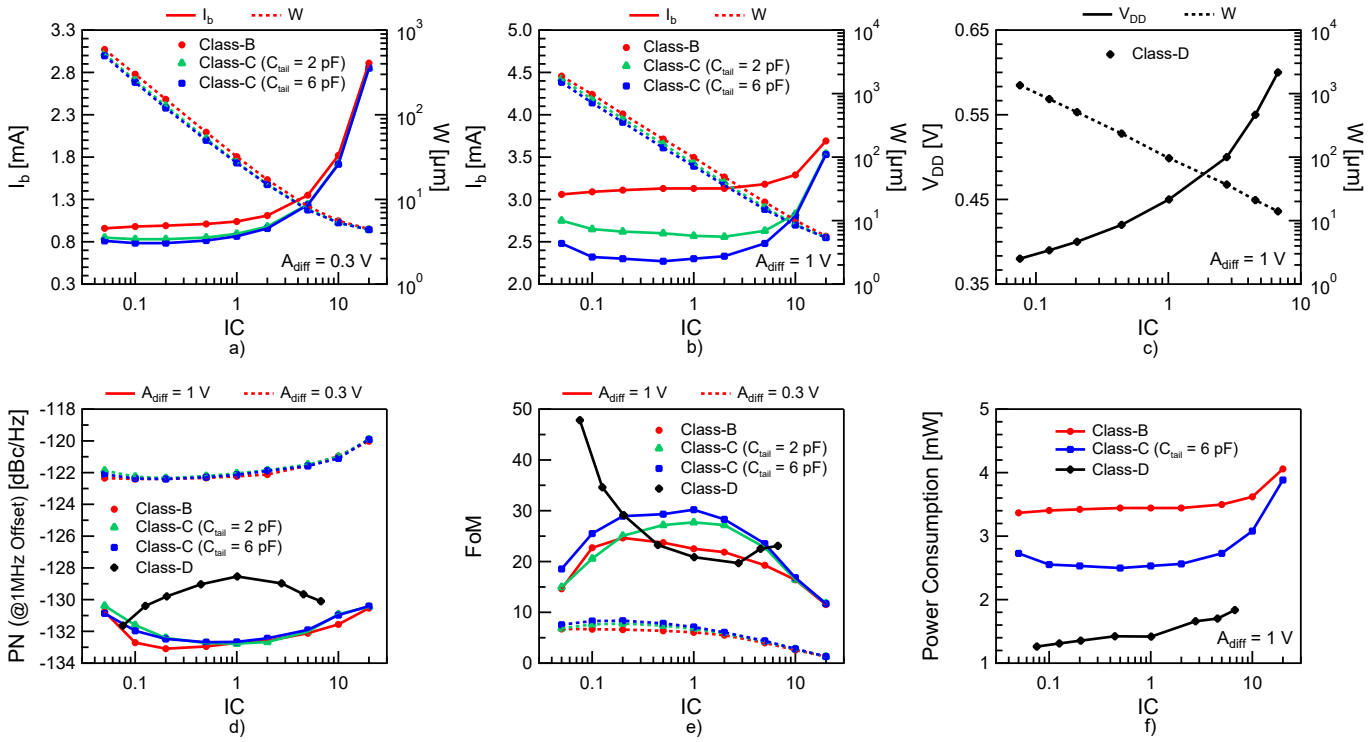

Fig. 2. Comparison between LC oscillators vs. IC: a) I_b and W for Class-B and Class-C ($A_\mathrm{diff} = 300\,\mathrm{mV}$); b) I_b and W for Class-B and Class-C ($A_\mathrm{diff} = 1\,\mathrm{V}$); c) V_DD and W for Class-D ($A_\mathrm{diff} = 1\,\mathrm{V}$); d) Phase noise @1 MHz carrier offset for Class-B, Class-C and Class-D; e) FoM for Class-B, Class-C and Class-D; f) Power consumption for Class-B, Class-C, and Class-D.

TABLE I
DESCRIPTION OF SIMULATION PARAMETERS

Parameter	Value	Formula
L_ch	40 nm	
$I_{\mathrm{spec}\square}$	650 nA	
f_0	1 GHz	
L_tank	8 nH	
Q_L	10	
r_L	5 Ω	$2\pi f_0 L_\mathrm{tank}/Q_L$
W/L		$I_b/\left(2\,IC\,I_{\mathrm{spec}\square}\right)$
C_tank	3.13 pF	$1/\left[(2\pi f_0)^2 L_\mathrm{tank}\left(1+1/Q_L^2\right)\right]$

B. Analysis of Class-B and Class-C oscillators

Two sets of simulation have been carried out: one having as a target a differential oscillation amplitude A_diff of 300 mV and another with 1 V. For the Class-C oscillator, the simulation has been done with two values of C_tail: 2 pF and 6 pF, which are both within the limit to avoid *squegging* since C_tank is around 3 pF [5]. Moreover, V_bias has been set for each IC to the minimum value which would guarantee a sufficient voltage headroom to the current source. Fig. 2a and 2b show the bias current I_b and width of the differential transistors W needed for reaching the above-mentioned amplitudes respectively depending on IC.

A general trend can be identified for both topologies at different A_diff values, i.e. an overall reduction of current when moving from SI to MI and WI at the cost of an exponential increase of the area (W). A reasonable trade-off is then experienced in MI, where IC is close to unity. In particular, for $A_\mathrm{diff} = 300\,\mathrm{mV}$, I_b increases slightly between WI and MI, while it starts rising fast going MI to SI. The Class-C current consumption decreases with increasing C_tail as expected due to the improved efficiency; it shows around 20% improvement with respect to Class-B with $C_\mathrm{tail} = 6\,\mathrm{pF}$ in WI and MI, while in SI there is not appreciable difference.

For $A_\mathrm{diff} = 1\,\mathrm{V}$, the increase of I_b shows up only going in deep SI, and there is a minimum around MI for Class-C. The lower increase of I_b in Class-B is due to the fact that the relation between I_b and A_diff, which comes from the nonlinear behavior of the oscillator, depends strongly on IC only at small A_diff, while it converges to the asymptotic value valid for WI for large A_diff [2]. The improvement in current consumption going from Class-B to Class-C is more evident in this case for all IC values.

As far as phase noise (PN) is concerned, its value at 1 MHz offset from the carrier frequency has been reported in Fig. 2d in order to check how it varies across IC and topology. This work focuses on far-out PN: it has been verified by simulation that the corner frequency f_{1/f^3} is lower than 1 MHz in all cases. Only a slight increase is noticed going from deep WI to deep SI, around $1.5-2\,\mathrm{dBc/Hz}$, and also between Class-B and Class-C. The difference between $A_\mathrm{diff} = 300\,\mathrm{mV}$ and 1 V cases, $\sim 10\,\mathrm{dBc/Hz}$, is due to the PN dependence on $1/A_\mathrm{diff}^2$.

As a result of the previous analysis, a unitless Figure of Merit FoM, defined as:

$$FoM = \frac{kT}{\mathcal{L}(\Delta f, IC)\, P_{DC}(IC)} \left(\frac{f_0}{\Delta f}\right)^2, \qquad (1)$$

which includes power and phase noise, has been plotted in Fig. 2e [10]. It shows that the FoM is maximum when biasing the differential transistors in WI for both topologies at small A_{diff}, while this remains valid at larger A_{diff} only for Class-B, while Class-C FoM has a peak around MI.

C. Analysis of Class-D oscillator and comparison with Class-B and Class-C

In order to carry out a fair comparison in terms of power consumption among the three oscillator topologies, some parameters have to be kept constant and particularly the differential oscillation amplitude A_{diff}. Moreover, also the IC has to be changed, setting it accordingly to the width of the differential transistors. In Class-B and Class-C the I_{b} is imposed with a current source, which allows to play with IC easily. On the other hand, in Class-D A_{diff} is determined by V_{DD} but the expression of I_{b} for all regions of operation as a function of terminal voltages is quite complex to handle. Nevertheless, a slight dependence of A_{diff} on W has been noticed, since it changes the channel resistance when in triode region. This effect has allowed to find different combinations of V_{DD} and W which result in the target $A_{\text{diff}} = 1\,\text{V}$. It has not been possible to get $A_{\text{diff}} = 300\,\text{mV}$ as well, since it would have required a too small V_{DD} for the oscillation to start.

Notice that some of these points are shown only for the sake of comparison, even if they are not practical: W is quite small, which results in a large channel resistance, risking to vanish the benefits of Class-D and to obtain long start-up time in a real circuit. A differential capacitance configuration has been used, since it has been shown that it provides better results in terms of frequency, power consumption and phase noise with respect to its single-ended counterpart [7]. Moreover, the inductor has been assumed to have the lower quality factor and its losses to dominate over those of the capacitance.

Fig. 2c shows the values of V_{DD} and W chosen to get $A_{\text{diff}} = 1\,\text{V}$. As the power supply gets lower, the differential transistors have to be biased more and more in WI in order to meet the specification, becoming wider and wider. As a consequence, the DC component of the current varies only slightly with IC. This is coherent with the expression of the current consumption for this topology found in [7] since at the same time V_{DD} is decreased and the tank quality factor is affected negatively by the higher channel resistance, causing an increase of the overall tank losses. Asymptotically, IC depends quadratically on V_{DD}, which is the gate voltage at DC, in SI. In fact, the DC current is kept almost constant (3.1-3.3 mA) by reducing W accordingly, and it depends exponentially on V_{DD} in WI. This trends can be identified in Fig. 2c.

As far as PN of Class-D is concerned, its value at 1 MHz offset from the carrier frequency has been reported in Fig. 2d. Compared to Class-B and Class-C, Class-D has a worse performance, due to the difficulty to guarantee the same losses for the tanks of the three topologies. Indeed, in the latter the differential transistors channel resistance loads directly the tank. In detail, the larger it is, the more severely the quality factor is affected. This effect is limited in WI where the W is very large, but it emerges toward MI. The reason for the phase noise to decrease again going in SI is that the increase of V_{DD} prevails on the decrease of Q_L and/or increase of noise factor, as deduced by the PN formula shown in [7].

The FoM of Class-D defined in (1) has been plotted in Fig. 2e. This topology allows for a somewhat higher FoM in WI with respect to the others, but, due to PN degradation, in MI and SI the Class-D performs worse. Nevertheless, even if the FoM is an useful parameter to compare different designs, it doesn't imply that having a good value means that all the specifications are met singularly. So, the power consumption by itself has been plotted in Fig. 2f. The progressive improvement going from Class-B to Class-C and Class-D for all regions of functioning, especially for WI, is then obvious.

IV. Conclusion

The goal of this work is to understand which LC oscillator topology gives the lowest power consumption to get a given amplitude at a given frequency without spoiling the phase noise performance. In this perspective, Class-B, Class-C and Class-D oscillators have been analyzed. Their bias current, supply voltage, width and phase noise have been simulated as a function of the inversion coefficient of the cross-coupled transistors. In order to quantify their overall performance, a FoM has been considered, showing that depending on IC, Class-D shows the best behavior in WI, while Class-C in MI. Nevertheless, comparing the power consumption, Class-D clearly is the less power-hungry for any IC value, taking advantage of the reduced supply voltage. MI is the best trade-off between power and area for Class-B and Class-C, while the region between WI and MI is the best one for Class-D.

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