Field Plate Design for Low Leakage Current in Lateral GaN Power Schottky Diodes: Role of the Pinch-Off Voltage

Jun Ma, Dante Colao Zanuz, and Elison Matioli, *Member, IEEE*

***Abstract*—In this work we demonstrate a general model to reduce the reverse leakage current (I_R) in high-voltage AlGaN/GaN Schottky diodes (SBDs) by engineering the pinch-off voltage (V_p) of their field plates (FPs). The maximum voltage drop at the Schottky junction (V_{SCH}) in OFF state can be significantly decreased by reducing $|V_p|$, which leads to a drastically diminished I_R. We used a tri-gate architecture as means to control the V_p and thus the I_R, as it offers great flexibility to engineer the V_p compared to conventional schemes. The $|V_p|$ of SBDs with tri-gate FPs was reduced by decreasing the width of the nanowires, which led to a very small I_R, below 10 nA/mm under reverse biases up to 500 V, and an increase of over 800 V in soft breakdown voltage (V_{BR}) at 1 µA/mm. These results reveal the importance of the V_p in reducing the I_R for SBDs, and unveil the potential of tri-gate structures as FPs for power devices.**

***Index Terms* - GaN, field plate, Schottky diode, breakdown, leakage current, tri-gate.**

I. Introduction

Lateral AlGaN/GaN SBDs are very promising for power conversions, offering excellent properties for high-voltage, high-power-density and high-frequency operation [1]-[10]. In addition, these devices can be monolithically integrated with GaN high electron mobility transistors (HEMTs) on large-size silicon substrates, which is highly desirable to reduce the cost, size and parasitics for future GaN power converters.

A major obstacle for current lateral AlGaN/GaN SBDs is however their large I_R. Efficient and reliable power conversion requires devices with small I_R below 1 µA/mm or preferably 0.1 µA/mm at high blocking voltages [11], yet most of current SBDs exhibit I_R over 0.1 µA/mm at a reverse bias as small as 100 V, leading to a small V_{BR} and a large power dissipation in OFF state. While many sophisticated techniques have been proposed to address this issue, their effect is limited by parasitic leakage paths under high biases, such as thermionic field emission and trap-assisted tunneling [12]-[19].

Recently we have demonstrated tri-anode AlGaN/GaN SBDs with small I_R ($\leq$ 0.1 µA/mm at -700 V) [1]. Small I_R was also reported by J. Hu *et al.* [7] using a gated-edge termination, in which the AlGaN barrier in the FP was partially recessed. The I_R in these reports are comparable to state-of-the-art GaN transistors and much smaller than other results from lateral AlGaN/GaN SBDs in the literature [2]-[5]. Yet the physical origin of such improvement is not well understood. More importantly, a general model for the reduction of I_R is still missing, which is crucial to unleash the full potential of lateral SBDs for the next generation of power converters.

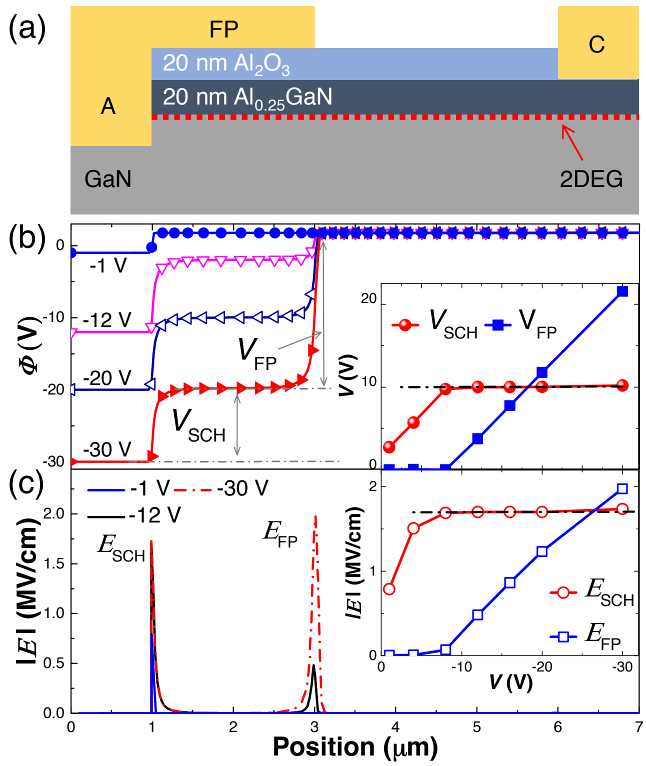

Fig. 1. (a) A cross-sectional schematic of a lateral AlGaN/GaN SBD with typical planar FP. Simulated distributions of (b) potential (Φ) and (c) electric field (E) at the channel in OFF state for different anode voltages, in which only in-plane electric field was considered. The insets show the summarized dependences of the V_{SCH} and the E_{SCH} on the anode voltage.

In this work we present a general approach to reduce the I_R in SBDs by designing the V_p of their FPs, which, in addition to explaining the improvement mentioned above, provides a pathway for high-performance lateral GaN power Schottky diodes. A reduction of $|V_p|$ results in a decreased V_{SCH} in OFF

J. Ma, D. C. Zanuz and E. Matioli are with the Power and Wide-band-gap Electronics Research Laboratory (POWERlab), École polytechnique fédérale de Lausanne (EPFL), CH-1015 Lausanne, Switzerland. (e-mail: jun.ma@epfl.ch; elison.matioli@epfl.ch).

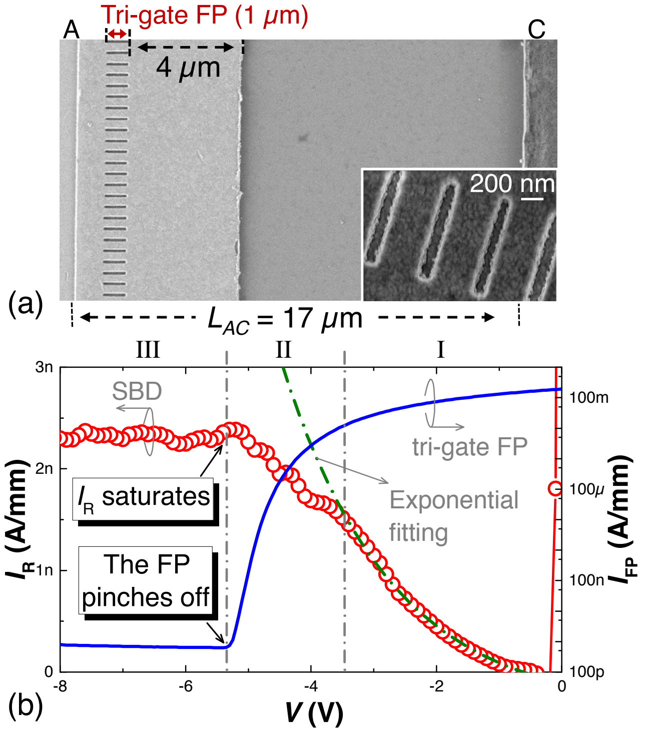

Fig. 2. (a) Top-view SEM images of the fabricated AlGaN/GaN SBD with a tri-gate FP. (b) I_R of the SBDs and the pinch-off characteristic of the tri-gate FPs as a function of the voltage. All characteristics were averaged from about 8 devices of the same kind and normalized by their total width of 60 µm. The turn-ON voltage (V_{ON}) of these SBDs was 0.9 ± 0.1 V, extracted at a forward current of 1 mA/mm.

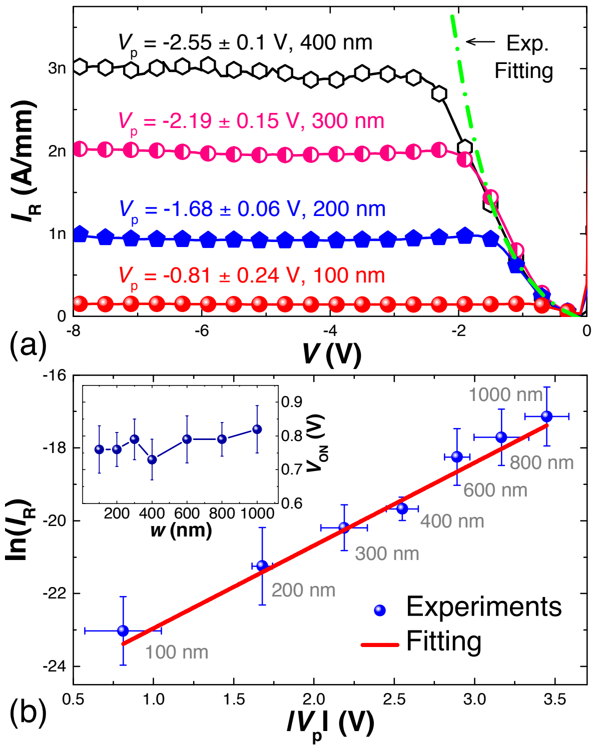

Fig. 3. (a) Comparison of the I_R in hybrid tri-anode SBDs with different w and thus different V_p. (b) A linear fitting of the ln(I_R) at -10 V and the |V_p|. The inset shows the V_{ON} of these devices as a function of w. The spacing between nanowires in these devices was 200 nm. I_R was normalized by their total width of 60 µm (the width of the device footprint) and the error bars were determined from about 8 devices of each kind.

state and correspondingly a smaller I_R. To verify the model, we used a tri-gate structure to reduce the |V_p| in AlGaN/GaN SBDs, which resulted in very small I_R, below 10 nA/mm at -500 V, along with an enhancement over 800 V in V_{BR}.

II. Model and Methodology

The I_R in SBDs is determined by three components: 1. Leakage by thermionic emission, which comprises the I_R of an ideal SBD; 2. Thermionic field emission, tunneling and other similar non-ideal effects ($I_{FE,T}$), which dominate the I_R in real devices [12]-[19]; 3. Leakage through buffer layers, which is negligible under low voltages for SBDs on high-resistivity buffer layers. Many sophisticated schemes have been proposed to reduce the $I_{FE,T}$ by reducing defects and traps [20]-[23], yet the I_R is still large in most of GaN-on-silicon SBDs. This is likely due to the high electric field under large reverse biases and also the high defect density in GaN on silicon [24]-[26].

However, $I_{FE,T}$ is not only determined by the density and energy levels of the traps, but also increases with the voltage drop at the Schottky junction (V_{SCH}) (or the electric field (E_{SCH})). In this work we propose an approach to reduce the V_{SCH} and E_{SCH} by reducing the |V_p| of the FPs, which in addition to reducing the I_R also increases the V_{BR} of the SBDs. To illustrate the principle, we simulated the distribution of potential (Φ) and electric field (E) in a typical SBD with a recessed anode and a conventional planar FP in OFF state (Fig. 1), using ATLAS SILVACO. When the reverse bias in the anode is smaller than |V_p|, which in this case is about 10 V (extracted by simulating a transistor with the FP as the gate), the voltage drops only at the Schottky junction (inset of Fig. 1(b)). As the reverse bias reaches |V_p|, the FP depletes the channel beneath and the voltage starts to drop at the cathode-side edge of the FP, resulting in a second peak of electric field. Then V_{SCH} saturates at |V_p|, regardless of further increase of the bias, as summarized in the insets of Figs. 1(b) and (c), respectively. These results agree well with Refs. [27] and [28], and suggest that the FP can be used to control the I_R in SBDs, as a smaller |V_p| reduces the maximum V_{SCH} and E_{SCH} at the Schottky junction and hence diminishes the I_R.

To reduce the |V_p|, a few ways can be adopted including a partial recess of the AlGaN barrier layer and so on. However, a precise control to obtain a series of V_p with these methods is very challenging, which makes them less suited to explore the |V_p| dependence of the I_R. Here we used a tri-gate structure to reduce the |V_p| [29], [30], as it offers great control to tune the V_p by changing the width of the nanowires (w) in the tri-gate. We implemented tri-gate FPs in SBDs for both conventional recessed anodes and novel tri-anodes [1] to justify our approach, and compared them with other literature results to show the generality of the model.

The fabrication of all SBDs in this work started with e-beam lithography to define the nanowires and the mesa, which were later etched using inductively coupled plasma with a depth of ~160 nm, followed by the formation of ohmic contacts in the cathode region. Then 20 nm of Al_2O_3 was deposited by atomic layer deposition as the FP oxide, which was selectively removed in part of the anode region to form the Schottky contact. Finally Ni/Au was deposited as the anode and then used

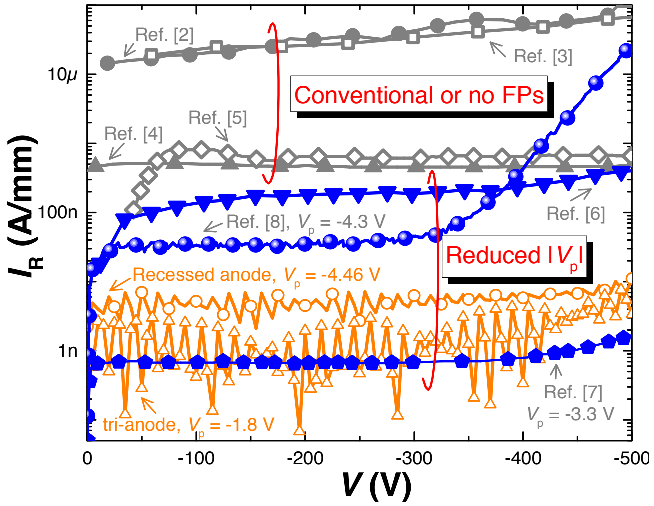

Fig. 4. Comparison of I_R from AlGaN/GaN-on-silicon SBDs with various FP designs.

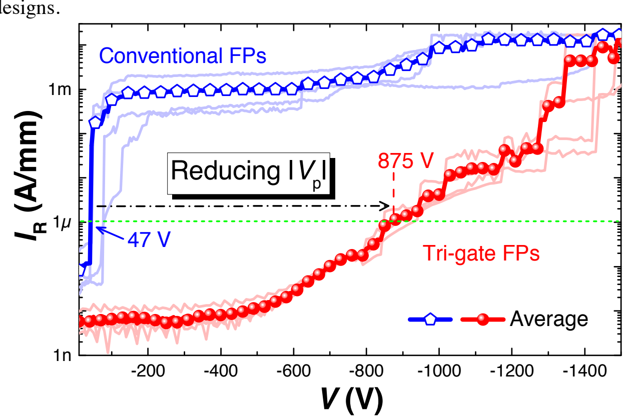

Fig. 5. Breakdown characteristics of the SBDs with and without the tri-gate

as the mask to remove the oxide in access regions by wet etching. All SBDs shared similar device dimensions such as a cathode-to-anode separation (L_{AC}) of 17 μm and a total device width of 60 μm.

III. Results and Discussion

In the model presented in Section II, the I_R should saturate when the V_{SCH} is pinned after the pinch-off of the FP. To verify this, we compared the I_R of an SBD and the pinch-off characteristics of its FP (Fig. 2). The SBD had 1 μm-long tri-gate FPs (Fig. 2(a)), in which the w and the spacing of the nanowires were 300 nm and 200 nm, respectively. These SBDs had recessed anodes with a recess depth of ~160 nm. The average pinch-off characteristic of the tri-gate FPs, shown in Fig. 2(b), was determined from transfer characteristics of tri-gate GaN MOSHEMTs on the same chip at V_{DS} of 5 V. The nanowires in the MOSHEMTs had a w of 300 nm with a length of 700 nm. As shown in Fig. 2(b), I_R increases exponentially with the reverse bias in Region I, which is dominated by $I_{FE,T}$. As the FP starts to pinch off the channel, the increase of I_R slows down (Region II). Finally I_R saturates as the FP completely pinches off the channel (Region III), agreeing well with our model.

To demonstrate the dependence of the I_R with the $|V_p|$, we studied tri-anode SBDs [1], since their $|V_p|$ can be reduced by decreasing the w of the tri-anode (which are basically tri-gate HEMTs without the oxide). Figure 3(a) shows the I_R of tri-anode AlGaN/GaN SBDs with different w, thus different V_p, which follow a similar exponential increase before the pinch off of their FPs and then saturate as V reaches V_p. As $|V_p|$ decreases for narrower nanowires, the saturated I_R diminishes due to the reduced V_{SCH}. This reduction of I_R is not likely caused by the change of the Schottky barrier height, as we observed little dependence of the V_{ON} on the w (the inset of Fig. 3(b)). Figure 3(b) shows a linear relationship of the $ln(I_R)$ with $|V_p|$, due to the exponential increase of I_R before the pinch off of the FPs (Fig. 3(a)). Such linear dependence was not affected by the choice of normalization of the I_R (either by device width, effective device width or number of nanowires).

The reduction of I_R with $|V_p|$ can be generally applicable to devices with different approaches to tune the pinch-off voltage, not only to tri-anode SBDs. For instance, a reduced $|V_p|$ was achieved by recessing the AlGaN barrier in the FP [7] or by thinner FP oxide [31], both of which led to a significant reduction of I_R. The I_R from state-of-the-art AlGaN/GaN-on-silicon SBDs with different FP designs were compared in Fig. 4. SBDs with no FPs or conventional FPs (grey) exhibited large I_R beyond 0.1 μA/mm at very small biases, while the I_R was much smaller in SBDs with reduced $|V_p|$ by either AlGaN recess (blue) or tri-gate FPs (orange). This observation from different groups in the literature supports our model correlating small I_R with small $|V_p|$, despite the different fabrication process and epi-layers.

One crucial benefit of the reduced I_R by decreasing the $|V_p|$ is the enhanced soft V_{BR}. Conventional FPs are usually based on oxide/AlGaN/GaN structures (Fig. 1(a)), which have large negative V_p due to the high carrier concentration in the 2DEG and charges in the oxide. This leads to a large V_{SCH}, causing the I_R to increase rapidly to 1 μA/mm (at which the V_{BR} is typically defined), and resulting in a very small V_{BR}. As the $|V_p|$ is reduced, the leakage current through the Schottky junction saturates at smaller levels, until it is dominated by the highly resistive buffer layers at larger voltages, rather than only by the leaky Schottky junction. This leads to a significantly improved V_{BR}, which is over 800 V in our case (Fig. 5).

IV. Conclusion

In this work we presented a general approach to reduce the I_R in SBDs by reducing the $|V_p|$ of their FPs, which led to ultra-low I_R below 10 nA/mm at -500 V and enhanced the V_{BR} by over 800 V. These results revealed the importance of a proper FP design for reducing the I_R in SBDs, unveiled the significant potential of the tri-gate FPs, and can potentially pave the path for efficient lateral SBDs for future power applications.

References

[1] J. Ma and E. Matioli, "High-voltage and low-leakage AlGaN/GaN tri-anode Schottky diodes with integrated tri-gate transistors," *IEEE Electron Device Lett.*, vol. 38, pp. 83-86, Jan. 2017. doi: 10.1109/LED.2016.2632044.

[2] C. -W. Tsou, K. -P. Wei, Y. -W. Lian, and S. S. H. Hsu, "2.07-kV AlGaN/GaN Schottky barrier diodes on silicon with high Baliga's Figure-

of-Merit," *IEEE Electron Device Lett.*, vol. 37, pp. 70-73, Jan. 2016. doi: 10.1109/LED.2015.2499267.

[3] Y. -W. Lian, Y. -S. Lin, J. -M. Yang, C. -H. Cheng, and S. S. H. Hsu, "AlGaN/GaN Schottky barrier diodes on silicon substrates with selective Si diffusion for low onset voltage and high reverse blocking," *IEEE Electron Device Lett.*, vol. 34, pp. 981-983, Jul. 2013. doi: 10.1109/LED.2013.2269475.

[4] M. Zhu, B. Song, M. Qi, Z. Hu, K. Nomoto, X. Yan, Y. Cao, W. Johnson, E. Kohn, D. Jena, H. G. Xing, "1.9-kV AlGaN/GaN lateral Schottky barrier diodes on silicon," *IEEE Electron Device Lett.*, vol. 36, pp. 375-377, Feb. 2015. doi: 10.1109/LED.2015.2404309.

[5] J. -G. Lee, B. -R. Park, C. -H. Cho, K. -S. Seo, and H. -Y. Cha, "Low turn-on voltage AlGaN/GaN-on-Si rectifier with gated ohmic anode," *IEEE Electron Device Lett.*, vol. 34, pp. 214-216, Jan. 2013. doi: 10.1109/LED.2012.2235403.

[6] S. Lenci, B. D. Jaeger, L. Carbonell, J. Hu, G. Mannaert, D. Wellekens, S. You, B. Bakeroot, and S. Decoutere, "Au-free AlGaN/GaN power diode on 8-in Si substrate with gated edge termination," *IEEE Electron Device Lett.*, vol. 34, pp. 1035-1037, Jul. 2013. doi: 10.1109/LED.2013.2267933.

[7] J. Hu, S. Stoffels, S. Lenci, B. D. Jaeger, N. Ronchi, A. N. Tallarico, D. Wellekens, S. You, B. Bakeroot, G. Groeseneken, and S. Decoutere, "Statistical analysis of the impact of anode recess on electrical characteristics of AlGaN/GaN Schottky diodes with gated edge termination," *IEEE Trans. Electron Devices*, vol. 63, pp. 3451-3458, Jul. 2016. doi: 10.1109/TED.2016.2587103.

[8] J. Hu, S. Stoffels, S. Lenci, B. Bakeroot, B. D. Jaeger, M. V. Hove, N. Ronchi, R. Venegas, H. Liang, M. Zhao, G. Groeseneken, and S. Decoutere, "Performance optimizaiton of Au-free lateral AlGaN/GaN Schottky barrier diode with gated edge termination on 200-mm silicon substrate," *IEEE Trans. Electron Devices*, vol. 63, pp. 997-1004, Jan. 2016. doi: 10.1109/TED.2016.2515566.

[9] E. Matioli, B. Lu, and T. Palacios, "Ultralow leakage current AlGaN/GaN Schottky diodes with 3-D anode structure," *IEEE Trans. Electron Devices*, vol. 60, pp. 3365-3370, Sep. 2013. doi: 10.1109/TED.2013.2279120.

[10] J. Ma, G. Santoruvo, P. Tandon, and E. Matioli, "Enhanced electrical performance and heat dissipation in AlGaN/GaN Schottky barrier diodes using hybrid tri-anode structure," *IEEE Trans. Electron Devices*, vol. 63, pp. 3614-3619, Jul. 2016. doi: 10.1109/TED.2016.2587801.

[11] B. Lu, D. Piedra and T. Palacios, "GaN power electronics," *The Eighth International Conference on Advanced Semiconductor Devices and Microsystems*, Smolenice, 2010, pp. 105-110. doi: 10.1109/ASDAM.2010.5666311.

[12] S. Turuvekere, N. Karumuri, A. A. Rahman, A. Bhattacharya, A. DasGupta and N. DasGupta, "Gate Leakage Mechanisms in AlGaN/GaN and AlInN/GaN HEMTs: Comparison and Modeling," *IEEE Trans. Electron Devices*, vol. 60, pp. 3157-3165, Oct. 2013. doi: 10.1109/TED.2013.2272700.

[13] S. Oyama, T. Hashizume, and H. Hasegawa, "Mechanism of current leakage through metal/n-GaN interfaces," *Appl. Surf. Sci.*, vol. 190, pp. 322-325, May 2002. doi: 10.1016/S0169-4332(01)00902-3.

[14] Y. Lei, J. Su, H. -Y. Wu, C. -H. Yang, and W. -F. Rao, "On the reverse leakage current of Schottky contacts on free standing GaN at high reverse biases," *Chin. Phys. B*, vol. 26, pp. 027105-1-027105-3, Dec. 2016. doi: 10.1088/1674-1056/26/2/027105.

[15] P. Pipinys and V. Lapeika, "Analysis of reverse-bias leakage current mechanisms in metal/GaN Schottky diodes," *Adv. Cond. Matter. Phys.*, vol. 2010, pp. 526929-1-526929-7, Jul. 2010. doi: 10.1155/2010/526929.

[16] Y. Lei, H. Lu, D. Cao, D. Chen, R. Zhang, Y. Zheng, "Reverse leakage mechaism of Schottky barrier diode fabricated on homoepitaxial GaN," *Solid State Electron.*, vol. 82, pp. 63-66, Feb. 2013. doi: 10.1016/j.sse.2013.01.007.

[17] H. Zhang, E. J. Miller, E. T. Yu, "Analysis of leakage current mechanisms in Schottky contacts to GaN and $Al_{0.25}Ga_{0.75}N$/GaN grown by molecular-beam epitaxy," *J. Appl. Phys.*, vol. 99, pp. 023703-1-023703-6, Jan. 2006. doi: 10.1063/1.2159547.

[18] D. Yan, H. Lu, D. Cao, D. Chen, R. Zhang, Y. Zheng, "On the reverse gate leakage current of AlGaN/GaN high electron mobility transistors," *Appl. Phys. Lett.*, vol. 97, no. 15, pp. 153503-1-153503-3, Oct. 2010. doi: 10.1063/1.3499364.

[19] S. Arulkumaran, T. Egawa, H. Ishikawa, T. Jimbo, "Temperature dependence of gate–leakage current in AlGaN/GaN high-electron-mobility transistors," *Appl. Phys. Lett.*, vol. 82, no. 18, pp. 3110-3112, Mar. 2003. doi: 10.1063/1.1571655.

[20] Z. H. Liu, G. I. Ng., H. Zhou, S. Arulkumaran, and Y. K. T. Maung, "Reduced surface leakage current and trapping effects in AlGaN/GaN high electron mobility transistors on silicon with SiN/Al_2O_3 passivation," *Appl. Phys. Lett.*, vol. 98, pp. 113506-1-113506-3, Mar. 2011. doi: 10.1063/1.3567927.

[21] S. K. Hong, K. H. Shim, and J. W. Yang, "Reduced gate leakage current in AlGaN/GaN HEMT by oxygen passivation of AlGaN surface," *Electron. Lett.*, vol. 44, pp. 1091-1093, Aug. 2008. doi: 10.1049/el:20081350.

[22] E. J. Miller, D. M. Schaadt, and E. T. Yu, "Reverse-bias leakage current reduction in GaN Schottky diodes by electrochemical surface tretment," *Appl. Phys. Lett.*, vol. 82, pp. 1293-1295, Feb. 2003. doi: 10.1063/1.1554484.

[23] J. K. Sheu, M. K. Lee, and W. C. Lai, "Effect of low-temperature-grown GaN cap layer on reduced leakage current of GaN Schottky diodes," *Appl. Phys. Lett.*, vol. 86, pp. 052103-1-052103-3, Jan. 2005. doi: 10.1063/1.1861113.

[24] J. Ma, X. Zhu, K. M. Wong, X. Zou, and K. M. Lau, "Improved GaN-based LED grown on silicon (111) substrates using stress/dislocationengineered interlayer," *J. Cryst. Growth*, vol. 370, pp. 265-268, May 2013. doi: 10.1016/j.jcrysgro.2012.10.028.

[25] P. Drechsel, P. Stauss, W. Bergbauer, P. Rode, S. Fritze, A. Krost, T. Markurt, T. Schulz, M. Albrecht, H. Riechert, and U. Steegmüller, "Impact of buffer growth on crystalline quality of GaN grown on Si(111) substrates," *Phys. Status Solidi A*, vol. 209, pp. 427-430, Jan. 2012. doi: 10.1002/pssa.201100477.

[26] J. Ma, Q. Zhuang, G. Chen, C. Huang, S. Li, H. Wang, and J. Kang, "Growth kinetic processes of AlN molecules on the Al-polar surface of AlN", *J. Phys. Chem. A*, vol. 114, pp. 9028-9033, Aug. 2010. doi: 10.1021/jp100084q.

[27] R. Coffie, "Analytical Field Plate Model for Field Effect Transistors," *IEEE Trans. Electron Devices*, vol. 61, pp. 878-883, Mar. 2014. doi: 10.1109/TED.2014.2300115.

[28] S. Karmalkar, M. S. Shur, G. Simin and M. A. Khan, "Field-plate engineering for HFETs," *IEEE Trans. Electron Devices*, vol. 52, pp. 2534-2540, Dec. 2005. doi: 10.1109/TED.2005.859568.

[29] J. Ma and E. Matioli, "High Performance Tri-Gate GaN Power MOSHEMTs on Silicon Substrate," *IEEE Electron Device Lett.*, vol. 38, no. 3, pp. 367-370, Mar. 2017. doi: 10.1109/LED.2017.2661755.

[30] S. Liu, Y. Cai, G. Gu, J. Wang, C. Zeng, W. Shi, Z. Feng, H. Qin, Z. Cheng, K. J. Cheng and B. Zhang, "Enhancement-mode operation of nanochannel array (NCA) AlGaN/GaN HEMTs," *IEEE Electron Device Lett.* vol. 33, pp. 354-356, Jan. 2012. doi: 10.1109/LED.2011.2179003.

[31] T. Boles, L. Xia, A. Hanson, A. Kaleta, and C. McLean, "Reverse leakage current and breakdown voltage improvements in GaN Schottky diodes", in *International Conference on Compound Semiconductor Manufacturing Technology (CS MANTECH)*, Denver, USA, May 2014.