# Ordered nanostructures on silicon substrates: from the top-down to the bottom-up

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PAR

Jelena VUKAJLOVIĆ PLEŠTINA

acceptée sur proposition du jury:

Prof. D. Damjanovic, président du jury
Prof. A. Fontcuberta i Morral, directrice de thèse
Dr Ph. Caroff, rapporteur
Prof. V. Dubrovskii, rapporteur
Prof. C.  Hébert, rapporteuse

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

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To my love and the best friend Roko and our angels Augustina and Ruđer…

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> Regrets, I've had a few
> But then again, too few to mention.

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# Abstract

Silicon is today the main material used in electronics. It is a very advanced and mature technology. It is therefore clear that new technological concepts and materials should be introduced through the integration on the silicon platform. III-V semiconductors, such as GaAs and InAs, are high performance semiconductors, with direct bandgap and high carrier mobility, what makes them very prominent candidates for future electronics and optoelectronics. Lattice, thermal and polarity mismatch have been for decades limiting their integration on Si in the form of thin film technology. The nanowire geometry brings new prospects in this direction by reducing the contact area between mismatched materials,. Now, while growth of defect-free III-V structures on silicon is important, use in applications requires the nanostructures to be placed deterministically following a certain design/order.

In this thesis we have studied different mechanisms to obtain ordered nanostructures on a silicon substrate, with the goal of increasing its functionality. The core part of this work was dedicated to the integration of III-V nanowires on Si in the form of ordered arrays. We have considered both GaAs and InAs nanowires. This process has several requirements: substrate fabrication and the growth process should be CMOS compatible, nanowires within the arrays should be grown vertically with a yield close to 100% and nanowires should be clones-looking and performing the same. An additional point to consider is that the fabrication process should be compatible with large scale techniques.

The substrate requirements for obtaining ordered arrays of Ga-assisted GaAs nanowires on silicon were identified. In particular, we focused on the initial stages of growth, that turned to be key for achieving a high yield in the arrays. We found that the positioning of the Ga droplet within the predefined holes on the substrate determined whether the nanowire would grow perpendicularly to the substrate. Our HRTEM studies on the titled nanowires show that the initial nanowire seeds seem to nucleate at the corner of the nanoscale holes. Instead, the crystal seeds of vertical nanowires occupy homogeneously the nanoscale holes. Achieving high yield in the growth of GaAs arrays on silicon also allowed us to study their evolution in time. We demonstrated that there is an incubation time for nanowires to start growing. This incubation time is different from NW to NW and leads to a relatively broad length distribution. We proposed a solution and showed how an increase in the supersaturation in the Ga droplet leads to the formation of homogeneous arrays.

Growth of InAs nanowires in ordered arrays on silicon was based on the concept of guided growth. We used a $SiO_2$ nanotube templates to promote vertical growth. Due to the directionality of MBE, achieving growth inside a nanotube was especially challenging. Our results

provided new insights on the role of different pathways of the In and $As_4$ adatoms during growth. In this part, large scale patterning by phase shift photolithography was demonstrated as an alternative to the conventionally used electron beam lithography.

Stain etching method for producing porous silicon was applied on top-bottom fabricated Si micropillars. This led to geometrically driven electrochemical dissolution of silicon trough the center of the microstructure forming microtubes. The optical properties were also studied and used to produce functional 3D light emitting device as well as 2.3% efficient solar cell.

This manuscript is structured in four chapters. In Chapter 2 the overview of fabrication techniques used for obtaining ordered arrays is presented, comparing top-down and bottom up techniques. We have focused on the VLS mechanism and on the role of the droplet. The last part of this chapter motivates the growth of nanowire arrays by introducing main applications, focusing mainly on solar cells and optoelectronic devices.

Chapter 3 presents the results of the thesis. The first part concerns the integration of GaAs and InAs nanowire arrays on silicon. The nanowires are obtained by a bottom-up process on a prepatterned substrate (top-down). The last part of the chapter presents results on the fabrication and functional characterization of ordered porous silicon microtubes. The chapter is introduced by a brief motivation and state-of-the-art section, followed by the submitted/published manuscripts.

Chapter 4 summarizes the results of the thesis and provides a brief outlook on the work.

# Résumé

Le silicium est, de nos jours, le matériau le plus largement utilisé dans le domaine de l'électronique. La technologie l'incombant est d'une maturité avancée et, dans ce contexte, il va sans dire qu'un nouveau concept ou innovant matériau doit être implémenté par une intégration sur la plateforme silicium. Les semiconducteurs III-V comme le GaAs ou le InAs possèdent une haute performance grâce à leur bandgap direct et leur haute mobilité de charges, ce qui en font d'excellents candidats pour de futurs systèmes dans le domaine de l'électronique et de l'optoélectronique. Une différence d'expansion thermique, de paramètre de maille ou encore de polarité furent, pendant des décennies, les principaux facteurs limitants de leur intégration sous forme de couche mince. La géométrie des nanofils apporte alors de nouvelles perspectives en réduisant l'aire de contact entre les différents matériaux. Mais bien que la croissance de nanostructures exempt de défauts soit importante, leur utilisation demande surtout un déterminisme contrôlé de leur position en imposant des designs/motifs.

Au fil de cette thèse nous avons étudié les différents mécanismes permettant d'obtenir des nanostructures ordonnées sur un substrat de silicium avec comme objectif l'augmentation de leurs fonctionnalités. Le cœur de ces travaux fût dédié à l'intégration de nanofils semiconducteurs III-V sur la plateforme silicium sous la forme de grilles ordonnées. Les nanofils de GaAs et d'InAs furent tous les deux étudiés. Ce procédé doit cependant remplir plusieurs conditions : D'une part la fabrication du substrat et les étapes de croissance doivent rester compatibles avec l'industrie CMOS, et d'autre part les nanofils se doivent d'être tous verticaux (ou presque) tout en restant identiques morphologiquement et fonctionnellement. Enfin, il est important de noter que les procédés de fabrication doivent rester compatibles avec une production à grande échelle (large surface).

Les conditions que doivent remplir le substrat afin d'obtenir des grilles ordonnées de nanofils de GaAs obtenus par la méthode “Ga-assisted” furent déterminées. Nous avons plus particulièrement étudié les toutes premières étapes de la croissance, qui s'avérèrent cruciales pour l'obtention de grilles fortement verticales. Une des découvertes clé fût le lien entre le positionnement des gouttes de gallium au sein de creux positionnés et la perpendicularité des nanofils. En effet, nos études HRTEM sur des nanofils inclinés montrèrent que leur graine semble germer contre les parois de ces creux positionnés, contrairement aux nanofils verticaux pour lesquels les graines occupent ces creux de manière homogène. L'obtention d'une verticalité élevée nous permit alors d'étudier l'évolution de ces grilles au cours du temps, permettant de mettre en lumière la présence d'un temps d'incubation avant la croissance de ces nanofils. Ce dernier s'avéra être différent d'un nanofil à l'autre et mener à une grande distribution

de taille. Nous proposons ici une solution et montrons comment une augmentation de la supersaturation au sein de la goutte de Ga mène à la formation de grilles homogènes.
La croissance de nanofils d'InAs en grilles ordonnées sur du silicium fût basée sur le concept de croissance guidée. Nous avons utilisé un template de nanotubes de quartz afin d'induire une croissance verticale. A cause de l'aspect fortement directionnel de la croissance MBE, l'obtention de grilles à verticalité élevée fut difficile. Nos résultats apportent une nouvelle perspective du rôle des différents chemins empruntés par les adatoms d'In et d'$As_4$ durant la croissance. Lors de cette section, le patterning à grande échelle par masque à décalage de phase est présenté comme une alternative à la lithographie par rayon d'électron conventionnellement utilisée.
La méthode "stain etching" fût utilisée pour la production de silicium poreux sur des micropillars de silicium. Une dissolution électrochimique du silicium situé au centre de ces microstructures permit alors la fabrication de microtubes. Nous avons également étudié la luminescence du silicium poreux et l'avons implémentée dans la fabrication d'éléments 3D émetteurs de lumière.
Cette thèse est organisée selon deux parties : Lors du Chapitre 1, une vision générale des différentes méthodes permettant d'obtenir des grilles à haute verticalité sera présentée, en comparant des techniques top-down et bottom-up. Notre intérêt fût centré sur la méthode VLS, et le rôle de la goutte préliminaire fût examiné avec attention. Enfin, une dernière section de ce chapitre met l'emphase sur les motivations menant à étudier la croissance de ces nanofils en grilles ordonnées en présentant plusieurs potentielles directions pour leur implémentation.
Le Chapitre 2 présente les résultats obtenus sur les grilles ordonnées de nanofils III-V et de Si. La première partie concerne les processus top-down et la mise en forme su silicium. La deuxième partie se centrera sur les procédés bottom-up permettant la croissance de structures GaAS, et enfin la troisième partie présentera les procédés bottom-up concernant les structures InAs.

# Contents

# List of abbreviations

| | |
|---|---|
| AFM | Atomic force microscope |
| EBL | Electron beam lithography |
| EDX | Energy-Dispersive X-ray |
| HAADF | High Angle Annular Dark Field |
| HRTEM | High Resolution Transmission Electron Microscopy |
| MBE | Molecular Beam Epitaxy |
| MOVPE | Metal Organic Vapor Phase Epitaxy |
| NIL | Nanoimprint Lithography |
| NWs | Nanowires |
| PSL | Phase Shift Lithography |
| RIE | Reactive ion etching |
| RHEED | Reflection High Energy Electron Diffraction |
| SAE | Selective Area Epitaxy |
| SEM | Scanning Electron Microscopy |
| TEM | Transmission Electron Microscopy |
| TPL | Triple Phase Line |
| UHV | Ultra High Vacuum |
| VLS | Vapor Liquid Solid |
| VSS | Vapor Solid Solid |
| WZ | Wurtzite |
| ZB | Zinc-blende |

# 1 Introduction

## 1.1 Miniaturization trend of technology

Almost 60 years ago Richard Feynman in his lecture under the title "There's Plenty of Room at the Bottom" has brought to the attention numerous possibilities that would rise from the ability to manipulate matter on an atomic scale. With his question: "Why cannot we write the entire 24 volumes of the Encyclopedia Britannica on the head of a pin?", he anticipated the need for different technologies that require miniaturization [1]. Six years after, Gordon Moore made a prediction that the number of transistors in a dense integrated circuit will double approximately every two years. This can be considered as a start of modern digital revolution that led to the dramatic increase in computing power, and decrease in relative cost [2]. In the last four decades, the size of complementary metal-oxide semiconductor (CMOS) chips scaled from around 10 $\mu$m down to the 10 nm, the latter the size of gates in transistors that should be commercialized this year[3]. Further miniaturization requires higher-resolution processes, but also new technological concepts and materials as the gain in functionality of the transistors will not be achieved anymore by reducing the size of transistors [4]. The electronic industry is based on the conventional top-down technology that relays on lithography and etching. One of the new concepts involves building-up the nanosized structures and devices with designed dimensions and properties, so called bottom-up construction or, simply, growth. Some examples of nanostructure achieved by bottom up approach are quantum dots, nanowires [5, 6], nanomembranes [7, 8, 9] and nanosheets [10, 11]. The work in this thesis concerns both top-down and bottom-up approaches, with the main focus on obtaining ordered arrays of III-V nanowires on silicon. The configuration of the obtained arrays would be ideal for nanowire-based solar cells and related energy harvesting applications.

## 1.2 Significance of nanowires in semiconductor research

In the last 15 years semiconductor nanowires have been the subject of many studies due to their great potential in future devices and as host for novel fundamental phenomena.

They fulfill some of the demands of upcoming technology that were mentioned above: reduced dimensionality, unique materials properties and the capability for bottom-up assembly. Nanowires can be defined as filamentary crystals, with diameters typically less than 100 nm and lengths greater than 1 $\mu$m. Their unique geometry gives rise to many interesting properties such as quantum confinement, high surface to volume ratio, optical resonances and so on. That is why, up to date, their good performance was demonstrated in very wide range of applications; eg. solar cells [12, 13, 14, 15], photodetectors [16, 17, 18], light emitting diodes [19, 20], lasers [21, 22, 23, 24, 25, 26], different types of transistors and memory devices [27, 28, 29, 30, 31, 32, 33] and advanced biological and chemical sensors [34, 35]. For reviews on the utilization of NWs in these applications, the reader can refer to Section 2.4. Moreover, small diameter of nanowires allows an eased strain relaxation when combining lattice mismatched materials in axial and radial heterostructures [36, 37]. This presents an additional advantage over planar and bulk materials, where lattice-mismatched heterostructures can only be grown as long as the strained layer is thin and below the critical layer thickness. This extends the possibilities of materials combinations, thus device engineering and their applications [38, 39, 40].

Among semiconductor nanowires, III-V nanowires hold a particular promise. Their superior electrical and optical properties, including direct bandgap and high electron mobility, make them ideal candidates for electronic and optoelectronic device applications [6, 41]. Furthermore, III-V nanowires can be grown epitaxially on Si without the formation of antiphase domain walls, antiphase defects or misfit dislocations, which will enable monolithic integration of III-V nanowire optoelectronic devices with established Si microelectronics technology [6, 41, 42, 43, 44, 45]. This important aspect will be further elaborated in Section 2.3, where we will present main challenges of integration of GaAs nanowires onto Si substrates.

Nanowire based devices can be based on a single nanowire, a finite number of interconnected nanowires or on the arrays of nanowires. Arranging NWs in ordered arrays can bring additional advantages, especially to the optical active devices (e.g. solar cells, photodetectors and light emitting diodes) due to their notable optical properties such as reduced reflectance [46, 47, 48], enhanced absorption [49, 50, 51] and spectral selectivity [52, 53, 54]. From the device fabrication point of view, the NW distribution should be found across the substrate in a deterministic manner. In general, self-assembly complicates the device architecture implementation. Different applications of nanowire arrays realized up to now will be presented in details in Section 2.4.

# 2 Fabrication of ordered nanostructures

## 2.1 Top-down and bottom-up approaches

Fabricating structures at the nanoscale level can be categorized into two distinct constructions: top-down and bottom-up. Top-down fabrication corresponds to a subtractive process in which material is removed to produce features of a controlled shape and size, starting from larger dimensions and reducing them to the required values. Bottom-up fabrication constitutes an additive process in which atoms and molecules are used to build up the desired objects, such as nanowires, or quantum dots. This approach builds upon on complex self-assembly mechanisms. The top-down process is intrinsically wasteful, so it is hard to make these technologies cost effective means of nanowire fabrication. This is specially the case for III-V semiconductors, built of scarce elements such as Ga, In and As. In the case of the Si nanowire arrays fabrication, both approaches can be used, since there are no limitations from material and related technological point of view (Si is an earth abundant material and its processing relies on very mature technology).

Despite their fundamental difference, there is a common step that both approaches should consider in order to provide ordered nanostructures. This step involves the patterning the substrate to define the sites where NWs will grow and thus the geometry of the array (size of the arrays, spacing and size of the nanostructures). For this purpose, different lithographic techniques can be employed, depending on the required spot size and exposed surface area.

In the top-down process patterning the pattern is defined in a resist that will serve as protective etching mask while bottom-up uses this step to define array of holes that will determine the position and size of nanowires. This is illustrated in Fig. 2.1. Nanowires can grow through different mechanisms what require different substrate preparation, as it will be discussed in details in the Section 2.2. In some cases, we need arrays of metal particles, that are fabricated by metal film deposition on the patterned resist followed by lift-off process, while in other the holes defined in the resist are transferred by etching into the thin dielectric layer on top of the substrate.

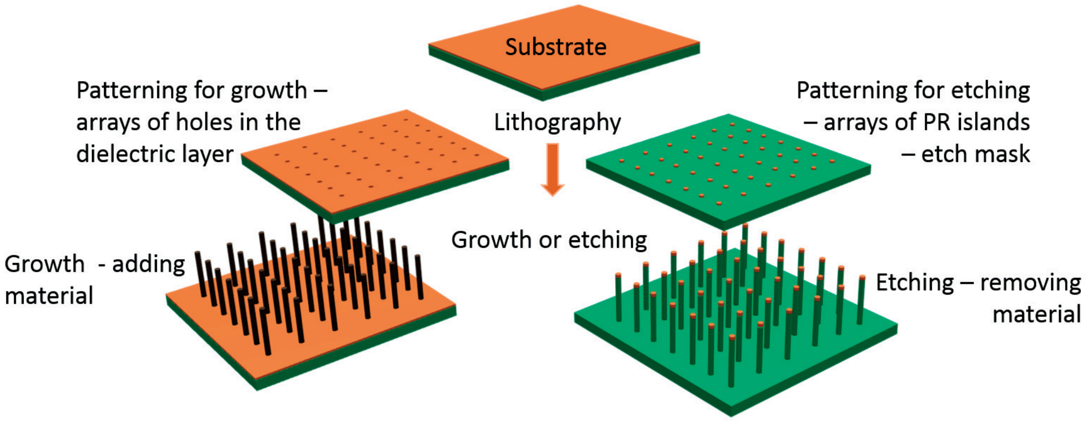

Figure 2.1 – Comparison of top down and bottom up approach for fabrication of ordered nanostructures

Here below we present a short overview of most signified patterning techniques used both for top down and for the bottom-up fabrication of ordered nanostructures and that are relevant for this thesis.

### 2.1.1 Conventional optical lithography (photolithography, PL)

This technique uses monochromatic or broad band light source to transfer a pattern from an opaque photomask to a light-sensitive layer, usually a photoresist (PR). Conventional photolithography is a simple technique that makes possible a resolution of about 1 $\mu$m using light of 400 nm [55, 56]. To achieve a better resolution, more advanced photolithography techniques have been developed in industry such as off-axis illumination, phase-shift mask, and optical proximity correction [57].

### 2.1.2 Phase shift photolithography

One of the examples of resolution enhancing photolithography for fabricating nanoscale structures is phase shift photolithography(PSL). It was employed in this thesis to define arrays of nanoscale Si pillars that were further developed into silicon oxide nanotubes. The latter served as NW growth templates [58]. Here we present the basic principle of the technique, the specific details on how it was employed in the frame of this thesis will be presented in Section 3.3. Phase shift photolithography (PSL) shares similar processes with conventional photolithography such as resist coating and baking, light exposure, resist developing [57, 59]. Fig. 2.2 shows a schematic drawing of the functioning principle of PSL. The only difference between conventional and PSL resides on the mask. A phase-shift mask (PSM) consists of a glass slide on which three dimensional structures such as ridges have been etched. Light passing through a transparent media undergoes a phase change as a function of its optical thickness [60, 61, 62]. By adjusting the thickness of the mask material, phase change of $\pi$

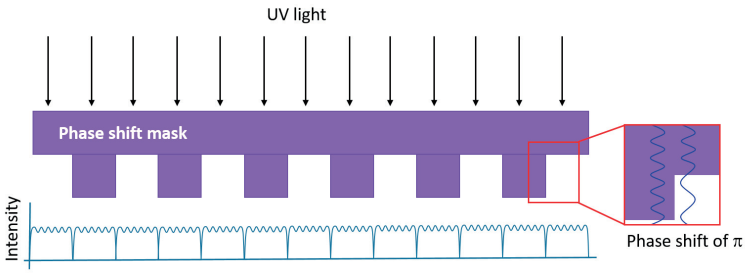

Figure 2.2 – Schematic illustration of the phase shift lithography. By adjusting the thickness of the mask material, phase shift of $\pi$ can be achieved.

can be achieved such that destructive interference is achieved. Fig. 2.2 outlines the expected profile of light intensity. In the positions of the mask ridges (phase shifters) the intensity sharply drops to zero. Depending on type of photoresist used, it is possible to transfer the corresponding slits (negative PR) or lines in the photoresist (positive PR). PSL enhances the spatial resolution of photolithography in a significant manner and enables the generation of features below 100 nm [60, 61].

### 2.1.3 Electron beam lithography (EBL)

Electron beam (e-beam) lithography is a commonly used method to define structures down to the nanoscale [63]. EBL is considered superior over conventional photolithography in terms of spatial resolution. The main advantage of EBL is that the spatial resolution is limited to the size of the interaction of the electron beam with the resist. Additionally, the electron beam writes the pattern, which can be modified at will. This mask-less form of lithography is very extended in research laboratories as it brings a lot of flexibility in the nanoscale pattern formation. Still, compared to photolithography, it has much lower throughput since the writing speed and transfer rate for the design data are limited by one or parallel beams [64]. The overall cost of this lithography is even higher for large area applications or studies. For this reason, alternatives that can replicate nanoscale patterns several times have been proposed as detailed here below.

### 2.1.4 Nanoimprint lithography (NIL)

Nanoimprint lithography is a relatively low cost, high throughput and high resolution lithographic method for the definition of advanced nanostructures. It is based on the mechanical embossing principle. A mold with nanoscale features is used to transfer the pattern by deforming a polymer. This is then cured either by heat or UV application so that the shape persists after the mold is removed. As a result the pattern stays imprinted in the resist [65, 66]. The different steps involved in the nanoimprinting process are outlined in Fig. 2.3. This method can be employed to generate patterns with resolutions superior than conventional photolithographic techniques. The resolution is comparable to EBL as most of the time the mold is

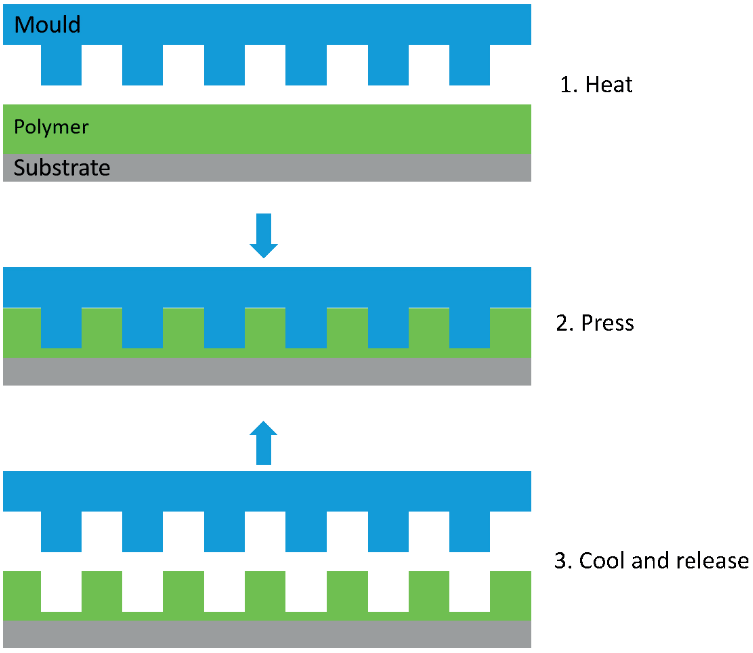

Figure 2.3 – Steps of nanoimprint lithography

defined with the help of EBL.The described patterning techniques are summarized in the Fig. 2.4.

When comparing the patterning techniques, resolution is not the only criterion that should be considered. Patterning technique should also be large scale compatible, what requires time and cost efficiency and should enable precise alignment between different lithographic levels/steps. As presented above, EBL provides impressive precision at the nanoscale, but the process is extremely time-consuming on a large scale [67]. PSL and NIL can be easily scaled up what makes them better candidates for industrial applications.

### 2.1.5 Further fabrication steps after the definition of the nanoscale pattern

After patterning, the next step that takes place in top down process is etching of the nanostructures through a mask or resist. If we are talking about patterning for nanowire growth, then the etching refers to the transferring of the nanoscale openings from the resist into the substrate. For the etching process to be efficient, the open areas in the resist should be etched selectively much faster than the resist itself, protecting the rest of the substrate. In general, there are two classes of etching processes:

1. Wet etching where the material is dissolved when immersed in a chemical solution
2. Dry etching where the material dissolved using reactive ions or a vapor phase etchant

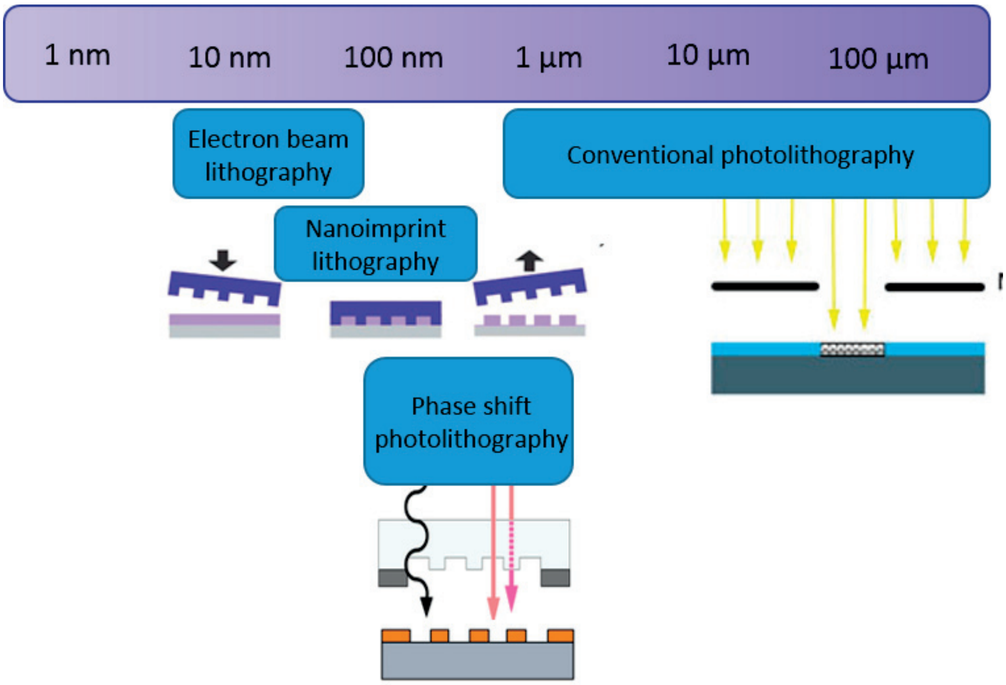

Figure 2.4 – Overview of resolutions of patterning techniques used both in top-down and bottom up approaches for arrays fabrication

### Wet etching

Wet or chemical etching is a simple process that works reasonably well for selectively etching thin films on substrates. The most typical wet etch solution for $SiO_2$ or $SiN$ is buffered hydrofluoric acid (B$HF$). It consists of a mixture of a buffering agent, such as ammonium fluoride ($NH_4F$), and hydrofluoric acid ($HF$)). One of the advantages is that it is highly selective to silicon or III-V surfaces, meaning the process will keep the rest of the substrate surface untouched. In principle this is what it makes it a good candidate for opening the holes in the dielectric layer to form a growth mask. However, its isotropic etching nature will result in undercutting of the mask by the same distance as the etch depth. As a consequence, the initial feature defined by lithography will significantly increase in size. This should be taken into account when designing the growth pattern.

### Dry etching

Contrary to wet processes, the dry etching process does not result in any undercutting. The most commonly used dry etching technique is reactive ion etching (RIE)[1]. RIE uses chemically reactive plasma to remove material from the unmasked regions of a patterned substrate. RIE

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[1] Also, vapor phase etching is classified as dry etching, but, in its nature, it is isotropic. The typical representatives of this technique are silicon dioxide etching using hydrogen fluoride ($HF$) and silicon etching using xenon diflouride ($XeF_2$).

involves chemical etching as well as physical removal of material by high energy ions that are accelerated towards the surface. This effect can introduce surface defects, which adversely affect nanostructure properties. Surface defects can be counterbalanced by further surface treatment [68]. The balance between the chemical and physical etching can be achieved by adjusting the gases ratio and is used to adjust the aspect ratio of the etched structures. Particularly, for the etching of high aspect ratio ordered structures, arrays density also plays a role. The etching of Si is usually achieved by using gas mixture of sulfur hexafluoride ($SF_6$) and Octafluorocyclobutane ($C_4F_8$ ). The latter acts as chemically inert passivation layer preventing reduction in the lateral size [69]. Beside $C_4F_8$, also mixtures of $CHF_3$ and oxygen, helium or argon can be applied. Silicon dioxide and nitride are etched with similar chemistries, just in different ratios of $SF_6$ and $C_4F_8$. RIE of III -V materials, uses two classes of gas mixtures. The first is based on chlorine chemistry, since gallium and other group III chlorides are volatile at relatively low temperatures [70]. Some of the gas mixtures used include $Cl_2$, $SiCl_4 - Cl_2$, $SiC_{14} - SF_6$, $CHC_{13}$, $COC_{12}$ and $C_{12}F_2$ combined with oxygen or argon. The second class of gas mixtures is based on methane or ethane and hydrogen and it is used for etching both gallium- and indium-based semiconductors. This non-chlorinated mixture shows controlled smooth, highly anisotropic etching of all III-V materials [71].

### 2.1.6 Bottom-up construction techniques

#### Metal-organic vapor phase epitaxy (MOVPE)

In Metal-organic vapor phase epitaxy (MOVPE) deposition occurs through the chemical decomposition of the precursors at the substrate surface In this system, group III atoms like Ga, In and Al, are provided by metalorganic while group V atoms, like As, P and Sb are provided by the hydride precursors. Because MOVPE is based on the surface enhanced chemical decomposition of precursors, substrate temperatures for typical layer growth tend to be higher than MBE. As for the latter, the sample can be rotated to obtain higher uniformity.

#### Molecular beam epitaxy (MBE)

MBE is a modern epitaxial growth technique dedicated to the epitaxy of semiconductor thin films with high purity due to the ultrahigh vacuum (UHV) of the chamber environment and purity level of the elemental growth species. In my thesis, I studied the growth of III-V nanowires using this technique. All growths were performed by a DCA P600MBE machine. The underlying principle of MBE growth can be simply explained by the following points:

1. Effusion cells (group III elements) and valved cracker cells (group V) are used to produce the molecular fluxes by heating up a solid source. Calibrations of the fluxes are performed with a beam flux monitor (BFM). The corresponding growth rate is established by reflection high-energy electron diffraction (RHEED). Here the formation of each monolayer can be determined in situ by the oscillation of intensity in the diffraction

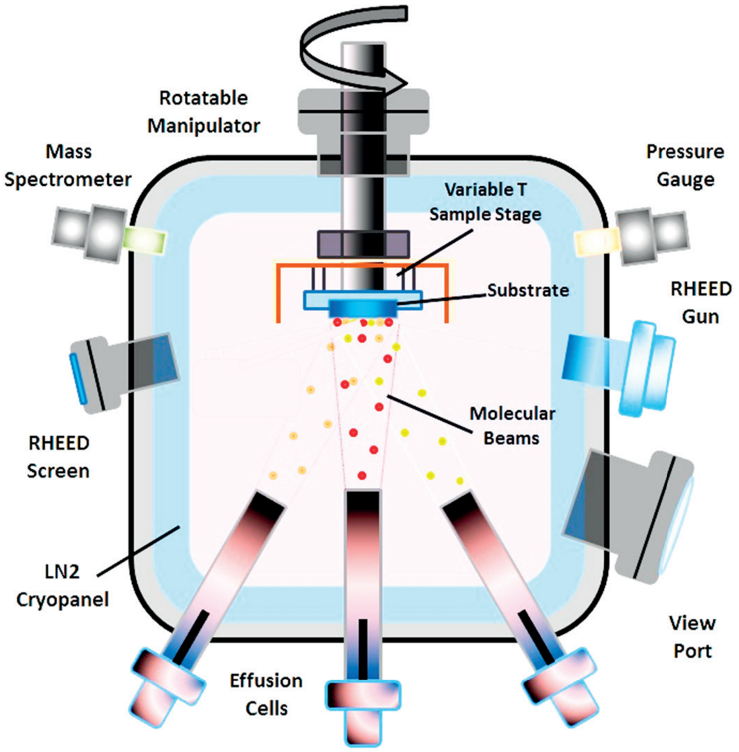

Figure 2.5 – Schematics of MBE growth chamber

spots of the crystalline surface.

2. Atomic flux is unperturbed thanks to the UHV environment and impinges on a heated substrate. The substrate temperature is set by manipulator heater and measured by pyrometer. Smooth rotation of the substrates and flux homogeneity ensure growth uniformity.
3. Thanks to the substrate temperature, ad-atoms diffuse or desorb till they get incorporated into the growing structure.

Fig. 2.5 shows the schematics of a typical MBE growth chamber with the main components indicated.

Based on the main characteristics of the two growth techniques presented so far, general comparison of their performances is summarized in the Table 2.1.

In the Section 3.3. we will discuss the new concept of so called template assisted growth that was very successfully realized by MOVPE technique. We will present our results and related challenges in adopting this idea to the MBE growth. The main difference of MBE respect to MOVPE that was considered was the UHV environment and directional beams what will be further elaborated in the Section 3.3.

Table 2.1 – Comparison of characteristics of MEB and MOVCD, adopted from Ref [72]

| MOVPE | MBE |
|---|---|
| High growth rate for bulk layers | Fast Switching for superior interfaces |
| Growth near thermodynamic equilibrium, excellent quality/crystallinity | Able to grow thermodynamically forbidden materials |
| Able to explicitly control background doping | Uniformity easier to tune, largely set by reactor geometry |

## 2.2 Nanowire growth mechanisms

Nanowire growth mechanisms can generally be summarized into two basics mechanisms: particle (catalytic) assisted growth and particle free growth where crystal growth anisotropy enhances the formation of the one-dimensional shape. Here below we describe the main points of these two main principles. One should note that crystal growth anisotropy also exists in the particle assisted growth.

### 2.2.1 Particle assisted growth — Vapor liquid solid mechanism

The most widely used method that uses a particle to promote the NW growth is the vapor-liquid-solid (VLS) mechanism. It was proposed for the first time by Wagner and Ellis in 1964 and its name reveals that the three phases are involved [73]: the Vapor (V) phase carries the precursors, constituents of the nanowire; the Liquid (L) metal catalyst gathers preferentially the vapor components forming an alloy; supersaturation of the components in the L phase results into the precipitation as solid phase (S), resulting in the one-dimensional structure. This mechanism also applies for the case where the catalyst particle is solid. In this case one refers to vapor-solid-solid mechanism (VSS). VLS method has been used to grow almost all III-V compound semiconductors including nitrides, phosphides, arsenides and antimonides. Depending on the type of catalyst being used, two subcategories of VLS mechanism can be differed [74]:

- Heteroparticle assisted growth
- Homoparticle assisted growth

#### Heteroparticle assisted growth

In heteroparticle assisted growth liquid metal particle of different material, typically gold, is used. In Fig. 2.6a we show schematics of this process in 4 different steps: (I) gold particle is lithographically positioned within the opening, (II) annealing the substrate at the temperature higher then eutectic and alloying with the growth compounds (for further explanation reader can refer to Fig. 2.8 and related text in Section 2.2.3, (III) supersaturation and precipitation of first monolayers and (IV) continuation of the growth as long as material is supplied. Au-assisted growth is broadly used and well investigated since Au-particles are easy to produce by evaporation and annealing and they promote stable VLS growth for variety of systems [75, 76, 77]. Regardless all these advantages, gold is a fast diffusing metal that can harm the properties of semiconductors [78]. Au is not CMOS compatible what limits integration of NW on Si platform by using this mechanism. This inspired the search for alternative metals for VLS growth e.g. Al for GaN NWs [79], Ni for GaAs NWs [80] or Pd for InAs NWs [81], and many other materials that have been reported [82]. Following the same idea, the homoparticle assisted growth was developed [83, 84, 85, 86, 87].

#### Homoparticle assisted growth

The homoparticle assisted growth, or so called self-assisted growth, is where the liquid metal particle is one of the elements constituting the wire. For III-V nanowires, the liquid particle is made of element of group III therefore we can refer to this growth method as group-III-assisted growth. In this process, having a full or patterned silicon oxide surface (e.g., a native, thermally grown, or deposited oxide) is a curtail, since it provides nucleation sites on surface imperfections [88]. A schematic drawing of the self-assisted growth of GaAs nanowires on Si patterned substrate is presented in Fig. 2.6b. The substrate has predefined holes for the droplet positioning (I). In the step II Ga droplet is formed within the opening. This is called as Ga predeposition step. After that, the $As_4 As_2$ flux is introduced and alloying starts (III) and finally supersaturation occurs and growth starts (IV).

### 2.2.2 Particle free growth — selective area epitaxy (SAE)

Unlike VLS, selective area epitaxy growth proceeds without liquid particle. It consists of purely a vapor-solid (VS) growth that occurs in openings in the dielectric mask. The growth conditions are set to enhance the 1-D growth within the opening while sticking coefficient of growth precursors is minimized on the mask surface [89, 90]. The characteristic steps of the growth are shown in the Fig. 2.6c. The nanowires grow in layer-by-layer growth mode which is continued even above mask layer due to the formation of slowly growing facets with low surface energy [91, 92].

### 2.2.3 Vapor Liquid Solid (VLS) mechanism of GaAs nanowires by MBE

Up to now, both VLS and SAE have been successfully used to obtain highly uniform arrays of III-V NWs as exemplified in Fig. 2.7. One advantage of VLS growth is that in addition to the control of the morphology, it can also provide control of the polytypism [93, 94, 95]. The polytypism refers to the possibility of one compound to exist in different crystalline phases. For III-V NWs this is translated into the coexistence of wurtzite (WZ) and zinc-blende (ZB) phases. This affects both the optical [96] and transport properties [97, 98] and has strong

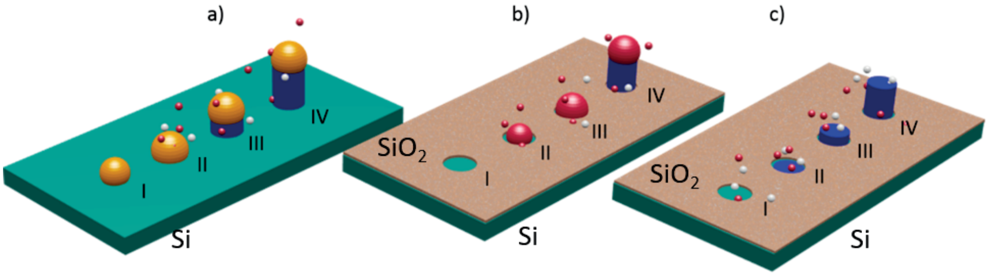

Figure 2.6 – Comparison of different growth mechanisms for obtaining NW - arrays: a) **Au-assisted VLS**: (I) the gold particle is formed by gold deposition on the patterned resist followed by lift off , (II) Supply of the growth material and alloying on the temperature above the eutectic one, III supersaturation is reached and precipitation of first layers (IV) growth proceeds while growth material is supplied. b) **Self-assisted VLS**: (I) in this case the pattern is defined in the oxide surface (II) the growth starts with group III predeposition step to form a droplets within the openings (for growth in self-assembly this is not needed, both materials can be supplied simultaniosly) (III) Group V elements are supplied and droplet increases due to the accommodation of the adatoms until supersaturation is reached, (IV) Growth is established and c) **Selective area epitaxy growth (SAE)** (I) Patterned surface with (111) substrate orientation is exposed to growth with both materials supplied in the same time (II)growth starts in layer by layer fashion within the opening without assistance of the particle on the top (III) The 1D growth continues above the oxide mask due to the preferential facet formation and (IV) it continues until material is supplied.

impact on the device applications.

Ga-assisted growth of GaAs arrays was central part of my thesis work, so herein, the most important aspects of this mechanism will be given in more details.

### The role of liquid droplet

The key element of VLS mechanism is the liquid phase. In the case of MOCVD growth it has the function of catalyst since it gathers the gas phase precursor molecules and decomposes them at a much higher rate than the rest of the surfaces. In MBE it acts only as preferential collector for the growth material that arrives in a form of molecular fluxes. The droplet promotes longitudinal growth and defines the nanowire position and radius.

Understanding the VLS mechanism starts with the understanding of the phase diagram of the liquid-solid phases involved in the NW growth. Phase diagrams can be used to choose the catalyst that can form a liquid alloy with the NW, but also to choose a specific composition and synthesis temperature so that there is coexistence of the liquid alloy and the solid NW material. In Fig. 2.8a we present the Au-Si phase diagram. This is a well-known reference system that helps explain the VLS process. In Fig. 2.8b we show the phase diagram of GaAs and molar Gibbs free energies of specific phases for a pressure of $10^{-6}$ Torr, which is in the

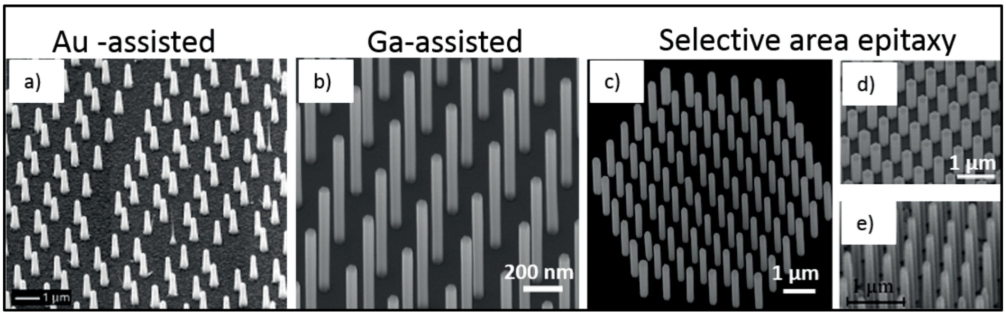

Figure 2.7 – Examples of ordered NW arrays obtained by 3 different growth mechanisms: a) Au-assisted InP NWs grown by MOCVD [6] (©2017 Nano Letters, American Chemical Society), b) Ga-assisted GaAs NW arrays grown by MBE [99], (©2017 Nanotechnology, IOP Publishing) c), d),e) NW arrays grown by selective area epitaxy - InAs (MOCVD) [100] (©2017 Journal of Crystal Growth, Elsevier), GaAs (MOCVD) [101]() InAs (MBE)[102] (©2017 Applied Physics Letters, AIP Publishing LLC), respectively.

range of pressures used for NW growth.

The Au-Si phase diagram on Fig. 2.8a shows an eutectic point at 363 °C. This is much lower than melting points of pure Au (1064 °C) and pure Si (1414°C). This temperature is the lowest temperature at which the mixture of Au and Si liquefies. Above the eutectic temperature Au particles can form liquid Au-Si droplets on the silicon surface (gold does not wet silicon surfaces). Between (AuSi)l and eutectic region, liquid phase and solid precipitate coexist ((AuSi)l+Si(s)). At the growth temperature, the metallic Au particle forms a liquid eutectic alloy with the Si supplied in the form of precursors in the vapor phase or the substrate. Further supply of Si in the droplets leads a liquid Au-Si to supersaturation. This causes precipitation of Si at the particle-semiconductor interface in the form of solid crystalline Si wire. Precipitation lowers the concentration of Si in the droplet, what re-establishes the equilibrium. For growth to continue, droplet needs a continuous supply of precursors that drive supersaturation and precipitation.

Figure 2.8b shows the phase diagram of GaAs as a function of temperature for a constant pressure of $10^{-6}$ Torr. The phase diagram of GaAs reveals the possibility for condensation of stoichiometric compound in a broad range of temperatures, both from the vapor and liquid phase. The stoichiometric composition is indicated with red line. The diagram gives information on the conditions that would be prone to self-assisted VLS and SEA NW growth. Ga-assisted VLS growth requires coexistence of Ga(l) GaAs(s) and vapor phases, what corresponds to region hatched in red in the phase diagram. SAE growth takes place in the region hatched in blue.

We move now to describe other considerations that are important for VLS. Both in Au and Ga assisted growth the liquid metal should not wet the substrate surface. Non-wetting of Ga on the substrate is usually achieved by coating it with a thin silicon dioxide. It has been shown that the initial conditions of the Ga droplet determine the orientation yield of the GaAs nanowires,

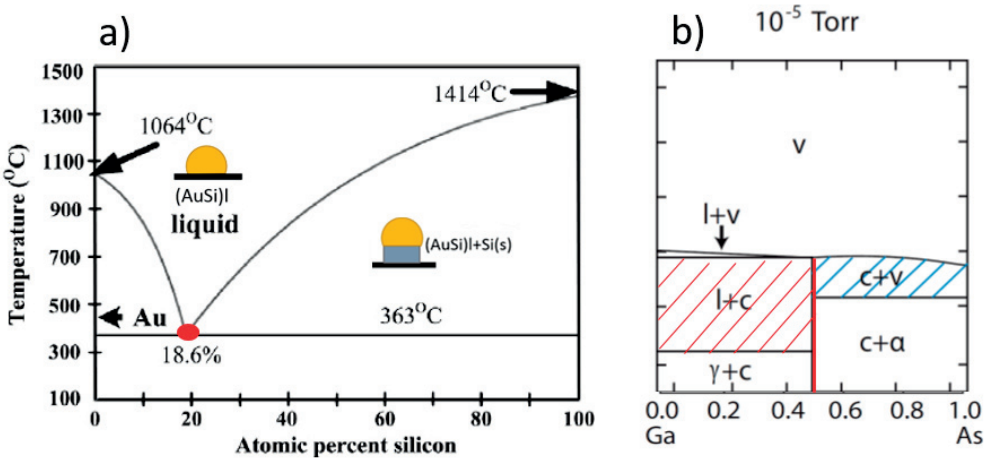

Figure 2.8 – a) Au-Si binary phase diagram indicates the various phases the Au-Si mixture at different temperatures and in different composition ranges, adopted from [103]. b) Binary phase diagram of GaAs for pressure of $10^{-6}$ Torr. Above and below-molar Gibbs free energies of the various phases at 100 K and 850 K. Adopted from [104], ©2017 Thin Solid Films, Elsevier.

especially when growing on silicon In particular, the contact angle of the Ga droplet should be around 90° in order for the nanowires to grow perpendicular to the substrate [105, 106]. The wetting of Ga can be engineered by modification of the composition of the silicon oxide $SiO_x$. For native oxide this is achieved by controllably varying the thickness [105, 106]. The situation is very different in the case of ordered growth. In this case the Ga droplet is wetting the open silicon surfaces and the wetting angle cannot be engineered. As it will be shown in Section 3.2, the positioning of the Ga droplet within the Si opening is crucial for controlling the nanowire orientation.

### Role of the surface energies

Nanowires exhibit an enhanced surface-to-volume ratio with respect to the bulk material, meaning that the role of surface becomes enhanced. Surface properties can as a consequence determine new phenomena, in addition to the liquid droplet configuration.

Let us consider the liquid droplet seated on a planar solid surface and surrounded by vapor, as illustrated in Fig 2.9. The surface energies of such a three-phase system are denoted as $\sigma_{LV}$ , $\sigma_{LV}SV$ and $\sigma_{SL}$ at the liquid-vapor, solid-vapor and solid-liquid phase boundaries, respectively. The values of surface energies determine the shape of the droplet which is described by the contact angle, $\beta$. The relation of surface energies and equilibrium contact angle if defined by Young's equation:

$$\sigma_{LV} \cos\beta = \sigma_{SV} - \sigma_{SL} \tag{2.1}$$

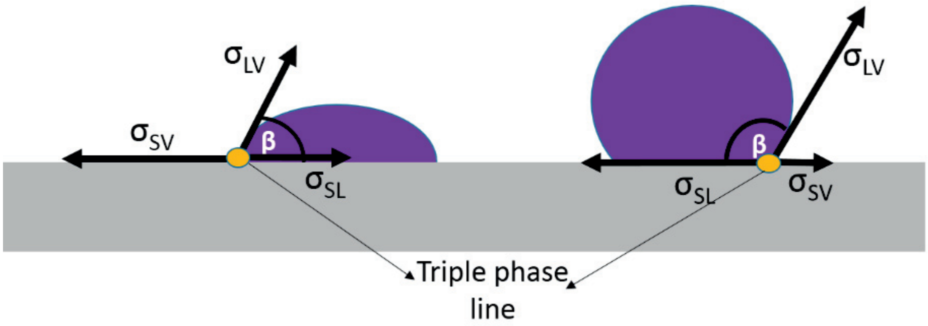

Figure 2.9 – Liquid droplet on solid surface with equilibrium two values of contact angle $\beta$

The accommodation of the growth material and nucleation can change the droplet's shape. These changes should be balanced by surface tension at the contact line for droplet to remain stable otherwise they can lead to the unbalanced net force that can affect NW orientation. The atomistic simulations and theoretical analyses have showed that the transition from stable to unstable symmetric wetting geometries is shown to be governed by Young's condition and coincides with a change in the sign of the resultant force at the triple junction (Carter capilary instability).

As it will be further discussed in Section 3.2, any variation of the droplet shape within the defined opening from the symmetrical one, can lead to formation of undesirable non-vertical wire or parasitic growth.

### Ga-assisted MBE - VLS growth

The VLS growth mechanism involves three phases and two interfaces (gas-solid and liquid-solid) and kinetics of this complex system consists of four general steps:

- Material transport in the gas phase
- Adsorption of growth species at the vapor-liquid interface
- Diffusion in the liquid phase
- Incorporation of atoms in a crystal lattice.

In Ga-assisted growth the growth starts with the Ga droplet formation. This acts as liquid reservoir and determines the NW diameter while further growth evolution is determined by the ratio of beam equivalent pressures (BEP) of group V element (As) and group III element (Ga), so called (V/III ratio). In the case of high Ga rate i.e. low V/III ratio, the Ga droplet will increase with time due to the accumulation of Ga adatoms, which will lead to the increase of the NW diameter. On the contrary, if the V/III ratio is too high, the Ga droplet will shrink over time which would give a tapered geometry [107, 108]. In the extreme case of too high V/III ratio, droplet would be completely consumed which would stop the growth. Between these two regimes it is possible to reach the steady state in which growth proceeds with constant droplet size and NW diameter. The length of NW, or better to say, axial growth rate was found to be proportional to the As flux, but also to exceed, even ten times, the deposition thickness [107, 109, 110]. To explain this effect one more kinetic process should be added in the list above, since the direct impingement of As and Ga and adsorption at the vapor-liquid interface is not sufficient to clarify the NW elongation rate. This involves the diffusion-induced contribution as the dominant mechanism without which MBE VLS growth cannot be understood. So, in addition to the direct impingement, droplet is fed by Ga adatoms by diffusive process on the substrate and along the NW sidewalls [85]. This is not the case for the group V growth species, since they desorb from the surface at the growth temperature. But, it was found that also for them an alternative pathway exists, which is related to the As-reemission from the substrate and NW sidewalls [110]. Considering all this effects, ordered arrays are ideal platform for studying growth kinetics. Several studies reported on size variation of the nanowires as a function of the inter-hole distance (pitch), both in the case of SAE and VLS growth mechanisms [111, 102, 112]. This dependence was explained by the existence of two separate growth regimes: (i) a competitive growth regime with shorter nanowires for narrow inter-holes distances and (ii) a diffusion-limited or independent growth regime for wider pitches. Furthermore, the directional beams in the MBE, where the incident angle of the deposition flux a is not perpendicular to the surface, give rise to the shadowing of NW sidewalls that can affect NW radial growth rate as well as the rate of their elongation [113]. This effect is particularly pronounced in the very dense arrays (short inter-wire distances).

## 2.3 III-V nanostructures on silicon substrate

Bottom-up assembly of nanowires allowed combining lattice mismatched materials, but also their monolithic integration onto Si substrates. In this section we will refer to the main challenge of this integration that involves control of the nanowire orientation. For all the application it is desirable that nanowires are grown vertical respect to the substrate. The main challenge arises from the polarity mismatch between Si substrate and III-V nanowires. Achieving the control over nanowire orientation was shown to be particularly difficult in the case of Ga-assisted VLS growth of GaAs NW arrays on Si. Within this work a lot of effort has been put toward understanding the key elements for controlling the orientation of GaAs NW what will be presented in Section 3.2.

Now, let's consider only general aspects related to the controlling of the orientation of GaAs nanowires on Si. The NWs grow in the direction that minimizes the total free energy. Even though, it was mentioned that in nanowires both zinc-blende and wurzite structure can be present, most of the nanowires show dominantly zinc-blende structure. Since in this crystal phase surface free energy is smaller along the <111> direction than, for example <100>, nanowires tend to grow in the <111> direction. Moreover, due to the polar nature of 111 planes,

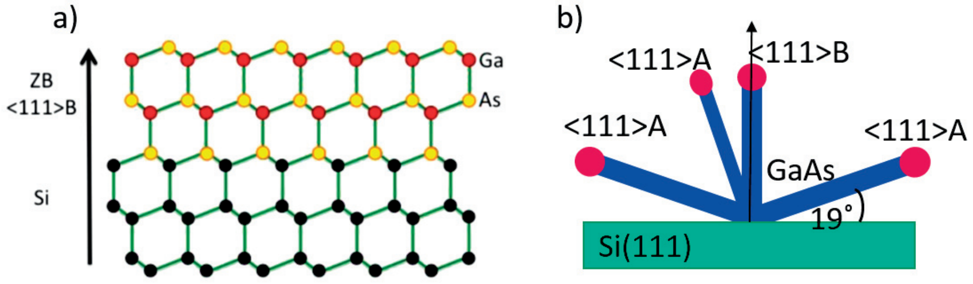

Figure 2.10 – a) Schematic drawing of the atomic arrangement in a zinc-blende crystal growing in <111>B direction on Si(111) substrate ([110] zone axis-the top surface has B polarity. b) Schematic illustration of the expected NW growth direction on Si(111) substrates. The out-of-plane <111> growth directions are four: one surface normal and other three at 19.5°.

this growth direction can be distinguished into <111>A and <111>B depending on the surface termination (the <111>A is group III (Ga) terminated while <111>B is group V(As) terminated as shown in Fig. 2.10a.

Due to the lower surface energy of the <111>B [114], GaAs NWs preferentially grow in this direction. This means that vertical growth is straight forward to obtained if one uses the substrate with the same orientations. The lack of polarity in Si yields four available and equivalent out-of-plane <111> directions — one normal to the surface and three under the angle of 19.5° respect to the substrate as can be seen on Fig. 2.10b. This means that tilted nanowires are consequence of the polarity mismatch between substrate and grown structures. It was experimentally observed that GaAs NWs can grow following different directions e.g. 34° or 51° [115] or even horizontally, crawling on the surface. This was explained by new theoretical model, called three dimensional multiple order twinning [116].

## 2.4 Application of nanowire arrays

In this section we focus on some of the applications for which using nanowire arrays is particularly beneficial. Primarily, this refers to the optoelectronic devices where photonic effects of the arrays can be used to tune the device properties. The applications are presented from the fabrication point of view emphasizing the importance of reproducible and controllable growth and fabrication in general. Furthermore, the goal is to stress the potential in the arrays engineering introduced by nanowire 3D architecture using different materials, combinations and forms of heterostructures.

### 2.4.1 Solar cells

Current investigations in the field of photovoltaics is directed towards generation of so called *next generation* solar cells. The idea is to introduce new concepts and technologies that would extend solar cells efficiency beyond the famous Shockley-Queisser limit and at the same time reduce the material consumption [117]. The potential of nanowires for surpassing the Shockley-Queisser efficiency limit was demonstrated by Krogstrup and coworkers on a single GaAs nanowire solar cell on Si substrate [118]. The photonic aspects leading to this increase in efficiency were brought a step further by analyzing all photonic contributions in the overall efficiency in nanowire arrays. The interest of using nanowires in photovoltaic applications comes from their intrinsic antireflection effect, and ability to direct light absorption with specifically designed arrays [119]. Their unique longitudinal geometry and high aspect-ratio allows tailoring the electrical and photonic design in an independent manner as : light is absorbed vertically, whereas carriers are separated radially [120]. Among the III-V materials, GaAs and InP are the most relevant ones for solar cells applications since their theoretical efficiencies exceed 30% [117].

Achieving ordered nanowire structures in one of these two materials could provide slightly better efficiencies of today's best solar cells, and in addition ensure the use of significantly less material than compared to the planar device and hence reduce the cost of electricity generated from solar irradiation. This arises from the fact that nanowires act as natural light concentrators [118, 121]. Fig. 2.11a (adopted from Ref. [121]) corresponds to absorption calculations in 2 $\mu$m long GaAs nanowires on a silicon substrate. The figure shows the results on the absorption cross-section of the NWs as a function of the diameter and wavelength. Absorption is enhanced for particular diameters. Interestingly, it exceeds their physical diameter. For example, nanowires with diameters between 350 and 400 nm and for wavelengths close to the bandgap absorb the light from the area about 3 times larger than their diameter. This point of the absorption map is in Fig. a) is marked by a yellow square. This implies that if we organize nanowire array by displacing them considering their absorption cross-section one should obtain the same absorption as in a thick enough film. Fig. 2.11b illustrates the effect of the nanowire distance in an array in the coupling of light in the nanowires, which then determines light absorption. The figure is a result of computation of the square of the electric field of light for a plane wave incident perpendicularly to the array. The calculations are performed for nanowires of 150 nm in diameter and are weighted by the solar spectrum 1.5 AM as a function of the pitch (nanowire distance). By increasing the pitch, light is able to penetrate better in the nanowire, resulting in improved light absorption. These calculations emphasize the importance of obtaining the optimal nanowire array design. This can only be the result of a well controlled growth process.

Up to date many nanowire arrays based solar cells were realized. Table 2.2 reviews highest efficiency reported for InP and GaAs nanowire arrays. So far, the best nanowire solar cell reported corresponds to an InP NW array fabricated using a top-down approach. The reported efficiency amounts to 19.6% [126]. This is very close to the 21.9%, corresponding to the best efficiency reported in planar devices with the same material [127]. This report confirms great potential of nanowires for building blocks of new generation solar cells, but in order to make their fabrication scalable and commercially available, fabrication should be completely directed towards bottom- up construction i.e. growth of ordered structures.

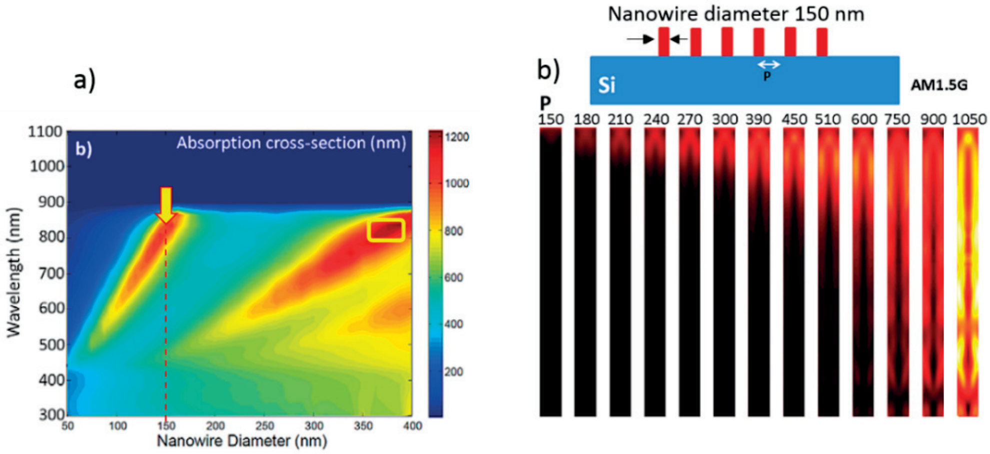

Figure 2.11 – a) diameter of the absorption cross-section of single vertical GaAs nanowires standing on a Si substrate as a function of the diameter. b) Average of the square of the electric field in the nanowire for different pitch. Adopted from [121], (©2017 Nanotechnology, IOP Publishing.

Table 2.2 – State of the art of most efficient nanowire-based solar cells

| Material | p-n junction | Growth technique | Growth mechanism | Efficiency (%) | Reference |
|---|---|---|---|---|---|
| InP | Axial | MOVPE | SAE | 10.5 | [122] |
| InP | Axial | MOVPE | VLS | 13.8 | [119] |
| GaAs | Axial | MOVPE | SAE | 6.4 | [123] |
| GaAs | Axial | MOVPE | SAE | 6.6 | [124] |
| GaAs | Axial | MOVPE | SAE | 7.5 | [122] |
| GaAs | Radial | MOVPE | VLS | 15.3 | [125] |

### 2.4.2 Light emitters

III-V materials are one of the best choices for making light emitters, due to their direct band gap and wide wavelength coverage. Their use within the frame of thin film technology has several limitations such as the low extraction efficiency and the challenge to reach orange and green wavelengths [128, 129, 130]. A good alternative to solve these challenges are nanowires and a significant amount of attention has been dedicated to the development of both the light emitting diodes (LED) and the lasers [131, 132, 133].

#### Light emitting diodes (LED)

The thin film LED technology faces the following materials science challenges that can be overcome by using nanowire geometry [128, 133]:

- The lattice and thermal coefficient mismatch between epilayers and substrate can cause high-density of cracks and misfit dislocations that act as non-radiative defects and reduce internal quantum efficiency,
- Presence of large polarization and piezoelectric fields caused by the intrinsic polarity of material that effects the efficiency of quantum wells used for light emission
- Large difference in refractive index between the semiconductor and air can lead to internal reflection of the emitted light. This reduces the external quantum efficiency.

The nanowire geometry allows the growth of high-quality crystals with low defect density, which can greatly increase the internal quantum efficiency. With the appropriate dimensions, it is possible to engineer their photonic properties and suppress the total internal reflection and enhance outcoupling of the light to the free-space. As an example, recently a InGaN NW array LED with more than 4 times higher light extraction efficiency compared to the conventional thin film LEDs was demonstrated [134]. In addition, nanowire LEDs can enlarge the electromagnetic range of emission compared to thin films. It is known that none of the existing semiconductor this films can access, the so called, green-yellow gap (spectral range between 550 and 590 nm) [130, 135] InGaN has the optimal band gap to achieve emission in this range of wavelengths. Due to the efficient strain relaxation in nanowires and their non-polar facets, InGaN/GaN NW heterostructure can be grown with a thick and high quality InGaN active region that can cover full visible region, as demonstrated in references [136, 137]. This increase in active area can also help reducing current densities at the junction which would ease the efficiency droop problem[2]. Moreover it can prevent the spatial separation of holes and electrons in the sidewall active region due to the absence of the internal electric fields [128, 138].

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[2] GaN based LED exhibit maximum efficiency only at very low current. The electrical-to-optical power conversion efficiency drops dramatically with higher input current. This so-called efficiency droop has been investigated for many years, and it still represents a key challenge to solid-state lighting.

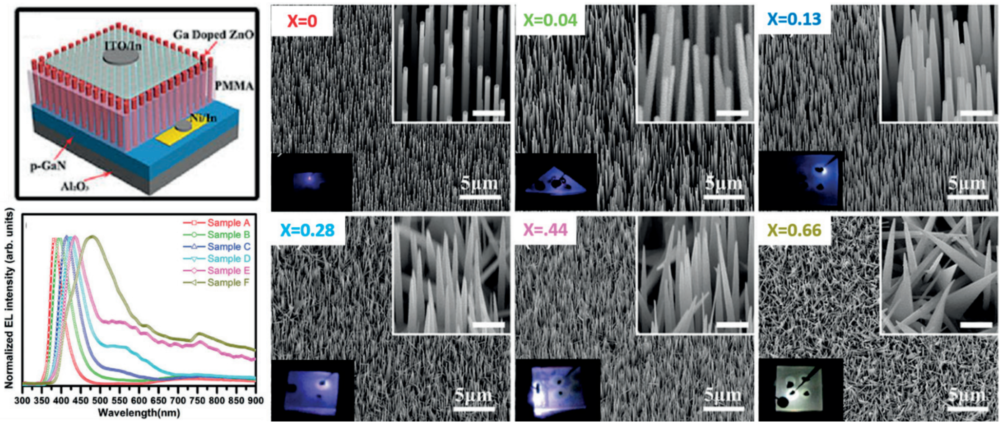

Figure 2.12 – Top left: device design, bottom left: EL spectra for different Ga content. SEM images of grown $Ga_xZn_{1-x}O$ NW arrays. SEM image of as grown $Ga_xZn_{1-x}O$ NWs on p-GaN(001) thin film with different Ga content, Insets on SEMs: EL emission of the n-GZO/p-GaN LEDs. Photo galleries of room-temperature EL emission from n-GZO/p-GaN LEDs at 20 V. Adopted from [139], ©2017 Laser & Photonics Reviews, John Wiley and Sons.

All these advantages initiated numerous studies that resulted in nanowire LED realized by using different material combinations (InGaAs, InAsP, InGaN and AlGaN, GaAs, AlGaAS, InGaP and so on), and forms of heterostructures (axial and radial) [128]. Several interesting examples of nanowire arrays LED realizations are listed in figures below. Fig. 2.12 shows how the addition of Ga in ZnO results in LED with the emission wavelength tuned from the UV to the visible range. The following figure, Fig. 2.13 demonstrates the capability of controlling the spatial distribution of the blue/near-UV LEDs composed of position controlled arrays of n-ZnO nanowires on a p-GaN thin film substrate. As previously mentioned, one of the greatest advantages of nanowire geometry and their fabrication by bottom-up approach is monolithic integration to the Si platform. Two example of achieving active LEDs by direct implementation of active devices on Si are shown in Fig. 2.14 and Fig. 2.15.

#### Lasers

The greatest advantage of using nanowires for lasing is simplified fabrication, since nanowires themselves, act both as gain medium and the cavity. In conventional semiconductor lasers fabrication consist of multistep process, including both epitaxial growth and top-down approach while unique geometry of the nanowires eliminates the need for post growth processing [143]. Current state-of-the-art in nanowire lasers shows wide range of emission wavelengths, from ultraviolet (UV), visible and near-infrared regions, realized by use of different materials, not only III-Vs; e.g. ZnO, GaN, InGaN, CdS, CdSe, CdSSe, GaAs, InGaAs, AlGaAs, ZnS, GaSb, InP [144].

GaAs is an important material for near infrared that can be used for optical data communication, spectroscopy and medical diagnosis. Very large surface recombination velocity of GaAs in the combination with the large surface-to-volume ratio of nanowire based devices impose

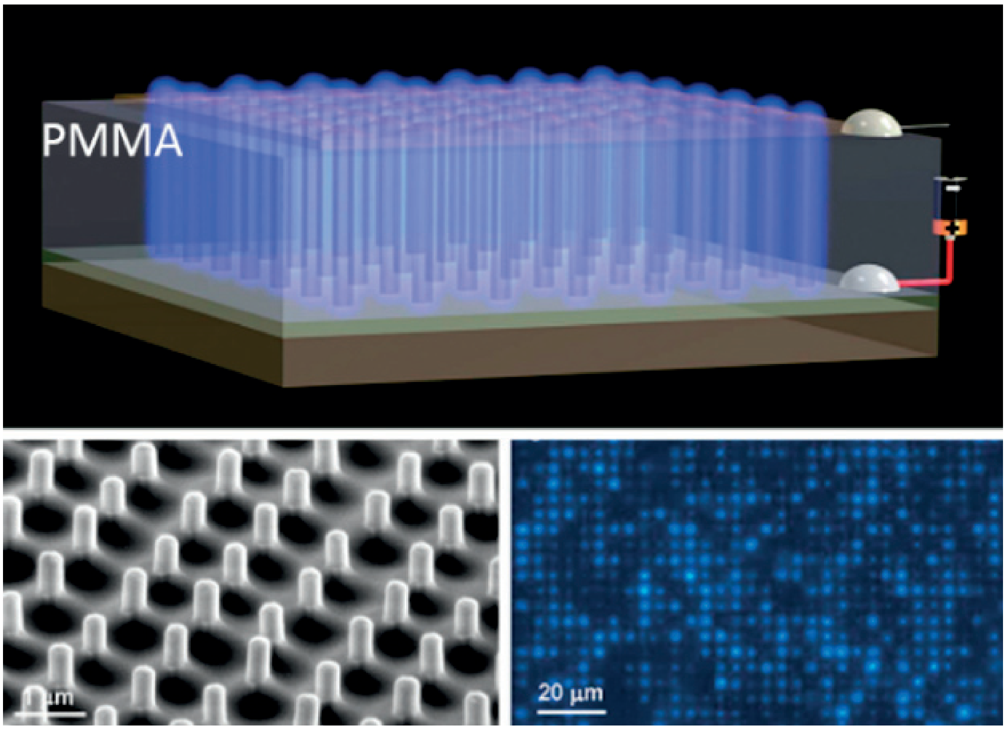

Figure 2.13 – Top: design overview of the LED. Bottom left: SEMs of ZnO arrays coated with $SiO_2$ and wrapped with PMMA - the tips are exposed, scale bar is 1 $\mu$m, bottom right: The optical image of a turned on LED (artificial bluish color). Adopted from [140], ©2017 Advanced Materials, John Wiley and Sons.

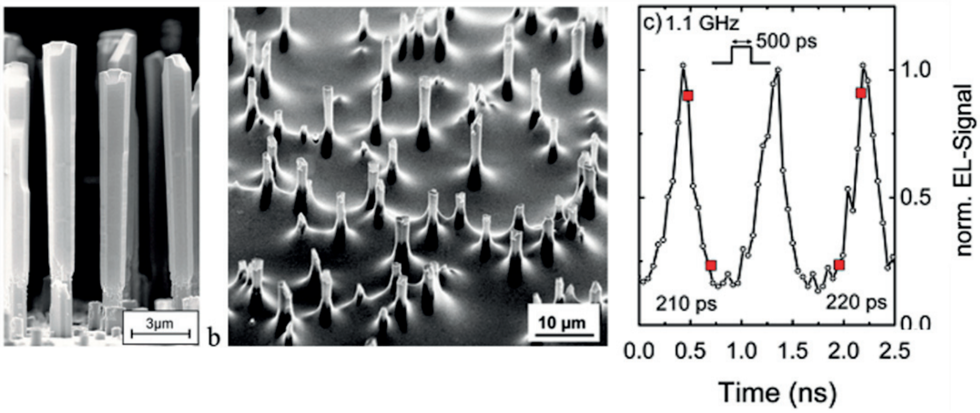

Figure 2.14 – Core-shell nanowire LED grown on Si(111). Left: SEM micrograph of the as-grown p-GaN/InGaN MQW(×5)/n-GaN core-shell, center: array section covered with spin-on-glas and Ni/Au contacts, c) 9 time-resolved electroluminescence signal — high-speed potential might be used for short-range optical data communication in free space or via polymer optical fiber. Adopted from [141], ©2017 Nano Letters, American Chemical Society.

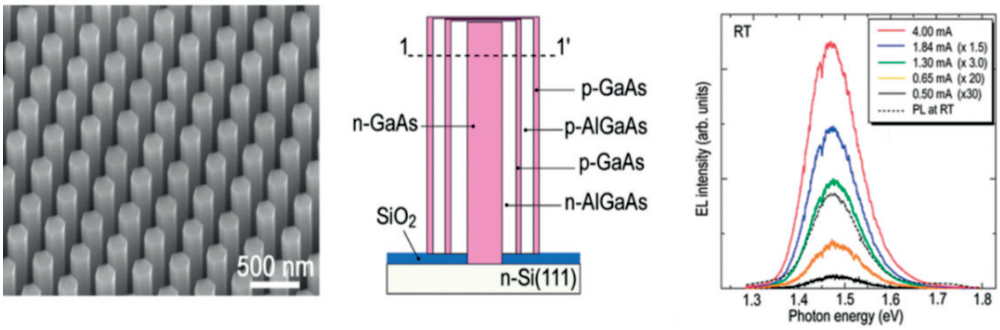

Figure 2.15 – Left: SEM image of vertically aligned AlGaAs/GaAs/AlGaAs core - multishell nanowire arrays on Si, center: Illustration of core-multishell nanowire, right: Electroluminescence (EL) spectra under several current injections at room temperature. Adopted from [142], ©2017 Nano Letters, American Chemical Society.

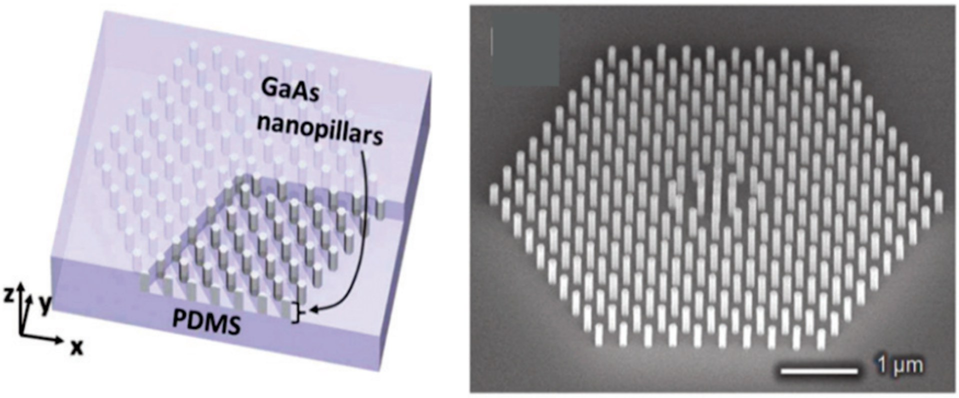

Figure 2.16 – Left: Schematic diagram of the photonic crystal lasers in PDMS, right: SEM of GaAs heterostrustures on grown on the substrate. Adopted from [148], ©2017 Nano Letters, American Chemical Society.

strong need for effective passivation of its surface. This is most commonly achieved by growing AlGaAs layer e.g. Using core-shell-cap GaAs/AlGaAs/GaAs design reference [145] which allowed the achievement of the room-temperature lasing. Alternative approach is the use of highly doped GaAs nanowires [146]. The emerging need for high-performance lasers for a viable photonic applications that would be employed in data storage, biomedical applications, solid-state lighting and display technologies has led to the development of photonic crystal lasers [147]. They combine lasing properties of single nanowire with the properties of array that behave like photonic crystal. One example is shown in Fig. 2.16. Scofield et al, demonstrated low-threshold single mode lasing at room-temperature using GaAs/InGaAs/GaAs axial heterostructures passivated by InGaP arranged in the arrays shown in Fig. 2.16 below [148]. In this case the arrays were obtained by catalyst-free selective-area metal-organic chemical vapor deposition on masked GaAs substrates.

Beside ordered arrays, also self-assembled NW arrays for laser application. Frost et al reported on electrically pumped laser emitting in the green ($\lambda$ = 533 nm) on (001) silicon substrate. They develop an edge-emitting InGaN/GaN disk-in-nanowire array [149].

### Photodetectors

Large surface-to-volume ratio and small dimensions of nanowires enables them to have higher light sensitivity than their bulk counterparts. As in case of the nanowire-based solar cells, they benefit from efficient absorption within a small volume of active material as well as from the antireflection and light trapping properties of standing nanowires. Also here, the ability to form different kinds of heterostructures and combine different material enables bandgap engineering what can be of particular interest for detection in the ultraviolet, visible and infrared range photodetection. Up to date both photodetectors with single nanowire and ensembles (array) were demonstrated. The most investigated material is GaN, but single nanowire detector devices were extended to many other material systems including InP ,GaAs , InAs, InSb , InAsP , InGaAs and GaAsSb [150]. One of the first demonstrations of III-V nanowire photodetectors was based on InAs nanowires grown on a Si substrate [151]. Furthermore, many other materials were investigated: GaAs, InP, InN, InGaAs, InAsSb and InAsP [150].

### Nanowire sensors

Nanowire architectures exhibit a variety of interesting properties that can be applied also in sensing technology [34, 152]. One typical example is gas sensing. Even though, the basic gas sensing mechanism remains the same, nanowire gas sensors and sensors arrays show many advantages over planar devices: ultra-sensitivity and fast response time due to their small size with high surface-to-volume ratio [153, 154], higher selectivity and stability [34, 155], light weight and low power consumption [156] and low-temperature operations [155, 157]. Beside gas sensing, nanowires have been employed as advanced sensor in medicine and life sciences; e.g. nanowire arrays were used for real time detection of proteins and for single virus detection [158]. Recently, Poggio group at University of Basel reported about the use of nanowires as sensors in new type of atomic force microscope [159]. They used individual as-grown GaAs/AlGaAs NWs to realize the vectorial scanning force microscopy of a patterned surface. This hold a great potential in revealing the anisotropy of atomic bonding forces.

# 3 Results and discussion

This chapter consists of three sections, each dedicated to the fabrication of different kinds of ordered nanostructures that are presented in Fig. 3.1. The sections are structured according to the approach employed to achieve the ordered structures, but also by materials.

The first section focuses on a top-down approach used to define silicon micro pillars that were further transformed into porous micro tubes. Typical SEM images of such structures are shown on the left in Fig. 3.1.

The second section explores the bottom-up assembly of GaAs nanowires on a patterned silicon substrate. We explain how we achieved a high vertical yield in a reproducible manner. A representative SEM image of a high yield array is exemplified in the central part of the figure below. Also we identified some of the key elements for the control of the nanowire orientation and uniformity of the arrays.

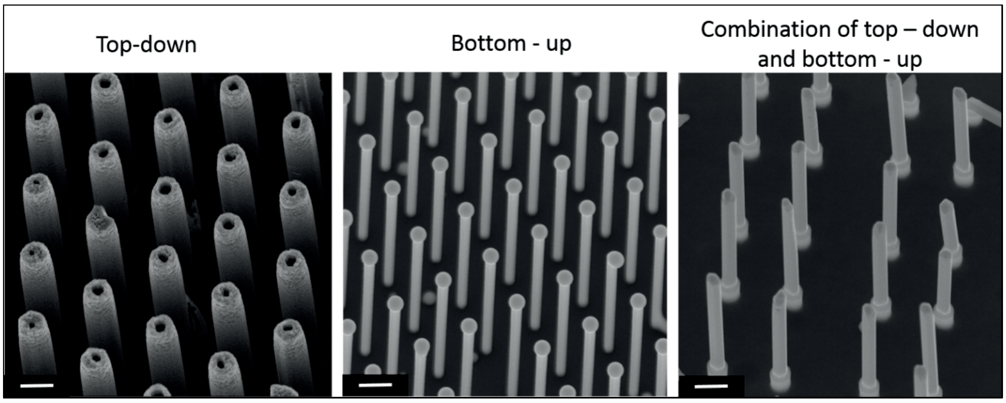

Figure 3.1 – Representative results for each structure type examined in this work. Left: Top-down silicon microstructure arrays (scale bar 2 $\mu$m), Center: Bottom-up GaAs nanowire array (scale bar 200 nm), Right: Array of hybrid heterostructure InAs/Si made by combining top-down and bottom-up approaches (scale bar 1 $\mu$m).

Finally, in the third part of this chapter we studied templated-growth of InAs nanowires on SiO2 tubes obtained on a Si substrate. We used a process flow that is compatible with large area nanoscale patterning. As a result we demonstrated the fabrication of of hybrid NW heterostructures composed of InAs and Si combining both top-down and bottom-up approaches. A small section of a InAs/Si array is shown in Fig. 3.1 on the right.

## 3.1 Microtube arrays: geometrically driven electrochemical dissolution of silicon

Mature silicon and nanofabrication technologies allow the fabrication of a variety of different forms of silicon micro and nano structures that find a broad range of applications [160, 161, 162]. One of the potential forms that could open up a wide range of novel applications such as energy conversion [163, 164, 165] and hydrogen storage [166, 167, 168] are tubular silicon structures. In addition, tubular Si arrays could be used as photonic devices [169, 170] and sensors [171]. In spite of all the available techniques, fabrication of these structures has remained challenging. Silicon nanotubes were previously realized by similar experimental procedure employed in the synthesis of carbon nanotubes [172, 173] and by using templates such as nanowires or anodized alumina for CVD deposition [164, 165, 173, 174]. Large scale ordered arrays of Si micro tubes were also realized by so called Poisson spot lithography [175]. It is a relatively novel approach based on the Poisson spot effect in a conventional optical lithography system. Poisson spot is a bright point which appears due to Fresnel diffraction at the center of the wave shadow of a circular object [176]. As an alternative to these relatively complicated techniques, several authors reported on the silicon tube formation by self-controlled electrochemical dissolution of mesoporous silicon layer [177, 178] as shown in Fig. 3.2.

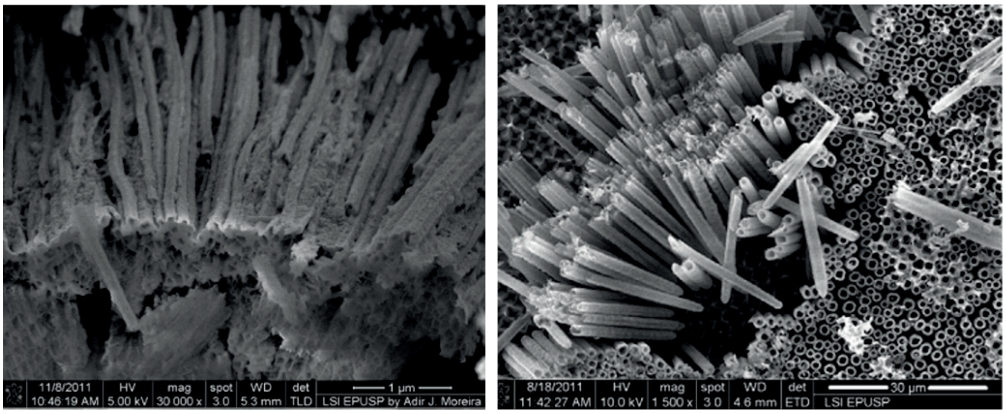

Figure 3.2 – Examples from the literature of Si micro and nano tubular structures made by self - controlled electrochemical dissolution of mesoporous silicon layer (adopted from left PSS Tube 18, right Tube 19) Adopted from [177](©2017 Physica Status Solidi A, John Wiley and Sons) and [178] (©2017 Materials Chemistry and Physics, Elsevier)

Porous silicon is a large surface to volume ratio material (in the order of 500 $m^2/cm^3$) very often formed by electrochemical dissolution of single crystalline silicon in HF containing solutions [179, 180]. This new form of silicon was intensively studied after its discovery in 1990 due to its novel properties, one of which is an efficient visible light emission [179, 180, 181, 182]. In this work we used so called stain etching to form porous silicon. It uses the HF solution containing some oxidant species like nitric acid $HNO_3$ or $V_2O_5$. The electrochemical nature of this process arises from the exchange of the charges between the electrolyte and the Si surface; i.e. hole injection from the electrolyte to the Si valence band [179, 180, 183]. This highlights the role of the oxidant — it provides hole needed for reaction to take place. In the case of nitric acid, the hole injection proceeds via the following reaction:

$$HNO_3(aq) + 3H^+(aq) \rightarrow NO_{(g)} + 2H_2O(l) + 3h^+_{VB} \tag{3.1}$$

Equations describing further steps of Si dissolutions can be found in the appendix of the paper.

In the publication included in this chapter we fabricated arrays of silicon micro pillars in a top-down approach that were subjected to further electrochemical etching. As a result we obtained ordered nanoporous structures. The pillars were etched at a higher rate in the middle, resulting in the formation of tubular structures. We investigated the functionality of the structures by characterizing the emission properties by photoluminescence and cathodoluminescence. We then went a step further to demonstrate a light emitting device and a solar cell.

In this work we investigated in detail the formation of holes inside the pillars that resulted in the creation of tubes. To understand this mechanism we first considered the band alignment of the semiconductor-electrolyte interface that is schematized in Fig. 3.3. The semiconductor-electrolyte interface is similar to the one of semiconductor-metal that leads to formation of Schottky barrier. In Fig. 3.3a one can see the energy levels in the p-type semiconductor and electrolyte before they are brought in to the contact. When two phases are brought in to contact (Fig. 3.3b) their chemical potentials equalize. This leads to the band bending and creation of a space charge region (SCR) i.e. barrier formation in the vicinity of the interface.

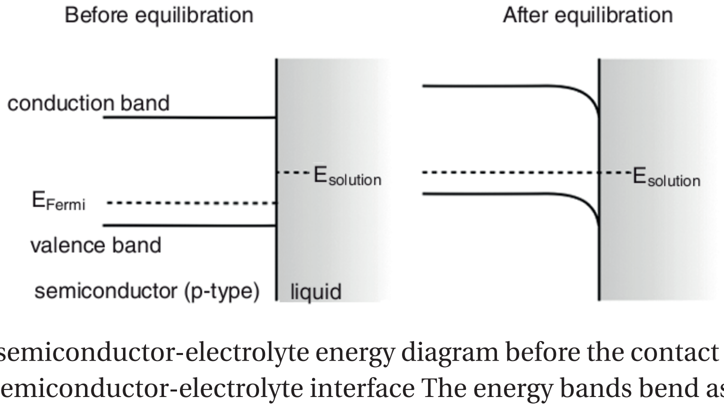

Figure 3.3 – p-semiconductor-electrolyte energy diagram before the contact b) equilibration of charge at the semiconductor-electrolyte interface The energy bands bend as a result of charge equilibration between the semiconductor and the liquid phase.

By investigating the effect of geometry and silicon doping we could understand the role of the depletion layer width in the dissolution process. We solved the Poisson equation for different curved geometries and by compared the widths of the SCR of the planar and curved geometries. The conclusion was that the width of the SCR is smaller in the planar than in the convex case. This means that the dissolution process should occur preferably at the top flat facet of the pillar with respect to the curved side surfaces. This presents the core of the tube formation mechanism. In the manuscript we show the influence of the pH level of the electrolyte and doping level of p-Si. We also used arrays with pillars with different geometries (from triangular to hexagonal) in order to validate the role of the geometry in the tube formation mechanism.

### 3.1.1 Paper included in this section

**Nanoporous silicon tubes: the role of geometry in nanostructure formation and application to light emitting diodes**

AUTHORS
Jelena Vukajlović Pleština*, Vedran Đerek*, Luca Francaviglia, Francesca Amaduzzi, Heidi Potts, Mile Ivanda, Anna Fontcuberta i Morral
**Equally contributing authors*

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MY CONTRIBUTION

- I fabricated pillar arrays for the etching experiments
- I did part of the etching experiments
- I performed SEM imaging
- I fabricated and measured the device
- I took active part in interpreting and analyzing the results
- I prepared figures
- I wrote parts of the paper

NOTE
The supporting material for this paper is included in the Appendix A.

# Nanoporous silicon tubes: the role of geometry in nanostructure formation and application to light emitting diodes

Jelena Vukajlović Pleština[1 ‡], Vedran Đerek, [2† ‡], Luca Francaviglia[1], Francesca Amaduzzi[1], Heidi Potts[1], Mile Ivanda[2,*], Anna Fontcuberta i Morral[1,*]

E-mail: anna.fontcuberta-morral@epfl.ch, ivanda@irb.hr

**Abstract**. Obtaining light emission from silicon has been the holy grail of optoelectronics in the last decades. One of the most common methods to obtain light emission from silicon is to reduce it to nanoscale structures, for example by producing porous silicon. Here we present a method for large area fabrication of porous silicon microtubes by stain etching of silicon micropillar arrays. We explain and model how the formation of the microtubes is influenced by the morphology of the substrate, especially the concave or convex character of the 3D features. Light emission is demonstrated at the micro and nanoscale respectively by photo and cathodoluminescence. Finally, we demonstrate a 0.55 cm$^2$ device that can work as a photodetector with 2.3% conversion efficiency under one sun illumination, and as a broadband light emitting diode; illustrating the applicability of our results for optoelectronic applications.

[1]Laboratoire des Matériaux Semiconducteurs, École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland
[2]Center of Excellence for Advanced Materials and Sensing Devices, Ruđer Bošković Institute, Bijenička cesta 54, Zagreb 10000, Croatia

KEYWORDS silicon, microtube, stain etching, depletion, light emission

## 1. Introduction

Silicon is the most widely used electronic material thanks to its abundancy, functional properties and high quality oxide. Despite many efforts in the last decades, it has been challenging to obtain light emission from macroscopic silicon due to the indirect nature of its bandgap[1–7]. Nanoscale silicon is an efficient light emitter in the visible spectral range, although still far from efficiencies of direct-bandgap semiconductors. One pathway to produce nanoscale silicon in high volumes is the utilization of porous silicon. Reported external efficiencies in photoluminescence in porous silicon can be as high as 23%, while electroluminescence efficiencies stay at the 1% level[8–14]. The functional properties of silicon nanocrystals and porous silicon are thus encouraging for possible future use as photodetectors and emitters on a chip[15,16].

Porous silicon can be generated by self-limited electrochemical etching in aqueous hydrofluoric acid (HF) or fluoride containing solutions[17–21]. Besides direct anodization in galvanostatic or potentiostatic conditions, it can also be prepared by electroless or stain etching. This technique involves an oxidant in etchant agent, such as $V_2O_5$ in a fluoride solution. The oxidant provides additional holes to initiate the oxidation reactions necessary for the porous silicon formation. The use of $V_2O_5$ is preferred over $HNO_3$[22] because it avoids bubble formation affecting the homogeneity of the layers[23,24]. More details about the chemistry of the stain etching using nitrates and $V_2O_5$ used in this study can be found in the SI. Electroless etching has been widely used for micro and nano-structuring of planar silicon substrates, resulting in roughened surface containing pits or porous structures[25,26]. Such surfaces were exploited for their high exposed area[27,28] or good light absorbing properties due to light trapping[29]. These porous structures contain silicon nanocrystals which show efficient photoluminescence and electroluminescence, enabling optoelectronic and sensing applications[29–37]. To the best of our knowledge, all examples of the solid state electroluminescent silicon devices presented so far have been based on planar geometry [10,33,38–41].

The stain etching process depends strongly on the electrolyte composition - fluoride concentration and pH, oxidant type and concentration, electrolyte temperature as well as on the properties of the silicon substrate such as the dopant type, charge carrier concentration and crystalline orientation. Silicon dissolution in fluoride containing electrolytes is primarily driven by the supply of holes in silicon[42–44]. More details on the chemical reactions involved in stain etching can be found in the SI 2. Bringing the semiconductor and the electrolyte in contact results in a redistribution of charges, as the Fermi level in the semiconductor and the redox level in the solution equalize. In the semiconductor, this results in band bending and thus depletion or accumulation of carriers close to the surface. Depletion is accompanied by the formation of a space charge layer (SCR) containing fixed ionized dopants. In the electrolyte, this results in the formation of an interfacial electrical double layer[45]. The SCR layer is a major self-limiting mechanism in dissolution of semiconductors, giving existence to the potential barrier, which acts as a barrier for charge transfer from the electrolyte to the silicon and vice versa[46]. In that sense, it can be used to avoid or facilitate dissolution in certain regions of the substrate and to create non-planar structures such as silicon microtubes[46,47].

In this work we exploit the effect of geometry in modifying the speed of stain etching of Si micropillars as well as the engineering of the SCR for obtaining ordered arrays of a variety of shapes – tubular structures with different porosity levels as well as very pointed cone structures. We elucidate the mechanism of tube formation, and illustrate their optical properties by photoluminescence (PL) and cathodoluminescence (CL). Finally we demonstrate one of potential applications by presenting a functional, large area 3D structured light emitting diode and a solar cell. This periodic tubular structures can find various applications the different fields starting from sensors[48], energy storage[49–51] and for anodes in electrochemical batteries[52,53] and also in photonics[54,55]. The porous layer can have an additional advantage in biological applications, such as in drug delivery[56]. The sharply pointed features are particularly interesting for applications in cell biology research [57,58].

## 2. The mechanism of nanoporous Si tubes formation

Silicon micropillar arrays formed by reactive ion etching were subjected to electroless stain etching in three different solutions: HNO (hydrofluoric acid - HF(48%) : nitric acid - $HNO_3$(70%): surfactant = 2000 : 2.5 : 1), BHNO (buffered HF (HF: $NH_4F$ = 12.5% : 87.5%) - BHF(7:1) : $HNO_3$(70%) : surfactant = 2000 : 5 : 1) and HVO (48% HF containing 0.05 M/L of the vanadium(V) oxide $V_2O_5$ which served as an oxidant). As a surfactant a general-purpose nonionic fluorosurfactant Zonyl FS-300 was used. For more details about micropillars fabrication and stain etching procedures see SI 1. Starting with the same geometry of pillars, but using different etching parameters (doping level of Si, pH of the solutions and etching time), we were able to obtain variety of different structures. Figure 1 shows scanning electron micrographs (SEM) of the different shapes obtained by stain etching of Si micropillars under different conditions – using the BHNO or HVO solutions on different substrates and for different durations. We show examples of three different groups of features: microtubes with very thin porous layer – figure 1 (a), microtubes with homogenous layer of nanostructured photo - and electro-luminescent porous silicon – figure 1 (b), and pointed structures that are consequence of the lateral etching of the pillars and tubes – figure1 (c). Further in the text we will show more details on the porous structures and elucidate the underlying formation mechanism.

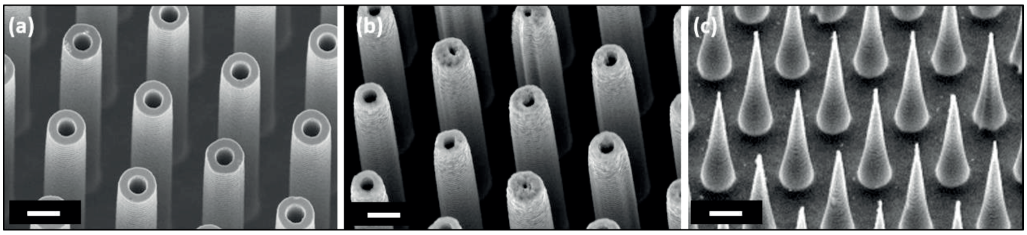

Figure 1 - Different shapes obtained by stain etching: (a) Si tubes by etching in BHNO solution, (b) silicon tubes covered by a layer of porous silicon by etching the tubes in the HVO solution and (c) silicon micro cones covered by a layer of porous silicon. Scale bar is 2 μm.

We start with presenting the process of tube formation by looking at the evolution of the structures during stain etching. We use 36 μm long p-type silicon micropillar arrays, with a resistivity of 15-25 Ωcm and the BHNO solution described above. Figure 2 shows SEMs of the different stages. The initial stages and evolution of the tube formation is presented in figure 2 (a). After 10 minutes the tube formation process is initiated in the central part of the top of the micropillar. This is followed by formation of additional pores which merge together over the duration of etching. After about 70 minutes the hole has drilled through the centre of pillar and turning it into a tube. The process continues during the following 50 minutes, widening the hole and becoming almost symmetric. An overview of the arrays before and after 150 min of etching is presented in figure 2(b). The process occurs homogeneously over the whole array. The outer diameter of the tube does not vary with the etching time, what is related to the doping level of Si that and the consequent thickness of the SCR, as it will be elucidated further down in the manuscript.

In order to further explore the mechanisms of the tube formation, we have investigated the effect of the solution pH and doping level of Si. We used Si pillars with 3 different doping levels: $10^{17}$, $5x10^{15}$ and $5x10^{14}$ $cm^{-3}$; as determined by the respective resistivity 0.1-0.5 Ωcm, 1-10 Ωcm and 15-25 Ωcm. All these structures were etched at pH 0 and 5, respectively with a HNO and BHNO solution. Representative SEMs of the structures obtained under the different conditions are shown in figure 3. The SEMs resulting from the etching at pH=0 - figure 3 (a-c), were obtained after only 5 minutes of etching. The SEM of the structures obtained with pH = 5 were performed after 150 min of etching. We note that the substrate and solution conditions affect directly the etching speeds. Different etching speeds as a function of pH and electrolyte composition have been reported in the past and will be explained later[46,59]. For some of the conditions (especially figure 3 (d,e)) the tubes become faceted. We attribute this to the different dissolution activation energies for the different crystalline planes. These depend both on the doping concentration[60] and pH[46,47,61,62], which explains why faceting was clearly observed only in some of the conditions.

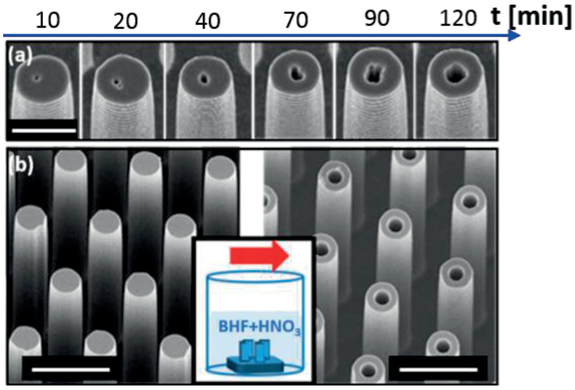

Figure 2 – SEMs of the Si pillars upon etching in the BHNO solution. a) Evolution of the morphology (b) original array and result after 150 min of etching.

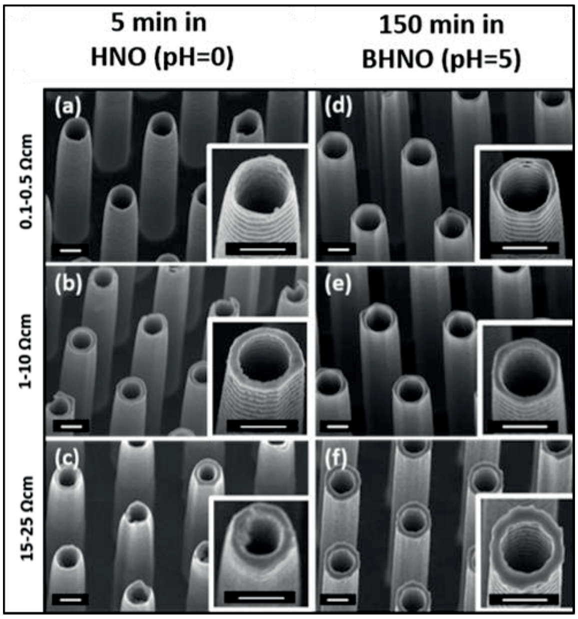

Figure 3 - Silicon tubes formed by stain etching (a-c) in the HNO solution at pH 0 for 5 min and (d-f) in the BHNO solution at pH 5 for 150 min. Different doping levels of Si were used, defined by resistivity values for each row respectively. Scale bar for all images is 2 μm.

So far, we have given a phenomenological illustration of the tube formation as a function of the pH and doping concentration. In the following, we move a step forward to model in a more precise manner the tube formation. For this, we consider the formation of the SCR at the semiconductor/electrolyte interface. It will be shown that the higher depletion length the pillar outer surface helps to redirect the etching to other regions –e.g. inside the pillar forming a tube- and thus to preserve the external walls[46,47]. In the case of the high aspect ratio silicon micropillars in contact with the electrolyte, the depletion layer is formed at the curved surface in the same way as in the case of the planar geometry. In order to explain the effect of geometry on the SCR formation at the semiconductor/electrolyte interface, charge depletion region widths were derived for representative geometries. Cylindrical and spherical concave and convex morphologies were chosen, both in the tubular and spherical geometry. The results on these configurations will help us understand the evolution of the SCR at the pillar surfaces and inside the tube once formed. Comparison with the planar configuration will also help us understand where dissolution is more preferable to start. The geometries used are sketched above the plot in figure 4. Solutions of the Poisson equation in silicon near the interface for the spherical and cylindrical convex and concave geometries were calculated. The resulting equations are a function of the SCR width for planar surfaces, $W_P$. Derivations in reference to the $W_P$ were obtained following the work by Luscombe and Frenzen[63], Zhang[64] and Nersesyan and Petrosyan[65]. For simplicity, the full depletion approximation was used[66]. As boundary conditions we fixed a finite potential at the surface, and vanishing potential and electric field at the boundary of the depletion region.

Table 1. Expressions the depletion region widths for spherical and cylindrical convex and concave geometries on the curvature radius $R$. $W_{Scv}$, $W_{Scc}$, $W_{Ccc}$ and $W_{Ccv}$ stand for depletion widths in spherical convex, spherical concave, cylindrical concave and cylindrical convex geometries, while $W_P$ stands for the depletion width of the planar semiconductor under the same conditions.

| Geometry | *Depletion width* |
|---|---|
| Spherical convex | $W_{Scv} = W_P\left(1 + \frac{W_P}{3R} + \frac{5W_P^2}{18R^2} + \cdots\right)$ |
| Spherical concave | $W_{Scc} = W_P\left(1 - \frac{W_P}{3R} + \frac{5W_P^2}{18R^2} + \cdots\right)$ |
| Cylindrical convex | $W_{Ccv} = W_P\left(1 + \frac{W_P}{6R} + \frac{W_P^2}{9R^2} + \cdots\right)$ |
| Cylindrical concave | $W_{Ccc} = W_P\left(1 - \frac{W_P}{6R} + \frac{W_P^2}{9R^2} + \cdots\right)$ |

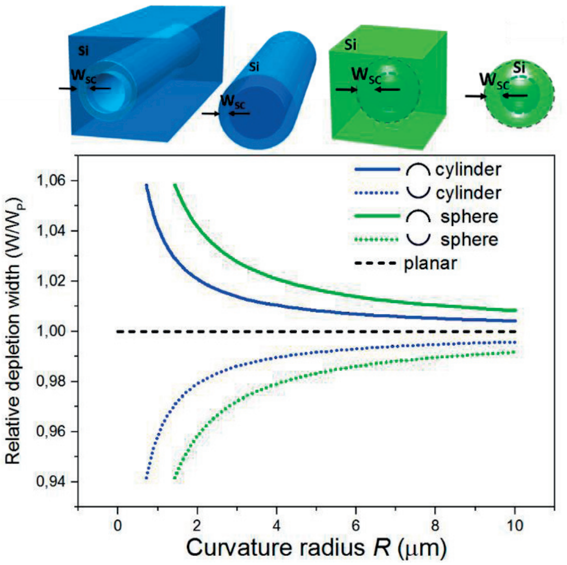

Figure 4. Dependence of the depletion region widths for cylindrical and spherical convex and concave geometries on the curvature radius $R$, compared to a semiconductor with depletion region width of $W_p$ in planar geometry, according to equations given in Table 1. Depletion region widths are given relative to the depletion width of a planar semiconductor,

$W_P$. Above the plot there are the schematics of considered geometries: concave and convex cylindrical (in blue) and concave and convex spherical (in green). The main equations describing the width of the SCR for the different geometries summarized in Table 1. For the derivation of the equations please see SI 4.

In figure (4) we show the relative difference in the width of the SCR for four different curved geometries, in relation to the width of the SCR for a planar semiconductor. We have calculated the SCR widths for a semiconductor sphere and infinite cylinder (the convex case), as well as for a spherical void inside a semiconductor, and for infinite cylindrical void inside of a semiconductor (concave case). The results show that in the case of concave geometries the width of the SCR is less than in the case of the planar semiconductor, while in the case of convex geometries the SCR widths are larger. Due to the relative nature of the calculations, the results are applicable to any semiconductor in depletion regime, regardless of the doping level or width of the SCR in planar geometry. The values of SCR are the highest for convex geometries and lowest for concave geometries. While the absolute difference is not very large, this becomes highly relevant for structures approaching the few micrometer size and below. The width of the SCR is smaller in the planar than in the convex case. As a consequence, the dissolution process should occur more preferably at the top flat facet of the pillar with respect to the curved side surfaces. In addition, once a small pore is formed, the surface becomes concave and SCR is reduced thereby increasing the dissolution rate. This is in the agreement with the time evolution of pore formation presented in figure 1. In the cases where the space charge region is thin, such as with highly doped silicon, etching can also occur on the side facets of the pillars. This etching is faster for preferred crystalline directions. As a consequence, facets with the lowest etching velocity develop. The sharp corners intersecting the facets exhibit a higher SCR due to their strongly reduced radius and therefore remain protected. This lateral etching and faceting of the pillars is clearly visible in figures 3 (d-e) as thinning of the sidewalls towards the top of the tube.

In order to further elaborate on the geometry dependence on the tube formation, we investigated the etching of pillars with other cross-section geometry: triangular, square, pentagonal and hexagonal. A representative SEM of the array of the structure is shown in figure 5 (a). We used wafers with the highest and lowest resistivity -15-25 Ωcm and 0.1-0.5 Ωcm- in order to validate the role of geometry and depth of SCR in the etching process. Figure 5 (b-f) shows SEM of the different pillars shapes after etching for 6 minutes in the HNO solution. We distinguish two different behaviours depending on the doping. For the highest resistivity (figure 5 (b-d)) the SCR is thick so that etching is preferential on the top of the pillar but also on the flat facets. Etchings proceeds homogeneously through the whole structure. The etching at the top of the pillar is shallow, compared to the structures obtained with the cylindrical pillars. For the lowest resistivity (figure 5 (e-f)), the SCR is so thin that etching occurs homogeneously through the whole structure. Interestingly, we observe that the tops of the pillars do not seem attacked. We attribute this to the facet selectivity of the reaction: e.g. (100) vs (110).

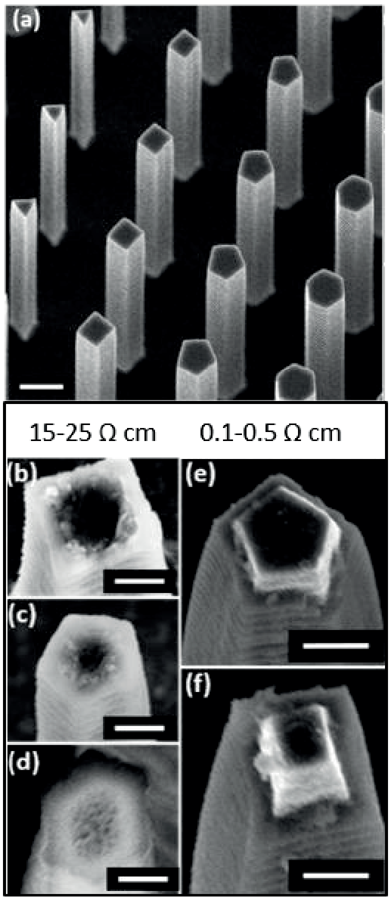

Figure 5. SEM of arrays with Si pillars with different cross-sections (a) and the corresponding morphology after 6 min etching in the HNO solution (b)-(f). Scale bars are 10 µm wide.

In order to elucidate the structure and composition of the porous structures, transmission electron microscopy transmission electron microscopy (TEM) was performed. The TEM analysis was performed on the Si pillars with lowest resistivity used (0.1-0.5 Ωcm) treated for 5 minutes in the HNO solution. In order to elucidate the structure and composition of the porous structures, scanning transmission electron microscopy (STEM) and energy dispersive x-ray spectroscopy (EDX) was performed in a FEI Tecnai Osiris microscope operated at 200kV. The pillars were broken off the substrate and transferred by softly wiping the sample with a TEM grid. Figure 6 (a) shows a STEM high angular annular dark field (HAADF) image of a pillar. The solid pillar and the hollow tube can clearly be distinguished. Figure 6 (b) presents the corresponding compositional EDX map, indicating silicon in blue and oxygen in green. We observe that the hollow tube is fully oxidized, while the solid part of the pillar shows an oxidized surface and significantly lower oxygen content in the center. Figure 6 (c-d) show a HAADF image and EDX map of the same pillar just below the beginning of the tube. We observe that the oxygen content at the surface of the pillar increases towards the top. As the oxidation rate of porous silicon is higher for higher porosity, this means that lateral etching is more pronounced on the side walls of the tubular part. Figure 6 (e) shows a HAADF image of the full tube, indicating a depth of approximately 11µm.

In addition, we characterized the tube depth for the sample with lowest doping level used (resistivity 15-25 Ωcm), treated for 150 min in the BHNO. Figure 7 (a) shows a typical SEM of the array cross-section prepared by ion beam thinning. We find that the depth of the tube is about a half of the initial pillar height. This result is similar to what we report in figure 6 (e), it seems that the tube does not progress till the bottom of the pillar. The tube progression may stop because of two possible reasons. First, the SCR at the bottom of the pillar may be influenced or screened by the bulk substrate. Secondly, the transport of the species necessary for the stain etching may be limited for high aspect ratio tubes and may deplete the solution inside. This could slow down or completely stops the advancement of tube formation [67].

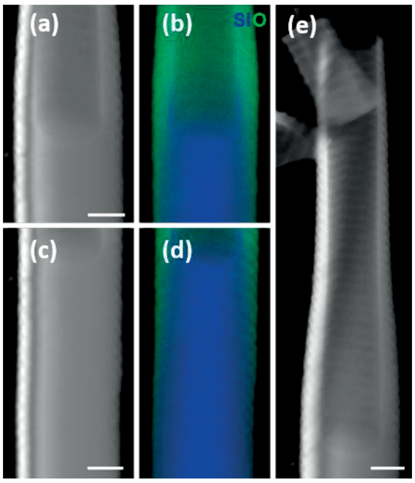

Figure 6 (a-d) HAADF and EDX compositional maps of the segments of the tube fabricated by 5 min etching of 35 µm long silicon pillars with resistivity 0.1-0.5 Ωcm in HNO solution (e) HAADF image of the drilled part of the same tube from (b-e). Both effects are visible drilling up to half height and lateral etching. The scale bar is 1 µm wide.

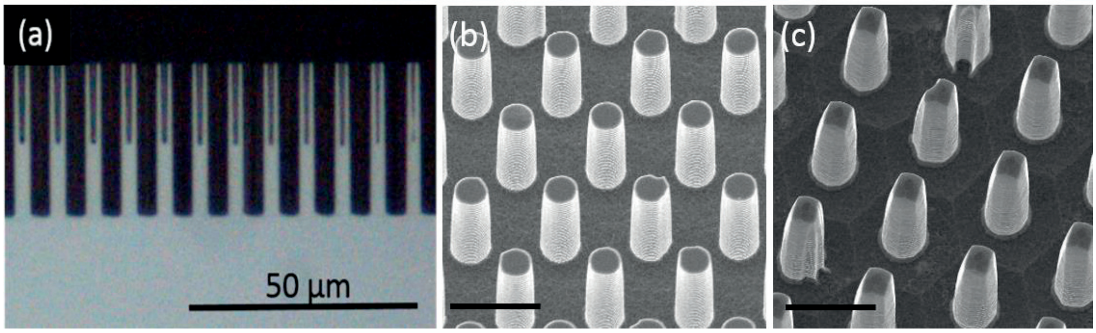

Figure 7 – (a) The cross-section prepared by ion beam thinning of the tube fabricated by 150 min etching of 35 µm long silicon pillars with resistivity 15-25 Ωcm in BHNO solution. The drilling goes half way through. (b) SEMs of short (12 µm) silicon pillars with resistivity 15-25 Ωcm in BHNO solution. In this case the drilling never occurred. There are no evidence of significant lateral etching (c) SEMs of short (12 µm) silicon pillars with resistivity 15-25 Ωcm in BHNO solution for 24 hours. Still no evidences of tube formation, just lateral etching and shortening of the pillars was observed. The scale bar for (b) and (c) is 5 µm and the tilt angle 20˚.

To try to understand if the stopping of tube progression can be assigned to any one of these options, a series of stain etching in both HNO and BHNO solutions for different times were performed on short pillars (12-18 µm) and for all three doping levels reported here. Figure 7 (b) shows a SEM of short (12 µm) silicon pillars with resistivity 15-25 Ωcm in BHNO solution. All the parameters are the same as in for the sample in figure 7 (a) beside the pillars height. No tube formation or significant lateral etching was detected. The tube formation was not observed not even after 24 hours of etching (figure 7 (c)), but we found that pillars got shortened, and they were etched laterally. This result indicates that the propagation of the tubes in not limited exclusively by the reaction induced depletion of solution species, but it is probably also related to the change in hole distribution due to vicinity of the bulk of the substrate. The result of the same experiment for the highest doping level used (0.1-0.5 Ωcm is presented in the SI 2.

## 3. Optical characterization

For the optical characterization of the Si tube arrays we used photoluminescence (PL) and cathodoluminescence (CL) spectroscopy. The samples used in the optical characterization and device fabrication were prepared in a two-step process. We started etching the pillars in the BHNO solution to create highly homogeneous tube arrays. We then exposed the structures to the HVO solution to form a more uniform porous layer -see refs.[24,44,68,69]-. We used silicon pillars with highest doping, since according to Nahidi the PL signal of the corresponding porous silicon is the strongest in this case [70].

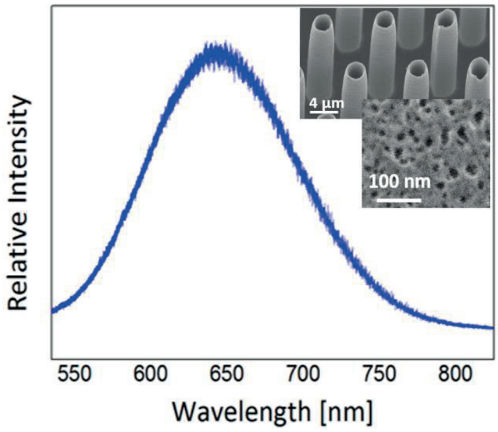

Figure 8. Photoluminescence spectrum of porous Si tubes fabricated by two-step stain etching process (BHNO and HVO)

Figure 8 shows a typical micro-PL spectrum of these samples. The excitation source is the 514.5nm line of an Argon-ion laser. A power of 1mW is projected on the sample by a 100X microscope objective. We observe a broad band centered around 650 nm. Similar PL spectra are observed in most porous silicon samples, regardless the preparation. The inset in the figure shows the part of the microtube array and the zoom to the surface of the single microtube to present the porosity level. The two most commonly encountered luminescence emission bands reported for porous silicon are the "slow" or "S" red band, and the "fast" or "F" blue band. The S band is centered between 600 and 850nm, and it decays in the 10-100 ms scale. The origin of this luminescence is usually explained as radiative recombination from spatially confined excitons in the silicon nanocrystal. The F band luminescence, usually centered between 420 and 500 nm, decays in the nanosecond time scale. It can be observed on porous silicon samples aged in air or intentionally oxidized. It is thought to originate from the structural defects in the silicon nanocrystal oxide shell or from the luminescence from very small silicon nanocrystals[39,71–75]. Other PL bands have been previously reported for porous silicon: the so-called UV band (centered around 350 nm), and the R band (ranging from 1100 to 1500 nm)[60].

We proceed now with the CL characterization of the tubes. With respect to PL, scanning electron microscopy cathodoluminescence (SEM-CL) can excite luminescence with a much higher spatial resolution: the SEM-CL e-beam probe is few nanometers in diameter with respect to at least few hundred nanometers for the laser spot in micro-PL. It is also worth noticing that CL offers a way to access excitation energies beyond the UV. To the best of our knowledge, CL studies of porous silicon are rare. Figure 9 presents the results from the CL studies, performed in an Attolight SEM-CL microscope at the acceleration voltage of 7kV. In figure 9 (a) we show the SEM of the investigated region along with the mapping of the CL signal. We observe light emission from the sidewall regions, where there is an oxide. In the arbitrary color coding of the CL map, red and green correspond to the emission centered at 650 nm and 446 nm respectively. This emphasizes a redshift of the emission at the bottom of the tubes, which corresponds to half height of the full pillar. This position is indicated by a yellow arrow on one of the pillars in figure 9 (a). This region has the appearance of a necklace and we will thereafter refer to it as the necklace. The spectra from the top of the tube and from the necklace region (marked by the ° and * respectively on the CL map) are presented in figure 9 (b). With respect to the PL measurements, the electron excitation allows to access higher energy emissions. In fact, both spectra present two bands that can be identified as the F and S bands. The intensity ratio between the two types of emission changes with the position on pillar. The spectrum obtained at the necklace has a higher S/F intensity ratio compared to the spectrum obtained at the tube tip/walls. The F band is related to the defects at the silicon/silicon oxide interface[71,72,76]. The necklace region corresponds to the area where the tube is actively forming. The oxidization may still be incomplete, which could account for a higher presence of defects and the increased intensity of the F band. Similarly, the CL emission of both bands dims while moving away from the tube, especially below the necklace. This can be related to the lower presence of oxide towards the microtube bottom, as shown by the EDX mappings in figure 6 (b-d). Between the F and S bands there is also a possible third band at 580 nm that is marked with an arrow in the blue spectrum in figure 9 (b). One possible explanation could be the blue shift of part of the S band due to quantum confinement in silicon nanoparticles[30].

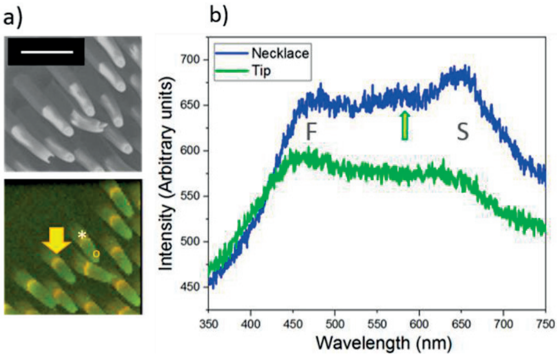

Figure 9 (a) – SEM (top) and CL map (below) of silicon micropillar arrays covered by luminescent porous silicon. In the CL maps, red and green correspond to the emission centered at 650nm and 466nm, respectively. The oxidation-related “F” band emission around 450 nm is especially bright at half height of the each pillar (necklace), while the quantum confinement related luminescence in the “S” band is dominant near the top of the porous pillars. Scale bar is 5 µm, (b) CL spectra acquired in two different positions on the tube – the green curve corresponds to the spectrum from the tube tip/wall and the blue curve to the spectrum taken from the interface at the so-called necklace.

## 4. Demonstration of 3D light emitting device

In this part, we demonstrate the functionality of these structures by fabricating a light emitting diode. For this, we evaporated an aluminum Ohmic contact to the back side of the sample and sputtered 100 nm of ITO on top of the porous silicon side as a transparent electrode. For more details experimental details see SI 1. The size of the active device was 7.15x7.75 mm$^2$, area that we used for the calculation of the current density -although the real effective area of the diode surface is higher. Current-voltage diode characteristics of the device are shown in the figure 10 (a). We show both the device characteristics in the dark and under AM 1.5G illumination conditions. Under solar illumination we obtain a $V_{OC}$ of 0.34 V, $J_{SC}$ of 25 mA/cm$^2$ and a fill factor of 27%. Fitting of the first quadrant of the current-voltage characteristics gives an ideality factor of 2.5 –more details in SI 3. We obtain a power conversion efficiency of 2.3%. The rectifying ratio of the solar cell in the dark between -4 and 4 V was $10^4$. The relatively high reverse currents, relatively low fill factor, $V_{OC}$ and PCE are indicative of high surface recombination of the photogenerated charge carriers. Dangling bonds in porous silicon provide defect levels in the bandgap of silicon and should be the main responsible for the observed charge recombination[76–81].

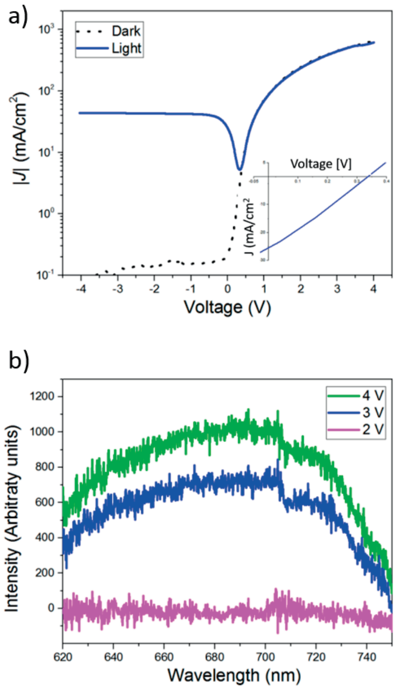

Figure 10 (a) Absolute J-V characteristics for the Si-tube array device taken in the dark and under illumination by a solar simulator set at the irradiance of 100 mW/cm$^2$. The inset shows the J-V curve between 0 V and 0.4V, outlining the $V_{OC}$ and $J_{SC}$. (b) Electroluminescence spectra of the same device at different operation voltages showing wide-band light emission.

We measured the electroluminescence of the device by applying a forward bias. The resulting spectra are shown in Figure 10 b). We observed wide band electroluminescence centred around 690 nm. EL emission starts to be detected for an applied voltage of 3 V and it further increases at higher bias till 4 V. For higher voltages the emission is quenched. The emission is recovered when the voltage is further reduced to the 3-4 V range. The reference planar devices prepared under the same conditions did not show any measurable EL. The EL device was stable during the whole length of the measurements –few hours.

## 5. Conclusions

In conclusion, we have investigated the electroless formation of porous silicon tubes, organized in an ordered manner. By looking at the tube formation as a function of the pillar size, geometry, doping we have pointed out to the main formation mechanisms. In particular, we have shown how the 3D geometry creates an inhomogeneous SCR that provides least resistance paths for an inhomogeneous etching. The optical properties of the porous structures are in agreement with the characteristics of Si nanocrystals and porous silicon, as shown by the photo and cathodoluminescence studies. Finally, we demonstrate the functionality of our 3D structures by fabricating a diode structure. The diode can work both as a solar cell or detector and as a light emitting diode. This work shows how silicon microtube arrays can be used for optoelectronics, with possible further advantages in photo electrochemistry, in battery electrodes and supercapacitors.

## AUTHOR INFORMATION

Corresponding Authors

*corresponding authors: anna.fontcuberta-morral@epfl.ch, ivanda@irb.hr

Present Addresses

† Department of Science and Technology (ITN), Linköping University, Campus Norrköping, SE-601 74 Norrköping, Sweden, is the present address of V.Đ.

Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript. ‡These authors contributed equally.

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## 3.2 Ordered arrays of GaAs nanowires on Si: study of initial stages and optimization of the yield

Integrating GaAs nanowires in the form of array on Si substrates opens great perspectives for next generation solar cells and for the optoelectronic industry. The best way to realize this integration is to perform growth without the assistance of gold via selective area epitaxy or self-assisted VLS growth. Gold free growth is a demand of compatibility with CMOS technology. The VLS mechanism is preferred over SAE since it provides a better control on the polytypsm. Most application using nanowire arrays need a precise engineering of the nanowire orientation and morphology. In this section we pave the way to convene with these requirements. In spite the strong arguments for obtaining ordered growth of GaAs on Si, the number of papers published on this topic are scarce. Figure 3.4 shows representative SEM images of high yield arrays of GaAs NW published by Plissard et al [99] and by Munshi et al [184]. They report on high yield arrays, with over 90% of vertical wires, and provide some key elements for achieving them. Among the others, authors point to a Ga predeposition step and the nature and thickness of dielectric layer to play an important role. In this thesis we took these initial works as a base to then look for more fundamental aspects governing the nanowire orientation.

This chapter is followed by two manuscripts on this topic. The first work resulted from serendipity. While studying the growth conditions and substrate preparation that led to higher yield in vertical growth of nanowires, we noticed that a certain batch gave much better results. It turned out that this substrate had an amorphous silicon layer between the oxide and the silicon substrate, originated in a mistake in the substrate fabrication. In this first paper high yield arrays were obtained thanks to the Ga droplet pinning on the amorphous Si inside of the nanoscale openings [185]. The existence of amorphous layer in the substrate prior

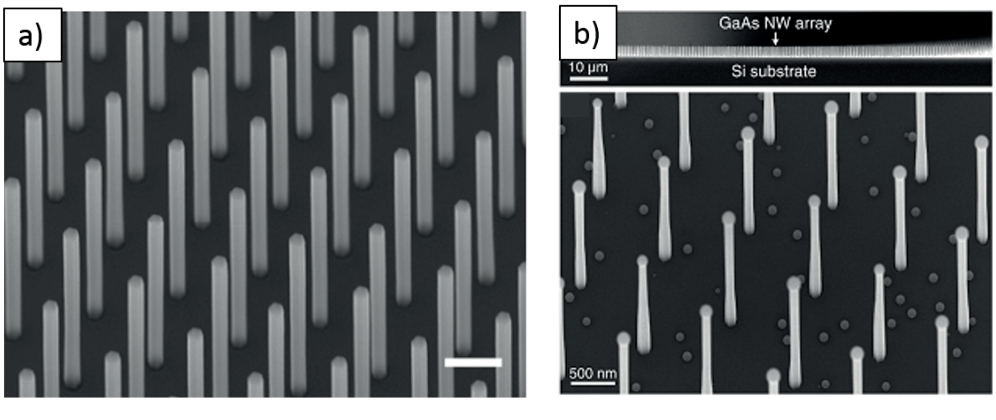

Figure 3.4 – High yield GaAs nanowires obtained from different authors: a) Plissard et al [99](©2017, Nanotechnology, IOP Publishing), b) Munshi et al, where NIL was used as patterning technique, so the large scale arrays were obtained [184] (©2017 Nano Letters, American Chemical Society).

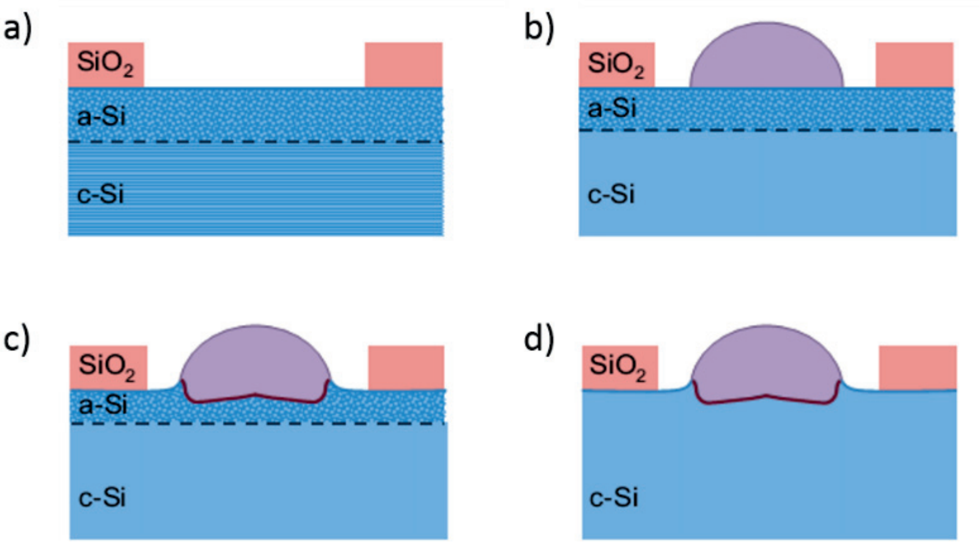

Figure 3.5 – Sketch of the proposed mechanism for the pinning of the Ga on the a-Si surface exposed to growth: (a) A patterned silicon substrate with an underlying thin layer of a-Si is introduced in the MBE. (b) The Ga droplets are formed on a-Si while this starts to crystallize. (c) The Ga droplets alloy with a-Si before it is completely crystallized. (d) The Ga droplets remain pinned on the substrate thanks to the alloy formed mostly at the triple-phase line of the droplet. Adapted from [185], ©2017, Nano Letters, American Chemical Society.

to growth was not intentional and it was discovered by cross-sectional TEM analysis. High yield growth required special growth conditions that involved the Ga predisposition step starting at temperatures well below the NW growth temperature. Normal range of growth temperatures for GaAs nanowires on Si are between 605 and 640°C [105, 99, 184]. In our case, high yield arrays were obtained only when the Ga predeposition started below the growth temperature (around 200°C). The reason for this is recrystallization of amorphous Si that occurs around 600°C [186]. If the growth temperature was reached before Ga supply started, the thin amorphous layer would recrystallize and the pinning of Ga droplet with amorphous silicon would not occur. In Fig. 3.5 we present a schematic drawing of the mechanism of the pinning of Ga droplet that yielded successful growth. The important point to note is that the Ga droplet on the surface of amorphous Si exhibit contact angle around 90o, optimal in promoting vertical growth (Fig 3.5a). The alloying of amorphous Si by Ga droplet during the heating process pinned the droplet. In this way, the contact angle was preserved even after total recrystallization of amorphous Si underneath. These results were very encouraging. However, the existence of the amorphous layer below the silicon dioxide could not be found in any other batch. For this reason we looked in other ways of preparing the substrate to obtain a high yield of vertical growth.

The correlation between droplet wetting angle and nanowire orientation is illustrated in Fig. 3.6a. Here, different wetting is obtained varying the surface energy of the substrate due to the change in native oxide composition (thickness) [105]. The optimal wetting angle leading

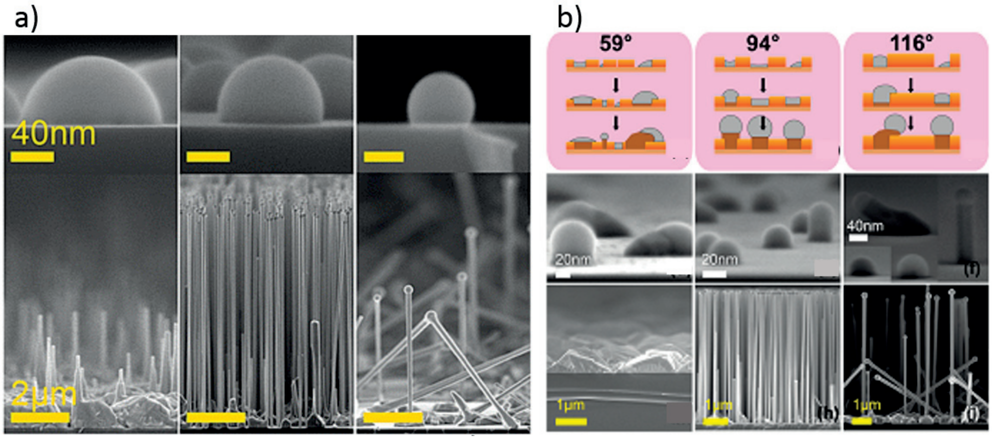

Figure 3.6 – a) SEM images of Ga droplet on the Si substrate with thin layer of native oxide. The thickness increase from left to right what changes the wetting properties, with direct impact to the growth. On the central figure the oxide thickness was around 1 nm, what was found to be the optimal one for vertical nanowire growth (adopted from [105], ©2017 Crystal Growth & Design, American Chemical Society). b) Energetically most favorable droplet configurations and their evolution upon nucleation of the GaAs, for Ga/SiO$_x$ equilibrium contact angles of 59°, 94°, and 116°, respectively and corresponding growths outcomes (adopted from [106], ©2017 Crystal Growth & Design, American Chemical Society)

to high yield of vertical wires in self-assembly was around 90o. This droplet configuration was obtained for a native oxide thickness around 1 nm. Using thinner or thicker native oxides lead to a contact angle different from this ideal value (Fig. 3.6a). In both cases growth was unsatisfactory, as shown on the corresponding figures below. This study by Matteini et all was extended to the identifying the mechanisms that lead to the different growth orientations [106]. First, it was demonstrated that pin holes in the oxide serve as Ga nucleation sites for the Ga droplets. The study was extended by a numerical model where they calculated the energies of formation of Ga droplets as a function of their volume and the oxide surface energy in several nucleation configurations. Different droplet configurations were associated with corresponding growth scenarios (vertical and tilted wire or parasitic growth).

Fig. 3.6b on the top shows the energetically most favorable droplet configurations and their suspected evolution upon nucleation of the GaAs, for Ga/SiO$_x$ equilibrium contact angles of 59°,94°, and 116°, respectively. Correlation between the Ga droplet configurations with the growth outcome is shown in SEM images shown below. The symmetrical droplet configuration leads to vertical growth, while non-uniformly spilled droplets tend to evolve into tilted NWs or parasitic growth. Up to one level, these results can be applied to guide and interpret the growth results of GaAs nanowires on patterned Si substrates. Before, we should point out to the differences between these two systems:

- The oxide used for the arrays is thermal oxide, which exhibits almost perfect stoichiometric composition and is therefore extremely stable with temperature compared with native $SiO_x$x. Its thickness was around 10 nm instead of ~1 nm.

- Nanoscale holes are predefined prior to the growth process. The formation of additional nucleation sites in the oxide layer is not possible due to the thickness and stability of the oxide.

### 3.2.1 Design and characterization of the growth substrate

Each sample contained arrays of holes with different nominal[1] diameters: 30, 45, 60, 75 and 90 nm. They were defined by e-beam lithography and transferred into the oxide layer by a combination of RIE and BHF. To ensure a precise etching of the oxide, the thickness of the oxide was characterized combining spectroscopic ellipsometry. The complete etching of the holes till the silicon substrate was also checked with atomic force microscopy (AFM). Also, the inter hole distance (pitch) was varied from 200 to 2000 nm with 200 nm increment, even though already in our previous work we reported that vertical yield was pitch independent [185].

Following the idea of reference [106], presented in Fig. 3.6b we started by looking for the optimal Ga droplet configuration within the openings. For this, we exposed the patterned substrates to the Ga pre-deposition for 2, 5, 7, 10 and 15 minutes. We used a Ga rate of 1.1 Å/s and substrate temperature of 630 °C,. The configurations of droplet within the different hole sizes were analyzed by SEM and AFM. In Fig. 3.7a we show representative SEM images of the droplets in the 45 and 90 nm holes obtained with a 5, 10 and 15 minute predeposition. The 45 nm holes are fully filled after 10 minutes. After 15 minutes the edge of the hole cannot be detected any more. For the largest holes, the droplet formed during 10 minutes seems to fill the hole, but the edges are still clearly visible. Also after the 15 minutes they inflate over the hole edge. The AFM measurements allowed us to access the droplet shape and profile, giving information on the droplet configurations (Fig. 3.8b). The impact of the droplet configuration on the vertical yield was tested by 1 h growth, under an $As_4$ partial pressure of $2 \times 10^{-6}$Torr. Representative SEM images of the growth are presented in Fig. 3.7b). The best yield was obtained for 45 nm holes and 10 min of Ga predeposition time, indicating which would be the optimal droplet shape and size. After 15 minutes of predeposition, Ga droplets are filling the 60—90 nm holes in a more symmetrical manner. This is also translated into a better yield with respect to the 10 min predeposition. Indeed, for shorter Ga predeposition time mainly parasitic growth was observed. These results are quantified by histograms that are presented in Fig. 3.8a. Figure 3.7c,d show closer view to the arrays with the best yield for each predeposition time. They are related to the hole sizes and Ga deposition step by the frame colors.

We find a relatively good correlation between the droplet configuration and the vertical yield. Still, this is not enough to understand what really determines nanowire orientation in the initial stages of the growth. We tried to capture the initial stages of growth by performing a

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[1] Final hole size were enlarged due to the BHF dip for 10-15% of its nominal values, what was carefully monitored by AFM. Further in the text we will use nominal values to refer to each hole size.

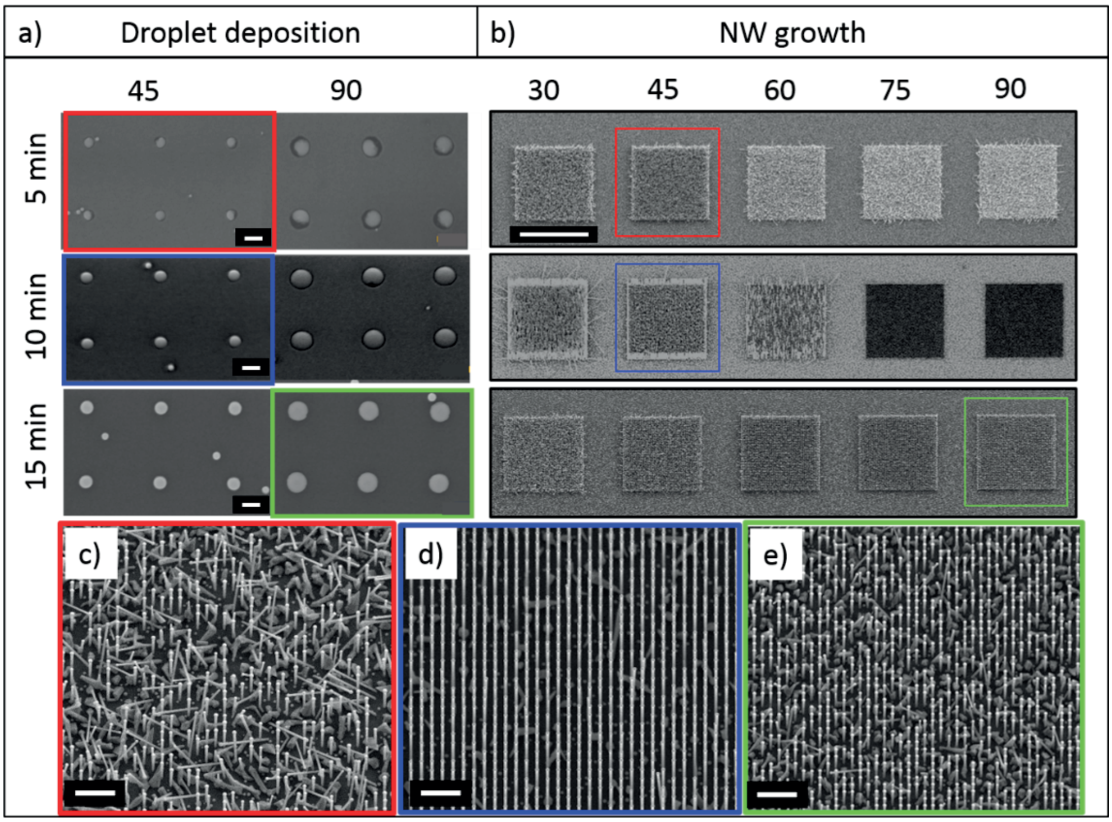

Figure 3.7 – a) SEM images of Ga droplet formed during 5, 10 and 15 minutes within openings of 45 and 90 nm. The scale bar is 200 nm. b) Large view on the yield of arrays with different holes sizes from 45 to 90 nm for different Ga predeposition times. Scale bar is 40 $\mu$m, and tilt angle 20°. c-e) closer view on the arrays grown after 5, 10 and 15 minutes of Ga predeposition. The hole size was 45 nm for c) and d) and 90 nm for e). The scale bar is 1 $\mu$m and the tilt angle 20°.

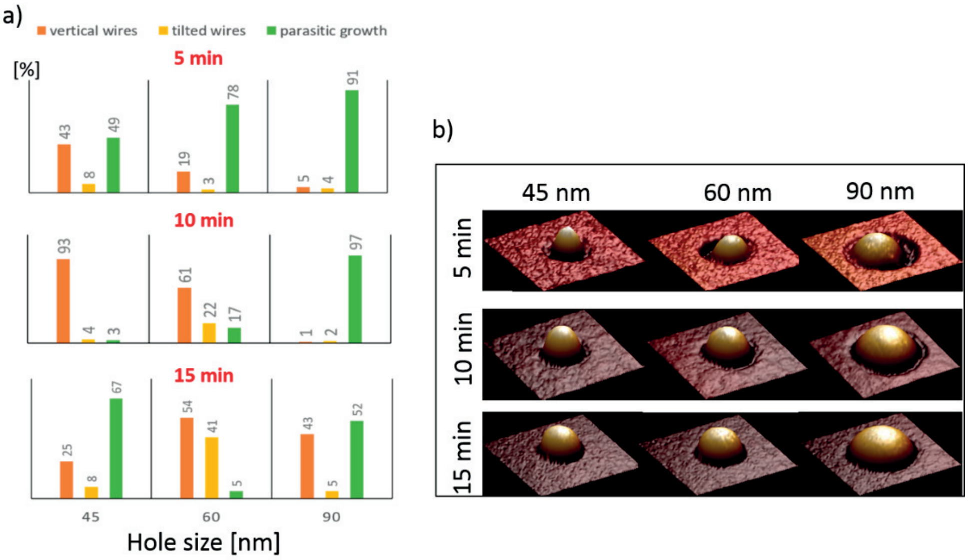

Figure 3.8 – a) The yield of vertical wires, tilted wires and parasitic growth as function of the hole size and Ga predeposition time: from top to bottom Ga predeposition time was 5 min, 10 min and 15 minutes. b) AFM topography of the droplet in different openings formed during different deposition times. The scale bar is 50 nm.

very short growth of 2 minutes. In order to understand how the seeds of NWs with different orientation start, we looked underneath the droplet at this stage of growth. For this, the droplets were removed by etching them in a HCl solution. In the first row of Fig. 3.9 we present SEM images of the growth after 2 minutes for 45, 60 and 90 nm holes while second row reveals the seed particles formed underneath the droplets. The third row shows growth results after 10 minutes where the grown features are well defined. Comparing the two bottom rows we can associate the GaAs seed formed at the side of the hole with the nucleation tilted wire or parasitic growth, and the one completely filling the bottom of the hole with vertical wire formation. It is interesting to note that tilted NWs nucleate faster than vertically oriented. In Fig. 3.10a the percentage of different features underneath the droplets for three hole sizes is presented. In the legend one can see how we categorized the observed features: seed formed on the side (yellow), and layers completely filling the bottom (orange). The third group of features correspond to the ones that could not be well categorized, so they were considered as special group (green). The EDX analysis was performed on the seeds in order to confirm GaAs precipitation. The SEMs with corresponding EDX spectra are shown in Fig. 3.10b. In both spectra, GaAs was detected. The vertical yield estimated based on the seed particle form matches very well with the one presented in Fig. 3.8. We can conclude that a droplet that nucleates asymmetrically within the opening will promote growth of the tilted wire or parasitic growth, while symmetrical droplets will lead the vertical growth.

A step further towards understanding the formation of tilted or vertical wires was to look into the crystal structure of the nuclei at the Si/GaAs interface. For this purpose FIB lamellae

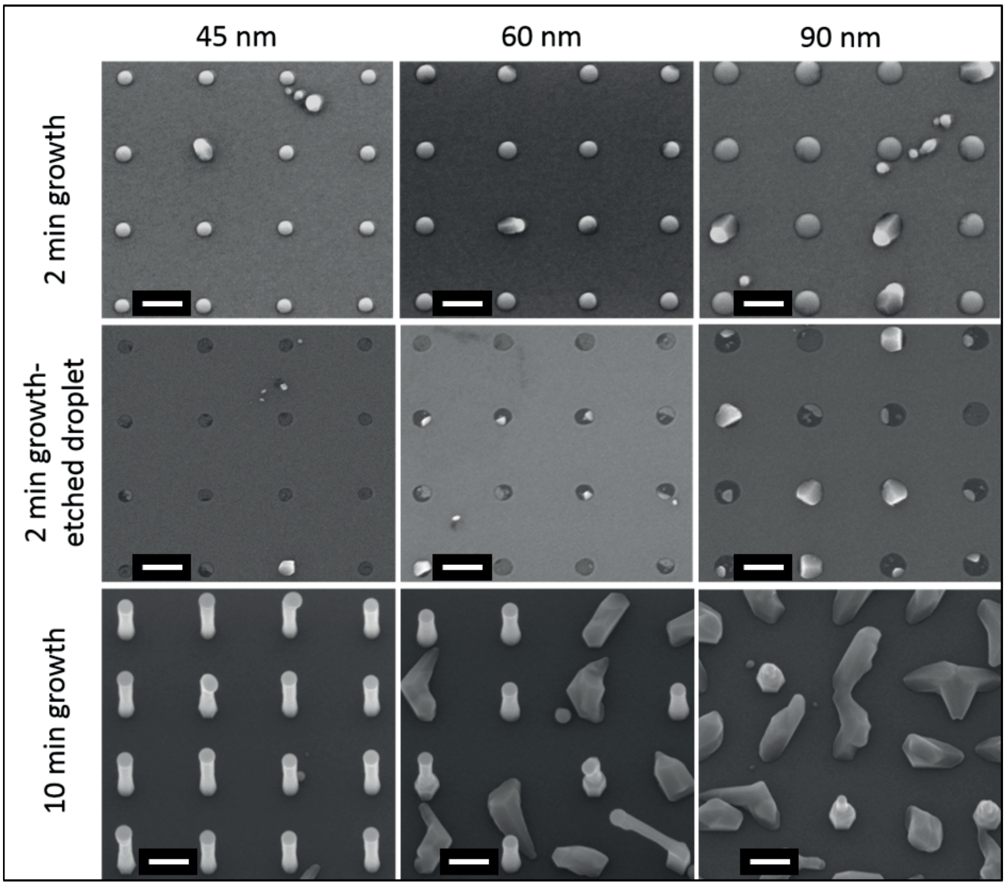

Figure 3.9 – Top row : 2 minute growth outcome for the 10 minutes Ga droplet using Ga flux of 1.1 Å/s and As partial pressure of $2 \times 10^{-6}$Torr. The results are shown for 45, 60 and 90 nm holes. One can observe higher occurrence of tilted wires in the bigger holes, where droplet wasn't symmetrically filling the opening. Central row: 15 minutes etching in HCL reveals GaAs seeds formed underneath the droplets. Bottom row: Results of the 10 min growth in the same conditions. The seeds forms can be related with the formation of vertical and tilted wires. The scale bar is 200 nm and tilt angle 20°.

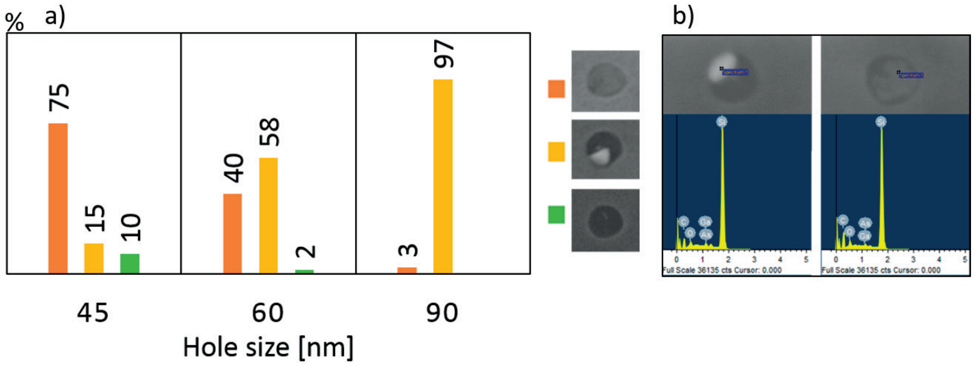

Figure 3.10 – The statistical analysis of the different GaAs seeds formed after 2 min of growth, revealed thanks to Ga droplet removal.

were prepared on the 10 nm grown sample in the 60 nm holes. The position of the cut was chosen in a way to get few examples of both structure types. Representative TEM images for tilted and vertical wire are shown in Fig. 3.11. The vertical nanowiress show the standard polytypic crystal structure with stacking defects perpendicular to the (111)B growth direction (as introduced in Section 2.3). In the case of the tilted nanowiress we found the presence of rotational twins at a 71° angle with respect to the substrate surface. This corresponds to the other possible growth direction of III-V nanowire on Si; i.e. (111)A, as it was explained in the Section 2.3. TEM investigations indicate the formation of the GaAs seed at the edge of the hole. This corresponds well with our assumption that the formation of the tilted nanowires starts at the edge of the holes. The sketch bellow presents droplet configurations with GaAs precipitating underneath.

To summarize, we can say that presented data nicely show how asymmetric droplet configuration relates to the different GaAs seed formation, which determines growth orientation with respect to the substrate surface.

Beside the vertical orientation of nanowires, their morphology needs to be controlled. The geometry of nanowire has direct impact on its optical and electrical properties, so for high performance devices, size distributions within the array (diameter and length) should be very narrow. Optimizing, both pattern fabrication and growth conditions, for reproducible growth of high vertical yield GaAs NW arrays we enabled the study of the evolution of size distributions in the initial stages of the growth. These results are presented in the second paper included in this chapter. The paper includes the time dependence of growth and the evolution of the NW morphology and model derived on the evolution of the NW elongation and diameter with time. Also, $As_4$ flux was considered as parameter that can be used for controlling the uniformity.

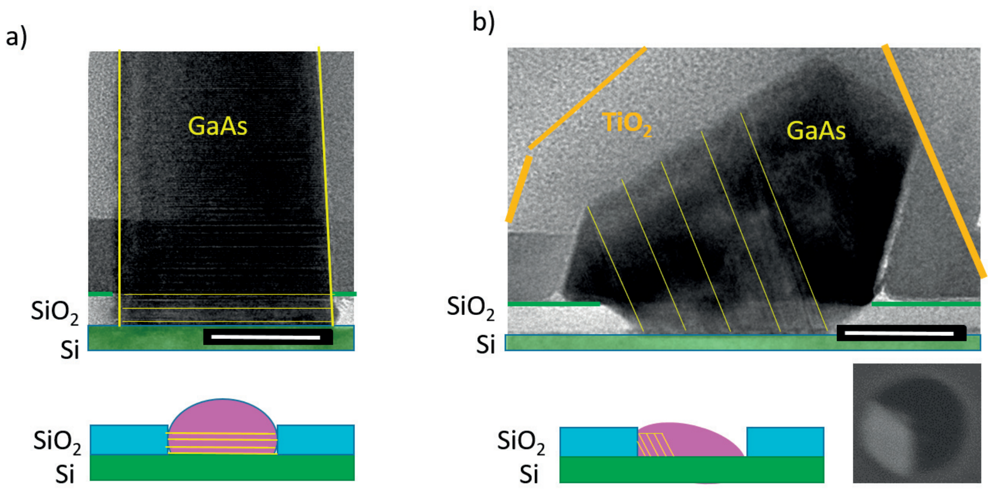

Figure 3.11 – Cross sectional TEM analysis of the tilted (a) and vertical (b) wires, both grown from the 60 nm holes. The growth occurs in two different 111 directions which determine the orientation of the nanowires. Crystalline structure can be associate with se seed formation under the droplet as sketched bellow TEM figures. SEM image of the tilted nanowire seed underneath the droplet is shown at bottom right.

### 3.2.2 Papers included in this section

**High Yield of GaAs Nanowire Arrays on Si Mediated by the Pinning and Contact Angle of Ga**

AUTHORS

Eleonora Russo-Averchi*, Jelena Vukajlovic Plestina*, Gözde Tütüncüoglu*, Federico Matteini, Anna Dalmau-Mallorquí, Maria de la Mata, Daniel Rüffer, Heidi A. Potts, Jordi Arbiol, Sonia Conesa-Boj, and Anna Fontcuberta i Morral

**equally contributing authors*

JOURNAL

Nano Lett., 2015, 15 (5), pp 2869-2874

MY CONTRIBUTION

- I took part in the substrate preparation and characterization
- I took the part in growth results analysis
- I took active part in the interpretation of the results

**Engineering the size distributions of ordered GaAs nanowires on silicon**

AUTHORS

Vukajlovic-Plestina, Jelena*; Kim, Wonjong*; Dubrovskii*, V.; Tütüncüoglu, Gözde; Lagier,

Maxime; Potts, Heidi; Friedl, Martin; Fontcuberta i Morral, Anna
**equally contributing authors*

JOURNAL
Submitted to Nano Letters

MY CONTRIBUTION

- I took part in the substrate preparation and characterization
- I planned the growth and other experiments
- I took part in growth results analysis (SEM imaging)
- I performed statistical analysis
- I took active part in the interpretation of the results
- I wrote parts of the manuscript

## 3.2. Ordered arrays of GaAs nanowires on Si: study of initial stages and optimization of the yield

NANO LETTERS
Letter
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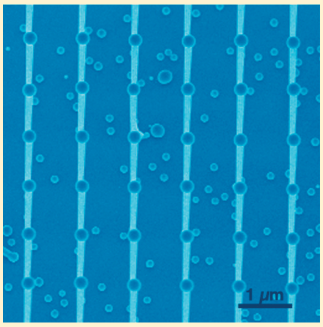
# High Yield of GaAs Nanowire Arrays on Si Mediated by the Pinning and Contact Angle of Ga

Eleonora Russo-Averchi,[†,∥] Jelena Vukajlovic Plestina,[†,∥] Gözde Tütüncüoglu,[†,∥] Federico Matteini,[†] Anna Dalmau-Mallorquí,[†] Maria de la Mata,[‡] Daniel Rüffer,[†] Heidi A. Potts,[†] Jordi Arbiol,[‡,§] Sonia Conesa-Boj,[†] and Anna Fontcuberta i Morral*[,†]

[†]Laboratoire des Matériaux Semiconducteurs, Ecole Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland
[‡]Institut de Ciència de Materials de Barcelona (ICMAB-CSIC), Campus de la UAB, 08193 Bellaterra, Catalonia, Spain
[§]ICREA and Institut Català de Nanociència i Nanotecnologia (ICN2), Campus UAB, 08193 Bellaterra, Catalonia, Spain

*Supporting Information*

**ABSTRACT:** GaAs nanowire arrays on silicon offer great perspectives in the optoelectronics and solar cell industry. To fulfill this potential, gold-free growth in predetermined positions should be achieved. Ga-assisted growth of GaAs nanowires in the form of array has been shown to be challenging and difficult to reproduce. In this work, we provide some of the key elements for obtaining a high yield of GaAs nanowires on patterned Si in a reproducible way: contact angle and pinning of the Ga droplet inside the apertures achieved by the modification of the surface properties of the nanoscale areas exposed to growth. As an example, an amorphous silicon layer between the crystalline substrate and the oxide mask results in a contact angle around 90°, leading to a high yield of vertical nanowires. Another example for tuning the contact angle is anticipated, native oxide with controlled thickness. This work opens new perspectives for the rational and reproducible growth of GaAs nanowire arrays on silicon.



**KEYWORDS:** *Ga-assisted GaAs nanowires, III−V on silicon, arrays, molecular beam epitaxy, vertical nanowires*

Semiconductor nanowires (NWs) have been the subject of extensive investigations in recent years, motivated in part by the unique physical properties provided by their essentially one-dimensional geometry. These novel properties, as well as new material combinations that can only be achieved with NWs,[1−3] offer a large number of potentially useful applications in a broad range of electronic, optoelectronic, and energy harvesting devices.[4−10] A particularly useful property is that their small diameter allows their growth on lattice-mismatched substrates.[11−13] A natural consequence is that NWs enable the integration of highly functional III−V compounds with silicon-based technologies.[14−17] This represents a unique opportunity to combine the advantages of III−V materials such as direct band gap and high mobility with Si, which is extensively used in microelectronics industry.[18,19]

In the past, regular arrays of NWs have been achieved by patterning a substrate with gold nanoparticles;[20−23] such a configuration demonstrated the rational use of NWs, showing their potential integration in mass-production applications. These pioneering works rely on the use of the gold droplets for the nucleation and growth of the NWs through the vapor−liquid−solid process (VLS); however, gold is a nondesired impurity in silicon technology, so other methods have been investigated for the growth of NWs on silicon substrates.[24−26] Ga-assisted growth is a successful example showing how this precious metal can be avoided for the growth of III−V NWs on III−V and on Si substrates.[27] Following this method, nanoscale gallium droplets collect arsenic from the gas phase. Subsequent supersaturation leads to the precipitation of GaAs underneath. The Ga droplet should be refilled continuously to ensure a sustainable growth. Applying this method, arrays of GaAs NWs have been obtained on patterned GaAs substrates,[28] whereas fabrication of GaAs NWs on a patterned Si surface has shown to be by far more challenging. One of the main challenges has been the reproducibility in obtaining high yield of vertical GaAs NWs. Key elements such as gallium predeposition, thickness and composition of the growth mask have shown to be important parameters for a successful growth.[29,30] Still, successful growths of GaAs NW arrays by the Ga-assisted method are rare in literature.[31−33]

In this work, we bring new elements of analysis for understanding how a high yield can be obtained for the growth of Ga-assisted GaAs arrays on silicon. We have found that the surface properties of the material exposed to growth is decisive for achieving highly controlled vertical GaAs NWs. We show in detail the case of amorphous silicon. Alloying of amorphous silicon with Ga in the predeposition step leads to a pinning of the droplet and adequate contact angle for vertical growth. Alternative layers such as native oxide are discussed at the end

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of the manuscript. Progress in the deterministic GaAs NW growth at selected positions on a Si substrate is the first step toward the rational fabrication of advanced devices on the silicon platform.

SEM micrographs of successful GaAs NWs arrays grown on Si(111) by a gallium predeposition during the heating of the substrate are shown in Figure 1. Figure 1a−d show tilted views of the NWs grown in patterns with a nominal hole diameter of 90 nm and an interhole distance of 400 nm at different magnification and with additional in plane rotation (d). Figure 1e shows the results for a larger interhole distance (1600 nm). The NWs are uniform in length and diameter. They present a slightly inverse tapering and a Ga droplet at their tip. The yield of vertical NWs—defined as number of openings nucleating vertical NWs divided by the total number of openings in the array—is 80%. The yield is independent from the interhole distance of the array. We notice that the 10% of the holes of the array do not lead to the nucleation of NWs because they seem to be closed. This could be due to an incomplete definition of the holes by the e-beam lithography. An optimization of the pattern definition could in principle lead to an improved yield of vertical wires. Only a few holes (5%) lead to the growth of tilted NWs. In the remnant, 5% of the holes we observe were parasitic and showed 2D growth. By subtracting the yield in hole fabrication, we obtain a yield in vertical nanowire growth of 89%. In the following, we demonstrate how this high yield can only be obtained in very special conditions of the nanoscale surfaces exposed to growth.

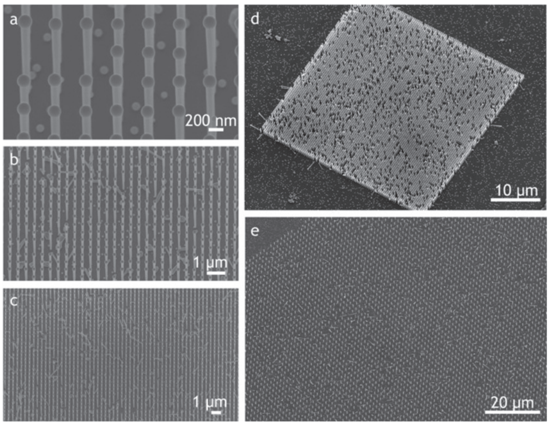

**Figure 1.** Scanning electron microscopy (SEM) images of GaAs nanowires grown on patterned Si(111) substrates at 630 °C, at a nominal Ga growth rate of 1 Å/s and under an As$_4$ partial pressure of $2 \times 10^{-6}$ Torr. (a−c) are 20° tilted images and (d−e) are tilted views with additional in-plane rotation. The yield of vertical nanowires is 80%. The hole diameter size is 90 nm for all the images. The interhole distance is 400 nm in (a−d) and 1600 nm in (e).

As found by other groups,[30,34] a gallium predeposition step has a strong influence on the yield of vertical NWs. We demonstrate how Ga predeposition is only useful in certain conditions by comparing growths in two different batches of Si wafers, one of them presenting amorphous silicon (a-Si) at the interface with the SiO$_2$ mask. Figure 2 (top) shows representative SEM images of the growth results obtained with and without the Ga predeposition, keeping all the other growth parameters unvaried. The two substrates originated from the same wafer, which we refer as "Wafer 1". As we can see in the picture, omitting the Ga predeposition step leads to an extremely low yield of vertical wires (6%) and a high density of nonvertical wires and parasitic growth. An identical set of growths, with and without the Ga predeposition, has been performed on a similar Si wafer of a different batch. We refer to these two samples as "Wafer 2". Figure 2 (bottom) shows the results of the growths. In this case, irrespective of the Ga predeposition, the yield of vertical wires is low and many tilted wires and parasitic growth are found on the substrates. The yield of vertical wires with Ga predeposition is 23%; omitting the Ga predeposition, the yield is 43%. We underline that these values of yield on substrates without the amorphous silicon layers are not reproducible. In this case, the yield oscillates between few and 45%. We show images from our best yield samples.

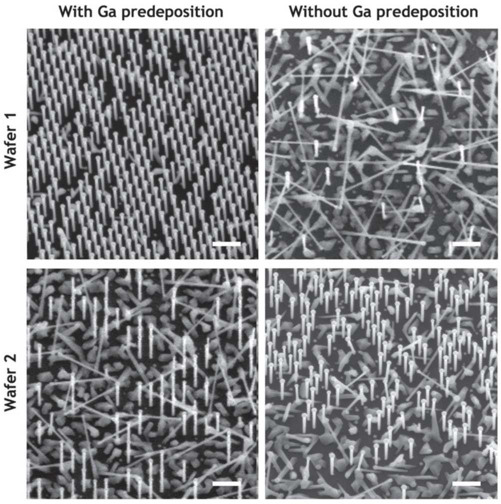

**Figure 2.** Tilted SEM micrographs of GaAs NWs grown in arrays defined on two different 4 in. wafers (Wafer 1 and Wafer 2) with and without the predeposition of Ga droplets. (Top) For the growth on Wafer 1, the yield of vertical wires strongly depends on the Ga predeposition. (Bottom) For the growth on Wafer 2, the yield of vertical nanowires is very low in both cases. For all the images, the interhole distance is 400 nm and the hole diameter size is 90 nm. The scale bar is 1 $\mu$m and the tilt angle is 20° for all the images.

We turn now to explain the fundamental difference between Wafer 1 and 2, since a priori they have been subject to identical sample preparation and growth protocols. To this purpose, lamellas containing cross sections of the substrates were prepared by focus ion beam (FIB) and the local structure and composition mapping investigated by transmission electron microscopy related techniques. We start by analyzing the structure of the Si chip in a region outside the pattern. Figure 3 displays cross-sectional high angle annular dark field (HAADF) images of representative samples of Wafer 1 and Wafer 2 taken at the interfaces between Si and the thermal SiO$_2$, and the corresponding energy-dispersive X-ray spectroscopy (EDX) maps. The same analyses have been performed on four chips, two of Wafer 1 and two of Wafer 2. Two samples correspond to remaining wafer pieces which had not been loaded in the MBE reactor, that is, they have been analyzed just after the sample preparation; the other two have been analyzed at the end of the

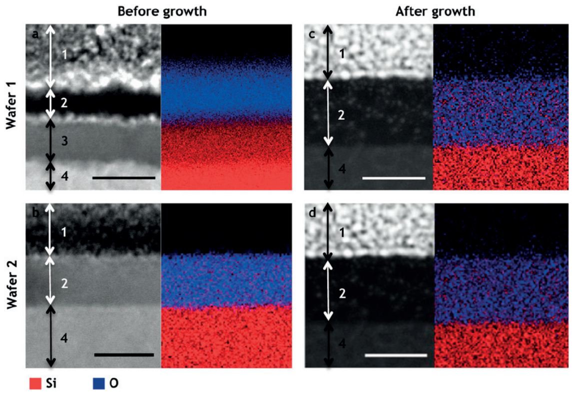

**Figure 3.** HAADF images of representative samples of Wafer 1 and Wafer 2, studied before and after growth, and corresponding EDX results, with the Si map in red and the O map in blue. The analysis is performed at the interface between the silicon substrate and the mask oxide. The numbers label the different layers analyzed: (1) protective layer for FIB preparation; (2) $SiO_2$; (3) a-Si layer; (4) c-Si. The sample from Wafer 1 shows an unexpected layer of a-Si that crystallizes after growth. The sample from Wafer 2 shows uniquely a thermal oxide layer grown directly on the crystalline silicon substrate. The scale bar is 20 nm.

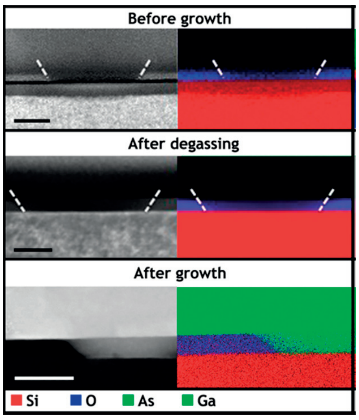

**Figure 4.** (Top) HAADF image of a nanoscale hole where the $SiO_2$, the amorphous Si and the crystalline Si can be distinguished and the corresponding EDX map. (Center) HAADF and EDX analysis of the hole degassed in the MBE reactor. The amorphous silicon layer is crystallized. (Bottom) HAADF and EDX analysis performed after the growth. A GaAs NW nucleates in the hole and grows vertically and also radially once higher than the hole. The scale bar is 50 nm. The lower EDX signal from the amorphous silicon layer is due to a different thickness produced by the faster erosion of amorphous with respect to crystalline silicon during the FIB process.

growth process and correspond to the samples depicted in Figure 2.

We first consider the pieces not loaded in the MBE (Figure 3a–b). The sample from Wafer 1 shows an amorphous layer between the crystalline silicon (c-Si) and the $SiO_2$. This 13 nm thick layer consists of a-Si, as confirmed by the lack of oxygen in the EDX analysis. Conversely, the piece from Wafer 2 shows the thermal oxide layer directly on top of the c-Si, as one would expect from the sample preparation. The $SiO_2$ layer of the chip from Wafer 1 has been found to be rather nonuniform, with thickness ranging from 10 to 20 nm, unlike for Wafer 2 sample, although an identical dry oxidation has been performed on the wafers. The analysis of the chips after growth is shown in Figure 3c–d. In this case, for both samples only thermal oxide is found on the crystalline silicon. Because the crystallization of amorphous silicon starts at temperatures higher than 500 °C, we think that it has crystallized during the heating of the substrate inside the growth chamber.[35,36] Our Si provider suggested that the amorphous layer was generated by the mechanical treatments such as slicing and lapping and by an insufficiently long chemical mechanical polishing (CMP) step at the end of the substrate preparation. We believe indeed that the large thickness of the layer of a-Si layer prevented its full crystallization during the thermal oxidation.

We turn now the attention to a patterned region of the silicon chip: cross-sectional HAADF images of nanoscale holes from Wafer 1 with the corresponding EDX maps are shown in Figure 4. The analysis has been performed prior to growth (Figure 4 top), after the degassing step in the MBE chamber (Figure 4 center) and after the growth (Figure 4 bottom). For the analysis of the sample after the degassing step the Ga shutter was kept closed, as we were interested in understanding the evolution of the substrate in itself. We observe the presence of an a-Si layer below the $SiO_2$ prior to degassing or growth. The a-Si layer, which is also observed at the position of the holes, is completely crystallized after the degassing and growth steps. After crystallization, the silicon surface at the bottom of the hole appears completely flat, as shown in Figure 4 (bottom).

Thus, we conclude that the presence of a layer of a-Si seems to be a necessary but not sufficient condition to guarantee a high yield of vertical wires and that the addition of the Ga predeposition is also required. We remind here that, in our case, the Ga shutter is opened at the very beginning of the growth process and, thus, is during the degassing step. During this time, the temperature of the Ga cell is ramping up to achieve a nominal Ga growth rate of 1 Å/s, and the substrate temperature is ramped up from 200 °C up to 770 °C at a rate of 50 °C/s for the degassing step. Therefore, the a-Si layer is expected to crystallize in a relatively short time once the substrate approaches the degassing temperature.[36] The Ga predeposition, however, already starts at lower substrate temperatures, when the a-Si layer has not yet crystallized. The Ga droplets are pinned on the a-Si at the bottom of the holes before it crystallizes. The a-Si reacts preferentially with the Ga, forming a Ga–Si alloy. This changes the force balance at the interface and thereby the contact angle. We have included a drawing of this process as well as measurements showing the preferential reaction with the substrate in the case of a-Si in the Supporting Information. As a consequence, when a-Si layer is used, the Ga predeposition should be performed during the heating process of the substrate.

Knowing that the characteristics of the Ga droplets affect the yield of vertical NWs,[37,38] we have looked for a more universal reason for the high yield. We compared the contact angle of the Ga droplets on amorphous and crystalline silicon, using the same process used for the successful nanowire growth. SEM micrographs of the Ga droplets obtained on the two kinds of surfaces are shown in Figure 5. The Ga droplets deposited directly on c-Si are also significantly larger than the ones observed on amorphous silicon. Gallium droplets pin in an easier manner on the surface of a-Si, leading to a higher density. The Ga droplets deposited on what initially was a-Si exhibit a

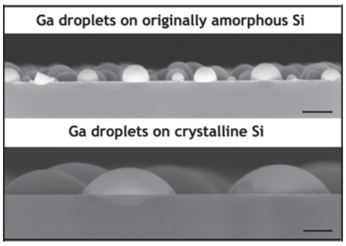

**Figure 5.** Cross-sectional SEM images of Ga droplets deposited on originally amorphous silicon (top) and on crystalline silicon (bottom). The droplets have different sizes and contact angles depending on the surface. The scale bar is 200 nm.

contact angle of 84 ± 4°; the ones deposited on c-Si have a contact angle of 52 ± 3°. It is well known that the contact angle affects the driving force in nanowire growth.[39] For example, contact angles much smaller than 90° render nucleation at the triple-phase line especially difficult.[40,41] Nucleation away from the triple-phase line favors nonvertical growth due to the so-called three-dimensional twining phenomenon.[37] An additional factor in patterned substrates is that the droplet should be smaller than the hole in order to avoid wetting on the oxide and raising of the triple-phase line away from the substrate. If the triple-phase line is located on the $SiO_2$, the loss of epitaxial relation with the substrate results in random orientation of the nanowires. Although this study has been performed on unpatterned substrates, we believe that it highlights important aspects of the initial stages of growth and how to obtain high yields of vertical wires.

We conclude that the size and the contact angle of the Ga droplets, resulting from their interaction with the substrate, play a fundamental role in the successful growth of vertical GaAs NW arrays by the VLS method. Our results suggest some possible modifications to the nanofabrication methods usually employed for arrays. In particular one should pay a particular attention to the wetting properties of the metal droplets at the open surfaces exposed to growth. Recent unpublished results show that an optimal contact angle close to 90° leads to high yield of vertical wires, which can be obtained by a careful control of the native oxide (see Supporting Information).[41] In that sense, we have used native oxide for engineering the contact angle of Ga droplets inside the nanoscale holes. Although the growth yield inside the holes is not yet close to 100%, most of the successful nanowires grow perpendicularly from the substrate (see Supporting Information). An advantage of this method is that the Ga droplet pins directly on the native oxide without the need for gallium predeposition. This initial data confirms the importance of engineering the contact angle of the metal used in VLS and could be used for other material systems. Finally, if amorphous silicon should be used at the interface between the substrate and the $SiO_2$ mask, it is necessary to use the optimal layer thickness around 15 nm, as the crystallization of the a-Si layer during the heating of the substrate for the growth becomes relevant (see Supporting Information). Alternatively, if the process should be compatible with thin amorphous silicon layers, the growth mask material should be reconsidered.

In conclusion, we have provided new elements for the achievement of a high yield of vertical GaAs NWs on a patterned Si substrate. The nature of the surface at the nanoscale holes opened in the mask is key. It determines the contact angle and position of the triple-phase line. We have obtained ideal conditions by using an oxidized Si substrate containing an amorphous layer at the interface with the crystalline substrate. Other treatments such as the creation of an appropriate native oxide layer may lead to a similar effect. The need of a gallium predeposition step depends on the nature of the substrate used. For example, it is not needed when engineered native oxide is used to pin the droplets with the required contact angle.

## ■ METHODS

**Sample Preparation.** Four inch ⟨111⟩ p-doped silicon wafers with a resistivity of 0.1−0.5 Ωcm have been patterned to realize the growth of GaAs NWs in arrays. After patterning, the wafers were diced into 35 × 35 $mm^2$ square chips sized for the MBE sample holder. The pattern consisted of a square arrangement of holes of sizes ranging between 90 and 150 nm; the interhole distance (or pitch) was varied between 200 and 2000 nm on the same substrate. The growth mask consisted of a 20 nm thick layer of thermal oxide obtained by dry oxidation in a Centrotherm furnace at 950 °C. The pattern was predefined in a ZEP resist with electron-beam lithography and then transferred on the oxide layer by a 12 s wet-chemical etching based on 7:1 buffered hydrofluoric acid solution (BHF). In order to ensure an oxide-free surface in the holes, the chips were shortly dipped in the same BHF solution prior to the introduction in the UHV chamber. The substrates were subsequently annealed at 500 °C for 2 h in UHV in order to ensure a pristine surface free of water and organic molecules. The substrate was then transferred to the growth chamber. There, they were degassed at 770 °C for 30 min to further remove any possible surface contaminants.

**Growth.** Ga-assisted GaAs NWs were synthesized at a nominal Ga growth rate of 1 Å/s, $As_4$ partial pressure of $2 \times 10^{-6}$ Torr, at a substrate temperature of 630 °C, and with 7 rpm rotation. In some of the growths, Ga was predeposited by keeping the shutter open since the ramp up of the substrate temperature for the degassing step. The $As_4$ source was opened once the growth temperature had been reached. Both sources ($As_4$ and Ga) were switched off simultaneously at the end of the growth. The samples were then cooled down to 200 °C and removed from the reactor.

*Wetting of Ga: Comparison between a-Si and c-Si.* A thin amorphous silicon layer was deposited by means of plasma-enhanced chemical vapor deposition (PECVD) on a Si(111) wafer. This a-Si and the c-Si substrates were exposed to BHF wet etching to ensure their surfaces were free of oxide; both samples have been heated to 770 °C for the degassing step with the increasing Ga deposition during the ramp up, simulating the initial step of our growth process. The contact angle and size of the droplets have been measured by cross section scanning electron microscopy.

*Transmission Electron Microscopy.* To characterize the morphology of the samples we used scanning electron microscopy (SEM) and transmission electron microscopy (TEM). High-angle annular dark-field scanning transmission electron microscopy and EDX analysis were performed using a FEI Tecnai OSIRIS microscope operated at 200 kV using the Super-X (0.9 rad collection angle) detector and Bruker Esprit software. TEM cross sections were prepared by using a Focus Ion Beam (FIB).

## ■ ASSOCIATED CONTENT

### Ⓢ Supporting Information

It contains a more detailed description of the proposed model, along with measurements showing the reaction of the Ga with the a-Si and the effect of the contact angle on successful vertical nanowire growth on Si. This material is available free of charge via the Internet at http://pubs.acs.org.

## ■ AUTHOR INFORMATION

### Corresponding Author

*E-mail: anna.fontcuberta-morral@epfl.ch.

### Author Contributions

‖These authors contributed equally to the work.

E.R.A., G.T., D.R., H.A.P., and F.M. contributed to the growth. E.R.A., J.V.P., G.T., and A.D.M. fabricated the samples and analyzed the results. J.A., M.d.l.M., and S.C.B. performed HAADF STEM and EDX analysis. E.R.A. made the figures and the artwork. E.R.A. and A.F.iM. wrote the manuscript in collaboration with all the authors. F.M. performed the contact angle measurements as a function of the nature of the native oxide of nonpatterned substrates. A.F.iM. supervised the project. All authors have given approval to the final version of the manuscript. We thank CMI and CIME for access to electron microscopy facilities and F. Bobard for the cross-section fabrication.

### Notes

The authors declare no competing financial interest.

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# Engineering the size distributions of ordered GaAs nanowires on silicon

*Jelena Vukajlovic-Plestina[1]*, Wonjong Kim[1]*, Vladimir G. Dubrovski[2,3,4]*, Gözde Tütüncüoğlu[1], Maxime Lagier[1], Heidi Potts[1], Martin Friedl[1], Anna Fontcuberta i Morral[1]*

[1]Laboratoire des Matériaux Semiconducteurs, École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland

[2]St. Petersburg Academic University, Khlopina 8/3, 194021 St. Petersburg, Russia.

[3]Ioffe Physical Technical Institute of the Russian Academy of Sciences, Politekhnicheskaya 26, 194021 St. Petersburg, Russia.

[4]ITMO University, Kronverkskiy pr. 49, 197101 St.Petersburg, Russia

## Abstract

Defect-free integration of III-V semiconductors on silicon can open new path toward CMOS compatible optoelectronics and novel design schemes in next generation solar cells. Ordered arrays of nanowires could accomplish this task, provided they are obtained in high yield and uniformity. In this work, we provide understanding on the physical factors affecting size uniformity in ordered GaAs arrays grown on silicon. We show that the length and diameter distributions in the initial stage of growth are not much influenced by the Poissonian fluctuation-induced broadening, but rather are determined by the long incubation stage. We also show that the size distributions are consistent with the double exponential shapes typical for macroscopic

nucleation with a large critical length after which the nanowires grow irreversibly. The size uniformity is dramatically improved by increasing the $As_4$ flux, suggesting a new path for obtaining highly uniform arrays of GaAs NWs on silicon.

## INTRODUCTION

Semiconductor nanowires (NWs) are filamentary crystals with a tailored diameter ranging between few and 100 nm. Their anisotropic morphology and small lateral size result in many interesting properties that are different from bulk materials. NWs have thus inspired a large variety of applications and fundamental studies, such as miniaturized optoelectronics, next generation energy harvesting, quantum communication and computing [1–7]. Very importantly, small footprint in contact with the substrate allows for facile strain relaxation in heteroepitaxy, enabling defect-free growth of NWs on lattice-mismatched substrates. This has opened the path for monolithic integration of high performance III-V materials with Si electronic platform.

Obtaining NWs in pre-defined positions constitutes the first step towards their utilization as devices in scalable platforms. Applications in electronics, optoelectronics and energy harvesting require a clear outline of the device structure on a chip[8–14]. In addition, in a bottom-up growth process, the structure of NW arrays can be extremely dependent on the inter-wire distance and the initial conditions such as the droplet size[15–17]. Preparing growth initiation in pre-defined sites is essential for understanding the fundamental aspects of the entire NW growth process that can otherwise be hidden in a self-assembly process. Only with this comprehension, we will reproducibly engineer the NW morphology and dimensions and thus promote their further transfer from laboratory to industry.

NWs are usually obtained by the bottom-up vapor-liquid-solid (VLS) method, in which a liquid metal droplet directs the NW growth. One of the approaches to fabricate ordered arrays of NWs relies upon the positioning of lithographically defined nanoscale droplets. Gold, the most used metal in VLS, should be avoided in any silicon platform with electronic or optoelectronic functionality [18,19]. Instead, self-catalyzed growth has arisen as a reliable alternative to gold-assisted VLS growth. In the case of GaAs, gallium droplets can also initiate and direct the growth of GaAs NWs. In order to obtain growth in pre-defined sites, nanoscale holes are created in a dielectric layer. Gallium is then selectively deposited into the holes, thereby initiating NW growth in these sites [20,21]. GaAs NW arrays on silicon substrates have been achieved by few groups, although yields close to 100% are rare[21–24]. Furthermore, fundamental studies of the initial stages of NW nucleation and growth and in particular the influence of the incubation time on the resulting length and diameter distributions within the NW ensembles in ordered arrays are still lacking.

Recently, it was predicted that Ga-assisted GaAs NWs should exhibit a sub-Poissonian diameter distribution.[18] Theoretical studies also showed that the NW length distribution can be narrowed with respect to Poissonian by a nucleation anti-bunching process, only in the absence of delay for NW nucleation[19]. Unfortunately, sub-Poissonian length distributions have never been observed in NW ensembles. A careful study on the NW length distributions necessitates a frame that guarantees that each NW grows under the same conditions and starts at the same time. Here, for the first time, we present the size (length and diameter) distributions of Ga-assisted GaAs NWs grown in the ordered arrays on Si. The high yield obtained allows us to reliable derive a model on the evolution of the NW elongation and diameter with time. Overall, this study opens a new avenue for the deterministic integration of III-V nanowires on silicon.

**RESULTS AND DISCUSSION**

We start by illustrating the initial stages of GaAs NW growth on patterned silicon substrate. The growth is performed on a (111)Si substrate covered with a 10 nm thick thermal oxide, in which we etch nanoscale holes with reactive ion etching (details on substrate fabrication and design can be found in the Methods section and SI 1). The yield of vertical NWs was higher than 85%. Figures 1 a-i show the typical scanning electron micrographs (SEM) of GaAs NW arrays obtained on 45 nm wide holes as a function of time. For this series of samples, we used the gallium flux corresponding to the GaAs growth rate of 1A/s, the $As_4$ partial pressure of $2\times10^{-6}$ Torr (unless indicated otherwise), at a substrate temperature of 635°.

Wide field SEM pictures of the arrays showing the consistent yield across a 100x100 $\mu m^2$ area are shown in SI 2. The high and uniform yield can only be achieved with a 10 min Ga pre-deposition step, denoted as growth time of 0 minutes in Fig.1 a. The SEM images present the NW morphology evolution after the intervals of 2, 3.5, 4, 4.25, 4.5, 5, 7.5 and 10 min in Fig1b-i, respectively. In order to follow more precisely the initial stages of growth, we have performed the atomic force microscopy (AFM) analysis of the same area. The average height and diameter of the nanostructures versus time are given in Fig. j-k, along with the corresponding statistical data for the size distributions for each point. These data were acquired by measuring at least 125 NWs for each sample. The data are illustrated in the line - box plots, where 50% of the distribution is within the box and the horiziontal band inside corresponds to the statistical median of the distribution. The bottom and the top of the line include 98% of the distribution, while the points outside of the line correspond to the measurements that fall farther from the main distribution.

The NW growth does not start right after the Ga pre-deposition. Rather, we observe a delay of 3.5 min under these growth conditions. The delay is detected in both the SEM micrographs and in Fig.1j. After 4 minutes of growth, we detect an increase in height and a sudden decrease in the diameter. The mean NW height increases very rapidly and the length distribution broadens once the NWs start emerging from the substrate. This effect is well understood, because increasing the number density of NWs that start at different time necessarily leads an enlargement of the distribution width. A similar long nucleation step has been previously reported for a variety of systems -including self-assembly- such as Au-catalyzed InAs NWs[25], In-catalyzed InAs NWs and Ga-catalyzed GaAs NWs grown without any gallium pre-deposition.[26]

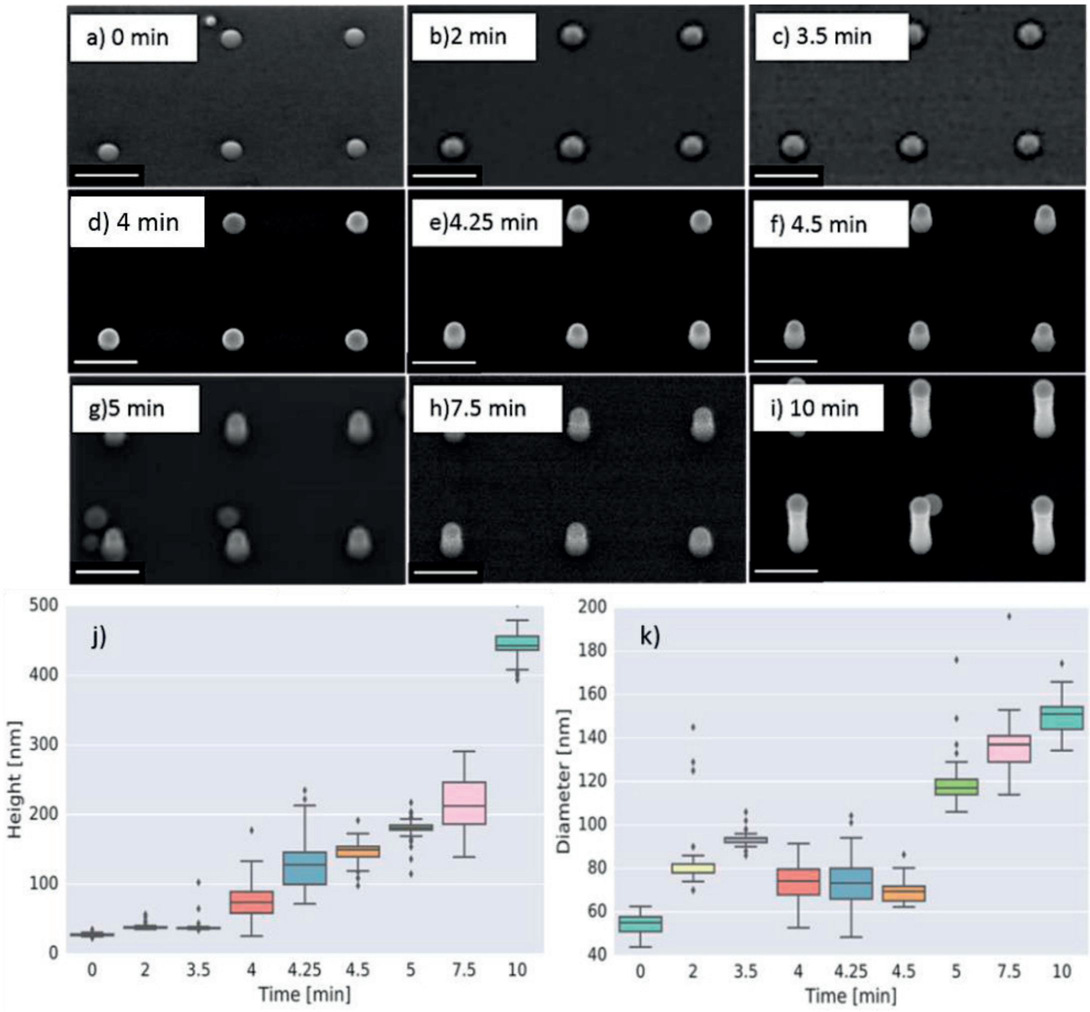

**Figure 1. Time series of GaAs NW arrays: a) – i)** SEM images of the array grown for from 0 minutes (droplet deposition) up to 10 minutes, The scale bar is 200 nm, and tilt angle is 20˚, the corresponding height (j) and diameter (k) distributions obtained by AFM.

We now turn to modeling the initial stages of NW growth in regular arrays. Figure 2 illustrates the parameters that are used to describe the evolution of NW height and diameter. Initially, the gallium droplets exhibit a radius $R_0$ at the base, which can be smaller than or equal to that of the hole. The contact angle of the droplets resting on the surface is denoted $\beta_D$ and should be close to $90^o$ (See SI3). During the incubation stage, most droplets just swell on the surface by increasing their base radius $R_D$ without changing much their contact angle, while almost no NWs start.

The NW nucleation requires that the droplet is lifted up to a certain macroscopic value of the height. In our model we use the dimensionless length $s = L/h >> 1$ Fig.2a)-(III) (with $h = 0.326$ nm as the height of GaAs monolayer). The NW initiation process is expected to exhibit a barrier activated character and proceed via macroscopic nucleation. This means that the critical length $s_c$, i.e., the length after which the NWs begin to grow regularly in vertical direction and at a fixed contact angle of the droplets on their tops, is much larger than unity. After growth has started ($s>s_c$), the droplets acquire the contact angle $\beta_{NW}$ which is larger than $\beta_D$. This abrupt change of the droplet shape leads to the corresponding decrease of the droplet base radius. The total height of the structures (droplets and NWs) equals $H = L + R(1-\cos\beta)/\sin\beta$, where $L$ is the NW length excluding the droplet, $R$ is the droplet base radius and $\beta$ is the contact angle. The volume of spherical cap droplet is given by $V = (\pi R^3/3) f(\beta) = i\Omega_{Ga}$. Here, $i$ is the number of gallium atoms in spherical cap (we neglect the influence of arsenic on the droplet volume due to its low concentration[27], $\Omega_{Ga}$ = 0.02 nm$^3$ is the elementary volume of liquid gallium and $f(\beta) = (1-\cos\beta)(2+\cos\beta)/[(1+\cos\beta)\sin\beta]$ is the geometrical function relating the volume of spherical cap to the cube of its base. The droplet base radius is related to $i$ as $R = R_{Ga}(\beta) i^{1/3}$, with $R_{Ga}(\beta) = [3\Omega_{Ga}/(\pi f(\beta))]^{1/3}$ being the shape-dependent characteristic size.

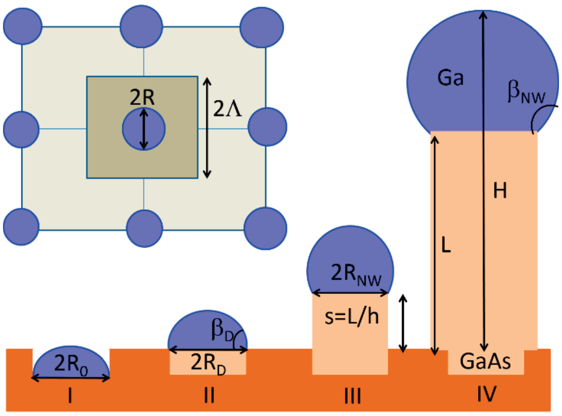

**Figure 2.** Proposed scheme of Ga-catalyzed VLS growth of GaAs NWs in regular arrays: **I** droplet pre-deposition (t=0), **II** formation of the initial NW monolayers after the incubation phase (t>0), **III** initial elongation of the NW and **IV** definition of the NW morphological parameters.

We start the modeling of the growth process by relating the material conservation with the model geometry shown in Fig. 2. If we assume that all gallium atoms impinging onto different surfaces will subsequently reach the droplet, the number of gallium atoms in the droplet changes in time according to [28]:

$$\frac{di}{dt}=\frac{v_{Ga}}{\Omega_{GaAs}}\left[(4\Lambda^2-\pi R^2)\cos\alpha_{Ga}+2RL\sin\alpha_{Ga}+\frac{\pi R^2}{\sin^2\beta}\right]-\frac{\pi R^2}{\Omega_{GaAs}}\frac{dL}{dt}\,. \qquad (1)$$

Here, $v_{Ga}=$ 6.6 nm/min is the gallium rate in our conditions and $\Omega_{GaAs}$ = 0.0452 nm$^3$ is the elementary volume of solid GaAs. The first term in the right hand side of Eq. (1) stands for the gallium collection from the surface area per NW, with $2\Lambda\cong$ 400 nm as the array pitch and $\alpha_{Ga}=$ 45$^{\circ}$ as the incident angle of the gallium beam. The second term describes the atoms collected by the NW sidewalls, the third gives the number of gallium atoms collected by the droplet and the fourth is the sink due to the NW axial growth. In the first approximation, the axial growth rate is proportional to the effective arsenic influx $v_{As}$, including a contribution from re-emitted arsenic species[25,27,29–33]

$$\frac{dL}{dt}=\chi_{As}v_{As}\,. \qquad (2)$$

In these conditions, the main contribution to $di/dt$ in Eq. (1) is given by the size-independent term $(v_{Ga}/\Omega_{GaAs})4\Lambda^2\cos\alpha_{Ga}$, explaining why we observe a pronounced regime of radial growth rather than droplet shrinking or self-stabilization[30,32]. From equations (1) and (2), the “invariant” variables for which the growth rates are size-independent are given by the number of gallium atoms in the droplet and the number of GaAs monolayers in the NW[34]:

$$\frac{di}{dt}=\frac{1}{\tau},\ \frac{ds}{dt}=\frac{1}{\tau_s}\ . \qquad (3)$$

The time $\tau\cong\Omega_{GaAs}/(4\Lambda^2 v_{Ga}\cos\alpha_{Ga})$ with our parameters is estimated at $1.5\times10^{-8}$ min. The time $\tau_s=h/(\chi_{As}v_{As})$ approximately equals 0.012 min (the $\chi_{As}v_{As}$ value approximately equals 28 nm/min and it is determined by fitting the data as will be discussed shortly). Equation (3) for $di/dt$ applies for droplets as well as NWs. Integrating it, we obtain the base radius in the form

$$R_D=\left[R_0^3+R_{Ga}^3(\beta_D)\frac{t}{\tau}\right]^{1/3} \qquad (4)$$

The droplet height is obtained simply by using the total height of the structure, H, with $R_D$ given by Eq, (4), and setting $L=0$ by the droplet definition:

$$H_D=R_D\frac{(1-\cos\beta_D)}{\sin\beta_D} \qquad (5)$$

Here, $\beta_D$ is the contact angle of the droplets resting on the surface. Assuming that the transformation from droplets to NWs occurs at a fixed volume of liquid gallium, the radius and height of NWs are given by

$$R_{NW}=\left[\frac{f(\beta_0)}{f(\beta)}\right]^{1/3}R_D$$

$$H_{NW} = \chi_{As} v_{As} t + R_{NW} \frac{(1-\cos\beta_{NW})}{\sin\beta_{NW}}, \qquad (6)$$

where $\beta_{NW}$ is the contact angle of the droplets seated at the NW tops.

Our goal now is to understand the evolution of NW array as an ensemble. The NW ensemble evolves from droplets to NWs, passing through an initial stage where there is coexistence of droplets and NWs. Consequently, the description of radius and height evolution should also include nucleation statistics. The mean radius and height within an ensemble containing both droplets and NWs should be obtained as a weighted average of the two populations. We use macroscopic nucleation theory in open systems to describe the statistical size distributions. We define $p_{NW}(t)$ as the normalized number density of NWs. In macroscopic nucleation theory[28], this $p_{NW}(t)$ is the double exponential function of time

$$p_{NW} = 1 - \exp\left[-\exp\left(\frac{t-t_*}{\Delta t}\right)\right]. \qquad (7)$$

Here, $t_*$ is moment of time corresponding to the maximum nucleation rate of NWs and $\Delta t$ is the duration of the incubation stage. The NWs that start at time $t_*$ will subsequently correspond to the maximum of the size distributions. The normalized number density of droplets, $p_D$, corresponds to $p_D(t) = 1 - p_{NW}(t)$. Using these number densities as probabilities to observe either a droplet or NW in a given site, the mean radius and height of the structures (denoted $\langle R\rangle$ and $\langle H\rangle$, respectively) are obtained as

$$\langle R\rangle = R_D p_D + R_{NW} p_{NW}$$
$$\langle H\rangle = H_D p_D + H_{NW} p_{NW} \qquad (8)$$

These expressions describe a competition between the two populations of droplets and nanowires throughout the incubation stage and the follow-up nucleation stage within the time interval $0 \le t \le t_c = t_* + \Delta t$. At $t > t_c$, the population of droplets diminishes to zero and the NWs continue growing with the mean radius and height given by

$$\langle R\rangle = \left[\langle R\rangle_c^3 + R_{Ga}^3(\beta_{NW})\frac{a(t-t_c)}{\tau}\right]^{1/3}$$
$$\langle H\rangle = \langle L\rangle_c + b\chi_{As} v_{As}(t-t_c) + \langle R\rangle \frac{(1-\cos\beta_{NW})}{\sin\beta_{NW}}. \qquad (9)$$

Here, the $a$ and $b$ factors describe possible differences in the material supply to longer NWs. Best fits of the mean diameter and height as a function of time following Eqs. (8) and (9) are shown in Fig. 3. They were obtained with $\beta_{NW} = 130^o$, $t_* = 4.5$ min, $\Delta t = 0.5$ min, $\tau = 6\times 10^{-8}$ min, $\chi_5 v_5$ = 28 nm/min, $a = 14$ and $b = 1$.

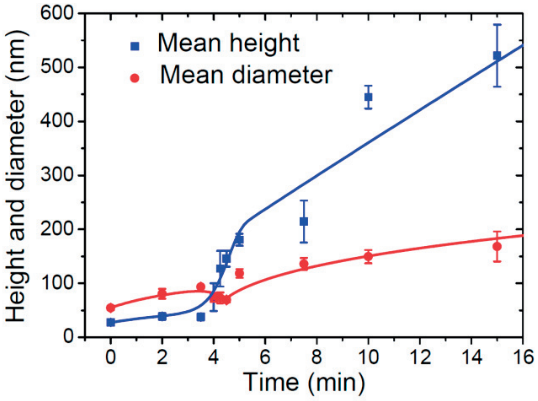

**Figure 3**. Mean NW height $H$ (including the droplet height) and top diameter $2R$ versus time (symbols) for GaAs NWs grown from holes of 45 nm nominal diameter (due to the HF dip, the actual hole size at the beginning of gallium deposition is actually larger, about 60 nm). The error bars represent standard deviation. The curves show best fits obtained from the model equations.

Let us now discuss the choice of the model parameters. The contact angle of the droplet sitting on the NW top is set to its typical value during growth[27]. We set $b = 1$, ignoring any difference between the NW elongation rate at the initial and steady state growth stages. The times $t_*$ and $\Delta t$ are determined from our experimental data. The fitting value of $\tau$ = $6 \times 10^{-8}$ min is close to that obtained earlier from geometrical considerations ($1.5 \times 10^{-8}$ min). The obtained value $\chi_5 v_5$ of 28 nm/min appears reasonable, in agreement with an atomic V/III flux ratio of 4.2. The value of $a = 14$ implies that Ga droplets receive a larger gallium influx in the steady state stage with respect to the beginning of growth. This can be due to re-emission or additional contributions of gallium adatoms diffusing from the NW sidewalls, the terms that were the omitted in material balance given by Eq. (1)[35].

We now move to modeling the NW size distributions. According to Refs. [36,37], whenever the number density of NWs is given by Eq. (7), there will be a broadening of the size distributions for both lengths and diameters in the initial stage of growth, simply because the distribution width increases from initially zero to its final value where the nucleation stage is completed. In the steady-state growth stage, the size distributions can be further broadened due to kinetic fluctuations. These Poissonian contributions to the broadening should contribute less than 5% for our short growth times (see SI 4). As a consequence, we ignore the effect of kinetic fluctuations in our model. The width of the resulting length distributions are now mostly determined by the incubation stage. The equations used to fit our experimental size distributions for the 10 min growth were the following:

$$f(L, L_*) = A \exp\left[\frac{L_* - L}{\Delta L} - \exp\left(\frac{L - L_*}{\Delta L}\right)\right] \quad , \qquad (10)$$

for the NW lengths without the droplet, with $L_*$ as the most representative length and $\Delta L = \chi_{As} v_{As} \Delta t$ as the distribution width. For the diameter distribution, we use the similar expression

$$f(R, R_*) = CR^2 \exp\left[\frac{R_* - R}{\Delta R} - \exp\left(\frac{R - R_*}{\Delta R}\right)\right] \qquad (11)$$

with the width $\Delta R = R_{Ga}^3(\beta_D)\Delta t/(3R_*^2\tau)$ . Details of derivation of these expressions are given in SI 4. The length and diameter histograms of NWs after 10 min of growth are shown in Fig.4, along with their best fits by the double exponential shapes given by Eqs. (10) and (11). With our parameters, the calculated values of the distribution widths equal $\Delta L = 14$ nm, $2\Delta R = 4.5$ nm (see SI 4), while from the fits they are 16 and 6.5 nm, respectively.

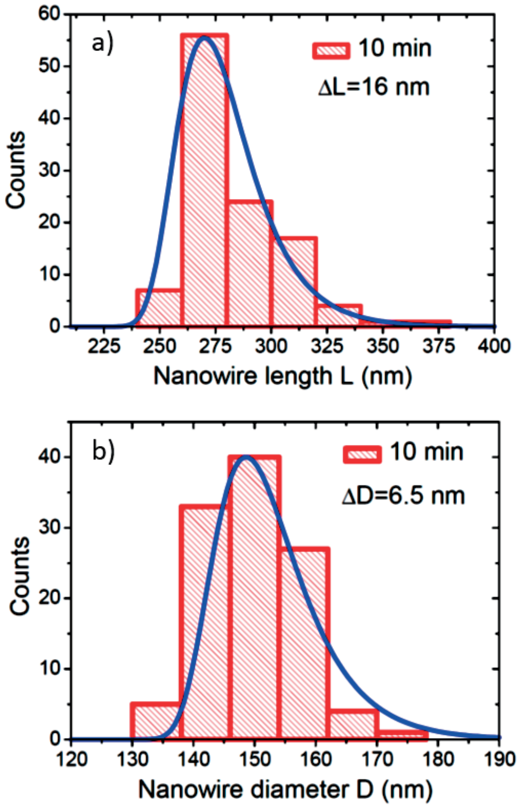

**Figure 4 a)** Length histogram of Ga-catalyzed GaAs NWs after 10 min of growth (without droplets), fitted by the double exponential distribution with $\Delta L =$ 16 nm**, b)** Diameter histogram of Ga-catalyzed GaAs NWs after 10 min of growth, fitted by the double exponential distribution with $\Delta D$ = 6.5 nm.

While obtaining a high yield of GaAs arrays is relevant for the integration of III-Vs on silicon, it would be even more important to obtain the most homogeneous size distribution possible. This brought us to explore the conditions that could further narrow the length and radius distributions of NWs. So far, our model indicates that the length distributions are primarily determined by the long incubation stage, i.e., different start times for the regular VLS growth of different NWs. In order to achieve more uniform arrays, we increased $As_4$ beam flux. Our intention was to achieve a higher supersaturation in the Ga droplet and thus increase the GaAs nucleation probability[38,39] . This should shorten the incubation time for NW growth and hence the decrease the initial size distribution width. We compare the elongation and diameter distributions of NWs obtained after 4 minutes of growth, since this corresponds to the incubation time for NWs obtained at lowest $As_4$ fluxes. We show results for $As_4$ equivalent beam pressures of $2x10^{-6}$ Torr, $2.5x10^{-6}$ Torr and $3x10^{-6}$ Torr in Fig. 5. We include both the SEM micrographs and the corresponding size distributions. As expected, by increasing the $As_4$ flux the NW incubation phase shortens. The length distribution width is also considerably narrowed. The mean values for lengths are (75±25), (125±12) and (180±10) nm, for histograms in Fig. 5a), b), and c) respectively. From the values of standard deviations, one can observe that the distribution narrows for more the factor 2 when As pressure was increased from $2x10^{-6}$ Torr to value of $3x10^{-6}$ Torr. These results confirm that increasing supersaturation in the Ga droplets is a good strategy for increasing the NW homogeneity in the arrays.

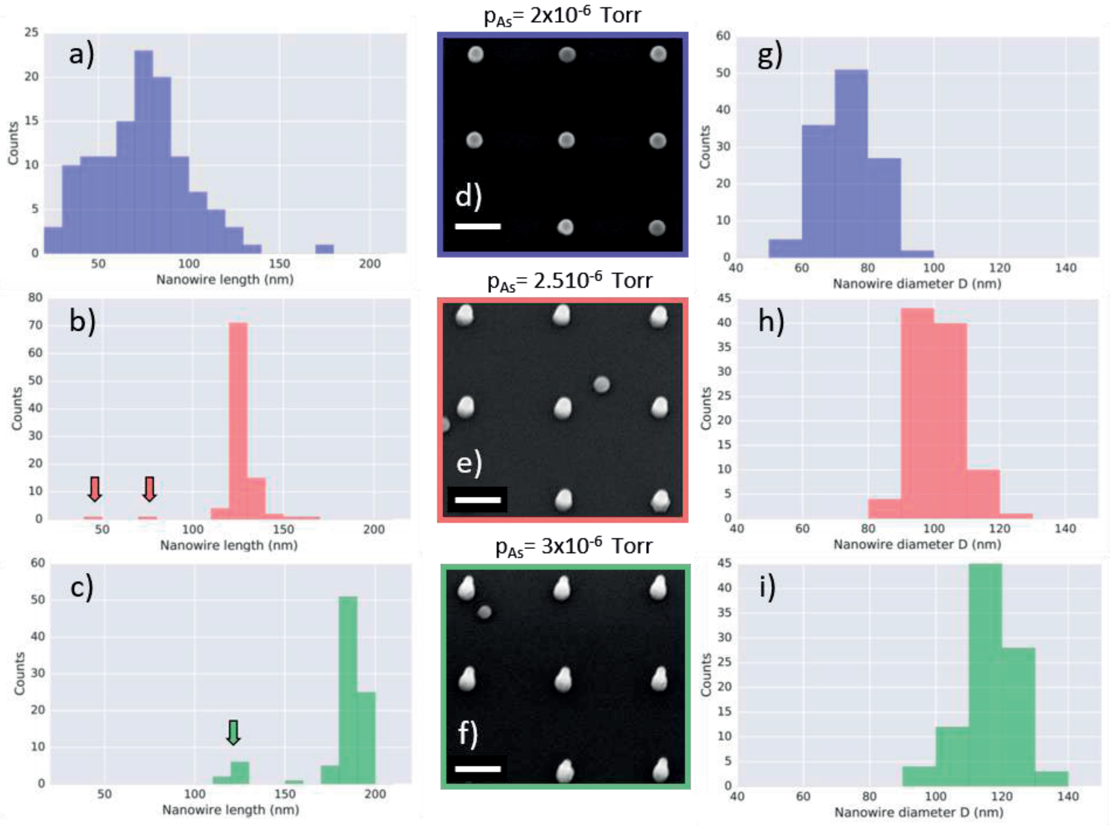

**Figure 5. As series grown for 4 minutes. a)-c)** NW length distributions for As pressure 2x10$^{-6}$ Torr, 2.5x10$^{-6}$ Torr and 3x10$^{-6}$ Torr respectively, **d) –f)** corresponding SEM micrographs, the scale bar is 200 nm, and the tilt angle 20 ˚, **g) – f)** NW diameter distributions. The effect of As pressure is evident in terms of higher growth rates and narrowing the distributions, particularly for the NW length.

The values indicated with arrows in b) and c) are probably the wires for which droplets were consumed or polycrystalline material (unsuccessful nucleation of NW). These features cannot be distinguished solely from AFM scans. In SI 4. We have also looked at the time evolution of NW growth under the highest supersaturation conditions. Fig 6a-d depicts representative SEM micrographs and the statistical morphological analysis as a function of the growth time. The incubation time of the NWs is shorter than 1 min. This represents a factor 4 in reduction of the incubation period by just a 50% an increase in the As$_4$ equivalent beam flux pressure. This confirms the strong non-linear relation between nucleation statistics and supersaturation.

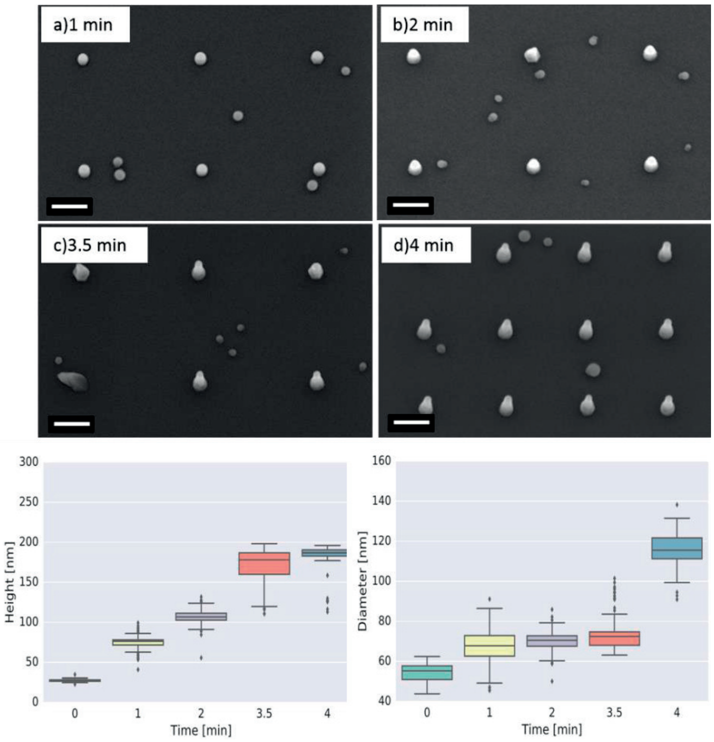

**Figure 6. Time series for 3x10$^{-6}$ Torr. a) –d)** SEM images of the arrays grown for different times, **e)** height distributions, **f)** diameter distributions as a function of time.

## CONCLUSIONS

In conclusion, we have provided a detailed study of the initial stages of growth of ordered GaAs NWs on silicon. The NW nucleation leads to a rapid shape transformation of droplets in which their base radius shrinks and the height increases accordingly. Our NWs grow under strongly gallium-rich conditions corresponding to the droplet swelling. The widths of both radius and length distributions do not follow Poissonian fluctuation-induced broadening for the short lengths investigated, but rather are determined by the long incubation stage. Interestingly, our statistical histograms do not show any pronounced asymmetry toward longer left tails, as in Refs[20,21]. Instead, they are well-fitted by the double exponential shapes typical for macroscopic nucleation with a large critical length after which NWs grow irreversibly. Our model describe well the observed distribution shapes, however, unraveling the exact mechanisms of NWs emerging from the substrate requires a separate study. Shortening the nucleation stage by increasing the $As_4$ flux effectively narrows the size distribution. Our results suggest that this parameter plays a key role for obtaining highly uniform arrays on silicon.

## Methods

### Substrate preparation

Four-inch ⟨111⟩ p-doped silicon wafers with a resistivity of 0.1–0.5Ωcm 10 nm were thermally oxidized in a Centrotherm furnace at 950°C. The thickness of silicon oxide was 15 nm. The pattern was predefined in a ZEP resist with electron-beam lithography and then transferred on the oxide layer by a 6 s dry etching using $CHF_3$/$SF_6$ chemistry followed by 2 s dip in 7:1 buffered hydrofluoric acid solution (BHF). Electron-beam resist was removed by oxygen plasma. After patterning, the wafers were diced into 35×35 mm$^2$ square chips sized for the MBE sample holder. In order to ensure an oxide-free surface in the holes, the chips were shortly dipped in the same BHF solution prior to the introduction in the UHV chamber. The final thickness of oxide before loading was 10 ± 1 nm. The substrates were subsequently annealed at 500 °C for 2 h in UHV in order to ensure a pristine surface free of water and organic molecules. The substrate was then transferred to the growth chamber. There, they were degassed at 770°C for 30 min to further remove any possible surface contaminants.

## Acknowledgements

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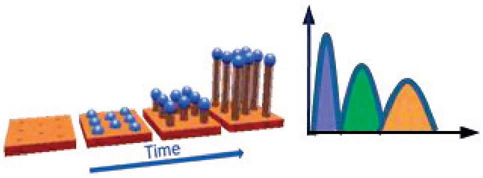

Growth process of Ga-assisted GaAs nanowires on silicon and the monitoring of their distribution in size.

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## 3.3 Combining top down and bottom up approaches: fabrication of ordered hybrid InAs/Si heterostructures using oxide templates

Guided growth, using oxide templates, was shown to be one of the promising ways for reproducible integration of III-V NWs on the Si substrate. This concept was introduced IBM Research-Zürich under the name template assisted selective area epitaxy (TASE) [187, 188]. In their work they have used this technique to create arbitrary shaped III-V semiconductors such as nanowires, cross junctions, nanostructures containing constrictions and 3D stacked nanowires [188], but also for vertical integration of NW in Si substrates with different crystalline orientation [189] and growth of heterostructures [190].They used MOVPE as the main growth technique. Their main achievements are summarized in Fig. 3.12.

In the work presented in this section, we also used $SiO_2$ template to guide the growth of InAs nanowires, but engaging MBE as growth technique. Growing inside nanotubes can be especially challenging in MBE. The sticking coefficient of the impinging species is negligible on the $SiO_2$ sidewalls and non-negligible at the bottom of the tubes (Si). However, due to the directionality of the beams, the material supply at the bottom of the tubes is relatively limited. In order to illustrate this, we have calculated the amount of In at the bottom of the tube as a function of the tube depth for three different tube diameters. These calculations assume that only direct impingement contributes to the growth at the bottom of the tubes, a growth rate of 0.2Å/s and a total time of 1 h. The results of the calculations are shown in Fig. 3.13. The angle of incidence was set to be 45°, which corresponds to the configuration of our MBE machine. The amount of material reaching the bottom of the tube drops when the tube depth approaches the value of the diameter. That is the point after which flux *doesn't see* the tube bottom any more. Observation of growth in the tubes deeper than their diameter would indicate alternative material pathways to the bottom of the tube, such as surface diffusion and reemission from the inner tube walls. This growth allows the study of fundamental aspects of MBE growth, in addition to the strongly desirable reproducible growth of high yield nanowire arrays on Si.

In this thesis we investigated for the first time the growth of III-V nanowires in silica nanotubes with MBE. Moreover, we provided a new substrate fabrication process, compatible with low-cost and large area fabrication. In order to obtained large scale of nanosized tubes we used phase shift lithography (PSL) to pattern the substrate (for more details on the technique see Section 2.1.2). Exposure was performed in two steps, where in the second one mask was rotated for 90° [67, 191]. The lithography steps are presented in Fig. 3.14.

According to the main concepts of PSL introduced in Section 2.1.2, in the position of phase shifter (step in the phase shift mask) the light intensity drops to zero and generates an underexposed line in the photoresist (Fig. 3.14 on the left). The second exposure, after rotating the mask for 90°, generates underexposed lines perpendicular to the previous ones. The only places that remain completely unexposed are the crossings of the lines, pointed by the arrow in the Fig. 3.14 right. If positive photoresist is used, this area will remain as a nanoscale island

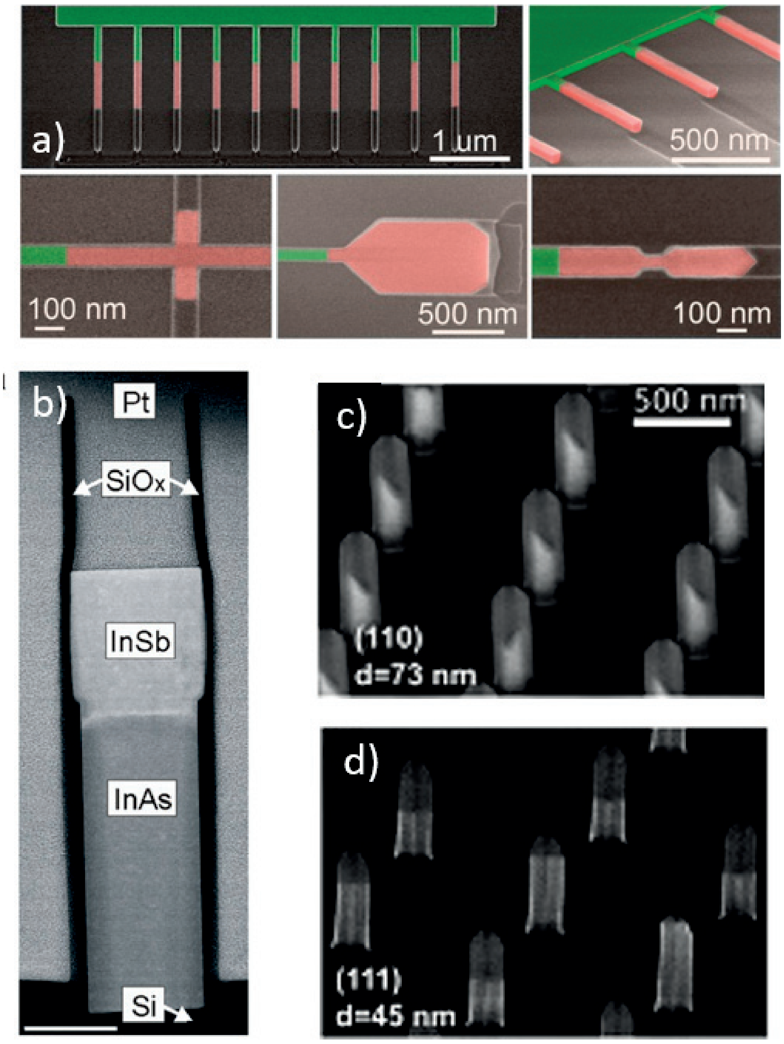

Figure 3.12 – Work carried out by IBM Zürich research using template assisted growth a) Scanning electron microscope images of single crystal structures fabricated using template-assisted selective epitaxy (silicon is colored in green, and the compound semiconductor in red)(adopted from [188], ©2017 Applied Physics Letters, AIP Publishing LLC) b) Cross-sectional transmission electron microscope (XTEM) analysis of an InAs-InSb heterostructure grown in a nanotube template. (adopted from [190], ©2017 Nanotechnology, IOP Publishing) c) and d) SEM images of InAs nanowires grown in nanotube templates with different diameters on the different substrate orientation Si(100) and Si (111), respectively.

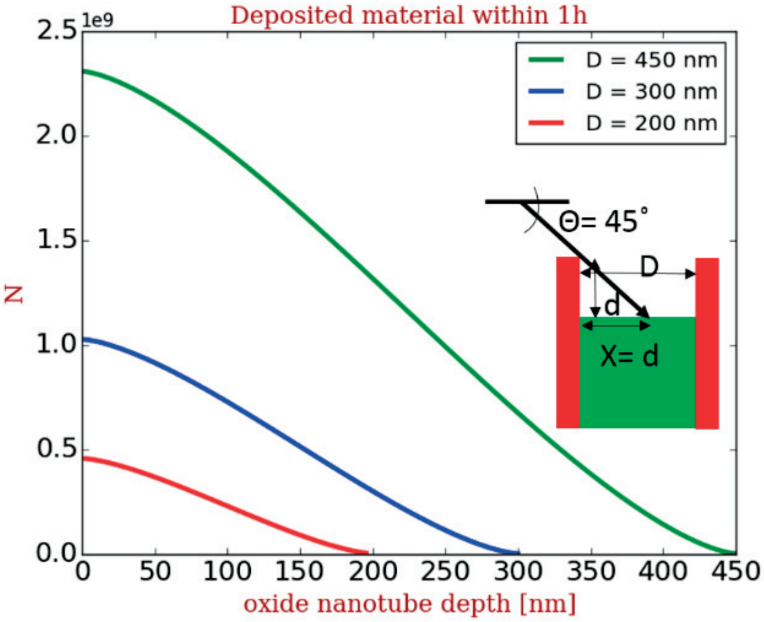

Figure 3.13 – Calculated number of directly impinging In atoms on the bottom of the tube during 1 hour deposition using In flux of 0.2 Å/s. Three different tube diameters are considered and the angle of impingement is set to be 45°.

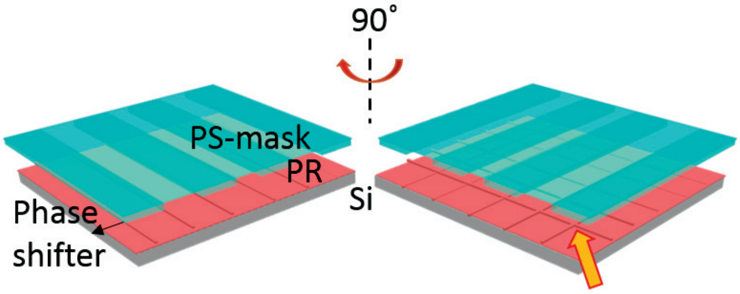

Figure 3.14 – Two steps of exposure for generating the nanosized pattern in photoresist (PR) using PSL. After first step the dark lines in PR are formed in the position of phase shifters (left). In the second step, after the rotation of the mask, the pattern is generated in unexposed positions - crossings of the dark lines, pointed by the arrow.

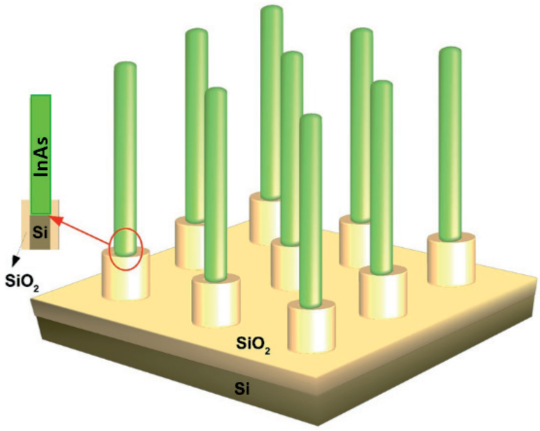

Figure 3.15 – Schematics of the InAs nanowire arrays grown in the SiO$_2$ nanotube substrate — formation of Si/GaAs heterostructure combining top-down and bottom-up approaches.

of photoresist. This can then be used as etching mask for the silicon nanopillar formation. Replacing positive photoresist by negative, it is possible to obtain a reversed image that would result in an arrays of holes. Therefore PSL can be used both to form the arrays of nanostructures and arrays of nanoscale openings. Further details on the nanotube fabrication are included in the paper following this section.

Finally, this substrate design is not only used to integrate III-V semiconductors on Si, but also to create a hybrid Si/III-V heterostructures. A scheme of this principle is presented in Fig. 3.15. Within the tube, the silicon is not emptied completely, what result in the formation of a hybrid III-V/Si nanowire.

### 3.3.1 Paper included in this section

**Molecular beam epitaxy of InAs nanowires in SiO$_2$ nanotube templates: challenges and prospects for integration of III-Vs on Si**

AUTHORS
Jelena Vukajlovic-Plestina, Vladimir G. Dubrovskii, Gözde Tütüncuoğlu, Heidi Potts, Ruben Ricca, Frank Meyer, Federico Matteini, Jean-Baptiste Leran, Anna Fontcuberta i Morral

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MY CONTRIBUTION

- I did the substrate preparation and characterization
- I planned the growth

- I did the growth results analysis (SEM)
- I performed statistical analysis
- I took active part in the interpretation of the results
- I wrote parts of the paper and prepared figures

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# Molecular beam epitaxy of InAs nanowires in $SiO_2$ nanotube templates: challenges and prospects for integration of III–Vs on Si

**Jelena Vukajlovic-Plestina**[1], **Vladimir G Dubrovskii**[2,3], **Gözde Tütüncuoğlu**[1], **Heidi Potts**[1], **Ruben Ricca**[1], **Frank Meyer**[1], **Federico Matteini**[1], **Jean-Baptiste Leran**[1] **and Anna Fontcuberta i Morral**[1]

[1] Laboratory of Semiconductor Materials, Institute of Materials, Ecole Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland
[2] St. Petersburg Academic University, Khlopina 8/3, 194021 St. Petersburg, Russia
[3] ITMO University, Kronverkskiy pr. 49, 197101 St. Petersburg, Russia
[4] Ioffe Physical Technical Institute of the Russian Academy of Sciences, Politekhnicheskaya 26, 194021 St. Petersburg, Russia

E-mail: anna.fontcuberta-morral@epfl.ch

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**Abstract**

Guided growth of semiconductor nanowires in nanotube templates has been considered as a potential platform for reproducible integration of III–Vs on silicon or other mismatched substrates. Herein, we report on the challenges and prospects of molecular beam epitaxy of InAs nanowires in $SiO_2$/Si nanotube templates. We show how and under which conditions the nanowire growth is initiated by In-assisted vapor–liquid–solid growth enabled by the local conditions inside the nanotube template. The conditions for high yield of vertical nanowires are investigated in terms of the nanotube depth, diameter and V/III flux ratios. We present a model that further substantiates our findings. This work opens new perspectives for monolithic integration of III–Vs on the silicon platform enabling new applications in the electronics, optoelectronics and energy harvesting arena.

S Online supplementary data available from stacks.iop.org/NANO/27/455601/mmedia

Keywords: nanowire, organized growth, templated growth, molecular beam epitaxy, integration of III–Vs on silicon, InAs

(Some figures may appear in colour only in the online journal)

## 1. Introduction

One-dimensional geometry of semiconductor nanowires (NWs) gives rise to many interesting physical properties which are not seen in bulk materials, such as electron quantum confinement [1–5] and optical resonances [6, 7]. Furthermore, small diameters of NWs allow for their dislocation-free growth on lattice-mismatched substrates. This feature may enable monolithic integration of high-quality III–V semiconductors with silicon electronic platform, overcoming the fundamental issues such as lattice, polarity and thermal expansion mismatch [8, 9]. To fully exploit the huge potential provided by the combination of NW geometry and excellent III–V semiconductors properties (direct band gap, superior carrier mobility and high absorption coefficient), the growth of these structures needs to be achieved in a Au-free and position-controlled way to avoid possible Au contamination [10–12] and ensure the required spatial positioning of NWs. In gold-free growth, the NW position is usually controlled by defining the arrays of holes in a dielectric mask using electron beam lithography for surface patterning [13–15]. This provides the nanoscale precision, but on the other hand the process is extremely time-consuming on a large (wafer) scale and unable to satisfy the condition of cost

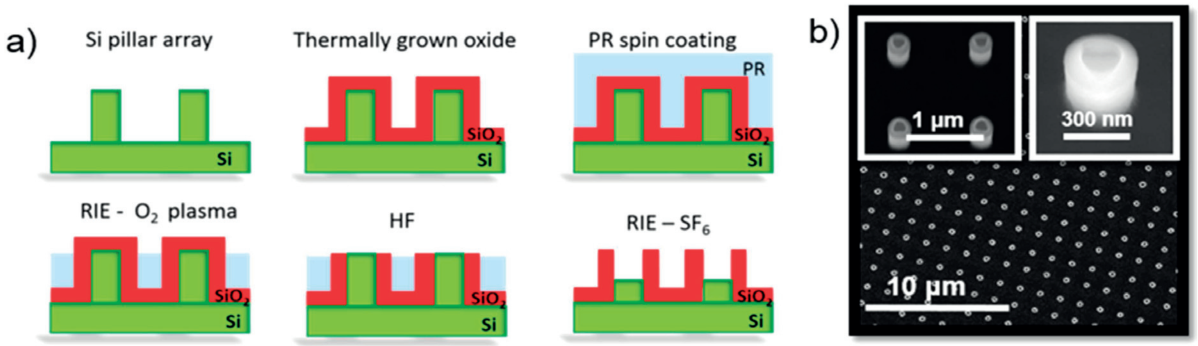

**Figure 1.** (a) Illustration of fabrication steps for silicon oxide nanotube template (ONT) and b) SEM images of an ONT array and close-view of a single nanotube.

effectiveness. Other techniques such as nanoimprint lithography [12, 16, 17] and phase shift lithography (PSL) [18] have previously been used to create large scale patterns for ordered NW growth.

In this work, we employ PSL as a patterning technique [18–20] to fabricate large areas of $SiO_2$ nanotubes on Si substrates to guide the subsequent growth of InAs nanowires by molecular beam epitaxy (MBE). A similar concept has recently been demonstrated by Borg *et al* with metal-organic vapor phase epitaxy (MOVPE). This MOVPE technique is usually referred to as template-assisted selective epitaxy (TASE) [21, 22]. MBE is characterized by highly directional material influxes, which makes it fundamentally different from MOVPE. The MBE template growth should be much more challenging since the material supply to the bottom of the nanotubes strongly depends on their depth. Consequently, we conduct a detailed experimental study of the template geometry influencing the yield of InAs nanowires, followed by a supporting theoretical model. Our results indicate that growth inside the nanotubes proceeds in the In-assisted vapor-liquid-solid mode rather than by selective area epitaxy. Furthermore, we demonstrate the nanowire growth in the tubes with a high aspect ratio, where the direct impingement onto the bottom of the tubes is no longer possible and the group III growth species are supplied only through surface diffusion and re-emission.

## 2. Experimental details

Large scale arrays of $SiO_2$ nanotubes were fabricated on (111) Si substrates. The fabrication process is shown in figure 1(a). First, Si nanopillars were defined by PSL followed by reactive ion etching, as in [18, 23]. The pillars were ~500 nm high and with diameters ranging from 150 to 450 nm. A 50 nm thick layer of $SiO_2$ was grown around them by thermal oxidation. Further processing steps are shown in figure 1(a) comprised coating with protective photoresist layer, controlled etching of photoresist up to the desired pillar height, oxide etching using HF and finally using reactive ion etching (RIE) to empty the silicon inside the nanopillars and form a $SiO_2$ nanotube. The entire process was optimized for 4 inch wafers, which were diced in four substrates for growth in our MBE machine. Each growth substrate contained five arrays with different geometries, with pitches of 1, 1.5 and 2 $\mu$m pillars and diameters varying from 150 nm up to 450 nm. The depth of the tubes varied between 50 and 400 nm. A scanning electron microscopy (SEM) image of a typical oxide nanotube template (ONT) array is shown in figure 1(b). The arrays and the nanotube morphology appear very homogenous across the wafer.

InAs nanowires were then grown in the ONTs in a DCA P600 MBE system. Before introduction into the MBE growth chamber, samples were dipped for 2 s in poly-silicon etch solution [$HNO_3$(70%):HF(49%):$H_2O$] in order to remove the native oxide and smoothen the silicon surface [24]. Growth parameters (the substrate temperature $T_S$, the growth time $t$, the In and $As_4$ beam equivalent pressures $P_{In}$ and $P_{As}$) were systematically varied one parameter at the time. The optimal growth temperature was found to be 500 °C, regardless of the nanotube geometry. At this temperature, we obtain growth inside the ONTs and at the same time avoid parasitic growth outside the nanotubes. The In and $As_4$ beam equivalent pressures were varied between 1.1 and 1.8 $\times$ $10^{-7}$ Torr and 0.7 and 1.3 $\times$ $10^{-5}$ Torr, respectively, similar to the conditions used in prior works for InAs nanowire growth [7]. Growth time was varied between 30 min and 5 h. No dependence on the array pitch was observed.

## 3. Results and discussion

### *3.1. Optimizing material supply for InAs nanowire growth: 200 nm deep tubes*

We start by recounting how the nanotube aspect ratio affects the material supply onto the bottom of the tube. A sketch of the nanotube geometry is shown in figure 2(a). As mentioned above, the As and In beams are directional, In adatoms are able to diffuse on the surface while As is highly volatile and almost non-diffusive [25–27]. The depth $H$ and diameter $D$ of the nanotube determine the amount of material reaching its bottom to start the nanowire growth. In our MBE system,

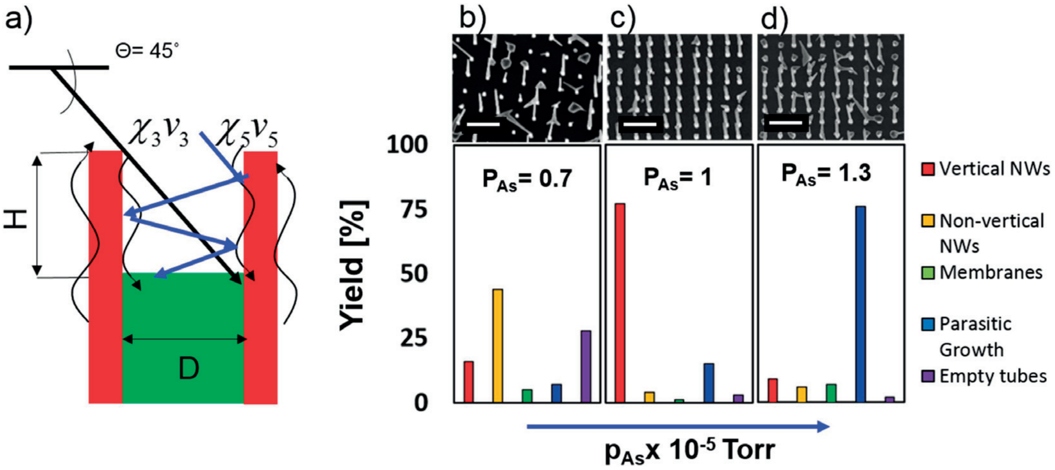

**Figure 2.** (a) Sketch of the $SiO_2/Si$ nanotube with the effective In and As fluxes $\chi_3 v_3$ and $\chi_5 v_5$, respectively. (b) to (d) Arsenic series of the InAs nanowire growth in the ONT with the resulting morphology presented top right. All samples were grown at $T_S = 500\,°C$ and $P_{In} = 1.4 \times 10^{-7}$ Torr for 90 min. The histograms show the yields of different structures obtained from the statistics analysis of the SEM images. The scale bar for the SEM images is 2 $\mu$m and the tilt angle is 20°. The $P_{As}$ values are given in the units of $10^{-5}$ Torr.

both cells are positioned at 45 °. Hence, at $H > D$ there is no direct impingement of both species at the bottom of the nanotube. In this case, initiation of the nanowire growth should be an extremely slow process as only diffusing species can reach the silicon bottom of the nanotube. Diffusion lengths of In on $SiO_2$ are typically between 0.5 and 0.8 $\mu$m, depending on the growth conditions [7, 15, 25]. The arsenic species ($As_2$ and $As_4$) should have the diffusion lengths of a few nm at most, however, arsenic can be re-emitted from the ONT surfaces and thereby contribute to the InAs growth even in the shadowed areas [26, 27]. In fact, the ONT creates local growth conditions inside the nanotubes which can be significantly different from the nominal conditions for two-dimensional (2D) growth. Therefore, in figure 2(a) the effective In (labeled '3') and As (labeled '5') atomic fluxes that reach the bottom of the nanotube are denoted $\chi_3 v_3$ and $\chi_5 v_5$, with $\chi_k$ containing information on the geometry and re-emission of the growth species within the nanotube.

We first investigated growth in the nanotubes whose diameters are similar to the depth ($D \simeq H$, aspect ratio $H/D \simeq 1$) using the growth conditions that yield InAs NW arrays on patterned Si substrates ($T_S = 500\,°C$, $P_{In} = 1.2 \times 10^{-7}$ Torr, $P_{As} = 6 \times 10^{-6}$ Torr) and the growth time of 60 min [5]. These conditions did not produce any nanowires inside the nanotubes, supporting the assumption that the effective V/III flux ratio inside the nanotube is different from the nominal value. As the diffusion length of In is much larger than that of As, much more In is collected inside the nanotube and the actual V/III ratio might be too low for nanowire growth. We gradually increased the growth time, the V/III ratio as well as the absolute fluxes of both As and In fluxes. Figures 2(b) to (d) show the effect of increasing the $P_{As}$ value at the fixed $T_S = 500\,°C$, $P_{In} = 1.4 \times 10^{-7}$ Torr and 90 min growth time. Below the SEM images, we show the corresponding yields measured for all types of structures: vertical nanowires, non-vertical nanowires, nanoscale V-shaped membranes [28], quasi-2D parasitic growth and empty nanotubes (i.e., absence of any growth). It is important to note that in many cases non-vertical nanowires and nanoscale V-shaped membranes nucleate on the oxide layer rather than on Si surface inside the nanotubes (see online supporting information 1).

For the lowest values of $P_{As}$ around $0.7 \times 10^{-5}$ Torr we observe a very low yield of vertical nanowires (less than 20%). Many non-vertical nanowires, some membranes and parasitic structures nucleate on the surface and many tubes remain empty. One can conclude that this $P_{As}$ is insufficient to nucleate vertical nanowires in the desired nucleation position, i.e. on bare Si surface in the bottom of the nanotubes. Increasing $P_{As}$ to $1 \times 10^{-5}$ Torr leads to a significant increase in the yield of vertical NWs up to 77%. The number of unwanted non-vertical nanowires and membranes is strongly decreased (down to 8% in total); the parasitic growth was found in 10% of the tubes, and 5% of the nanotubes remain empty. By further increasing $P_{As}$ to $1.3 \times 10^{-5}$ Torr, we again observe a dramatic change. In this case, less than 5% of empty tubes are observed, while vertical nanowires (~10%) are replaced by parasitic structures (almost 75%), non-vertical nanowires and membranes (about 10% in total). These noticeable differences in the yields of vertical NWs versus other structures are clearly visible on the SEM images shown in figures 2(b) to (d). Qualitatively, parasitic growth could be due to the reduction of the In diffusivity for higher As fluxes [29, 30].

Figure 3 shows the representative SEM images of the sample with the highest yield of vertical nanowires after 90 min of growth. The high yield is homogeneous over the area of the array. In table 1, we compare the optimized growth conditions for the high yield of vertical InAs nanowires on standard patterned Si substrates [5] and in the 200 nm nanotubes with $D \simeq H$. Clearly, higher fluxes and V/III ratios are required to grow nanowires in the ONTs.

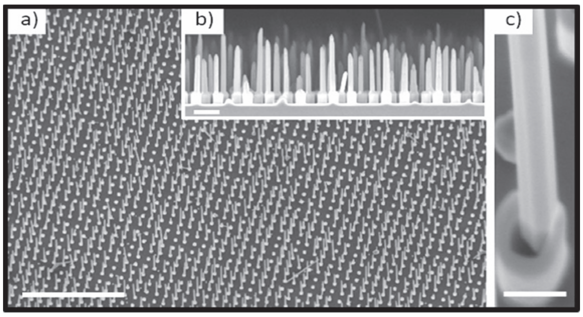

**Figure 3.** (a) InAs nanowires grown under optimized conditions in the ONTs with the tube depth of 200 nm and the aspect ratio of one. The scale bar is 10 $\mu$m and the tilt angle is 20°. (b) Cross section of the same sample. The scale bar is 1 $\mu$m. (c) Single NW growing from the nanotube, the scale bar is 200 nm and the tilt angle is 20°.

In order to understand the growth mechanism, we now take a closer look at the nanowires growing in the tubes. A typical SEM image of an InAs nanowire growing vertically from a nanotube is shown in figure 3(c). It is clearly seen that the nanowire does not fully fill the nanotube volume. Therefore, InAs nanowires do not start growing on the entire available area of bare Si in the bottom of the nanotube. This strongly suggests that the growth inside the nanotube does not proceed via the selective area epitaxy mode. Rather, at a low effective V/III ratio inside the nanotube (compared to its nominal value for 2D growth), locally In-rich conditions are very favorable for nucleation of In droplets that can subsequently promote the In-catalyzed vapor-liquid-growth of InAs nanowires [31, 32]. A similar reasoning was recently reported by Robson *et al* for the growth of InAs nanowires on patterned Si substrates where the initial nucleation step was In-assisted [33]. The nanowires should then be positioned at the edges of the nanotubes because In droplets have better chances to nucleate at the tube corners for surface energetic reasons (i.e., replacing the energetically costly liquid-vapor surface to less energetic liquid–solid interface [34, 35]).

We now analyze the influence of the nanotube diameter on the vertical nanowire yield, keeping the nanotube depth at 200 nm. The representative SEM images are shown in figure 4. For 160 nm diameter, we observe a large variety of structures: non-vertical wires, membranes and empty tubes (figure 4(a)). For diameters between 200 and 350 nm, uniform vertical nanowires are obtained (figures 4(b) and (c)). Interestingly, InAs nanowires stop growing for diameters larger than 500 nm (figure 4(d)). These results further support the idea of local growth conditions created inside the nanotubes. They also show that the different template openings will require different growth conditions to produce vertical nanowires.

### *3.2. Effect of nanotube depth*

The next parameter explored was the nanotube depth $H$. Clearly, the $H$ (or $H/D$) value strongly influences the local V/III ratio inside the ONTs, with the case of $H > D$ resulting in a very poor supply of the growth species onto the bottom of the nanotubes. This should lead to a longer delay before the nanowire growth can start. Figure 5 shows the nanowire arrays obtained after 90 min of growth with the parameters optimized for 200 nm deep tubes ($T_S = 500\,°\mathrm{C}$, $P_{\mathrm{In}} = 2 \times 10^{-7}$ Torr, $P_{\mathrm{As}} = 1 \times 10^{-5}$ 90 min growth time) and variable $H = 50$, 200 and 400 nm. The exact tube depths were determined from the cross-sections prepared by ion beam thinning, as shown in the insets of figure 5. The yield of vertical nanowires in shallow nanotubes (50 nm) is about 70%; however, we observe more V-shaped membranes than in 200 nm-deep tubes. In this particular case, most membranes nucleate on Si surface inside the nanotubes rather than on the oxide surface (see section 2 in the supporting information). Since smaller depths should relate to higher arsenic inputs, these results are in agreement with [28], where higher V/III ratios gave higher yield of membranes.

As expected, increase of the depth to 400 nm leads to the growth of very few structures and instead most nanotubes remain empty. The absence of growth in this case could be due to insufficient time to nucleate the structures under a low material supply and probably inappropriate effective V/III ratio in the bottom of the nanotubes under these conditions. Therefore, below we present a more detailed growth study in 400 nm deep nanotubes.

### *3.3. Growth in deep nanotubes*

Considering that the growth in nanotubes with $H > D$ is controlled by surface diffusion and re-emission and hence should be much slower than in shallow tubes, we have first explored the effect of growth time under the same growth conditions as in sections 3.2 and 3.3. The representative SEM images for this time series are shown in figure 6. Clearly, increasing the growth time has a positive effect on the yield. After 1.5 h of growth, very few wires were obtained and tubes mainly remained empty, as presented in the (figure 6(a)). The insert in the same figure show closer view to a spontaneous NW growing from the nanotube (left) and the mostly empty tubes (right). For the 5 h growth the yield is pointedly improved (figure 6(c)). The measured overall yield of all structures (mainly vertical and tilted wires) is about 2%, 4% and 67% for the 1.5, 3 and 5 h growths, respectively. A closer look at the 5 h growth results reveals a remarkable difference in the nanowire morphologies that co-exist in one sample. One can observe thin and single crystalline nanowires, similar to those grown for shorter times, and nanowires with multi-grain structure whose crustal quality has significantly degraded with respect to the shorter growth times. These differences are shown in the inset of figure 6(c).

The images shown in the insert to figure 6(a) reveal that some nanowires exhibit different morphologies inside and outside the nanotube, e.g. the diameter shrinks outside of the nanotube and the morphology becomes visibly more defective. This is consistent with the local environments for growth being different in the initial nucleation stage and after the nanowire leaves the template. As in section 3.1, the nanowires are positioned at the nanotube edges. We also tried to improve the vertical yield in the 400 nm-deep nanotubes by increasing

**Table 1.** Comparison between the optimal growth conditions for InAs nanowires on standard patterned Si substrates and ONTs with a tube depth of 200 nm and aspect ratio of one.

| Substrate type | $T_S$ [°C] | $P_{In} \times 10^{-7}$ [Torr] | $P_{As} \times 10^{-5}$ [Torr] | $t$ [min] |
|---|---|---|---|---|
| Standard patterned Si substrate [5] | 500 | 1.2 | 0.6 | 60 |
| Nanotube templates; depth 200 nm | 500 | 1.4 | 1 | 90 |

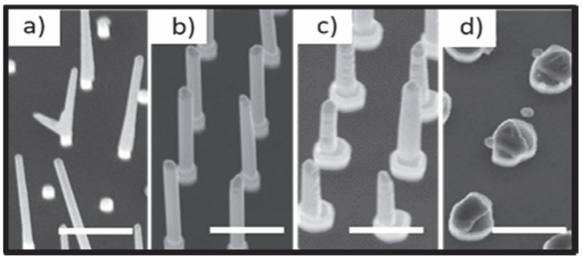

**Figure 4.** SEM images of InAs NWs grown in ONTs. The tube depth $H = 200$ nm and the growth conditions were the same for all samples. The only parameter varied was the tube diameter $D$: (a) 160 nm, (b) 200 nm, (c) 350 nm and (d) 550 nm. The scale bar is 1 $\mu$m and the tilt angle is 20° for all images.

the material fluxes and keeping the growth time at 90 min. However, this just led to an increase in parasitic growth. The details of this study are given in the online supporting information (section 3).

### *3.4. Theoretical model*

We now turn to physical modeling of MBE growth of InAs nanowires in ONTs. We will try to explain the experimentally observed trends such as

(i) The optimum arsenic flux to obtain high vertical yield should be neither too low nor too high;
(ii) It is more difficult to grow regular nanowires in deep tubes (with $H > D$);
(iii) There is an optimum tube diameter range for a given tube height giving the highest vertical yield (for example, $D = 200$–$350$ nm for $H = 200$ nm).

As in [33], we assume that high vertical yields are achieved by the mononuclear vapor–liquid–solid growth in the initial stage, assisted by In droplets as illustrated by scenario (I) in figure 7(a). This view is supported by the fact that most vertical nanowires do not fully cover the template bottom. Scenario (II) in figure 7(a) corresponds to strongly As-rich conditions, leading to the true selective area epitaxy. The signature of this growth mode would be the completely filled template, which was not observed (one should not mix this case with the template filled by the radial nanowire growth in a later stage, as seen in figures 6(b) and (c)). On the other hand, in scenario (III) with the excessive In influx, the droplet will inflate too quickly and the nanotube will soon be filled with In liquid. This liquid will subsequently spread out of the tube, producing multiple and irregular structures. Scenario (IV) in figure 7(a) illustrates the polynuclear growth regime [36] in which two or more droplets emerge in one tube, enabling the growth of more than one nanowires per tube. This is not desirable for growing regular and single-crystalline nanowires, because radial merging of the neighboring nanowires often lead to the formation of poly-crystallites [37].

Continuous In liquid starts forming in the tube in the limiting geometry shown in figure 7(b). The nanowire length including the droplet height reaches the tube height when $L + H_{\text{drop}} = H$, where $L$ is the nanowire length. Assuming that the nanowire is half a cylinder, the arsenic-limited regime of axial nanowire growth [38–41] yields the linear time dependence $L = 2\chi_5 v_5 t$. If we assume that all In atoms arriving into the tube at the rate $\chi_3 v_3$ are subsequently collected by the droplet whose contact angle $\beta$ remains time-independent, the radius of the droplet base $R$ will grow with time as in [38]: $R = [2\Omega_3/\Omega_{35} f(\beta)](\chi_3 v_3 - \chi_5 v_5)t$. Here, $\Omega_3$ is the elementary volume in the In liquid, $\Omega_{35}$ is the volume of InAs pair in the solid state and $f(\beta)$ is the geometrical function relating the volume of half a spherical cap to the radius of its base. Now, the droplet width $R_{\text{drop}}(t_*) = R(t_*)/\sin\beta$ in scenario (I) must remain smaller than the tube diameter $D$ by the moment of time $t_*$ at which $L(t_*) + R(t_*)(1 - \cos\beta)/\sin\beta = H$. Using the above equations for $L(t)$ and $R(t)$, this condition is quantified as

$$\frac{\chi_5 v_5}{\chi_3 v_3} > \frac{c_3[H - D(1 - \cos\beta)}{D + c_3[H - D(1 - \cos\beta)]}, \tag{1}$$

where $c_3 = \Omega_3/[\Omega_{35} f(\beta)\sin\beta]$ is the shape constant.

On the other hand, the mononuclear growth within the tubes requires that the waiting time between two successive nucleation events for In droplets, $t_{\text{nucl}} = 1(\pi D r_c J_{\text{corner}})$, is longer than the time $t_{\text{growth}}$ required to fill the template bottom by one nanowire base [36]. Here, $r_c$ is the radius of the critical nucleus and $J_{\text{corner}}$ is the nucleation rate at the corner of the tube. The $t_{\text{growth}}$ can be approximated as $t_{\text{growth}} \cong D/[2c_3(\chi_3 v_3 - \chi_5 v_5)]$. This yields a lower limit for the tube diameter of the form $D^2 < [2c_3(\chi_3 v_3 - \chi_5 v_5)]/[\pi r_c J_{\text{corner}}]$. Combining this with equation (1), we obtain the two conditions for high vertical yield

$$1 - \frac{D^2}{D^2_{nucl}} > \frac{\chi_5 v_5}{\chi_3 v_3} > \frac{c_3[H - D(1 - \cos\beta)}{D + c_3[H - D(1 - \cos\beta)]} \tag{2}$$

Here, the characteristic 'nucleation' diameter is given by $D^2_{\text{nucl}} = (2c_3\chi_3 v_3)/(\pi r_c J_{\text{corner}})$ and increases with the In flux $v_3$. Therefore, for a given geometry, there is an optimal range of the effective V/III flux ratios to avoid both polynucleation (lower limit) and overloading the template with liquid In (upper limit). The SEM images shown in figure 7(c) perfectly support the existence of scenarios (I), (III) and (IV).

Figure 8(a) shows the corresponding diagrams for the typical $\beta = 120°$ [38–40], $c_3 = 0.27$ and $D_{\text{nucl}} = 350$ nm, at

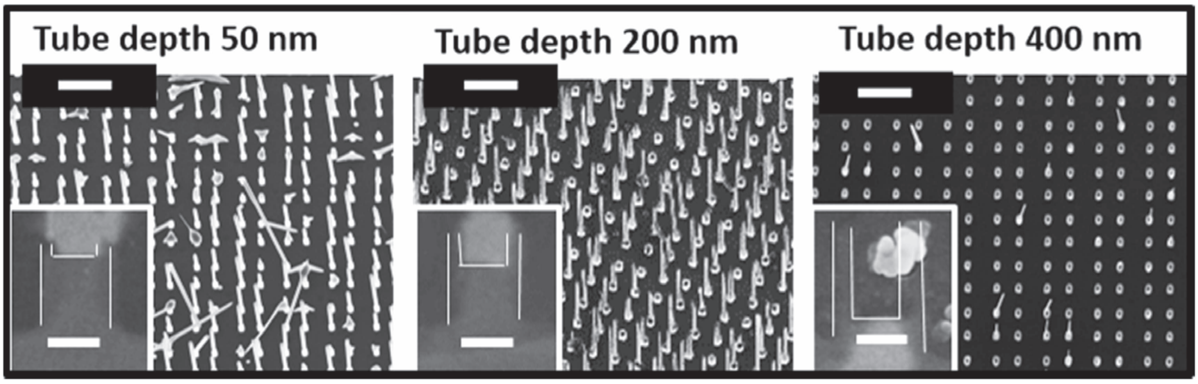

**Figure 5.** InAs NWs growth in the ONTs with different tube depth. The scale bar in the SEM images is 1 $\mu$m and the tilt angle is 20°. The scale bars in the cross-sectional images is 200 nm.

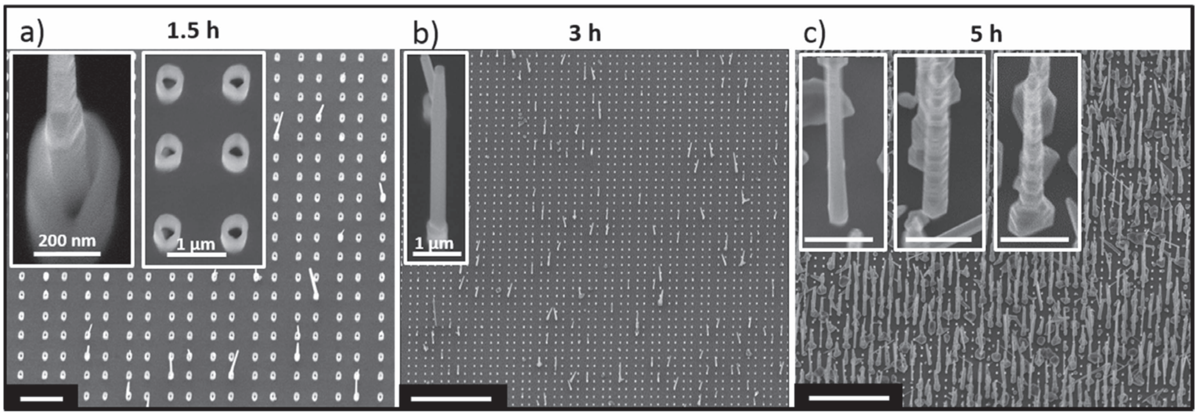

**Figure 6.** 20° tilted SEM images illustrating the time evolution of the morphology in 400 nm deep ONTs. The scale bar is 2 $\mu$m in the 1.5 h image and 10 $\mu$m otherwise.

three different tube depths $H$. These graphs explain qualitatively the major effects. First, the vapor–liquid–solid nucleation of InAs NWs is more difficult in deeper tubes. In fact, increasing $H$ can reduce the optimum region in figure 8(a) to nothing. Second, for a given $H$, there are the optimum regions in both the nanotube diameters $D$ and effective V/III flux ratios $\chi_5 v_5/\chi_3 v_3$ to grow nanowires with high yields, as observed experimentally (sections 3.1 and 3.2).

Up to now, we have focused on the initial growth stage which proceeds as long as the nanowire reaches its full length within the template. After the nanowire leaves the template, the In collection becomes less effective and the As flux onto the droplet increases, both effects leading to increasing the actual V/III influx ratio into the droplet. According to the diagram shown in figure 8(a), this should reduce the droplet size until it disappears completely, as in [33, 39]. After that, the growth is transitioned to the vapor–solid mode and becomes limited by the material transport of In atoms to the nanowire top [42, 43]. Consistent with our experimental observations, we assume that the nanowire radius continues increasing linearly with time due to the In incorporation on the sidewalls:

$$R = R_0 + v_R t. \tag{3}$$

Here, $R_0$ is the initial nanowire radius at the beginning of this growth stage and $v_R$ is the radial growth rate. The axial elongation can be written in the form [42]

$$\frac{\mathrm{d}L}{\mathrm{d}t} = v_3\left(1 + \frac{2\varphi_3}{\pi}\frac{\lambda_3}{R}\right), \tag{4}$$

with $\varphi_3$ as the indium collection efficiency at the nanowire sidewalls and $\lambda_3$ as the diffusion length of In adatoms.

Using equations (3) in (4) and integrating, we obtain

$$L = v_3 t + \Lambda_3 \ln\left(1 + \frac{v_R t}{R_0}\right), \tag{5}$$

with $\Lambda_3 = (2\varphi_3 v_3/\pi v_R)\lambda_3$ as the effective collection length of indium on the top part of the NW sidewalls. The unusual logarithmic dependence arises due to lateral growth, and is converged to the more common expression $L = v_3 t[1 + (2\varphi_3\lambda_3)/(\pi R_0)]$ only for small times. For long enough growth times, the nanowires elongate at a lower rate according to $L \cong v_3 t$, as observed in our experiments. Figure 8(b)) shows the reasonable fits by equations (3) and (5)

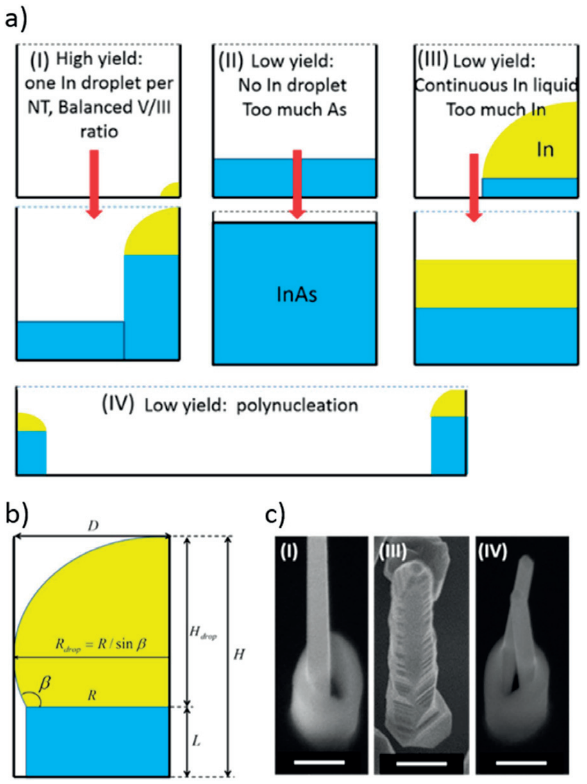

**Figure 7.** (a) Cross-sectional sketches of the nanotubes. (I) High vertical yield under a balanced V/III ratio resulting in mononuclear In-assisted nucleation of nanowires. (II) Strongly As-rich conditions corresponding to the selective area growth. (III) Strongly In-rich conditions producing continuous In liquid within the tube. (IV) Polynucleation resulting in irregular poly-crystallites. (b) Model geometry showing the maximum droplet size within the nanotube template. (c) 20° tilt SEM images supporting scenarios (I), (III) and (IV). The scale bar is 200 nm for all SEM images.

to the measured time dependences of the mean length and radius, obtained with $R_0 = 20$ nm, $v_R = 50$ nm h$^{-1}$, $v_3 = 60$ nm h$^{-1}$ and $\Lambda_3 = 1200$ nm. The representative SEM images of the corresponding time series are shown in the inserts to figure 8(b). More details on the radial growth are given in section 4 of the online supporting information.

## 4. Conclusion

We have demonstrated the MBE template growth of InAs nanowires in large scale silicon dioxide nanotubes on silicon. Geometrical parameters such as the nanotube depth and diameter have been investigated in order to maximize the vertical nanowire yield. The most critical parameter for such growth is the As flux or the effective V/III flux ratio. It has been shown that the maximum vertical yield is achieved for a balanced V/III ratio which should be neither too high nor too small for a given geometry of the ONT. We have presented evidences of In-assisted vapor–liquid–solid growth in the initial stage within the nanotubes under local conditions that are different from the vapor environment. Our theoretical model explains satisfactorily the relation between the growth conditions and the nanotube geometry for obtaining the high vertical yield, as well as the nanowire growth kinetics in a later stage. Overall, this study constitutes the first step toward using the $SiO_2$ nanotubes as templates for the cost-effective and Au-free MBE growth of III–V nanowires on large area silicon substrates.

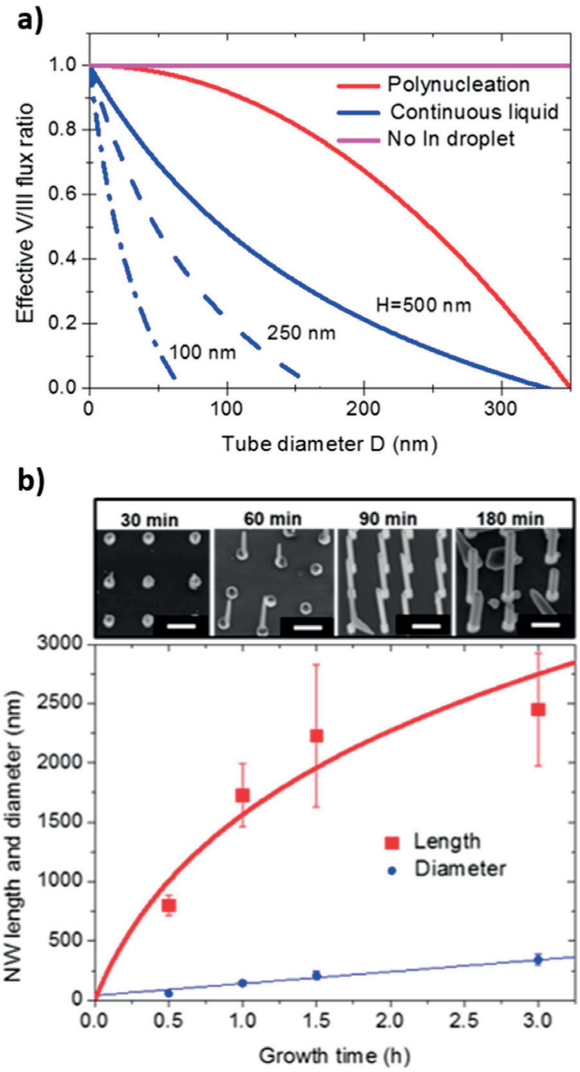

**Figure 8.** (a) Diagram showing the optimum regions for high yield of vertical InAs nanowires in the ONTs in terms of the effective V/III flux ratio and the nanotube diameter. The best zone is separated by the upper limiting curve corresponding to polynucleation in the tubes and the lower limiting curve corresponding to the formation of continuous In liquid in the tubes. The V/III ratio of one corresponds to the absence of the droplet nucleation or their consumption. (b) Mean nanowire radius and length versus time: experimental data (symbols) fitted by the model (lines) with the corresponding 20° tilted SEM images shown above. The nanowires were grown in the ONTs with nominal depths 50–100 nm. The growth conditions used were $T_S = 500$ °C, $P_{In} = 1.4\times10^{-7}$ Torr, $P_{As} = 1\times10^{-5}$. The scale bar is 1 $\mu$m.

## Acknowledgments

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# 4 Conclusions and outlook

This work was dedicated to the fabrication of ordered nanostructures on Si for the increase of its functionality. Top-down and bottom up approaches were used to realize Si and III-V nanostructures. The top-down processes were implemented for the processing of Si substrates. Bottom-up approaches were employed for the further nanostructuring of silicon or growth of III-V nanowires by MBE.

In the first part of the thesis conventional photolithography and RIE was employed to fabricate arrays of Si micropillars. These arrays were further subjected to the stain etching, procedure typically used to prepare porous Si. Combining the cylindrical geometry and electrochemical nature of the porous Si formation we obtained ordered tubular structures. We designed some experiments to explain the mechanism of tube formation. In that purpose we studied key parameters of the stain etching process: doping level of silicon, the pH of the etching solution and geometry by studying pillars with different cross sections. We found that the cylindrical symmetry drives the preferential dissolution of Si trough the center of the pillar. This was confirmed by solving Poisson equation for planar and cylindrical case to calculate the width of depletion region formed on the Si/electrolyte interface. These calculations indicated that the depletion region is thicker on the sidewalls with respect to the planar top. The difference in the thickness of the depletion region results in preferred etching zones and prevents the dissolution from the side, since the depletion region acts as barrier for charge exchange needed for the reaction to occur. By understanding the mechanism, we have been able to obtain different morphologies, e.g. pointed structures, tube with very porous sidewalls and tubes with very thin porous layer. We demonstrated a simple and reproducible process for generating features that were previously challenging to obtain. We then moved to the functionalization of the porous arrays exploiting the luminescence properties of porous Si. Firstly the optical properties were studied by photo and catodoluminescence. The tubes showed expected visible emission what was used to demonstrate functional device that act as LED and also as a solar cell with 2.3% efficiency. We believe further device engineering could significantly improve its performance. For example, luminescence can be tuned by varying the properties of porous layer. Moreover, the study of different passivation layers could be used to improve device performance. Also, the optimizing the contacts can lead in that direction. The process of tube formation can be also investigated on the nanoscale, by using arrays of nanopillars as initial structures.

The rest of the thesis is dedicated to the controlled growth of GaAs and InAs nanowires arrays on Si. We started by studying the control of the orientation and uniformity of GaAs nanowires . High yield was obtained mainly by understanding and controlling the initial stages of growth. The shape and position of the Ga droplets within the openings was shown to have a strong impact on the nanowire final orientation. The main finding is that the droplet should fill symmetrically the opening in order to yield vertical growth. This means that Ga pre-deposition time should be optimized for each hole size. Indeed, we observed improvement of the yield towards bigger holes when more Ga was supplied to the surface. We manage to obtain yield over 90% only for 45 nm holes in which Ga was deposited for 10 minutes using Ga flux of 1.1 Å/s. This indicates that for tailoring the diameter of the nanowires (determined by the opening size) other growth parameters should be optimized; e.g. $As_4$ flux or the growth temperature. Also, we believe the oxide thickness could also be optimized for each opening size. We also found that modifying the surface within the openings can change the wetting properties of Ga. We reported on the Ga pinning by a-Si, that mediated the growth of high yield vertical arrays. This special substrate configuration required special set of growth conditions, including Ga deposition that starts at relatively low temperatures, prior to the recrystallization of a-Si. All this implies that substrate properties and growth conditions are strongly correlated trough complex surface energetics. Entangling this correlation is needed in order to engineer the arrays so high performance devices e.g. solar cells or photodetectors can be fabricated. Furthermore, arrays should be uniform and within this study we tried to understand the evolution of size distributions by studying nucleation statistics. We found that $As_4$ flux has strong impact on the arrays uniformity since it determines the duration of the nucleation stage. Recent work of Dubrovskii predicts that the length distributions may be narrowed down to sub-Poissonian shapes under the appropriate growth conditions. This suggests that other growth parameters should be systematically studied in order to get uniform arrays. For this the fundamentals of tilted and vertical nanowires formation should be fully understood since growth parameters can also affect the yield. It has been demonstrated that substrate characteristics play important role, and therefore should also be studied in more details — e.g. size distributions of the holes should be determined since it can influence the yield and uniformity. These observations make a strong basis for further studies that would potentially enable integration of GaAs on the Si platform.

Finally, we studied the guided growth of InAs nanowires using silicon dioxide templates. This was very challenging to combine with MBE directional fluxes. We found that growth can occur even in deep tubes where there is no direct impingement. This suggests that material is supplied by alternative pathways like surface diffusion and reemission. By modeling the process, we found the correlation between template geometry and growth conditions to obtain high yield growth. Additional novelty in this work is large scale arrays that we obtained by using phase shift lithography as patterning technique. Moreover, InAs nanowire were not integrated on the Si substrate in the conventional way, but rather by growing them on top of Si pillars that were within the template. In this was we formed hybrid heterostructure combining top-down and bottom up approaches. The substrate fabrication process relies only on standard Si processing techniques. This process can be transferred to the growth and integration of other materials on Si.

# A Microtube arrays supporting information

Supporting Information

SI 1

Chemistry governing the stain etching dynamics can be described by a single process in which a large assortment of structuring types is introduced by the variation of boundary conditions[1]. Silicon dissolution in fluoride containing electrolytes is primarily driven by the supply of electron holes in silicon, leading to either direct dissolution of silicon, or to the surface oxidation and dissolution of the oxide by the HF[2]:

$$Si + 4HF_2^- + h^+ \rightarrow SiF_6^{2-} + 2HF + H_2 + e^- \tag{1}$$

$$Si + 2H_2O + nh^+ \rightarrow SiO_2 + 4H^+ + (4-n)e^- \xrightarrow{6\mathrm{HF}} H_2SiF_6 + 2H_2O \tag{2}$$

The positive holes $h^+$ for the reaction can be introduced to the surface of silicon in contact with the electrolyte by anodic injection, photo injection or in this case by ether the nitric acid or the vanadium pentoxide as the oxidant species in the solution[3]:

$$HNO_3 + 2H^+ \rightarrow HNO_2 + H_2O + 2h^+ \tag{3a}$$

$$HNO_2 + H^+ \rightarrow NO^+ + H_2O \rightarrow NO + h^+ + H_2O \tag{3b}$$

$$VO_2^+ + H^+ \rightarrow VO^{2+} + OH^- + h^+ \tag{4}$$

In both cases of direct (Eq. 1) and indirect (Eq. 2) dissolution of silicon, the chemical reaction is limited by the supply of holes. Removal of holes from a volume of silicon will effectively passivate that volume from dissolution by this mechanism. Likewise, increasing the supply of holes in an area of silicon will lead to the preferential etching of that area.

## SI 2. Calculations of depletion region width for different geometries

Thickness of the depletion layer in planar silicon $W_p$ formed in contact with an equipotential surface, such as metal or electrolyte can easily be calculated by solving the Poisson equation inside the semiconductor, with the assumption of equipotential boundary condition on the surface of silicon, and a choice of the potential such that the potential as well as the electric field inside the bulk of the semiconductor vanish. In the complete depletion approximation $W_p$ is given by[4]:

$$W_p = \sqrt{\frac{2\varepsilon U_S}{eN_d}} \tag{1}$$

where $\varepsilon$ is the dielectric constant of silicon, $U_S$ the potential drop in the depletion layer, $e$ elementary charge and $N_d$ the doping density of silicon.

During the formation of macroporous silicon, the existence of the depletion layer in *p*-type silicon leads to the formation of randomly distributed macro-pores at the surface, with the adjoining pore walls of the thickness of $2W$ being passivated towards etching by depletion of holes, with $W$ being the effective depletion layer width.

For non-planar silicon surfaces in contact with the electrolyte the solution of the Poisson equation in silicon near the interface differs from the planar case due to a smaller or larger volume of space charge available per surface area that is compensating the redistributed surface charge due to the equilibration of the Fermi levels between the semiconductor and the electrolyte. To demonstrate the effect of geometry on the properties of the semiconductor/electrolyte interface we have calculated the depletion layer lengths from first principles in a semiconductor with applied surface equipotential condition for simplified spherical and cylindrical convex and concave geometries in comparison with the planar geometry.

The general form for the Poisson equation for the semiconductors is[4]:

$$\nabla^2 U = -\frac{\rho}{\varepsilon} = \frac{e}{\varepsilon}\left(n - p + N_A - N_D\right) \tag{2}$$

In the complete depletion approximation only the ionized dopants are present in the space charge region. In our case, the semiconductor was p-doped silicon:

$$\nabla^2 U = \frac{eN_A}{\varepsilon} \tag{3}$$

If we assume that all the p-dopants are ionized, $N_d = N_A$, so using (1) we can write:

$$\nabla^2 U = \frac{2U_S}{W_p^2} \tag{4}$$

This will simplify the comparison of the depletion widths to the planar case. Plugging the spherical and cylindrical forms of the Laplacian, the Poisson equation for the spherical geometry is:

$$\frac{1}{r^2}\frac{\partial}{\partial r}\left(r^2\frac{\partial U}{\partial r}\right)=\frac{2U_S}{W_p^2} \tag{5}$$

and for cylindrical geometry:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial U}{\partial r}\right)=\frac{2U_S}{W_p^2}. \tag{6}$$

The convex boundary conditions used were (cf Figure 4 in the paper):

$$U(R)=U_S\ ;\ U(R-w)=0\ ;\frac{\partial U(R-w)}{\partial r}=0 \tag{7}$$

while the concave boundary conditions used were:

$$U(R)=U_S\ ;\ U(R+w)=0\ ;\frac{\partial U(R+w)}{\partial r}=0 \tag{8}$$

where $W_p$ stands for the depletion region width in the planar geometry, $r$ is the radial coordinate, $U$ is the potential, $U_S$ the surface potential, $R$ the (curvature) radius of a sphere/cylinder and $w$ the depletion layer width.

After plugging the boundary conditions (7) and (8) into general solutions of the differential equations (5) and (6), the expressions for the depletion layer widths were obtained in the limit of $w \ll R$. The depletion width for the spherical convex geometry $W_{Scv}$ is given by:

$$W_{Scv}=W_P\left(1+\frac{W_P}{3R}+\frac{5W_P^2}{18R^2}+O\left(\frac{W_P}{R}\right)^3\right), \tag{10}$$

depletion width for the spherical concave geometry $W_{Scc}$ is given by:

$$W_{Scc}=W_P\left(1-\frac{W_P}{3R}+\frac{5W_P^2}{18R^2}+O\left(\frac{W_P}{R}\right)^3\right), \tag{11}$$

depletion width for the cylindrical convex geometry $W_{Ccv}$ is given by:

$$W_{Ccv}=W_P\left(1+\frac{W_P}{6R}+\frac{W_P^2}{9R^2}+O\left(\frac{W_P}{R}\right)^3\right) \tag{12}$$

and the depletion width for the cylindrical concave geometry $W_{Ccc}$ is given by:

$$W_{Ccc}=W_P\left(1-\frac{W_P}{6R}+\frac{W_P^2}{9R^2}+O\left(\frac{W_P}{R}\right)^3\right). \tag{13}$$

Therefore, structuring the surface of silicon into an array of micropillars prior to stain etching introduces local spatial inhomogeneity to the etching process, with the concave cylindrical sides of the pillars having slightly larger depletion widths in comparison to the planar tops of the pillars. Due to the symmetry of the pillar, the point where the depletion region width has minimal width is at the center point of each pillar, enabling the rapid initiation of the stain etching process.

The details of the calculations completed by assistance of a Wolfram Mathematica® CAS are attached at the end of this SI as a Mathematica® notebook.

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In[1]:=

```
(* Poisson equation, planar case, p-type silicon *)

Poissplan = D[U[r], {r, 2}] == e * Nd / eps
PPgensol = DSolve[Poissplan, U[r], r]
```

Out[1]= $U''[r] == \frac{e\,Nd}{eps}$

Out[2]= $\left\{\left\{U[r] \to \frac{e\,Nd\,r^2}{2\,eps} + C[1] + r\,C[2]\right\}\right\}$

In[156]:=

```
(* General solution for the planar case: *)
Uplan[r_] := Palpha + r * Pbeta + (e * Nd * r^2) / (2 * eps)
DUplan[r_] := D[Uplan[r], r]

(* Boundary conditions *)
cond1pl = Uplan[r] == Us /. r → 0
cond2pl = Uplan[r] == 0 /. r → Wp
cond3pl = -DUplan[r] == 0 /. r → Wp

(* Particular solution *)
psolplan = Solve[{cond1pl, cond2pl}, {Palpha, Pbeta}]
```

Out[158]= $Palpha == Us$

Out[159]= $Palpha + Pbeta\,Wp + \frac{e\,Nd\,Wp^2}{2\,eps} == 0$

Out[160]= $-Pbeta - \frac{e\,Nd\,Wp}{eps} == 0$

Out[161]= $\left\{\left\{Palpha \to Us,\ Pbeta \to -\frac{2\,eps\,Us + e\,Nd\,Wp^2}{2\,eps\,Wp}\right\}\right\}$

In[21]:=

```
(* Additional condition *)
cond3pl /. {Palpha → Us, Pbeta → -(2 eps Us + e Nd Wp^2)/(2 eps Wp)}
```

Out[21]= $-\frac{e\,Nd\,Wp}{eps} + \frac{2\,eps\,Us + e\,Nd\,Wp^2}{2\,eps\,Wp} == 0$

In[22]:= $\text{Solve}\left[-\frac{e\,Nd\,Wp}{eps} + \frac{2\,eps\,Us + e\,Nd\,Wp^2}{2\,eps\,Wp} == 0 == 0,\ Wp\right]$

Out[22]= $\left\{\left\{Wp \to -\frac{\sqrt{2}\ \sqrt{eps}\ \sqrt{Us}}{\sqrt{e}\ \sqrt{Nd}}\right\},\ \left\{Wp \to \frac{\sqrt{2}\ \sqrt{eps}\ \sqrt{Us}}{\sqrt{e}\ \sqrt{Nd}}\right\}\right\}$

```
(* Solution for the planar case - we take the positive branch *)
```

```
In[162]:= (* ****************** Poisson equation, 1D cylindrical case ****************** *)

          Poisscyl = (1/r) * (D[r * D[U[r], r], r]) == 2 Us/Wp^2
          PCgensol = DSolve[Poisscyl, U[r], r]
```

Out[162]= $\frac{U'[r] + r\,U''[r]}{r} == \frac{2\,Us}{Wp^2}$

Out[163]= $\left\{\left\{U[r] \to \frac{r^2\,Us}{2\,Wp^2} + C[2] + C[1]\,Log[r]\right\}\right\}$

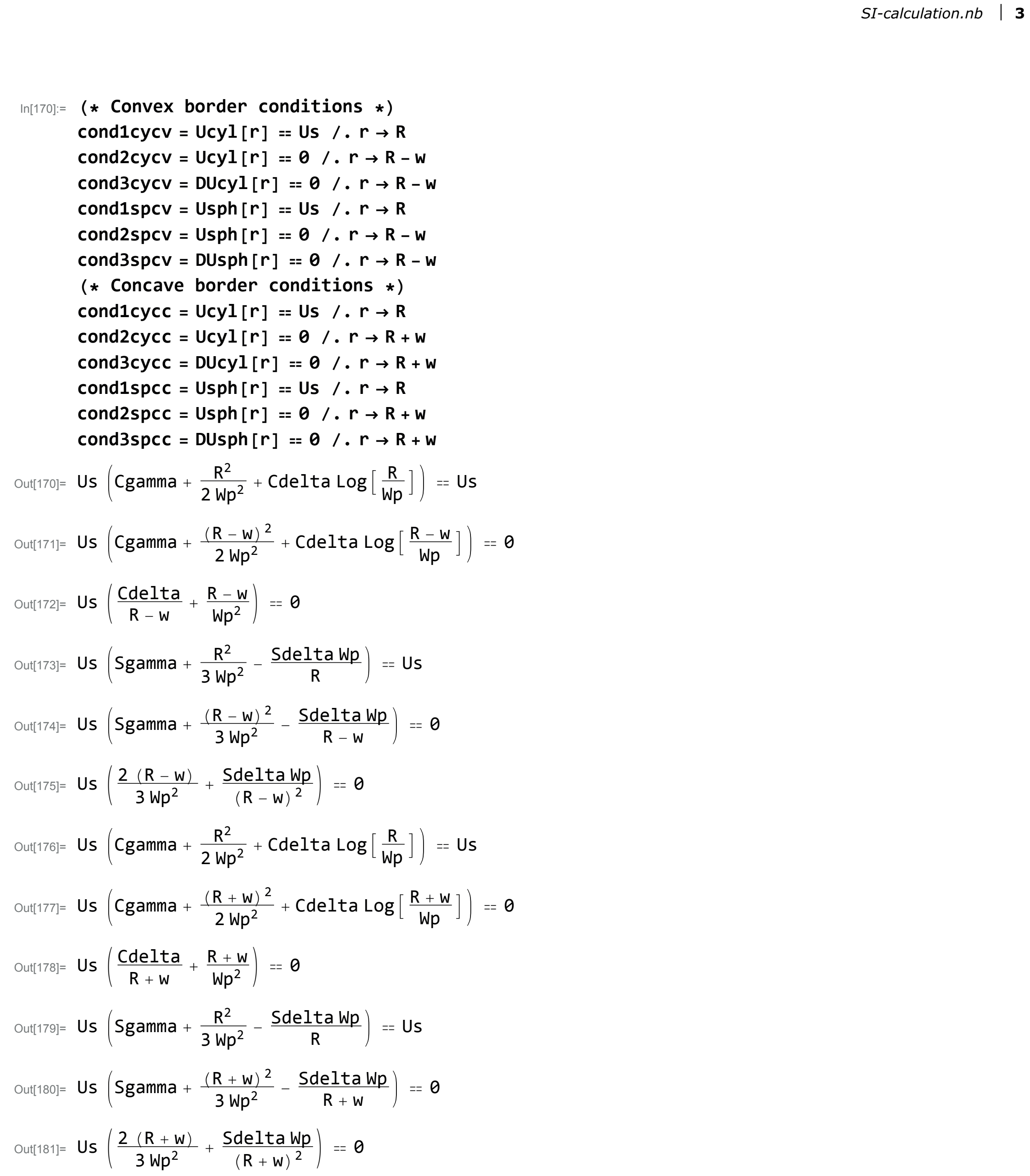
```
In[164]:= (* ****************** Poisson equation, 1D spherical case ****************** *)
          Poisssph = (1/r^2) * (D[r^2 * D[U[r], r], r]) == 2 Us/Wp^2
          PSgensol = DSolve[Poisssph, U[r], r]
```

Out[164]= $\frac{2\,r\,U'[r] + r^2\,U''[r]}{r^2} == \frac{2\,Us}{Wp^2}$

Out[165]= $\left\{\left\{U[r] \to \frac{r^2\,Us}{3\,Wp^2} - \frac{C[1]}{r} + C[2]\right\}\right\}$

```
In[166]:= (* We can rewrite those down in a nicer way *)

          Ucyl[r_] := Us * (Cgamma + Cdelta * Log[r / Wp] + (1/2) * (r / Wp)^2)
          DUcyl[r_] := D[Ucyl[r], r]
          Usph[r_] := Us * (Sgamma - Sdelta/(r / Wp) + (1/3) * (r / Wp)^2)
          DUsph[r_] := D[Usph[r], r]
```



In[170]:=
```
(* Convex border conditions *)
cond1cycv = Ucyl[r] == Us /. r → R
cond2cycv = Ucyl[r] == 0 /. r → R - w
cond3cycv = DUcyl[r] == 0 /. r → R - w
cond1spcv = Usph[r] == Us /. r → R
cond2spcv = Usph[r] == 0 /. r → R - w
cond3spcv = DUsph[r] == 0 /. r → R - w
(* Concave border conditions *)
cond1cycc = Ucyl[r] == Us /. r → R
cond2cycc = Ucyl[r] == 0 /. r → R + w
cond3cycc = DUcyl[r] == 0 /. r → R + w
cond1spcc = Usph[r] == Us /. r → R
cond2spcc = Usph[r] == 0 /. r → R + w
cond3spcc = DUsph[r] == 0 /. r → R + w
```

Out[170]= $\text{Us}\left(\text{Cgamma}+\frac{R^2}{2\,\text{Wp}^2}+\text{Cdelta}\,\text{Log}\left[\frac{R}{\text{Wp}}\right]\right) == \text{Us}$

Out[171]= $\text{Us}\left(\text{Cgamma}+\frac{(R-w)^2}{2\,\text{Wp}^2}+\text{Cdelta}\,\text{Log}\left[\frac{R-w}{\text{Wp}}\right]\right) == 0$

Out[172]= $\text{Us}\left(\frac{\text{Cdelta}}{R-w}+\frac{R-w}{\text{Wp}^2}\right) == 0$

Out[173]= $\text{Us}\left(\text{Sgamma}+\frac{R^2}{3\,\text{Wp}^2}-\frac{\text{Sdelta}\,\text{Wp}}{R}\right) == \text{Us}$

Out[174]= $\text{Us}\left(\text{Sgamma}+\frac{(R-w)^2}{3\,\text{Wp}^2}-\frac{\text{Sdelta}\,\text{Wp}}{R-w}\right) == 0$

Out[175]= $\text{Us}\left(\frac{2\,(R-w)}{3\,\text{Wp}^2}+\frac{\text{Sdelta}\,\text{Wp}}{(R-w)^2}\right) == 0$

Out[176]= $\text{Us}\left(\text{Cgamma}+\frac{R^2}{2\,\text{Wp}^2}+\text{Cdelta}\,\text{Log}\left[\frac{R}{\text{Wp}}\right]\right) == \text{Us}$

Out[177]= $\text{Us}\left(\text{Cgamma}+\frac{(R+w)^2}{2\,\text{Wp}^2}+\text{Cdelta}\,\text{Log}\left[\frac{R+w}{\text{Wp}}\right]\right) == 0$

Out[178]= $\text{Us}\left(\frac{\text{Cdelta}}{R+w}+\frac{R+w}{\text{Wp}^2}\right) == 0$

Out[179]= $\text{Us}\left(\text{Sgamma}+\frac{R^2}{3\,\text{Wp}^2}-\frac{\text{Sdelta}\,\text{Wp}}{R}\right) == \text{Us}$

Out[180]= $\text{Us}\left(\text{Sgamma}+\frac{(R+w)^2}{3\,\text{Wp}^2}-\frac{\text{Sdelta}\,\text{Wp}}{R+w}\right) == 0$

Out[181]= $\text{Us}\left(\frac{2\,(R+w)}{3\,\text{Wp}^2}+\frac{\text{Sdelta}\,\text{Wp}}{(R+w)^2}\right) == 0$

In[47]:=

```
(****************************************************************************
 ***********)
(* Cylindric convex
 case                                                                      *)
(***************************************************************************
*************)

(* Particular solutions for cylindric convex case from cond1 and cond2 *)
psolcycv = Solve[{cond1cycv, cond2cycv}, {Cgamma, Cdelta}]
```

Out[47]=

$$\left\{\left\{\text{Cgamma}\to-\left(\left(R^2\,\text{Log}\left[\frac{R}{\text{Wp}}\right]-2\,R\,w\,\text{Log}\left[\frac{R}{\text{Wp}}\right]+w^2\,\text{Log}\left[\frac{R}{\text{Wp}}\right]-R^2\,\text{Log}\left[\frac{R-w}{\text{Wp}}\right]+2\,\text{Wp}^2\,\text{Log}\left[\frac{R-w}{\text{Wp}}\right]\right)\Big/\left(2\,\text{Wp}^2\left(\text{Log}\left[\frac{R}{\text{Wp}}\right]-\text{Log}\left[\frac{R-w}{\text{Wp}}\right]\right)\right)\right),\ \text{Cdelta}\to-\frac{2\,R\,w-w^2-2\,\text{Wp}^2}{2\,\text{Wp}^2\left(\text{Log}\left[\frac{R}{\text{Wp}}\right]-\text{Log}\left[\frac{R-w}{\text{Wp}}\right]\right)}\right\}\right\}$$

In[48]:=

```
(* Plug Cgamma and Cdelta in cond3cycv *)
cond3cycv /.
```

$$\left\{\text{Cgamma}\to-\left(\left(R^2\,\text{Log}\left[\frac{R}{\text{Wp}}\right]-2\,R\,w\,\text{Log}\left[\frac{R}{\text{Wp}}\right]+w^2\,\text{Log}\left[\frac{R}{\text{Wp}}\right]-R^2\,\text{Log}\left[\frac{R-w}{\text{Wp}}\right]+2\,\text{Wp}^2\,\text{Log}\left[\frac{R-w}{\text{Wp}}\right]\right)\Big/\left(2\,\text{Wp}^2\left(\text{Log}\left[\frac{R}{\text{Wp}}\right]-\text{Log}\left[\frac{R-w}{\text{Wp}}\right]\right)\right)\right),\ \text{Cdelta}\to-\frac{2\,R\,w-w^2-2\,\text{Wp}^2}{2\,\text{Wp}^2\left(\text{Log}\left[\frac{R}{\text{Wp}}\right]-\text{Log}\left[\frac{R-w}{\text{Wp}}\right]\right)}\right\}$$

Out[48]=

$$\text{Us}\left(\frac{R-w}{\text{Wp}^2}-\frac{2\,R\,w-w^2-2\,\text{Wp}^2}{2\,(R-w)\,\text{Wp}^2\left(\text{Log}\left[\frac{R}{\text{Wp}}\right]-\text{Log}\left[\frac{R-w}{\text{Wp}}\right]\right)}\right)==0$$

In[49]:=

```
(* This condition is satisfied when the bracket == 0 *)
```

$$\frac{R-w}{\text{Wp}^2}-\frac{2\,R\,w-w^2-2\,\text{Wp}^2}{2\,(R-w)\,\text{Wp}^2\left(\text{Log}\left[\frac{R}{\text{Wp}}\right]-\text{Log}\left[\frac{R-w}{\text{Wp}}\right]\right)}==0$$

Out[49]=

$$\frac{R-w}{\text{Wp}^2}-\frac{2\,R\,w-w^2-2\,\text{Wp}^2}{2\,(R-w)\,\text{Wp}^2\left(\text{Log}\left[\frac{R}{\text{Wp}}\right]-\text{Log}\left[\frac{R-w}{\text{Wp}}\right]\right)}==0$$

```
(* This can be rearanged for clarity *)
```

In[50]:=

$$\text{Together}\left[\frac{R-w}{\text{Wp}^2}-\frac{2\,R\,w-w^2-2\,\text{Wp}^2}{2\,(R-w)\,\text{Wp}^2\left(\text{Log}\left[\frac{R}{\text{Wp}}\right]-\text{Log}\left[\frac{R-w}{\text{Wp}}\right]\right)}\right]==0$$

Out[50]=

$$\left(-2\,R\,w+w^2+2\,\text{Wp}^2+2\,R^2\,\text{Log}\left[\frac{R}{\text{Wp}}\right]-4\,R\,w\,\text{Log}\left[\frac{R}{\text{Wp}}\right]+2\,w^2\,\text{Log}\left[\frac{R}{\text{Wp}}\right]-2\,R^2\,\text{Log}\left[\frac{R-w}{\text{Wp}}\right]+4\,R\,w\,\text{Log}\left[\frac{R-w}{\text{Wp}}\right]-2\,w^2\,\text{Log}\left[\frac{R-w}{\text{Wp}}\right]\right)\Big/\left(2\,(R-w)\,\text{Wp}^2\left(\text{Log}\left[\frac{R}{\text{Wp}}\right]-\text{Log}\left[\frac{R-w}{\text{Wp}}\right]\right)\right)==0$$

In[51]:=

```
(* This is zero if nominator is zero,
or denominator is infinite. We're interested in zero nominator *)
```

$$\text{FullSimplify}\left[-2\,R\,w+w^2+2\,\text{Wp}^2+2\,R^2\,\text{Log}\left[\frac{R}{\text{Wp}}\right]-4\,R\,w\,\text{Log}\left[\frac{R}{\text{Wp}}\right]+2\,w^2\,\text{Log}\left[\frac{R}{\text{Wp}}\right]-2\,R^2\,\text{Log}\left[\frac{R-w}{\text{Wp}}\right]+4\,R\,w\,\text{Log}\left[\frac{R-w}{\text{Wp}}\right]-2\,w^2\,\text{Log}\left[\frac{R-w}{\text{Wp}}\right]==0\right]$$

Out[51]=

$$w^2+2\,\text{Wp}^2+2\,(R-w)^2\left(\text{Log}\left[\frac{R}{\text{Wp}}\right]-\text{Log}\left[\frac{R-w}{\text{Wp}}\right]\right)==2\,R\,w$$

In[52]:= **(* This can be rearanged into:**

$$-2Rw{*}w^2+2Wp^2 - (R-w)^2\text{Log}\left[\left(\tfrac{R-w}{R}\right)^2\right]==0$$

$$(R-w)^2-R^2+2Wp^2- (R-w)^2\text{Log}\left[\left(\tfrac{R-w}{R}\right)^2\right]==0$$

$$(R-w)^2\left(1-\text{Log}\left[\left(\tfrac{R-w}{R}\right)^2\right]\right)==R^2-2Wp^2$$

**Finally, everyithing / $R^2$**

***)**

$$\left(\frac{R-w}{R}\right)^2\left(1-\text{Log}\left[\left(\frac{R-w}{R}\right)^2\right]\right)==1-2\,(Wp/R)^2$$

**(* Substitution x→ $2(Wp/R)^2$ and y→ $((R-w)/R)^2$**

Out[52]= $$\frac{(R-w)^2\left(1-\text{Log}\left[\frac{(R-w)^2}{R^2}\right]\right)}{R^2}==1-\frac{2\,Wp^2}{R^2}$$

In[53]:= $$y\,(1-\text{Log}[y])==1-x$$

Out[53]= $$y\,(1-\text{Log}[y])==1-x$$

```
(* This transcendental equation can be represented
  as x[y] and expended into series about the point y=1 *)
```

In[54]:= $$\text{seriesY}=\text{Series}\left[1-y\,(1-\text{Log}[y]),\ \{y,1,5\}\right]$$

Out[54]= $$\frac{1}{2}(y-1)^2-\frac{1}{6}(y-1)^3+\frac{1}{12}(y-1)^4-\frac{1}{20}(y-1)^5+O[y-1]^6$$

In[55]:=

```
(* To get y[x] we invert the series *)
seriesX1 = InverseSeries[seriesY, x]
InverseSeries[seriesX1, y]
(* wee see that upon inverting the inverted series we get the same as seriesY,
down to a constant *)
```

Out[55]= $$1+\sqrt{2}\sqrt{x}+\frac{x}{3}-\frac{x^{3/2}}{18\sqrt{2}}+\frac{2x^2}{135}+O[x]^{5/2}$$

Out[56]= $$\frac{y^2}{2}-\frac{y^3}{6}+\frac{y^4}{12}-\frac{y^5}{20}+O[y]^6$$

In[57]:=

```
(* We are interested in the branch where y<1, because for the convex case W≤R -
  so we must change the formula a bit to select the second branch *)
```

$$\text{seriesX2}=1-\sqrt{2}\sqrt{x}+\frac{x}{3}+\frac{x^{3/2}}{18\sqrt{2}}+\frac{2x^2}{135}+O[x]^{5/2}$$

Out[57]= $$1-\sqrt{2}\sqrt{x}+\frac{x}{3}+\frac{x^{3/2}}{18\sqrt{2}}+\frac{2x^2}{135}+O[x]^{5/2}$$

In[58]:=

```
(* To verify, we can invert again and see if we get the same *)
InverseSeries[seriesX2, y]
```

Out[58]= $$\frac{y^2}{2}-\frac{y^3}{6}+\frac{y^4}{12}-\frac{y^5}{20}+O[y]^6$$

In[61]:=

```
(* Clearly, Mathematica has selected the wrong branch,
but we know better so the seriesX2 is the physical solution *)
(* We declare seriesX2 as the y[x_]*)
y[x_] := Normal[seriesX2]

(* We get the solution for w: *)
Solve[y == (R - w)^2 / R^2, w]
```

Out[62]=

$$\left\{\left\{w \to -R\left(-1+\sqrt{y}\right)\right\},\ \left\{w \to R\left(1+\sqrt{y}\right)\right\}\right\}$$

In[63]:=

```
(* We pick the first solution since we know the W will be smaller than R,
and we plug in the definition for x *)
w[R_] = R (1 - Sqrt[y[x]])  /. x → 2 Wp^2 / R^2
```

Out[63]=

$$R\left(1-\sqrt{1+\frac{2\,Wp^2}{3\,R^2}+\frac{8\,Wp^4}{135\,R^4}-2\sqrt{\frac{Wp^2}{R^2}}+\frac{1}{9}\left(\frac{Wp^2}{R^2}\right)^{3/2}}\right)$$

In[66]:=

```
(* For Wp/R<<1, we can expand this into series about 0 -
 first we have to rewrite it for Mathematica, defining z→Wp/R *)
```

$$\text{wsubst} = R\left(1-\sqrt{1+\frac{2\,z^2}{3}+\frac{8\,z^4}{135}-2\,z+\frac{1}{9}\,z^3}\right)$$

```
wseries = Normal[Series[wsubst, {z, 0, 5}]]
```

Out[66]=

$$R\left(1-\sqrt{1-2\,z+\frac{2\,z^2}{3}+\frac{z^3}{9}+\frac{8\,z^4}{135}}\right)$$

Out[67]=

$$R\,z+\frac{R\,z^2}{6}+\frac{R\,z^3}{9}+\frac{103\,R\,z^4}{1080}+\frac{41\,R\,z^5}{360}$$

```
(* since Rz==Wp, this comes down to: *)
```

In[68]:=

$$\text{wseries} = Wp\left(1+\frac{1}{6}\,\frac{Wp}{R}+\frac{1}{9}\left(\frac{Wp}{R}\right)^2+\frac{103}{1080}\left(\frac{Wp}{R}\right)^3+\frac{41}{360}\left(\frac{Wp}{R}\right)^4+O\left[\left(\frac{Wp}{R}\right)^5\right]\right)$$

Out[68]=

$$Wp\left(1+\frac{Wp}{6\,R}+\frac{Wp^2}{9\,R^2}+\frac{103\,Wp^3}{1080\,R^3}+\frac{41\,Wp^4}{360\,R^4}+O\left[\frac{Wp^5}{R^5}\right]^1\right)$$

```
(* Which means that depletion width is always larger than in the planar case,
for the cylindrical convex case *)
```

In[69]:=

```
(**************************************************************************************
***********)
(* Cylindric concave
 case                                                                                *)
(************************************************************************************
*************)

(* Particular solutions for cylindric concave case from cond1 and cond2 *)
psolcycc = Solve[{cond1cycc, cond2cycc}, {Cgamma, Cdelta}]
```

Out[69]=

$$\left\{\left\{\text{Cgamma} \to -\left(\left(R^2 \operatorname{Log}\left[\frac{R}{\text{Wp}}\right] + 2\,R\,w \operatorname{Log}\left[\frac{R}{\text{Wp}}\right] + w^2 \operatorname{Log}\left[\frac{R}{\text{Wp}}\right] - R^2 \operatorname{Log}\left[\frac{R+w}{\text{Wp}}\right] + 2\,\text{Wp}^2 \operatorname{Log}\left[\frac{R+w}{\text{Wp}}\right]\right) \Big/ \left(2\,\text{Wp}^2 \left(\operatorname{Log}\left[\frac{R}{\text{Wp}}\right] - \operatorname{Log}\left[\frac{R+w}{\text{Wp}}\right]\right)\right)\right),\ \text{Cdelta} \to -\frac{-2\,R\,w - w^2 - 2\,\text{Wp}^2}{2\,\text{Wp}^2 \left(\operatorname{Log}\left[\frac{R}{\text{Wp}}\right] - \operatorname{Log}\left[\frac{R+w}{\text{Wp}}\right]\right)}\right\}\right\}$$

In[70]:=

```
(* Plug Cgamma and Cdelta in cond3cycv *)
cond3cycc /.
```

$$\left\{\text{Cgamma} \to -\left(\left(R^2 \operatorname{Log}\left[\frac{R}{\text{Wp}}\right] + 2\,R\,w \operatorname{Log}\left[\frac{R}{\text{Wp}}\right] + w^2 \operatorname{Log}\left[\frac{R}{\text{Wp}}\right] - R^2 \operatorname{Log}\left[\frac{R+w}{\text{Wp}}\right] + 2\,\text{Wp}^2 \operatorname{Log}\left[\frac{R+w}{\text{Wp}}\right]\right) \Big/ \left(2\,\text{Wp}^2 \left(\operatorname{Log}\left[\frac{R}{\text{Wp}}\right] - \operatorname{Log}\left[\frac{R+w}{\text{Wp}}\right]\right)\right)\right),\ \text{Cdelta} \to -\frac{-2\,R\,w - w^2 - 2\,\text{Wp}^2}{2\,\text{Wp}^2 \left(\operatorname{Log}\left[\frac{R}{\text{Wp}}\right] - \operatorname{Log}\left[\frac{R+w}{\text{Wp}}\right]\right)}\right\}$$

Out[70]=

$$\text{Us}\left(\frac{R+w}{\text{Wp}^2} - \frac{-2\,R\,w - w^2 - 2\,\text{Wp}^2}{2\,(R+w)\,\text{Wp}^2 \left(\operatorname{Log}\left[\frac{R}{\text{Wp}}\right] - \operatorname{Log}\left[\frac{R+w}{\text{Wp}}\right]\right)}\right) == 0$$

In[71]:=

```
(* This condition is satisfied when the bracket == 0 *)
```

$$\left(\frac{R+w}{\text{Wp}^2} - \frac{-2\,R\,w - w^2 - 2\,\text{Wp}^2}{2\,(R+w)\,\text{Wp}^2 \left(\operatorname{Log}\left[\frac{R}{\text{Wp}}\right] - \operatorname{Log}\left[\frac{R+w}{\text{Wp}}\right]\right)}\right) == 0$$

Out[71]=

$$\frac{R+w}{\text{Wp}^2} - \frac{-2\,R\,w - w^2 - 2\,\text{Wp}^2}{2\,(R+w)\,\text{Wp}^2 \left(\operatorname{Log}\left[\frac{R}{\text{Wp}}\right] - \operatorname{Log}\left[\frac{R+w}{\text{Wp}}\right]\right)} == 0$$

```
(* This can be rearanged for clarity *)
```

In[72]:=

$$\text{Together}\left[\left(\frac{R+w}{\text{Wp}^2} - \frac{-2\,R\,w - w^2 - 2\,\text{Wp}^2}{2\,(R+w)\,\text{Wp}^2 \left(\operatorname{Log}\left[\frac{R}{\text{Wp}}\right] - \operatorname{Log}\left[\frac{R+w}{\text{Wp}}\right]\right)}\right)\right] == 0$$

Out[72]=

$$\left(2\,R\,w + w^2 + 2\,\text{Wp}^2 + 2\,R^2 \operatorname{Log}\left[\frac{R}{\text{Wp}}\right] + 4\,R\,w \operatorname{Log}\left[\frac{R}{\text{Wp}}\right] + 2\,w^2 \operatorname{Log}\left[\frac{R}{\text{Wp}}\right] - 2\,R^2 \operatorname{Log}\left[\frac{R+w}{\text{Wp}}\right] - 4\,R\,w \operatorname{Log}\left[\frac{R+w}{\text{Wp}}\right] - 2\,w^2 \operatorname{Log}\left[\frac{R+w}{\text{Wp}}\right]\right) \Big/ \left(2\,(R+w)\,\text{Wp}^2 \left(\operatorname{Log}\left[\frac{R}{\text{Wp}}\right] - \operatorname{Log}\left[\frac{R+w}{\text{Wp}}\right]\right)\right) == 0$$

In[73]:= **(* This is zero if nominator is zero,
or denominator is infinite. We're interested in zero nominator *)**

$$\mathtt{FullSimplify}\left[2\,R\,w + w^2 + 2\,Wp^2 + 2\,R^2\,\mathrm{Log}\left[\frac{R}{Wp}\right] + 4\,R\,w\,\mathrm{Log}\left[\frac{R}{Wp}\right] + 2\,w^2\,\mathrm{Log}\left[\frac{R}{Wp}\right] - 2\,R^2\,\mathrm{Log}\left[\frac{R+w}{Wp}\right] - 4\,R\,w\,\mathrm{Log}\left[\frac{R+w}{Wp}\right] - 2\,w^2\,\mathrm{Log}\left[\frac{R+w}{Wp}\right] == 0\right]$$

Out[73]=
$$2\,R\,w + w^2 + 2\,Wp^2 + 2\,(R+w)^2\left(\mathrm{Log}\left[\frac{R}{Wp}\right] - \mathrm{Log}\left[\frac{R+w}{Wp}\right]\right) == 0$$

In[74]:= **(* This can be rearanged into:**

$$2Rw+w^2+2Wp^2-(R+w)^2\ \mathrm{Log}\left[\left(\frac{R+w}{R}\right)^2\right]==0$$

$$(R+w)^2-R^2+2Wp^2-(R+w)^2\ \mathrm{Log}\left[\left(\frac{R+w}{R}\right)^2\right]==0$$

$$(R+w)^2\left(1-\mathrm{Log}\left[\left(\frac{R+w}{R}\right)^2\right]\right)==R^2-2Wp^2$$

**Finally, everything $/R^2$ *)**

$$\left(\frac{R+w}{R}\right)^2\left(1-\mathrm{Log}\left[\left(\frac{R+w}{R}\right)^2\right]\right) == 1-2\,(Wp/R)^2$$

**(* Substitution x→ $(Wp/R)^2$ and y→ $2((R+w)/R)^2$**

Out[74]=
$$\frac{(R+w)^2\left(1-\mathrm{Log}\left[\frac{(R+w)^2}{R^2}\right]\right)}{R^2} == 1-\frac{2\,Wp^2}{R^2}$$

In[75]:= $$y\,(1-\mathrm{Log}[y]) == 1-x$$

Out[75]= $$y\,(1-\mathrm{Log}[y]) == 1-x$$

**(* This transcendental equation can be represented
as x[y] and expended into series about the point y=1 *)**

In[76]:= $$\mathtt{seriesY} = \mathtt{Series}\left[1-y\,(1-\mathrm{Log}[y]),\ \{y,1,5\}\right]$$

Out[76]=
$$\frac{1}{2}(y-1)^2-\frac{1}{6}(y-1)^3+\frac{1}{12}(y-1)^4-\frac{1}{20}(y-1)^5+O[y-1]^6$$

In[77]:=
```
(* To get y[x] we invert the series *)
seriesX1 = InverseSeries[seriesY, x]
InverseSeries[seriesX1, y]
(* wee see that upon inverting the inverted series we get the same as seriesY,
down to a constant *)
```

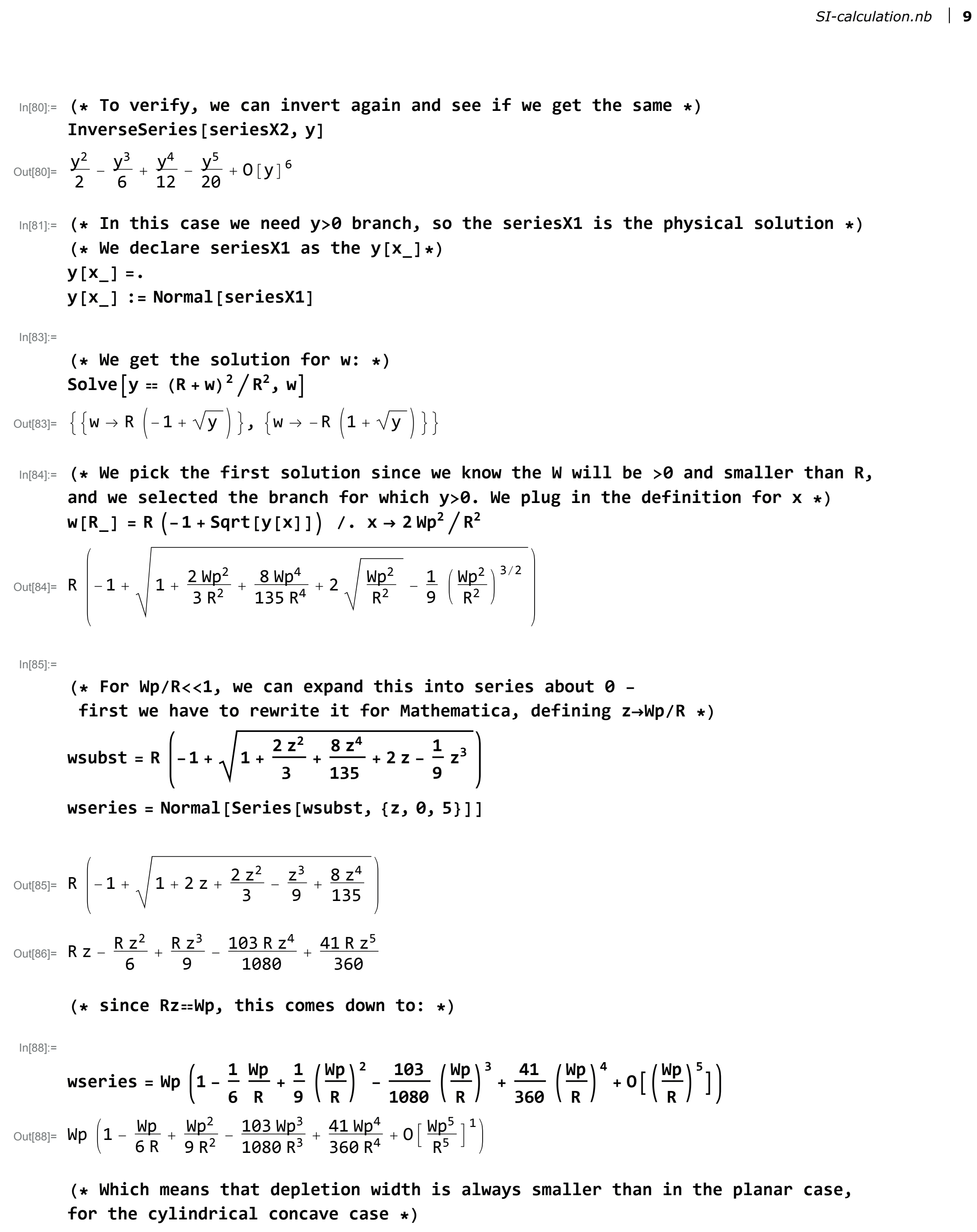
Out[77]=
$$1+\sqrt{2}\,\sqrt{x}+\frac{x}{3}-\frac{x^{3/2}}{18\sqrt{2}}+\frac{2\,x^2}{135}+O[x]^{5/2}$$

Out[78]=
$$\frac{y^2}{2}-\frac{y^3}{6}+\frac{y^4}{12}-\frac{y^5}{20}+O[y]^6$$

In[79]:= **(* In the other branch y<1 - we don't need that branch now *)**

$$\mathtt{seriesX2} = 1-\sqrt{2}\,\sqrt{x}+\frac{x}{3}+\frac{x^{3/2}}{18\sqrt{2}}+\frac{2\,x^2}{135}+O[x]^{5/2}$$

Out[79]=
$$1-\sqrt{2}\,\sqrt{x}+\frac{x}{3}+\frac{x^{3/2}}{18\sqrt{2}}+\frac{2\,x^2}{135}+O[x]^{5/2}$$



In[80]:=
```
(* To verify, we can invert again and see if we get the same *)
InverseSeries[seriesX2, y]
```

Out[80]=
$$\frac{y^2}{2}-\frac{y^3}{6}+\frac{y^4}{12}-\frac{y^5}{20}+O[y]^6$$

In[81]:=
```
(* In this case we need y>0 branch, so the seriesX1 is the physical solution *)
(* We declare seriesX1 as the y[x_]*)
y[x_] =.
y[x_] := Normal[seriesX1]
```

In[83]:=
```
(* We get the solution for w: *)
Solve[y == (R + w)^2 / R^2, w]
```

Out[83]=
$$\left\{\left\{w\to R\left(-1+\sqrt{y}\right)\right\},\left\{w\to -R\left(1+\sqrt{y}\right)\right\}\right\}$$

In[84]:=
```
(* We pick the first solution since we know the W will be >0 and smaller than R,
and we selected the branch for which y>0. We plug in the definition for x *)
w[R_] = R (-1 + Sqrt[y[x]]) /. x → 2 Wp^2 / R^2
```

Out[84]=
$$R\left(-1+\sqrt{1+\frac{2\,Wp^2}{3\,R^2}+\frac{8\,Wp^4}{135\,R^4}+2\sqrt{\frac{Wp^2}{R^2}}-\frac{1}{9}\left(\frac{Wp^2}{R^2}\right)^{3/2}}\right)$$

In[85]:=
```
(* For Wp/R<<1, we can expand this into series about 0 -
 first we have to rewrite it for Mathematica, defining z→Wp/R *)
```

$$\text{wsubst} = R\left(-1+\sqrt{1+\frac{2\,z^2}{3}+\frac{8\,z^4}{135}+2\,z-\frac{1}{9}\,z^3}\right)$$

```
wseries = Normal[Series[wsubst, {z, 0, 5}]]
```

Out[85]=
$$R\left(-1+\sqrt{1+2\,z+\frac{2\,z^2}{3}-\frac{z^3}{9}+\frac{8\,z^4}{135}}\right)$$

Out[86]=
$$R\,z-\frac{R\,z^2}{6}+\frac{R\,z^3}{9}-\frac{103\,R\,z^4}{1080}+\frac{41\,R\,z^5}{360}$$

```
(* since Rz==Wp, this comes down to: *)
```

In[88]:=

$$\text{wseries} = Wp\left(1-\frac{1}{6}\,\frac{Wp}{R}+\frac{1}{9}\left(\frac{Wp}{R}\right)^2-\frac{103}{1080}\left(\frac{Wp}{R}\right)^3+\frac{41}{360}\left(\frac{Wp}{R}\right)^4+O\left[\left(\frac{Wp}{R}\right)^5\right]\right)$$

Out[88]=
$$Wp\left(1-\frac{Wp}{6\,R}+\frac{Wp^2}{9\,R^2}-\frac{103\,Wp^3}{1080\,R^3}+\frac{41\,Wp^4}{360\,R^4}+O\left[\frac{Wp^5}{R^5}\right]^1\right)$$

```
(* Which means that depletion width is always smaller than in the planar case,
for the cylindrical concave case *)
```

```
(****************************************************************************************
 ***********)
(* Spheric convex
 case                                                                         *)
(*******************************************************************************
*************)
```

In[21]:=
```
(* Particular solutions for spherical convex case from cond1 and cond2 *)
psolspcv = Solve[{cond1spcv, cond2spcv}, {Sgamma, Sdelta}]
```

Out[21]=
$$\left\{\left\{\text{Sgamma}\to-\frac{3\,R^2\,w-3\,R\,w^2+w^3-3\,R\,Wp^2}{3\,w\,Wp^2},\ \text{Sdelta}\to-\frac{2\,R^3\,w-3\,R^2\,w^2+R\,w^3-3\,R^2\,Wp^2+3\,R\,w\,Wp^2}{3\,w\,Wp^3}\right\}\right\}$$

In[22]:=
```
(* Plug Sgamma and Sdelta in cond3cycv *)
cond3spcv /.
```
$$\left\{\text{Sgamma}\to-\frac{3\,R^2\,w-3\,R\,w^2+w^3-3\,R\,Wp^2}{3\,w\,Wp^2},\ \text{Sdelta}\to-\frac{2\,R^3\,w-3\,R^2\,w^2+R\,w^3-3\,R^2\,Wp^2+3\,R\,w\,Wp^2}{3\,w\,Wp^3}\right\}$$

Out[22]=
$$\text{Us}\left(\frac{2\,(R-w)}{3\,Wp^2}-\frac{2\,R^3\,w-3\,R^2\,w^2+R\,w^3-3\,R^2\,Wp^2+3\,R\,w\,Wp^2}{3\,(R-w)^2\,w\,Wp^2}\right)==0$$

In[23]:=
```
(* This condition is satisfied when the bracket == 0 *)
```
$$\left(\frac{2\,(R-w)}{3\,Wp^2}-\frac{2\,R^3\,w-3\,R^2\,w^2+R\,w^3-3\,R^2\,Wp^2+3\,R\,w\,Wp^2}{3\,(R-w)^2\,w\,Wp^2}\right)==0$$

Out[23]=
$$\frac{2\,(R-w)}{3\,Wp^2}-\frac{2\,R^3\,w-3\,R^2\,w^2+R\,w^3-3\,R^2\,Wp^2+3\,R\,w\,Wp^2}{3\,(R-w)^2\,w\,Wp^2}==0$$

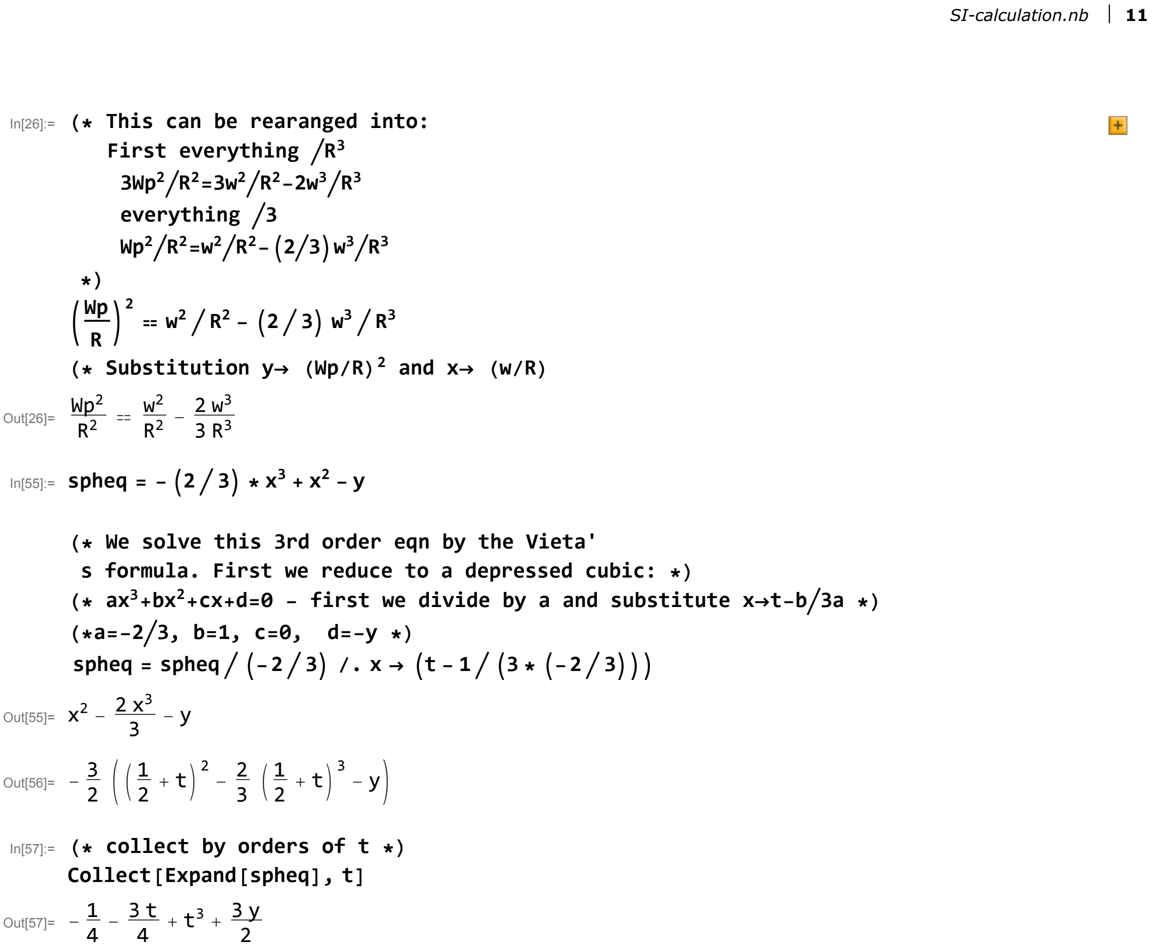
```
(* This can be rearanged for clarity *)
```

In[24]:=
$$\text{Together}\left[\left(\frac{2\,(R-w)}{3\,Wp^2}-\frac{2\,R^3\,w-3\,R^2\,w^2+R\,w^3-3\,R^2\,Wp^2+3\,R\,w\,Wp^2}{3\,(R-w)^2\,w\,Wp^2}\right)\right]==0$$

Out[24]=
$$\frac{-3\,R\,w^2+2\,w^3+3\,R\,Wp^2}{3\,(R-w)\,w\,Wp^2}==0$$

In[25]:=
```
(* This is zero if nominator is zero,
or denominator is infinite. We're interested in zero nominator *)
```
$$\text{eqncc}=-3\,R\,w^2+2\,w^3+3\,R\,Wp^2==0$$

Out[25]=
$$-3\,R\,w^2+2\,w^3+3\,R\,Wp^2==0$$



In[26]:=
```
(* This can be rearanged into:
   First everything /R³
    3Wp²/R²=3w²/R²-2w³/R³
    everything /3
    Wp²/R²=w²/R²-(2/3)w³/R³
 *)
(Wp/R)^2 == w^2 / R^2 - (2 / 3) w^3 / R^3
(* Substitution y→ (Wp/R)^2 and x→ (w/R)
```

Out[26]= $\frac{Wp^2}{R^2} == \frac{w^2}{R^2} - \frac{2\,w^3}{3\,R^3}$

In[55]:=
```
spheq = - (2 / 3) * x^3 + x^2 - y

(* We solve this 3rd order eqn by the Vieta'
 s formula. First we reduce to a depressed cubic: *)
(* ax³+bx²+cx+d=0 - first we divide by a and substitute x→t-b/3a *)
(*a=-2/3, b=1, c=0,  d=-y *)
spheq = spheq / (-2 / 3) /. x → (t - 1 / (3 * (-2 / 3)))
```

Out[55]= $x^2 - \frac{2\,x^3}{3} - y$

Out[56]= $-\frac{3}{2}\left(\left(\frac{1}{2}+t\right)^2 - \frac{2}{3}\left(\frac{1}{2}+t\right)^3 - y\right)$

In[57]:=
```
(* collect by orders of t *)
Collect[Expand[spheq], t]
```

Out[57]= $-\frac{1}{4} - \frac{3\,t}{4} + t^3 + \frac{3\,y}{2}$

In[121]:=

```
(* depressed cubic: t^3+pt+q==0 *)
p = -3 / 4
q = -1 / 4 + 3 * y / 2
(* Viete solutions to a depressed cubic:
   t[k_]:=2*Sqrt[-p/3]*Cos[(1/3)*ArcCos[((3*q)/(2*p))*Sqrt[-3/p]]-2*π*k/3] for k=0,
1,2 *)
tk0 = 2 * Sqrt[-p / 3] * Cos[(1 / 3) * ArcCos[((3 * q) / (2 * p)) * Sqrt[-3 / p]]] /. y → Wp^2 / R^2
tk1 = 2 * Sqrt[-p / 3] *
   Cos[(1 / 3) * ArcCos[((3 * q) / (2 * p)) * Sqrt[-3 / p]] - 2 * π / 3] /. y → Wp^2 / R^2
tk2 = 2 * Sqrt[-p / 3] * Cos[(1 / 3) * ArcCos[((3 * q) / (2 * p)) * Sqrt[-3 / p]] - 4 * π / 3] /.
  y → Wp^2 / R^2
(* Here are the 3 solutions *)
fineq0 = FullSimplify[tk0]
fineq1 = FullSimplify[tk1]
fineq2 = FullSimplify[tk1]
```

Out[121]= $-\frac{3}{4}$

Out[122]= $-\frac{1}{4}+\frac{3\,y}{2}$

Out[123]= $\text{Cos}\left[\frac{1}{3}\,\text{ArcCos}\left[-4\left(-\frac{1}{4}+\frac{3\,\text{Wp}^2}{2\,\text{R}^2}\right)\right]\right]$

Out[124]= $-\text{Sin}\left[\frac{\pi}{6}-\frac{1}{3}\,\text{ArcCos}\left[-4\left(-\frac{1}{4}+\frac{3\,\text{Wp}^2}{2\,\text{R}^2}\right)\right]\right]$

Out[125]= $-\text{Sin}\left[\frac{\pi}{6}+\frac{1}{3}\,\text{ArcCos}\left[-4\left(-\frac{1}{4}+\frac{3\,\text{Wp}^2}{2\,\text{R}^2}\right)\right]\right]$

Out[126]= $\text{Cos}\left[\frac{1}{3}\,\text{ArcCos}\left[1-\frac{6\,\text{Wp}^2}{\text{R}^2}\right]\right]$

Out[127]= $-\text{Sin}\left[\frac{1}{3}\,\text{ArcSin}\left[1-\frac{6\,\text{Wp}^2}{\text{R}^2}\right]\right]$

Out[128]= $-\text{Sin}\left[\frac{1}{3}\,\text{ArcSin}\left[1-\frac{6\,\text{Wp}^2}{\text{R}^2}\right]\right]$

```
In[91]:= (* Let's verify the solutions *)
x0 = FullSimplify[(tk0 - 1/(3 * (-2/3)))]
x1 = FullSimplify[(tk1 - 1/(3 * (-2/3)))]
x2 = FullSimplify[(tk2 - 1/(3 * (-2/3)))]

ident0 = Wp^2/R^2 == z^2 - 2 z^3/3 /. z → x0
ident1 = Wp^2/R^2 == z^2 - 2 z^3/3 /. z → x1
ident2 = Wp^2/R^2 == z^2 - 2 z^3/3 /. z → x2
FullSimplify[ident0]
FullSimplify[ident1]
FullSimplify[ident2]
```

Out[91]= $\frac{1}{2}+\mathrm{Cos}\left[\frac{1}{3}\mathrm{ArcCos}\left[1-\frac{6\,\mathrm{Wp}^2}{R^2}\right]\right]$

Out[92]= $\frac{1}{2}-\mathrm{Sin}\left[\frac{1}{3}\mathrm{ArcSin}\left[1-\frac{6\,\mathrm{Wp}^2}{R^2}\right]\right]$

Out[93]= $\frac{1}{2}-\mathrm{Sin}\left[\frac{1}{6}\left(\pi+2\,\mathrm{ArcCos}\left[1-\frac{6\,\mathrm{Wp}^2}{R^2}\right]\right)\right]$

Out[94]= $\frac{\mathrm{Wp}^2}{R^2} == \left(\frac{1}{2}+\mathrm{Cos}\left[\frac{1}{3}\mathrm{ArcCos}\left[1-\frac{6\,\mathrm{Wp}^2}{R^2}\right]\right]\right)^2-\frac{2}{3}\left(\frac{1}{2}+\mathrm{Cos}\left[\frac{1}{3}\mathrm{ArcCos}\left[1-\frac{6\,\mathrm{Wp}^2}{R^2}\right]\right]\right)^3$

Out[95]= $\frac{\mathrm{Wp}^2}{R^2} == \left(\frac{1}{2}-\mathrm{Sin}\left[\frac{1}{3}\mathrm{ArcSin}\left[1-\frac{6\,\mathrm{Wp}^2}{R^2}\right]\right]\right)^2-\frac{2}{3}\left(\frac{1}{2}-\mathrm{Sin}\left[\frac{1}{3}\mathrm{ArcSin}\left[1-\frac{6\,\mathrm{Wp}^2}{R^2}\right]\right]\right)^3$

Out[96]= $\frac{\mathrm{Wp}^2}{R^2} == \left(\frac{1}{2}-\mathrm{Sin}\left[\frac{1}{6}\left(\pi+2\,\mathrm{ArcCos}\left[1-\frac{6\,\mathrm{Wp}^2}{R^2}\right]\right)\right]\right)^2-\frac{2}{3}\left(\frac{1}{2}-\mathrm{Sin}\left[\frac{1}{6}\left(\pi+2\,\mathrm{ArcCos}\left[1-\frac{6\,\mathrm{Wp}^2}{R^2}\right]\right)\right]\right)^3$

```
Out[97]= True

Out[98]= True

Out[99]= True
```

```
(* All three solutions are correct. However,
in our case we know that W≤R, so (W/R)<1. Also, (W/R)>0,
so we're looking for a solution in the interval of 0<(W/R)≤1.  *)
```

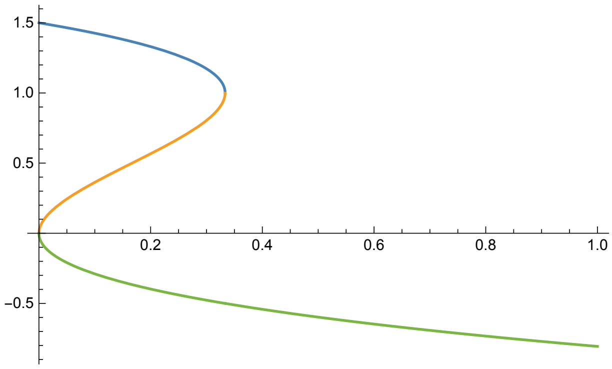
In[116]:=
```
Clear[x]
ident0 = 1/2 + Cos[1/3 ArcCos[1 - 6 * x]]
ident1 = 1/2 - Sin[1/3 ArcSin[1 - 6 * x]]
ident2 = 1/2 - Sin[1/6 (π + 2 ArcCos[1 - 6 x])]
Plot[{ident0, ident1, ident2}, {x, 0, 1}]
```

Out[117]= $\frac{1}{2} + \mathrm{Cos}\left[\frac{1}{3}\,\mathrm{ArcCos}[1 - 6\,x]\right]$

Out[118]= $\frac{1}{2} - \mathrm{Sin}\left[\frac{1}{3}\,\mathrm{ArcSin}[1 - 6\,x]\right]$

Out[119]= $\frac{1}{2} - \mathrm{Sin}\left[\frac{1}{6}\left(\pi + 2\,\mathrm{ArcCos}[1 - 6\,x]\right)\right]$

Out[120]=



```
(* We see that the solution ident1=
 1/2-Sin[1/3 ArcSin[1-6x]] is well defined within 0<(W/R)≤1 *)
```

In[140]:=
```
series = Series[ident1, {x, 0, 6}];
sol = W / R == Normal[series] /. x → Wp^2 / R^2;
FullSimplify[Solve[sol, W], {Wp > 0, R > 0}]
```

Out[142]=
$$\left\{\left\{W \to Wp + \frac{Wp^2}{3\,R} + \frac{5\,Wp^3}{18\,R^2} + \frac{8\,Wp^4}{27\,R^3} + \frac{77\,Wp^5}{216\,R^4} + \frac{112\,Wp^6}{243\,R^5} + \frac{2431\,Wp^7}{3888\,R^6} + \frac{640\,Wp^8}{729\,R^7} + \frac{1\,062\,347\,Wp^9}{839\,808\,R^8} + \frac{36\,608\,Wp^{10}}{19\,683\,R^9} + \frac{14\,003\,665\,Wp^{11}}{5\,038\,848\,R^{10}} + \frac{745\,472\,Wp^{12}}{177\,147\,R^{11}}\right\}\right\}$$

In[143]:=
```
Wseries = Wp (1 + Wp / (3 R) + 5 Wp^2/(18 R^2) + 8 Wp^3/(27 R^3) + 77 Wp^4/(216 R^4) + O[Wp / R]^5)
```

Out[143]= $Wp\left(1 + \frac{Wp}{3\,R} + \frac{5\,Wp^2}{18\,R^2} + \frac{8\,Wp^3}{27\,R^3} + \frac{77\,Wp^4}{216\,R^4} + \left(O\left[\frac{Wp}{R}\right]^1\right)^5\right)$

```
(* So, for spherical convex case depletion
 width is always larger than in the planar case *)
```

```
(*************************************************************************************
 ***********)
(* Spheric concave
 case                                                                               *)
(********************************************************************************
*************)
```

In[187]:=

```
(* Particular solutions for spherical convex case from cond1 and cond2 *)
psolspcc = Solve[{cond1spcc, cond2spcc}, {Sgamma, Sdelta}]
```

Out[187]=

$$\left\{\left\{\text{Sgamma}\to-\frac{3\,R^2\,w+3\,R\,w^2+w^3+3\,R\,Wp^2}{3\,w\,Wp^2},\ \text{Sdelta}\to-\frac{2\,R^3\,w+3\,R^2\,w^2+R\,w^3+3\,R^2\,Wp^2+3\,R\,w\,Wp^2}{3\,w\,Wp^3}\right\}\right\}$$

In[188]:=

```
(* Plug Sgamma and Sdelta in cond3cycv *)
cond3spcc /.
```

$$\left\{\text{Sgamma}\to-\frac{3\,R^2\,w+3\,R\,w^2+w^3+3\,R\,Wp^2}{3\,w\,Wp^2},\ \text{Sdelta}\to-\frac{2\,R^3\,w+3\,R^2\,w^2+R\,w^3+3\,R^2\,Wp^2+3\,R\,w\,Wp^2}{3\,w\,Wp^3}\right\}$$

Out[188]=

$$\text{Us}\left(\frac{2\,(R+w)}{3\,Wp^2}-\frac{2\,R^3\,w+3\,R^2\,w^2+R\,w^3+3\,R^2\,Wp^2+3\,R\,w\,Wp^2}{3\,w\,(R+w)^2\,Wp^2}\right)==0$$

In[189]:=

```
(* This condition is satisfied when the bracket == 0 *)
```

$$\left(\frac{2\,(R+w)}{3\,Wp^2}-\frac{2\,R^3\,w+3\,R^2\,w^2+R\,w^3+3\,R^2\,Wp^2+3\,R\,w\,Wp^2}{3\,w\,(R+w)^2\,Wp^2}\right)==0$$

Out[189]=

$$\frac{2\,(R+w)}{3\,Wp^2}-\frac{2\,R^3\,w+3\,R^2\,w^2+R\,w^3+3\,R^2\,Wp^2+3\,R\,w\,Wp^2}{3\,w\,(R+w)^2\,Wp^2}==0$$

```
(* This can be rearanged for clarity *)
```

In[190]:=

$$\text{Together}\left[\left(\frac{2\,(R+w)}{3\,Wp^2}-\frac{2\,R^3\,w+3\,R^2\,w^2+R\,w^3+3\,R^2\,Wp^2+3\,R\,w\,Wp^2}{3\,w\,(R+w)^2\,Wp^2}\right)\right]==0$$

Out[190]=

$$\frac{3\,R\,w^2+2\,w^3-3\,R\,Wp^2}{3\,w\,(R+w)\,Wp^2}==0$$

In[191]:=

```
(* This is zero if nominator is zero,
or denominator is infinite. We're interested in zero nominator *)
eqncc = 3 R w^2 + 2 w^3 - 3 R Wp^2 == 0
```

Out[191]=

$$3\,R\,w^2+2\,w^3-3\,R\,Wp^2==0$$

In[192]:=

```
(* This can be rearanged into:
   First everything /R^3
    3Wp^2/R^2=3w^2/R^2+2w^3/R^3
    everything /3
    Wp^2/R^2=w^2/R^2+(2/3)w^3/R^3
 *)
(Wp/R)^2 == w^2/R^2 + (2/3) w^3/R^3
(* Substitution y→ (Wp/R)^2 and x→ (w/R)
```

Out[192]=

$$\frac{Wp^2}{R^2} == \frac{w^2}{R^2} + \frac{2\,w^3}{3\,R^3}$$

In[195]:=

```
spheq = (2/3) * x^3 + x^2 - y

(* We solve this 3rd order eqn by Viete
 formula. First we reduce to a depressed cubic: *)
(* ax^3+bx^2+cx+d=0 - first we devide by a and substitute x→t-b/3a *)
(*a=(2/3), b=1, c=0,  d=-y *)
spheq = spheq/(2/3) /. x → (t - 1/(3 * (2/3)))
```

Out[195]=

$$x^2 + \frac{2\,x^3}{3} - y$$

Out[196]=

$$\frac{3}{2}\left(\left(-\frac{1}{2}+t\right)^2+\frac{2}{3}\left(-\frac{1}{2}+t\right)^3-y\right)$$

In[197]:=

```
(* collect by orders of t *)
Collect[Expand[spheq], t]
```

Out[197]=

$$\frac{1}{4}-\frac{3\,t}{4}+t^3-\frac{3\,y}{2}$$

In[206]:=

```
(* depressed cubic: t^3+pt+q==0 *)
p = -3/4
q = 1/4 - 3 y/2
(* Viete solution to a depressed cubic:
   t[k_]:=2*Sqrt[-p/3]*Cos[(1/3)*ArcCos[((3*q)/(2*p))*Sqrt[-3/p]]-2*π*k/3] for k=0,
1,2 *)
tk0 = 2 * Sqrt[-p/3] * Cos[(1/3) * ArcCos[((3 * q) / (2 * p)) * Sqrt[-3/p]]] /. y → Wp^2/R^2
tk1 = 2 * Sqrt[-p/3] *
   Cos[(1/3) * ArcCos[((3 * q) / (2 * p)) * Sqrt[-3/p]] - 2 * π/3] /. y → Wp^2/R^2
tk2 = 2 * Sqrt[-p/3] * Cos[(1/3) * ArcCos[((3 * q) / (2 * p)) * Sqrt[-3/p]] - 4 * π/3] /.
  y → Wp^2/R^2
(* Here are the 3 solutions *)
fineq0 = FullSimplify[tk0]
fineq1 = FullSimplify[tk1]
fineq2 = FullSimplify[tk1]
```

Out[206]= $-\frac{3}{4}$

Out[207]= $\frac{1}{4}-\frac{3\,y}{2}$

Out[208]= $\mathrm{Cos}\left[\frac{1}{3}\,\mathrm{ArcCos}\left[-4\left(\frac{1}{4}-\frac{3\,\mathrm{Wp}^2}{2\,R^2}\right)\right]\right]$

Out[209]= $-\mathrm{Sin}\left[\frac{\pi}{6}-\frac{1}{3}\,\mathrm{ArcCos}\left[-4\left(\frac{1}{4}-\frac{3\,\mathrm{Wp}^2}{2\,R^2}\right)\right]\right]$

Out[210]= $-\mathrm{Sin}\left[\frac{\pi}{6}+\frac{1}{3}\,\mathrm{ArcCos}\left[-4\left(\frac{1}{4}-\frac{3\,\mathrm{Wp}^2}{2\,R^2}\right)\right]\right]$

Out[211]= $\mathrm{Cos}\left[\frac{1}{3}\,\mathrm{ArcCos}\left[-1+\frac{6\,\mathrm{Wp}^2}{R^2}\right]\right]$

Out[212]= $\mathrm{Sin}\left[\frac{1}{3}\,\mathrm{ArcSin}\left[1-\frac{6\,\mathrm{Wp}^2}{R^2}\right]\right]$

Out[213]= $\mathrm{Sin}\left[\frac{1}{3}\,\mathrm{ArcSin}\left[1-\frac{6\,\mathrm{Wp}^2}{R^2}\right]\right]$

In[214]:= **(* Let's verify the solutions *)**

**x0 = FullSimplify[(tk0 - 1/(3 * (2/3)))]**

**x1 = FullSimplify[(tk1 - 1/(3 * (2/3)))]**

**x2 = FullSimplify[(tk2 - 1/(3 * (2/3)))]**

**ident0** = $\frac{Wp^2}{R^2} == z^2 + \frac{2\,z^3}{3}$ **/. z → x0**

**ident1** = $\frac{Wp^2}{R^2} == z^2 + \frac{2\,z^3}{3}$ **/. z → x1**

**ident2** = $\frac{Wp^2}{R^2} == z^2 + \frac{2\,z^3}{3}$ **/. z → x2**

**FullSimplify[ident0]**

**FullSimplify[ident1]**

**FullSimplify[ident2]**

Out[214]= $-\frac{1}{2} + \mathrm{Cos}\left[\frac{1}{3}\,\mathrm{ArcCos}\left[-1 + \frac{6\,Wp^2}{R^2}\right]\right]$

Out[215]= $-\frac{1}{2} + \mathrm{Sin}\left[\frac{1}{3}\,\mathrm{ArcSin}\left[1 - \frac{6\,Wp^2}{R^2}\right]\right]$

Out[216]= $-\frac{1}{2} - \mathrm{Cos}\left[\frac{1}{3}\,\mathrm{ArcCos}\left[1 - \frac{6\,Wp^2}{R^2}\right]\right]$

Out[217]= $\frac{Wp^2}{R^2} == \left(-\frac{1}{2} + \mathrm{Cos}\left[\frac{1}{3}\,\mathrm{ArcCos}\left[-1 + \frac{6\,Wp^2}{R^2}\right]\right]\right)^2 + \frac{2}{3}\left(-\frac{1}{2} + \mathrm{Cos}\left[\frac{1}{3}\,\mathrm{ArcCos}\left[-1 + \frac{6\,Wp^2}{R^2}\right]\right]\right)^3$

Out[218]= $\frac{Wp^2}{R^2} == \left(-\frac{1}{2} + \mathrm{Sin}\left[\frac{1}{3}\,\mathrm{ArcSin}\left[1 - \frac{6\,Wp^2}{R^2}\right]\right]\right)^2 + \frac{2}{3}\left(-\frac{1}{2} + \mathrm{Sin}\left[\frac{1}{3}\,\mathrm{ArcSin}\left[1 - \frac{6\,Wp^2}{R^2}\right]\right]\right)^3$

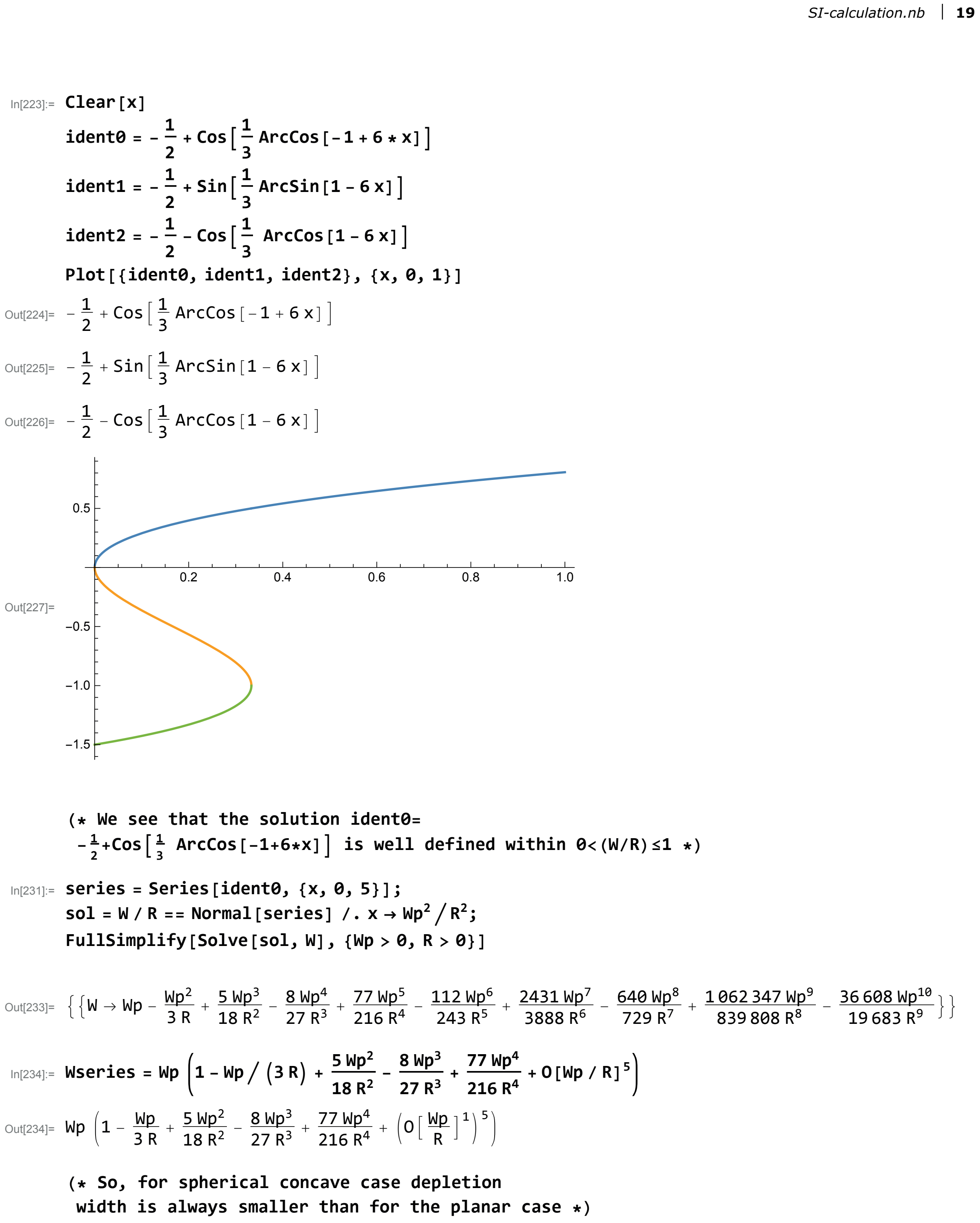
Out[219]= $\frac{Wp^2}{R^2} == \left(-\frac{1}{2} - \mathrm{Cos}\left[\frac{1}{3}\,\mathrm{ArcCos}\left[1 - \frac{6\,Wp^2}{R^2}\right]\right]\right)^2 + \frac{2}{3}\left(-\frac{1}{2} - \mathrm{Cos}\left[\frac{1}{3}\,\mathrm{ArcCos}\left[1 - \frac{6\,Wp^2}{R^2}\right]\right]\right)^3$

Out[220]= True

Out[221]= True

Out[222]= True

```
(* All three solutions are correct. However,
in our case we know that W≤R, so (W/R)<1. Also, (W/R)>0,
so we're looking for a solution in the interval of 0<(W/R)≤1.  *)
```



In[223]:= Clear[x]

$$\text{ident0} = -\frac{1}{2} + \text{Cos}\left[\frac{1}{3}\,\text{ArcCos}[-1 + 6 * x]\right]$$

$$\text{ident1} = -\frac{1}{2} + \text{Sin}\left[\frac{1}{3}\,\text{ArcSin}[1 - 6\,x]\right]$$

$$\text{ident2} = -\frac{1}{2} - \text{Cos}\left[\frac{1}{3}\,\text{ArcCos}[1 - 6\,x]\right]$$

```
Plot[{ident0, ident1, ident2}, {x, 0, 1}]
```

Out[224]= $-\frac{1}{2} + \text{Cos}\left[\frac{1}{3}\,\text{ArcCos}[-1 + 6\,x]\right]$

Out[225]= $-\frac{1}{2} + \text{Sin}\left[\frac{1}{3}\,\text{ArcSin}[1 - 6\,x]\right]$

Out[226]= $-\frac{1}{2} - \text{Cos}\left[\frac{1}{3}\,\text{ArcCos}[1 - 6\,x]\right]$

Out[227]=

(* We see that the solution ident0= $-\frac{1}{2}+\text{Cos}\left[\frac{1}{3}\,\text{ArcCos}[-1+6*x]\right]$ is well defined within 0<(W/R)≤1 *)

In[231]:=

$$\text{series} = \text{Series}[\text{ident0}, \{x, 0, 5\}];$$
$$\text{sol} = W / R == \text{Normal}[\text{series}]\ /.\ x \to \text{Wp}^2 \big/ R^2;$$

```
FullSimplify[Solve[sol, W], {Wp > 0, R > 0}]
```

Out[233]= $\left\{\left\{W \to \text{Wp} - \frac{\text{Wp}^2}{3\,R} + \frac{5\,\text{Wp}^3}{18\,R^2} - \frac{8\,\text{Wp}^4}{27\,R^3} + \frac{77\,\text{Wp}^5}{216\,R^4} - \frac{112\,\text{Wp}^6}{243\,R^5} + \frac{2431\,\text{Wp}^7}{3888\,R^6} - \frac{640\,\text{Wp}^8}{729\,R^7} + \frac{1\,062\,347\,\text{Wp}^9}{839\,808\,R^8} - \frac{36\,608\,\text{Wp}^{10}}{19\,683\,R^9}\right\}\right\}$

In[234]:= $\text{Wseries} = \text{Wp}\left(1 - \text{Wp} \big/ (3\,R) + \frac{5\,\text{Wp}^2}{18\,R^2} - \frac{8\,\text{Wp}^3}{27\,R^3} + \frac{77\,\text{Wp}^4}{216\,R^4} + O[\text{Wp} / R]^5\right)$

Out[234]= $\text{Wp}\left(1 - \frac{\text{Wp}}{3\,R} + \frac{5\,\text{Wp}^2}{18\,R^2} - \frac{8\,\text{Wp}^3}{27\,R^3} + \frac{77\,\text{Wp}^4}{216\,R^4} + \left(O\left[\frac{\text{Wp}}{R}\right]^1\right)^5\right)$

(* So, for spherical concave case depletion width is always smaller than for the planar case *)

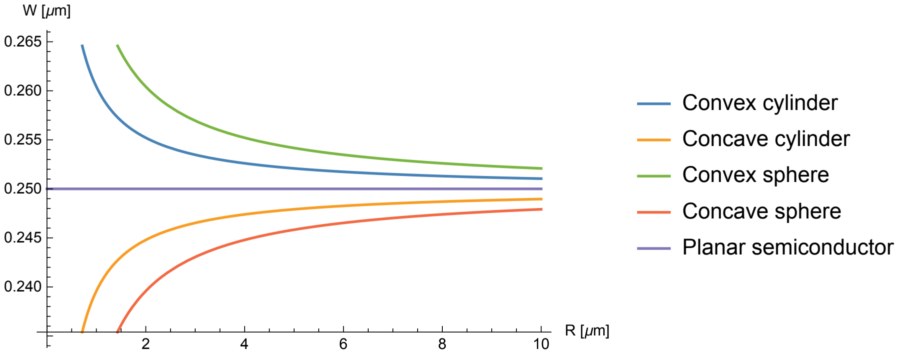
In[235]:=

```
(* Let's compare all the solutions *)

(* Let's say that Wp=250 nm *)
Wp = 0.25
Wcylcv[R_] := Wp (1 + Wp / (6 * R))
Wcylcc[R_] := Wp (1 - Wp / (6 * R))
Wsphcv[R_] := Wp (1 + Wp / (3 * R))
Wsphcc[R_] := Wp (1 - Wp / (3 * R))
Wplanar[R_] := Wp
graphic = Plot[{Wcylcv[R], Wcylcc[R], Wsphcv[R], Wsphcc[R], Wplanar[R]}, {R, 0, 10},
  PlotLegends → LineLegend[{"Convex cylinder", "Concave cylinder", "Convex sphere",
     "Concave sphere", "Planar semiconductor"}], AxesLabel → {"R [μm]", "W [μm]"}]
```

Out[235]= 0.25

Out[241]=



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# Jelena Vukajlović Pleština

## WORK EXPERIENCE

2013 – PRESENT

**École Polytechnique Fédérale de Lausanne**
**Lausanne, Switzerland**

- Large scale integration of $III-V$ semiconductors into silicon (Innovative Training Network — NanoEmbrace funded under the European Commission FP7)
- Development of 3D nanowire-based $GaAs$ solar cells
- Fabrication of silicon nanostructures for cell drug delivery
- Porous silicon micro-nano structures for sensors and LED
- Tutoring master and bachelor students (semester projects)

2011 – 2013

**Medical High School, Split, Croatia**

- Physics Teacher

## EDUCATION

SINCE 2013 Ph.D.
**École Polytechnique Fédérale de Lausanne**
**Lausanne, Switzerland**
Thesis advisors: Prof. Anna Fonctuberta i Morral

2010 M.Sc. Degree
**University of Zagreb — Faculty of Science**
**Zagreb, Croatia**
*Thesis title: "Raman spectroscopy of stractural phase transitions in* $BaTi0_3$ *nanowires."*
Thesis advisors: Dr. Andreja Gajović

## FURTHER EDUCATION

2014 *The effective and collaborative researcher*
Soft skills training, New Castle, United Kingdom
2014 *School of Nanostructures Growth Mechanisms*
Rome, Italy

## SCIENTIFIC CONFERENCES

2015 *Nanowire Growth Workshop* (*talk, poster*)
Barcelona, Spain
2014 *Micro and Nano Engineering* (*poster*)
Lausanne, Switzerland
2013 *Nanowire Growth Workshop* (*organisation*)
Barcelona, Spain

## PERSONAL DETAILS

| | |
|---|---|
| DATE OF BIRTH | 4th April 1982,M. Lošinj, Croatia |
| NATIONALITY | Croatian |
| SEX | female |
| STATUS | married |

✉ Av. Gustave-Coderey 6, 1110 Morges, Switzerland
☎ +41 (0)76 708 34 47
✍ Jelena.VukajlovicPlestina@epfl.ch

## SKILLS AND COMPETENCES

### Micronano Fabrication Techniques

- Photolithography
- Electron beam lithography
- Dry and wet etching
- Thin film technologies — thermal evaporation, sputtering, atomic layer deposition, dry and wet oxidation, diffusion
- Polydimethylsiloxan packing (PDMS) — fabrication of flexible nanostructure arrays
- Molecular beam epitaxy — growth of $III-V$ semiconductor nanostructures

### Metrology Techniques

- Scanning electron microscopy (SEM)
- Energy-dispersive X-ray spectroscopy (EDX)
- Optical measurements — spectroscopic ellipsometry, spectroscopic reflectrometry, Raman spectroscopy
- Electrical measurements — photovoltaic characterisation

### Computing

- Linux, Windows
- MEEP – finite-difference time domain simulations
- Clewin, KLayout — physical layout editors
- ImageJ, Origin — image processing, analysis and statistics
- Microsoft Office, LibreOffice, LaTeX

### Communication

- Documenting Work, Publishing and Presenting Results
- Teamwork, Organization, International Collaboration
- Leadership, Tutoring, Science Outreach

### Languages

| | |
|---|---|
| ENGLISH | Full professional proficiency |
| FRENCH | Basic communication skills |
| GERMAN | Basic communication skills |
| ITALIAN | Basic communication skills |
| CROATIAN/SERBIAN | Native proficiency |

## REFERENCES

**Prof. Anna Fontcuberta i Morral, EPFL, Lausanne**
Anna.Foncuberta-Morral@epfl.ch

- Associate professor, Head of Laboratory of Semiconductor Materials (LMSC) and Ph.D. Thesis advisor

**Dr. Philippe Flückiger, EPFL, Lausanne**
Phlippe.Fluckiger@epfl.ch

- Operational director of Center for Micronanotechnology (CMI) at EPFL