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Condition for the negative capacitance effect in metal–ferroelectric–insulator–semiconductor devices

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Abstract

In this paper, we report a detailed study of the negative capacitance field effect transistor (NCFET). We present the condition for the stabilization of the negative capacitance to achieve the voltage amplification across the active layer. The theory is based on Landau's theory of ferroelectrics combined with the surface potential model in all regimes of operation. We demonstrate the validity of the presented theory on experimental NCFETs using a gate stack made of P(VDF-TrFE) and SiO_2. The proposed analytical modeling shows good agreement with experimental data.

Keywords: ferroelectric, polarization, minor loops, negative capacitance, surface potential, NC-FET, P(VDF-TrFE)

(Some figures may appear in colour only in the online journal)

1. Introduction

Salahuddin suggested that the ferroelectric transistor could provide a new mechanism to amplify the surface potential above the gate voltage due to the negative capacitance effect [1, 2]. Several experiments showed proof of negative capacitance in ferroelectric materials [3, 4]. Recent studies propose a non-hysteretic behavior of negative capacitance FET with a subthreshold slope less than 30 mV/dec, but the device is only in the simulation state [5]. Recently ferroelectric transistors were reported with under-thermal characteristics that presented [6] both hysteretic and non-hysteretic negative capacitance behaviors [7–9]. The difference between the reported devices and the transistor proposed by Salahuddin [1] is the insertion of a linear dielectric as a buffer layer due to the diffusion of the ferroelectric into the silicon [10]. We should clarify that the surface potential enhancement due to the ferroelectric's negative capacitance effect is entirely different from the amplifying effect on the tunneling current through the gate oxide as a result of the presence of a ferroelectric layer in tunneling read-only memory devices [11–13]. The ferroelectric stability condition to obtain the negative capacitance effect for this kind of device has not previously been reported. This work describes the physical explanation of the stability condition, setting its boundaries based on the electrical and physical properties of the materials. The condition is obtained based on the basic Maxwell [14] charge equations and Tsividis model of the MOS transistor [15]. The stated stability condition is then validated with measurements on fabricated devices that illustrated voltage amplification and hysteresis at the same time. Based on the presented theory, a complete set of equations is reported to design a negative capacitance transistor.

2. Theoretical condition to obtain negative capacitance

In this section, we demonstrate the analytical modeling of the metal–ferroelectric–oxide–silicon field effect transistor and derive the theoretical condition for the occurrence of negative capacitance. The device is schematically depicted in figure 1, where the gate dielectric of a conventional MOSFET is replaced by a stack of a linear and ferroelectric dielectric. Each layer can be defined as a single capacitor so that the entire gate stack can be considered as an in-series

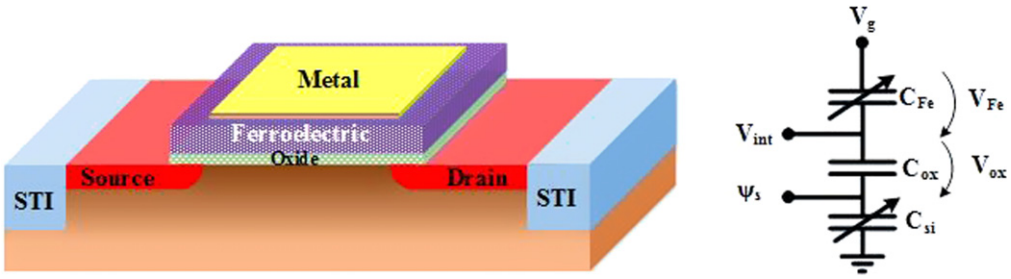

Figure 1. (left) Generic ferroelectric transistor; (right) equivalent scheme of the device capacitance. The ferroelectric capacitance and the silicon capacitance are bias- dependent.

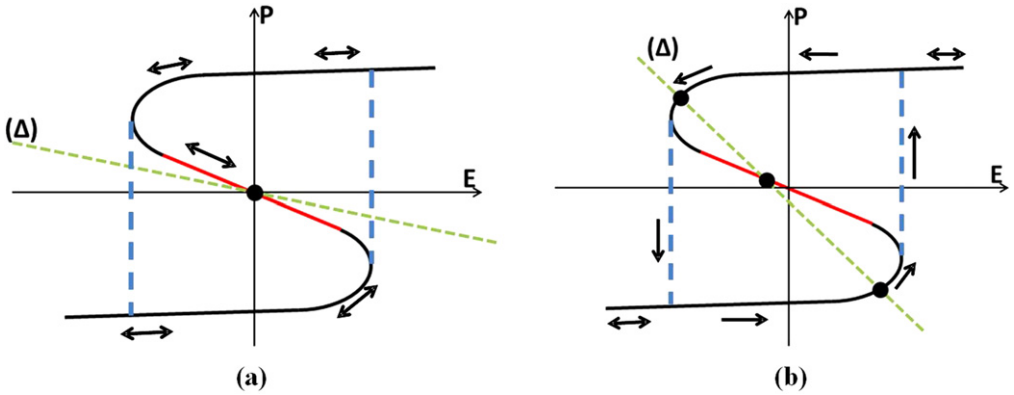

Figure 2. Charge line intersecting the polarization. (a) The condition for the negative capacitance is fulfilled. In (b), the condition for negative capacitance does not appear, and we encounter hysteresis [15].

combination of capacitors (figure 1). The ferroelectric layer has been considered ideal, and the formation of the dead layer at the interface with the electrode is neglected in our calculations [16]. Regarding the equivalent circuit that is depicted in figure 2,

$$V_g = V_{Fe} + V_{ox} + \psi_s, \tag{1}$$

where V_g is the gate voltage, V_{Fe} and V_{ox} are the voltage drop over ferroelectric and linear dielectrics and ψ_s is the silicon surface potential. We will consider the case that there are no trapped charges on the $SiO_2 - PVDF$ interface [13]. Thus, the electric displacement is conserved [17], which can be expressed as:

$$\begin{aligned} D_{Fe} &= D_{ox}, \\ \epsilon_0 E_{Fe} + P &= \epsilon_0 k_{ox} E_{ox}, \\ P &= \epsilon_0 k_{ox} \frac{V_{ox}}{t_{ox}} - \epsilon_0 \frac{V_{Fe}}{t_{Fe}}, \end{aligned} \tag{2}$$

where D_{Fe} and D_{ox} are the displacements of the ferroelectric and oxide respectively, E_{Fe} and E_{ox} are the electric field inside the ferroelectric and oxide thin films, P is the ferroelectric polarization, t_{Fe} and t_{ox} are the ferroelectric and oxide thicknesses, k_{ox} is the relative permittivity of the oxide, and ϵ_0 is the vacuum permittivity. By substituting the voltage drop across the linear oxide from equation (1), the ferroelectric polarization can be calculated as follows:

$$P = \epsilon_0 k_{ox} \frac{V_g}{t_{ox}} - E_{Fe} t_{Fe} \epsilon_0 \left(\frac{1}{t_{Fe}} + \frac{k_{ox}}{t_{ox}} \right) - \frac{\epsilon_0 k_{ox}}{t_{ox}} \psi_s, \tag{3}$$

Equation (3) represents the charge stability of the system in a certain gate voltage. In order for the negative capacitance to occur, the slope of the charge line that is defined by equation (3) must be *smaller* than the negative slope of the ferroelectric polarization as presented in figure 2.

In the case of figure 2(a), the charge line intersects the polarization at only one point, and the entire system is stable, contrary to the case of figure 2(b) where the charge line intersects the polarization curve at three points, resulting in instability and hysteresis. Hence, for the stable operation of a negative capacitance device, the slope of the Δ must be *smaller* than the negative slope of the ferroelectric polarization.

In order to calculate the slope of the charge line, we must express the surface potential with respect to the ferroelectric voltage. Due to the fact that the surface potential cannot be expressed mainly by a unique compact analytical expression in all regions of operation, we study the MOS transistor in different regions. We start with strong inversion; the surface potential in strong inversion has an almost constant value of $\psi_s \cong 2\phi_F + 6\phi_t$, where ϕ_F is the Fermi potential and ϕ_t is the thermal voltage. By considering the equation (3), the charge

line can be stated as

$$\Delta = \epsilon_0 k_{ox}\frac{V_g}{t_{ox}} - E_{Fe}t_{Fe}\epsilon_0\left(\frac{1}{t_{Fe}} + \frac{k_{ox}}{t_{ox}}\right) - \frac{\epsilon_0 k_{ox}}{t_{ox}}(2\phi_F + 6\phi_t). \quad (4)$$

The slope of the charge line at a gate voltage that sets the transistor in the strong inversion will be

$$\frac{\partial\Delta}{\partial E_{Fe}} = -t_{Fe}\epsilon_0\left(\frac{1}{t_{Fe}} + \frac{k_{ox}}{t_{ox}}\right). \quad (5)$$

In the case of weak inversion, the surface potential can be approximated by a linear function [17]. The slope of the surface potential with reference to the gate voltage can be calculated as

$$n = \left(\frac{d\psi_s}{dV_g}\right)^{-1} = 1 + \frac{\gamma}{2\sqrt{\psi_s}}, \quad (6)$$

where γ is the body factor.

The surface potential varies from ϕ_F to $2\phi_F$ in the weak inversion region. Therefore, the n does not vary greatly, and we can approximate it by an average surface potential value. Thus, we will have an average slope at $\psi_s = (3/2)\phi_F$,

$$n = 1 + \frac{\gamma}{2\sqrt{(3/2)\phi_F}}. \quad (7)$$

With this approximation, the surface potential has a linear dependence on the gate voltage. Returning to equation (3),

$$P = \epsilon_0 k_{ox}\frac{V_g}{t_{ox}} - \epsilon_0 V_{Fe}\left(\frac{1}{t_{Fe}} + \frac{k_{ox}}{t_{ox}}\right) - \frac{\epsilon_0 k_{ox}}{t_{ox}}\frac{V_{int}}{n}, \quad (8)$$

$$P = \epsilon_0 k_{ox}\frac{V_g}{t_{ox}} + \frac{\epsilon_0 k_{ox}}{n t_{ox}}V_g - E_{Fe}t_{Fe}\epsilon_0\left(\frac{1}{t_{Fe}} + \frac{k_{ox}}{t_{ox}}\left(1 - \frac{1}{n}\right)\right). \quad (9)$$

Equation (9) describes the charge line for an NC-MOS transistor that is biased in weak inversion. The slope of the charge line can be expressed as

$$\frac{\partial\Delta}{\partial E_{Fe}} = -\epsilon_0 t_{Fe}\left(\frac{1}{t_{Fe}} + \frac{k_{ox}}{t_{ox}}\left(1 - \frac{1}{n}\right)\right). \quad (10)$$

This last result shows that the slope of the charge line is not constant regarding the gate voltage which means the slope of the charge line is influenced by the slope of the surface potential. The slope of the charge line decreases as the $1/n$ parameter increases, implying that having a steep slope transistor is constituted as an advantage in achieving negative capacitance. The $1/n$ parameter depends on the fabrication criteria.

In depletion, the surface potential cannot be approximated by a linear function and the charge line becomes a second-degree equation. Again, the important factor is the slope of the parabola. To have continuity, the slope of the charge line that depends on the gate voltage must be continuous and monotonic. Thus, we can state that the charge line slope is high in the depletion region, lowers gradually in weak inversion, and increases again in the inversion region.

As previously mentioned, to have a successful negative capacitance MOSFET, the slope of the charge line must be *smaller* than the negative slope of the polarization (figure 2). Next we will calculate the negative part of the ferroelectric S-shape polarization. The S-shape hysteresis is defined according to Landau's theory [18]:

$$E = \alpha_0(T - T_c)P + B(T)P^3, \quad (11)$$

where α_0 and $B(T)$ are material parameters, T_c is the ferroelectric Curie temperature and T is the temperature. In order to calculate the negative slope of the polarization, we will consider the first order approximation in this region. The polarization has a value near zero in the negative capacitance zone which allows us to neglect the P^3 term compared with the first order term,

$$E = \alpha_0(T - T_c)P. \quad (12)$$

Hence, the derivation of the ferroelectric polarization in the negative region is:

$$\frac{\partial P}{\partial E} = \frac{1}{\alpha_0(T - T_c)}. \quad (13)$$

We can state theoretically that the negative capacitance appears only in weak inversion where the slope of the charge line is minimum. Therefore, we report the mathematical condition to obtain the negative capacitance effect in metal–ferroelectric–oxide–semiconductor FETs,

$$\frac{\partial\Delta}{\partial E_{Fe}} \leqslant \frac{\partial P}{\partial E}, \quad (14)$$

$$-\epsilon_0\left(\frac{1}{t_{Fe}} + \frac{k_{ox}}{t_{ox}}\left(1 - \frac{1}{n}\right)\right) \leqslant \frac{1}{\alpha_0(T - T_c)}, \quad (15)$$

where $\gamma = \sqrt{2q\epsilon_s N_A}/(\epsilon_{ox}/t_{ox})$, $\phi_F = \phi_t \ln(N_A/n_i)$, and n is presented in equation (7). With this algorithm, we have given a complete set of equation to design a negative capacitance ferroelectric MOS transistor. The following parameters (t_{ox}, t_{Fe}, N_A, α_0, T_c, and ϵ_{ox}) should be considered for a successful design.

The slope of the charge line in an NC-FET varies with the gate voltage. In the case that the slope of the charge line and the negative slope of the ferroelectric polarization are close, the stability of the system is not consistent for all gate voltages. Once the slope of the charge line attains the ferroelectric polarization slope, the system reaches equilibrium and the negative capacitance effect appears. Further increasing the gate voltage leads the system to instability as the slope of the charge line exceeds the slope of the ferroelectric polarization. The variation of this slope and the possibility of obtaining hysteresis and the negative capacitance effect is qualitatively demonstrated in figure 3. It can be seen that devices with a larger surface potential derivative (subthreshold slope closer

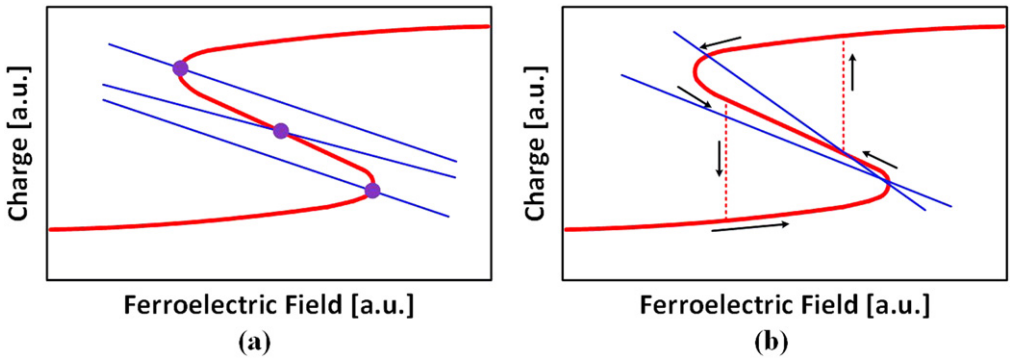

Figure 3. The charge line that changes the slope due to the operation regime of the ferroelectric transistor. (a) The slope of the charge line changes with the bias but the stability condition remains on the entire range of the applied voltage. (b) The condition for stability is fulfilled only on a small interval of applied voltage so that negative capacitance can be obtained together with hysteresis.

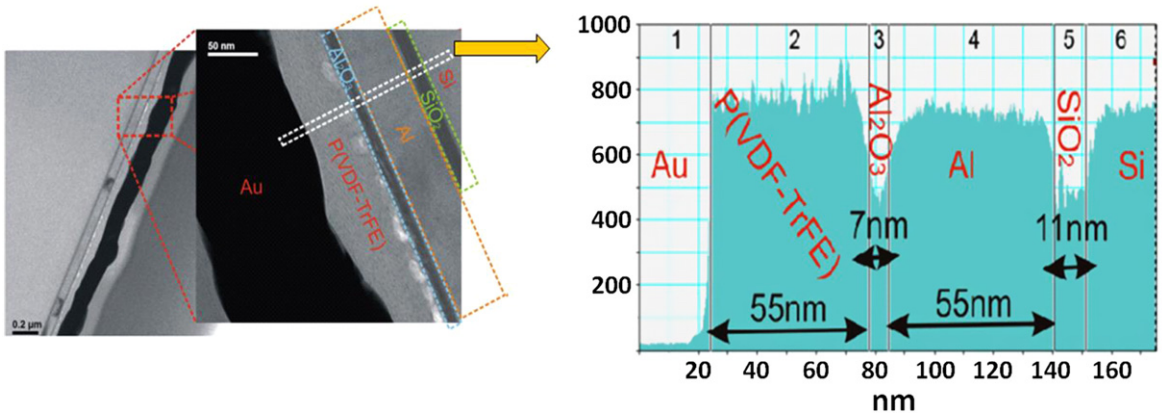

Figure 4. TEM analysis of the device gate stack. The thickness of each layer is depicted in the right image.

to 60 mV/dec) have a larger zone where the negative capacitance effect can be observed.

The obtained gain of the Fe-FET can be also calculated based on the negative slope of the polarization (dP/dE_{Fe}) and the subthreshold slope of the series MOS transistor under the ferroelectric layer (considering the Fe-FET as a ferroelectric capacitor in series with a conventional MOSFET) [19]. The amplification effect of the ferroelectric depends on the α_0 parameter, high amplification corresponds to low α_0. In addition to amplification, the negative capacitance stability also depends on this parameter, higher α_0 corresponds to the wider zone of negative capacitance. The condition of the stability highly depends on the ferroelectric material properties and the electrical characteristic of the corresponding MOS transistor. This could be the main reason that many trials for measuring negative capacitance had failed [20].

3. Experimental verification

We have verified the stated condition in our fabricated devices [7].The gate stack is composed of P(VDF − TrFE)70:30 and a thin layer of SiO_2. Between these two insulators, a layer of Al was introduced to provide access to the internal contact. A thin layer of Al_2O_3 was formed during Al deposition. The TEM image of the gate cross section is demonstrated in figure 4.

The polarization curve and its derivative regarding the ferroelectric field are presented in figure 5. The Al_2O_3 layer was taken into consideration for the polarization extraction. The polarization–voltage hysteresis in figure 5 is slightly different compared to other experimental results reported in the literature [21]. Usually, the P–E diagram of a ferroelectric capacitor is symmetric [21] while the polarization hysteresis loop of a ferroelectric field effect transistor has an S-like behavior only in one branch of the hysteresis [22] where the negative capacitance condition is fulfilled, as shown in figure 5.

Next, the slope of the PVDF S-shape polarization will be calculated. The $\alpha_0 = 9.02 \times 10^9$ J m/cm V K [23] and the $T_c = 355$°K [24]. Calculating the negative slope of the polarization for *PVDF*,

$$\frac{\partial P}{\partial E} = \frac{1}{\alpha_0 (T - T_c)} = 2.0157 \times 10^{-14} \frac{\text{C}}{\text{cm V}}. \qquad (16)$$

Figure 6 demonstrates the measured charge line slope (continuous line) and the calculated slope of the S-shape polarization (dotted line). The system is stable where the slope of the charge line is *smaller* than the slope of the polarization. The dotted line represents the threshold imposed

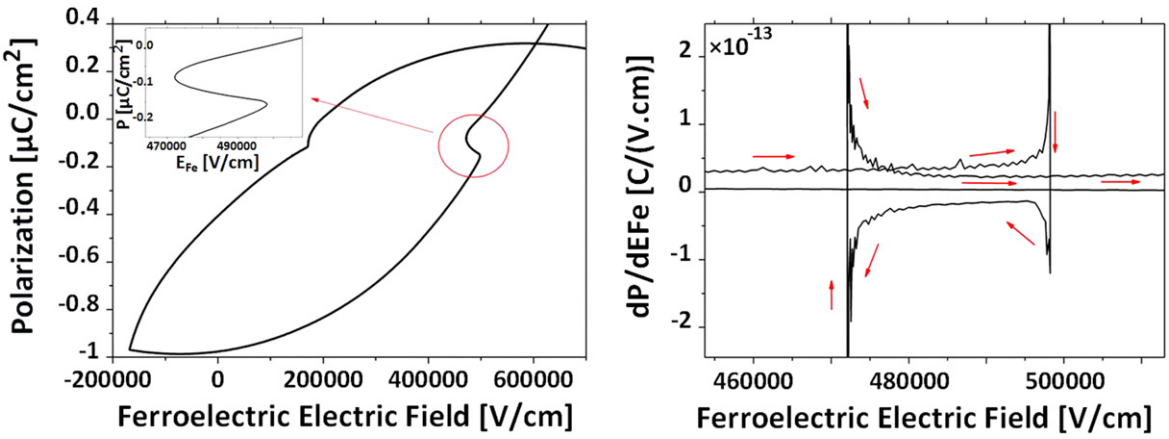

Figure 5. The ferroelectric polarization extracted from measurements (left) and the polarization derivative with respect to the ferroelectric field (right).

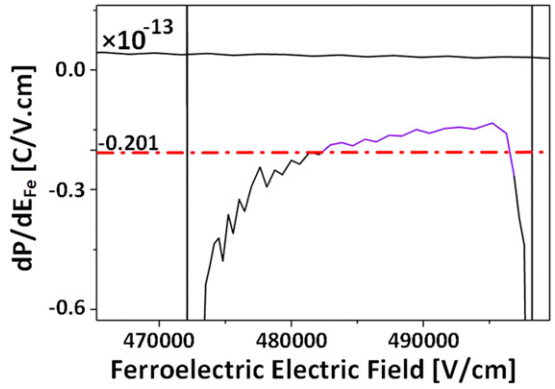

Figure 6. Negative capacitance area where the system reaches stability. This graph illustrates the condition from equation (14) applied to the measured device. The continuous line ($\partial P/\partial E$) is the measured value, and the dotted line is the theoretical threshold limit calculated from the literature data, equation (16), in order to achieve negative capacitance. We can observe that above this threshold, the measurement starts to go into the instability regime and the ferroelectric pops off the negative capacitance regime.

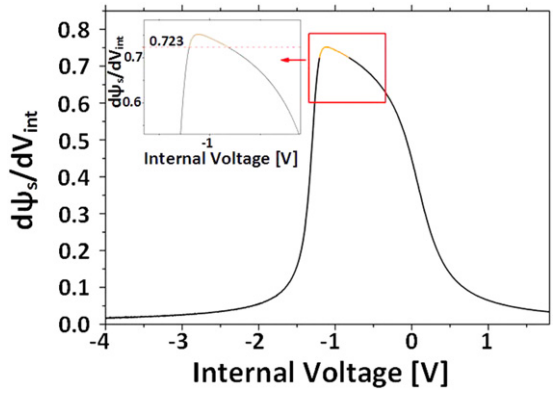

Figure 7. The surface potential derivative with respect to the internal potential. The highlighted zone corresponds to the points where we have obtained negative capacitance. We can clearly observe that the points that correspond to the negative slope of the polarization belong to the area where the derivative of the surface potential has a value higher than 0.723. Better fabricated MOS transistors with a higher derivative of the surface potential with respect to the internal voltage will result in a wider area of negative capacitance effect.

by the ferroelectric material for the system to achieve the stability as stated in equation (14).

These results prove the stated theory in this paper accurately. Even if the threshold of the ferroelectric does not cover the whole area of negative capacitance, one can observe that it covers the zone where the system is stable. After this limit, noise starts prevailing, and the system exits the stability regime.

We have stated that the slope of the charge line is changing according to the derivative of the surface potential regarding the internal potential. The surface potential was extracted based on the Tsividis model, and its derivative is plotted in figure 7.

Figure 7 shows that the slope of the charge line lowers significantly, if the derivative of the surface potential exceeds a certain value. In our case, this value is 0.723. A better MOS with a subthreshold slope closer to the 60 mV/dec thermal limit has a derivation of the surface potential closer to 1. The surface potential derivative closer to 1 means that the negative capacitance zone is extended and providing amplification over multiple decades of the current.

Another question that arises is why we have not obtained the negative slope of the polarization also on the other side of the hysteresis. The ferroelectric material must be polarized at a certain value to have a stable system. Here, we cannot sufficiently polarize the ferroelectric due to the thin oxide that results from exploring the minor loops of the ferroelectric. An inconvenience of this fact is that the ferroelectric polarization curve can shift between two successive measurements because of the remaining dipoles that are already polarized from the previous measurement. One can observe the asymmetry of the polarization curve towards the negative side.

4. Conclusions

In this paper, a negative capacitance condition for a metal–ferroelectric–oxide–semiconductor FET was presented. The

theory was based on a physical model using basic Maxwell's equations and the Tsividis model for an MOS transistor. The condition was verified on measured Fe-FETs, which presented negative capacitance together with hysteresis. The devices were fabricated with an organic ferroelectric where we could observe voltage amplification, and we found an excellent agreement with the presented theory. A complete set of equations was presented to design a negative capacitance transistor.

References

[1] Salahuddin S and Datta S 2008 Use of negative capacitance to provide voltage amplification for low power nanoscale devices *Nano Lett.* **8** 405–10

[2] Catalan G, Jiménez D and Gruverman A 2015 Ferroelectrics: negative capacitance detected *Nat. Mater.* **14** 137–9

[3] Khan A I, Bhowmik D, Yu P, Kim S J, Pan X, Ramesh R and Salahuddin S 2011 Experimental evidence of ferroelectric negative capacitance in nanoscale heterostructures *Appl. Phys. Lett.* **99** 113501

[4] Tadros-Morgane R, Vizdrik G, Martin B and Kliem H 2011 Observation of negative capacitances in Al/P(VDF-TrFE)/SiO_2/nSi structures *J. Appl. Phys.* **109** 014501

[5] Yeung C W, Khan A I, Jen-yuan C, Salahuddin S and Hu C 2012 Non-hysteretic negative capacitance FET with sub-30 mV/dec swing over 10 6 X current range and ION of 0.3mA/um without strain enhancement at 0.3V VDD *SISPAD 2012* pp 257–9

[6] Jaesung J, Woo Y C, Jung-Dong P, Jae W S, Hyun-Yong Y and Changhwan S 2015 Negative Capacitance in Organic/Ferroelectric Capacitor to Implement Steep Switching MOS Devices *Nano Lett.* **15** 4553–6

[7] Alexandru R, Giovanni a S, David J and Adrian M I 2010 Metal-ferroelectric-metal-oxide-semiconductor field effect transistor with sub-60mV/decade subthreshold swing and internal voltage amplification *IEEE International Electron Devices Meeting* pp 395–398

[8] Alexandru R, Giovanni a S and Adrian M I 2011 Test structure and method for the experimental investigation of internal voltage amplification and surface potential of ferroelectric MOSFETs *Solid-State Electron.* **65–66** 151–6

[9] Giovanni a S, Didier B and Adrian M I 2008 Demonstration of subthrehold swing smaller than 60mV / decade in Fe-FET with P (VDF-TrFE)/SiO_2 gate stack *Nano* **8** 479–81

[10] Dong-Won K, Jeong-Hwan K, Joo-Nam K, Hyung-Jin P, Ho-Seung J and Byung-Eun P 2008 Characterization of metal-ferroelectric-semiconductor structure using ferroelectric polymer polyvinylidene fluoride-trifluoroethylene (PVDF-TrFE) (51/49) *Integr. Ferroelectr.* **98** 121–7 (July 2015)

[11] Baginsky I L and Kostsov E G 1993 Information writing mechanisms in thin-film mfis-structures *Ferroelectrics* **143** 239–50

[12] Baginskii I L, Erkov V G, Kostov E G and Likhachev A A 1991 Injection amplification effect in the metal-ferroelectric-insulator-semiconductor thin film structure *Thin Solid Films* **202** 191–203

[13] Kentaro I and Hidetoshi T 1977 Memory modes of ferroelectric field effect transistors *Solid-State Electron.* **20** 529–37

[14] Buck J and Hayt W 2011 *Engineering Electromagnetics* vol 7 (New York: McGraw-Hill)

[15] Cano a and Jimenez D 2010 Multidomain ferroelectricity as a limiting factor for voltage amplification in ferroelectric field-effect transistors *Appl. Phys. Lett.* **97** 11–4

[16] Bratkovsky A M and Levanyuk A P 2001 Very large dielectric response of thin ferroelectric films with the dead layers *Phys. Rev.* B **63** 132103

[17] Tisividis Y 1999 *Operation and Modeling of the MOS Transistor*

[18] Ploss B 2000 Dielectric nonlinearity of PVDF-TrFE copolymer *Polymer* **41** 6087–93

[19] Alexandru R and Adrian M I 2012 Analytical model for predicting subthreshold slope improvement versus negative swing of S-shape polarization in a ferroelectric FET *Proc. 19th Int. Conf. on Mixed Design of Integrated Circuits* pp 55–9

[20] Krowne C M, Kirchoefer S W, Chang W, Pond J M and Alldredge L M B 2011 Examination of the possibility of negative capacitance using ferroelectric materials in solid state electronic devices *Nano Lett.* **11** 988–92

[21] Khan A I, Chatterjee K, Wang B, Drapcho S, You L, Serrao C, Bakaul S R, Ramesh R and Salahuddin S 2015 Negative capacitance in a ferroelectric capacitor *Nat. Mater.* **14** 182–6

[22] Salvatore G A, Rusu A and Ionescu A M 2012 Experimental confirmation of temperature dependent negative capacitance in ferroelectric field effect transistor *Appl. Phys. Lett.* **100** 163504

[23] Ahluwalia R, Sullivan M B, Srolovitz D J, Zheng J W and Huan A C H 2008 Multiscale kinetic model for polarization switching in ferroelectric polymer thin films *Phys. Rev.* **78** 1–9

[24] Giovanni a S, Livio L, Didier B, Igor S, Nava S and Adrian M I 2010 Ferroelectric transistors with improved characteristics at high temperature *Appl. Phys. Lett.* **97** 2008–11