GigaRad Total Ionizing Dose and Post-Irradiation Effects on 28 nm Bulk MOSFETs

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***Abstract*—The DC performance of both n- and pMOSFETs fabricated in a commercial-grade 28 nm bulk CMOS process has been studied up to 1 Grad of total ionizing dose and at post-irradiation annealing. The aim is to assess the potential use of such an advanced CMOS technology in the forthcoming upgrade of the Large Hadron Collider at CERN. The total ionizing dose effects show limited influence in the on-current of all the tested nMOSFETs. Nonetheless, the leakage current increases significantly, affecting the normal device operation of the nMOSFETs. These phenomena can be linked to the charge trapping in the oxides and at the Si/oxide interfaces, related to both the gate oxide and the shallow trench isolation oxide. In addition, it has been observed that the radiation-induced effects are partly recovered by the long-term post-irradiation annealing. To quantify the total ionizing dose effects on DC characteristics, the threshold voltage, subthreshold swing, and drain induced barrier lowering have also been extracted for nMOSFETs.**

***Index Terms*—Total ionizing dose, TID, 28 nm bulk CMOS, gate oxide, shallow trench isolation, annealing, HL-LHC**

I. Introduction

To extend the discovery potential at the forefront of research in high-energy physics, the Large Hadron Collider (LHC) at CERN will soon be upgraded for a tenfold increase in the integrated luminosity. This gives rise to an unprecedentedly high radiation level up to 10 MGy (1 Grad) of total ionizing dose (TID) and $10^{16}\mathrm{neutrons/cm^2}$ of hadron fluence over ten years of operation. Nowadays, the large majority of the radiation-tolerant front-end (FE) Application-specific integrated circuits (ASICs) in the detector systems of the LHC are built in a commercial 250 nm CMOS technology, by adopting circuital and layout radiation-hardness techniques. To go through a 10-year operation reliably under a much higher event rate and radiation level, ATLAS and CMS experiments need to be equipped with much more radiation-hardened tracking systems with a higher granularity and bandwidth [1], [2].

It has been demonstrated that without any special processing, the radiation damage in MOSFETs gets reduced by thinning the gate oxide [3]. However, the high-k metal gate (HKMG) configuration has been introduced as the gate stack in advanced CMOS technologies, whose radiation-induced effects remain to be explored [4]. Furthermore, the role of the shallow trench isolation (STI) oxide in radiation-induced effects needs further investigation in ultra-scaled MOSFETs [5]. In consideration of the foreseen radiation level for the innermost circuits of the detector systems, this work conducted the first characterization of up to 1 Grad of TID and post-irradiation annealing effects on both n- and pMOSFETs, which are fabricated in a commercial 28 nm bulk CMOS process. DC measurements were performed to assess the impact of such a high level of TID on those crucial device parameters. This includes the threshold voltage, subthreshold swing, on-current, off-state leakage current, and drain induced barrier lowering (DIBL).

II. Experimental Details

Both n- and pMOSFETs are fabricated in a high-performance 28 nm bulk CMOS process. The test chip includes ten transistors for each type with several widths ($W_{max} = 3\,\mu\mathrm{m}, W_{min} = 100\,\mathrm{nm}$) and lengths ($L_{max} = 1\,\mu\mathrm{m}, L_{min} = 30\,\mathrm{nm}$). The same type of MOSFETs share the contacts for source and substrate but have individual contacts for gate and drain. The irradiation and DC measurements have been performed sequentially at room temperature on both n- and pMOSFETs. The irradiation was conducted with CERN's in-house X-ray generator at a dose rate of 8.82 Mrad/h(SiO_2), reaching 1 Grad of TID. In order to maximize the radiation damage, the chips were powered on ($|V_{GS}| = |V_{DS}| = V_{DD}$) during irradiation. In addition, DC measurements were carried out after irradiation so as to explore the post-irradiation annealing effects. More experimental details can be referred to [6].

III. Results and Discussions

A. TID effects on transfer characteristics

The main degradation mechanism of TID in MOSFETs is linked to the radiation-induced charge buildup in the oxides (Q_{ot}) and at the Si/oxide interfaces (Q_{it}), which can be related to both the STI oxide and the gate oxide [7], [8]. From a circuit design perspective, TID effects manifest as a threshold voltage (V_{TH}) shift, a subthreshold swing ($SubS$) degradation, a on-current (I_{on}) variation, and an increased off-state leakage current (I_{off}), as seen from the DC characteristics of two representative transistors for both n- and pMOSFETs in Fig. 1 and Fig. 2.

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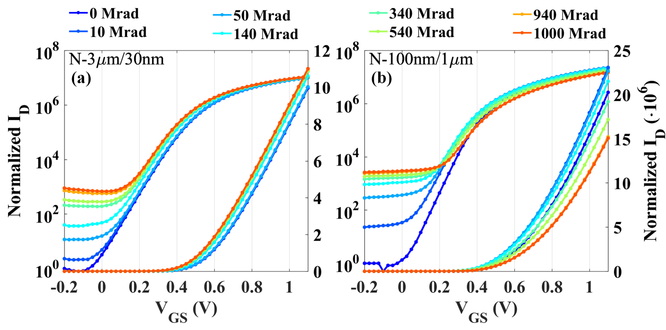

Fig. 1. Normalized I_D versus V_{GS} characteristics of the nMOSFETs with the largest and smallest W/L ratio (3 µm/30 nm and 100 nm/1 µm) with respect to total ionizing dose at $V_{DS} = 1.1$ V.

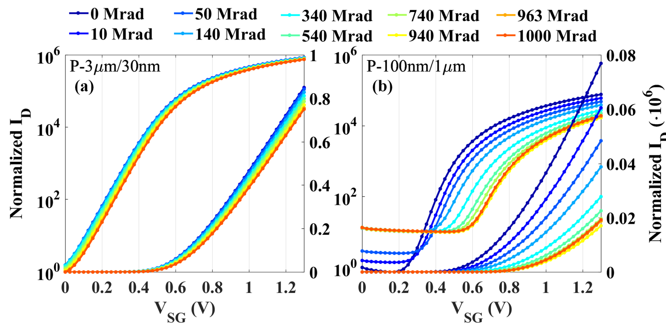

Fig. 2. Normalized I_D versus V_{SG} characteristics of the pMOSFETs with the largest and smallest W/L ratio (3 µm/30 nm and 100 nm/1 µm) with respect to total ionizing dose at $V_{SD} = 1.1$ V.

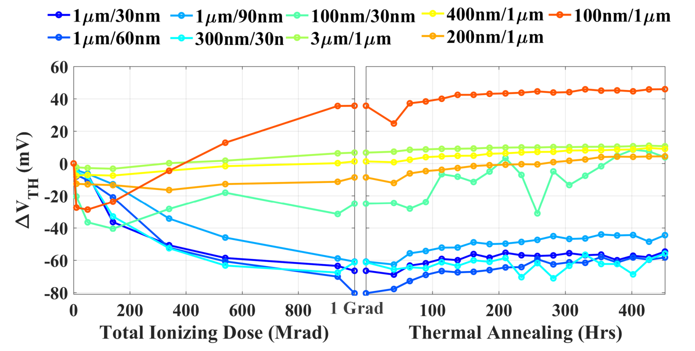

Fig. 3. Threshold voltage shift (ΔV_{TH}) of the tested nMOSFETs at $V_{DS} = 1.1$ V as a function of total ionizing dose and post-irradiation annealing time.

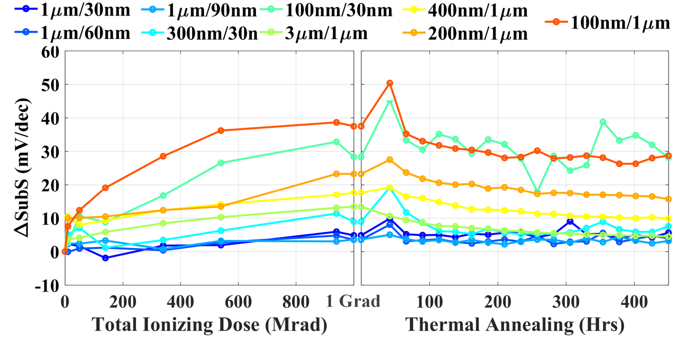

Fig. 4. Subthreshold swing degradation ($\Delta SubS$) of the tested nMOSFETs at $V_{DS} = 1.1$ V as a function of total ionizing dose and post-irradiation annealing time.

1) Threshold voltage: The oxide trapped charges are positive, tending to decrease the threshold voltage of both n- and pMSOFETs [9]. For pMOSFETs [10], the interface charged traps are also positive, adding another negative shift in threshold voltage. This addition leads to a significantly decreased threshold voltage, as seen in Fig. 2. Starting from here, the remaining analysis will focus on nMOSFETs. The interface charged traps are negative for nMOSFETs, which tends to increase the threshold voltage. However, due to the late-formation of radiation-induced interface traps [11], the charge trapping in oxide traps dominates in the beginning. Therefore, the threshold voltage decreases first for all of the irradiated nMOSFETs, as seen in Fig. 3. Then two kinds of charged traps start to show competing behaviors. The net effect is strongly dependent on the device geometry. For the transistors with a larger W/L (3 µm/30 nm, etc.), the oxide trapped charges are dominant throughout the whole irradiation process. This leads to a continuously decreased threshold voltage, as shown in Fig. 1(a) and Fig. 3. However, for the transistors with a smaller W/L (100 nm/1 µm, etc.), the interface charged traps start from a certain point to be dominant and to compensate the negative shift in threshold voltage due to oxide trapped charges. This results in an overall positive threshold voltage shift for the transistor with 100 nm/1 µm, as clearly illustrated in Fig. 1(b) and Fig. 3. It should be mentioned that the maximum threshold voltage shift (~80 mV) is within the process-related variation. Moreover, it is much less than the reported value (~235 mV) for the same size of nMOSFET (1 µm/60 nm) fabricated in a 65 nm CMOS bulk technology [5].

2) Subthreshold swing: The subthreshold swing degrades due to the charge trapping at the radiation-induced interface traps. Most of the irradiated nMOSFETs present a negligible subthreshold swing degradation, as seen in Fig. 4. Two narrowest transistors (100 nm/1 µm and 100 nm/30 nm) have the most significant increase in subthreshold swing. For the transistor with 100 nm/1 µm, this can also be seen from the subthreshold region of the I_D-V_{GS} curves, as shown in Fig. 1(b). Remember that this discussion does not exclude the effect of mobility reduction, which lowers down the on-current and affects the extraction of subthreshold swing in the subthreshold region. It should be also mentioned that the subthreshold swing degradation is mush less than the reported value for the same size of nMOSFET (1 µm/60 nm) in the 65 nm CMOS bulk process [5].

3) On-current and off-state leakage current: A maximum of 25% of on-current variation is observed in Fig. 5(a), which is acceptable for most applications. This demonstrates the limited radiation-induced effects of both the STI oxide and the gate oxide on the strong inversion region of the irradiated nMOSFETs. These transistors should be able to work well in the switched-on operation region. It is also noted that the trend of the on-current variation in Fig. 5(a) is corresponding with that of the threshold voltage shift shown in Fig. 3. This indicates that in most cases, the threshold voltage shift is the major contributor to the on-current variation.

The significantly increased off-state leakage current is the

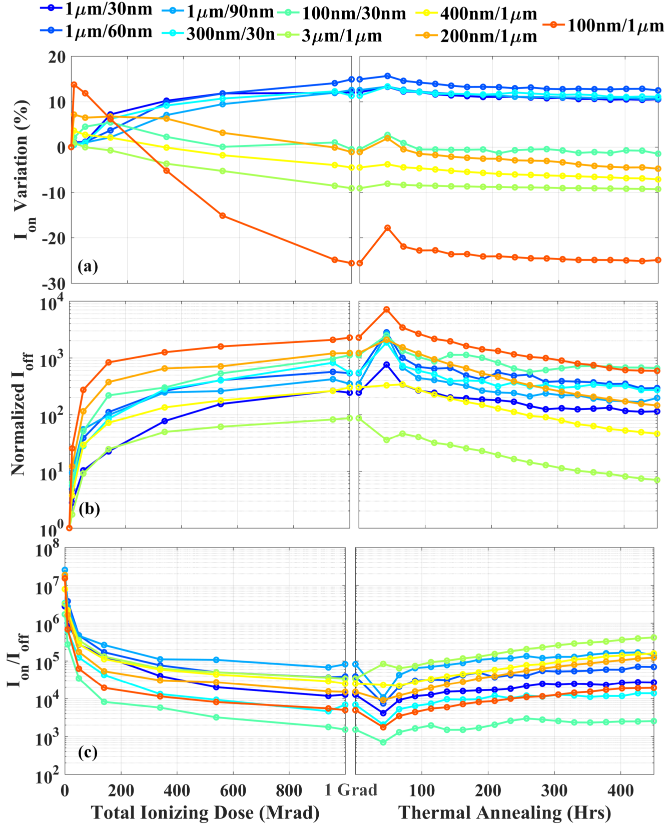

Fig. 5. On-current (I_{on}) variation, normalized off-state leakage current (I_{off}) and on/off-current ratio (I_{on}/I_{off}) of the tested nMOSFETs at $V_{DS} = 1.1$ V as a function of the total ionizing dose and post-irradiation annealing time. I_{on} is extracted when $V_{GS} = 1.1$ V and I_{off} is obtained when $V_{GS} = 0V$.

most serious effect on all of the tested nMOSFETs, as demonstrated in Fig. 5(b). It can be attributed to the positive charge trapping in the STI oxide, which is able to invert the adjacent p-type silicon layer along the STI sides of channel at a higher TID. This forms two parasitic conductive paths allowing two currents to flow from drain to source, even when the transistor is switched off [12]. However, for most of the irradiated nMOSFETs, this charge trapping is not strong enough to influence the electrostatic potential in the middle of the channel, resulting in a limited effect on the threshold voltage and the on-current. Therefore, there are still three orders of magnitude of the on/off-current ratio, remaining as a sufficient margin for most applications, as seen in Fig. 5(c).

4) Radiation-induced gate leakage current: The obvious increase in the gate leakage current is shown in Fig. 6. The mechanism for this increase has been mainly attributed to the trap-assisted inelastic tunneling process [13]. With the positive bias at the gate terminal, the electrons can tunnel to the oxide traps and then to the gate electrode. The related traps are most likely to be the trivalent silicon atoms with an unpaired electron, back bonded to three oxygen atoms. This kind of traps can be generated through the breaking of the strained Si-Si bonds by the radiation-induced hole trapping in oxygen vacancies. Therefore, the increase of the gate leakage current gives information about the trapped holes in the gate oxide.

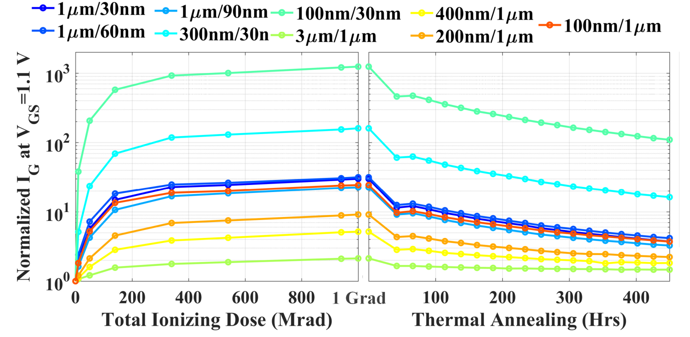

Fig. 6. The increase in gate leakage current (I_G) of the tested nMOSFETs at $V_{GS} = V_{DS} = 1.1$ V as a function of total ionizing dose and post-irradiation annealing time.

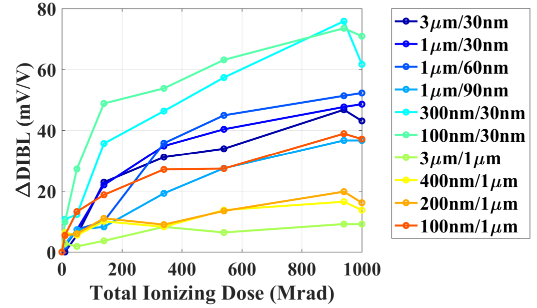

Fig. 7. Radiation-enhanced drain induced barrier lowering (DIBL) of the tested nMOSFETs as a function of total ionizing dose. The DIBL effect is extracted with transfer characteristics at $V_{DS} = 10$ mV and $V_{DS} = 1.1$ V.

B. Radiation-enhanced drain induced barrier lowering

The DIBL effect represents one of the most fundamental short-channel effects in nano-scale MOSFETs. It has been demonstrated that the positive charge trapping in the STI oxide enhances the DIBL effect by decreasing the drain to gate coupling, enhancing the electric field near the STI corners, and increasing the surface potential of the lowly-doped substrate along the STI oxide [14]. The radiation-enhanced DIBL effect is illustrated in Fig. 7 as a function of the total ionizing dose. The DIBL effect is calculated as $DIBL = -(V_{TH}^{V_{DS}=1.1V} - V_{TH}^{V_{DS}=0.01V})/(1.1V - 0.01V)$. It is seen that the radiation enhancement of the DIBL effect is negligible for nMOSFETs with a longer channel, while the enhancement increases a lot for the smaller nMOSFETs. The minimum size of nMOSFET shows the strongest radiation-enhanced DIBL effect, which approaches almost 80 mV/V after 1 Grad of TID.

C. Post-irradiation annealing effects on transfer characteristics

To observe the long-term post-irradiation annealing, all of the irradiated nMOSFETs are kept at the same bias condition as irradiation ($V_G = V_D = 1.1$ V and $V_S = V_B = 0$ V), and measured every 24 hours at room temperature. The extracted parameters are plotted together with the ones with respect to total ionizing dose, as shown in Figs. 3 to 6.

As seen in Fig. 4, the subthreshold swing degradation recovers slightly for all of the irradiated transistors, indicating the slight annealing of interface charged traps. Besides, there is

a insignificant increase for the threshold voltage (Fig. 3) and the on-current doesn't change a lot (Fig. 5(a)), demonstrating the competitive annealing of oxide trapped holes over the interface charged traps. The radiation-induced off-state leakage current, as shown in Fig. 5(b), decreases significantly. This presents the annealing of the trapped holes in the STI oxide. As seen in Fig. 6, there is a significant decrease for the radiation-induced gate leakage current. Since the radiation-induced gate leakage current is most likely to be linked to the traps generated during hole trapping in the gate oxide, the recovery of the gate leakage current indicates the information about the annealing of the trapped holes in the gate oxide.

For all of the irradiated nMOSFETs, the long-term post-irradiation process partly recovers the overall performance degradation. Especially, both the gate and off-state leakage current recover significantly, showing the annealing of the oxide trapped charges in both the gate oxide and STI oxide even at room temperature. For the ASICs in the detector systems, this might be represented as the problematic operation immediately after receiving a continuous irradiation and the later normal operating behavior after a certain time of post-irradiation annealing.

IV. Conclusion

In this work, 1 Grad of total ionizing dose and post-irradiation annealing effects have been investigated in both n and pMOSFETs fabricated in a commercial 28nm bulk CMOS technology. Due to the interplaying effects of oxide and interface charged traps, the radiation-induced effects are strongly dependent on the device geometry. The irradiated nMOSFETs show a maximum 25% of on-current variation, a less than 80 mV of threshold voltage shift and a up to 38 mV/dec of subthreshold swing degradation. Total ionizing dose shows insignificant effect on the strong inversion region of the irradiated nMOSFETs. In contrast, the off-state leakage current increases significantly and the radiation enhancement of the DIBL effect is seen for all of the irradiated nMOSFET. Still, three orders of magnitude of the on/off-current ratio still remain after 1 Grad of TID as a sufficient margin for most applications. A significant increase in the gate leakage current is also observed. However, the long-term post-irradiation annealing recovers part of the overall performance degradation, especially for the gate and off-state leakage current, even at room temperature.

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