Growth of GaAs nanowires on Si (111) for photovoltaic applications

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To Chiara..

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Abstract

The goal of this thesis is to master the synthesis of GaAs nanowires ensembles on Si for their application in solar cells. Semiconductor nanowires present promising characteristics for photovoltaic applications: they benefit from their longitudinal high aspect ratio geometry to enhance light absorption, minimize material consumption and efficiently collect the carriers. To fully unleash their potential, the following properties have to be controlled: number density, diameter and orientation. The latter is of utmost importance to have uniform junctions and to avoid leakages/shortcuts, whereas number density and diameter allow to tune light absorption and minimize material utilization. Our nanowires have been grown by molecular beam epitaxy (MBE), a well-known technique for the high crystalline quality and atomically sharp interfaces in thin film applications. Moreover, to develop a scalable technique and to avoid any possible contamination we used a self-assembly and self-catalyzed approach, which involves only Ga and As, without any patterning of the surface. In a first place we studied the occurrence of GaAs nanowires growth for different types of silicon oxides, such as thermal oxide, native oxide and hydrogen silsesquioxane (HSQ). We determined the critical thicknesses to achieve nanowire growth and investigated the influence of surface roughness. This comparison study lead us to choose native oxide as oxide of choice for GaAs nanowires growth on Si. With this type of oxide, reproducibility and uniformity of results outpaced the others. Successively we developed a simple technique to control native oxide thickness and characterized the chemical composition and wetting. Once the behavior of the oxide properties as a function of oxide thickness was clarified we studied their influence over nanowire growth. We found that impacted the overall possibility of nanowires growth and to control their orientation with respect to the substrate. The root cause of the change in growth morphology was identified to be in the different thermal stability of the oxides with different compositions, and the wetting properties. The understanding of the influence of the surface properties over nanowires nucleation was of paramount importance to achieve reproducible, uniform and scalable growth of vertical nanowires. Once full control over the substrate was achieved, we investigated the tailoring of diameter and density by growth conditions using the self-assembly of Ga droplets. We demonstrated an approach to tailor diameter-density distribution that minimize nanowires-array reflectivity. These results give a clear pathway on how to obtain fully controlled nanowires growth in terms of diameter, density and orientation, paving the way to the development of GaAs nanowires based solar cells on Si.

Keywords

nanowires, molecular beam epitaxy, crystal growth, III-V semiconductors.

Riassunto

L' obiettivo di questa tesi è di acquisire controllo sul processo di sintesi di nanofili di GaAs su silicio per applicazioni in campo solare. I nanofili semiconduttori presentano promettenti caratteristiche per le applicazioni in campo fotovoltaico: essi beneficiano del loro particolare rapporto dimensionale diametro/ lunghezza, per massimizzare l'assorbimento di luce, minimizzare il consumo di materiale e per estrarre efficientemente i portatori. Per realizzare il loro potenziale, le seguenti proprietà devono essere controllate: la densità di nanofili per unità di superficie, il diametro e l'orientazione. Proprio quest'ultima è di estrema importanza per avere giunzioni uniformi e per evitare perdite/corto-ciruiti. Mentre invece la densità di nanofili e il diametro permettono di controllare lo spettro di assorbimento della luce e minimizzare il consumo di materiali. I nostri nanofili sono stati cresciuti con la tecnica di epitassia a flusso molecolare (MBE), tecnica molto conosciuta per l'alta qualità cristallina e per le nette interfacce a livello atomico nelle applicazioni di film sottili. Inoltre, per sviluppare una tecnica scalabile di produzione e per evitare contaminazioni abbiamo preferito un approccio di autocatalisi e autoassemblaggio, che include esclusivamente l'uso di gallio e arsenico, senza nessuna preparazione della superficie con tecniche di litografia. In primo luogo abbiamo studiato l'influenza di diversi tipi di ossido, come ossido termico, ossido nativo e ossido derivato da idrogenosilsequioxano (HSQ) sulla crescita dei nanofili. Abbiamo quindi determinato uno spessore critico per la riuscita del processo e investigato l'influenza della rugosità della superficie. Questo studio comparativo ci ha portato a scegliere l'ossido nativo come miglior ossido per la crescita di nanofili di GaAs su Si, in termini di riproducibilità e uniformità dei risultati. Successivamente abbiamo sviluppato una tecnica per controllare lo spessore dell'ossido, per caratterizzarne la composizione chimica e le proprietà di superficie. Una volta chiarificato il comportamento delle suddette proprietà in funzione dello spessore, abbiamo studiato la loro influenza sul processo di crescita. Abbiamo scoperto che le proprietà dell'ossido impattano la possibilità di crescita di nanofili e la loro orientazione rispetto alla superficie. La causa di questo cambiamento in morfologia di crescita è la diversa stabilità termica degli ossidi a seconda della loro composizione chimica, e a seconda della loro " bagnabilità ». La comprensione dell'influenza delle proprietà di superficie sulle prime fasi di formazione dei nanofili è di fondamentale importanza per ottenere nanofili perpendicolari rispetto alla superficie, in modo riproducibile, uniforme e scalabile. Una volta acquisito il controllo sulle proprietà di superficie e sulla loro influenza, abbiamo studiato il controllo del rapporto densità-diametro attraverso le condizioni di crescita. Utilizzando un processo di autoassemblaggio di gocce di gallio abbiamo dimostrato un approccio per ottenere combinazioni di diametro-densità in modo da minimizzare la riflessione della luce da parte della foresta di nanofili. Questi risultati indicano un chiaro approccio per ottenere crescita di nanofili con le desiderate proprietà in termini di diametro, densità e orientazione, aprendo la via allo sviluppo di celle solari basate su nanofili di GaAs su superfici di Si.

Parole chiave

Nanofili, MBE, crescita di cristalli, semiconduttori III-V.

Contents

1 General introduction

The purpose of this chapter is to put the scientific research of this thesis into context with the current energy landscape, providing the motivation of the materials' and geometry choice. In a second step the general and specific objectives are outlined.

1.1 Energy Landscape

Energy has been shaping the global political and economic landscape in the last century, due to the localized distribution of the resources. However major changes are coming ahead: global warming and the limited volume of non-renewable resources are driving towards a historical change towards renewable energy resources, and the COP 21 agreement signs the beginning of it.

The energy production started to shift towards renewable resources, such as solar and wind, which are more homogeneously distributed on the global scale. This trend is observed in the installed global photovoltaic (PV) capacity, which has been growing exponentially in the last 20 years (see Figure 1 (a)), leading to a dramatic drop in cost (see Figure 1 (b) and Swanson law [1]).

Part of this trend is due to the incentives and benefits from government policies stimulating economically the sector. The initial high cost of the PV technology prevented mass deployment until the early 2000, when finally the financial subsidies brought a drastic cost reduction. The technological advances, together with more effective business models drastically reduced the upfront costs and increased adoption.

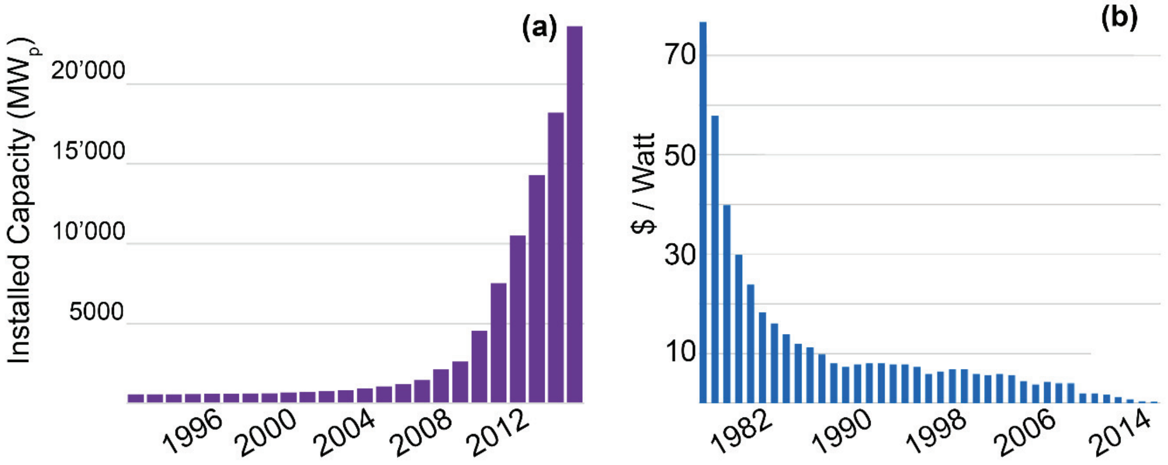

Figure 1 (a) Installed PV capacity since 1992 in megawatt peak. Data taken from [2] [3]. (b) Price per Watt of crystalline Si solar cell during the last ~50 years [4] [1] [5].

The price trend was followed by efficiency improvement of Si solar cells up to 25% on the lab scale (keep in mind that the best module performances are~20%), approaching the theoretical limit of 29% [6]. Key to the successful improvement of the technology was the quality of the raw material, which makes nowadays the 60% of the module cost [7]. The high contribution of Si to the final module cost is counterintuitive considering that Si is among the most abundant elements on earth. Nevertheless, the degree of purity of Si needed for solar is extremely high (impurity % required < 10^{-6}), requiring expensive purification processing.

1.2 Why GaAs

Another approach to further improve the solar cell performances is to explore materials with better properties. Among the different candidates, GaAs and InP are the most promising one given the highest theoretical efficiency limit (~34%) [8]. However GaAs is a more technologically relevant, given Ga wider availability on the earth's crust in comparison to In. We therefore choose to focus only on GaAs. This material presents ideal characteristics for solar energy conversion: strong absorption, direct bandgap and low non radiative energy losses. Given these properties, it is no surprise that it holds the record for the highest power conversion systems than any material system (28.8% lab and 24.1% module) [9]. However GaAs is not widespread because production has been demonstrated not to be cost effective in high volume manufacturing [10]. Several companies attempted to bring GaAs "up to scale", but unsuccessfully. It is worth mentioning Alta Devices^{TM}, a company in California who developed flexible GaAs solar cells 1µm thick with record efficiency (28.4%). Their performances attracted the interest of several investors (KPCB, August Capital and Dow Ventures just to mention a few), raising 120M$ in venture capital. Despite the competitive product, the price per watt did not reach competitive levels (~12$/W, 1 order of magnitude more than Si). New approaches that involve solar concentrators are being developed to increase GaAs competitiveness. The good performances of GaAs solar cells at high temperature allow the introduction of concentrators which reduces the solar panel dimensions. However also this approach did not prove yet its cost competitiveness.

A possible solution to overcome the GaAs issue that hinder its competitiveness is to lower the manufacturing costs. This could be achieved by integrating GaAs on Si to leverage the infrastructure of the latter to lower production costs, and the top performance of the compound semiconductor enhance conversion. The characteristic larger bandgap of GaAs (~1.42eV) than Si (~1.1eV) allow the combination of the two to form a dual junction solar cell with better performances. However the integration of GaAs on silicon presents several issues such as lattice and polarity mismatch and a large difference in thermal expansion coefficients [11]. These dissimilarities generates a variety of technical hurdles that have to be taken into account to successfully combine the two materials:

- Antiphase boundaries: GaAs is a polar semiconductor, since it is formed by Ga, a group III elements, and As, a group V element. This is not the case for Si, a group IV element (apolar). Therefore, even though Silicon and GaAs have identical crystalline structures (face centered cubic (fcc)), the two fcc lattices of GaAs are not identical: one is occupied by Ga atoms, the other one by As atoms. As a consequence, in the case of GaAs growth on silicon the first monolayer can either be partially gallium and partially arsenic, since silicon has the same probability to bond with As and Ga atoms. This lead to the coexistence of areas with Ga atoms and areas with As atoms on the initial layer, where As-As bonds and Ga-Ga bonds are formed at the interface between domains. These defects are called antiphase boundaries (APBs), and degrade significantly the device performance [11].

- Thermal mismatch: Si and GaAs thermal expansion coefficient differ of 60% at room temperature, and at elevated temperatures it narrows down only slightly. Such a mismatch causes thermal stress in the GaAs layer, distorting the GaAs lattice up to bending and cracking [11]. The latter completely deteriorate the properties.

- Lattice mismatch: GaAs has a bigger lattice constant than Si since its atoms are bigger (a_{GaAs}=5.65Å and a_{Si}=5.43Å). This lattice mismatch causes strain in the GaAs lattice during growth, and the energy associated to it scales linearly with the thickness of the GaAs epilayer h [12]. In other words, up to a critical thickness of the epilayer the energy can be accommodated elastically, and beyond that is accommodated plastically, forming misfits and dislocations at the interface. In the case of GaAs on Si the mismatch is ~4%, which correspond to a critical thickness of ~1nm [13], out of interest for PV applications.

1.3 GaAs nanowires on Silicon

The apparent unfeasibility of combining GaAs with Si, imposed by lattice, polarity and thermal mismatch, can be overcome by using GaAs nanostructure geometries. The advantage of the latter is the reduced contact area, which moderate the strain, limiting the formation of dislocations and misfits at the interface up to complete elastic relaxation [14]. At the same time the nanostructures are mainly formed by a single nucleation event on the substrate and separate, overcoming also the anti-phase boundary formation. As such, nanostructures are the only viable opportunity to successfully integrate GaAs on Si (beyond the critical thickness mentioned in the previous section). In the present work the nanostructures of our choice are nanowires, since their characteristics suite perfectly PV applications: the geometry is advantageous to capture light [15], it allows enhanced design flexibility [16] [17] and it minimizes material usage [18].

To better understand the advantages of these nanostructures we have to step back to the conventional PV geometry, and understand its design constraints. Commercial solar panels are formed by different 2D layers, where the design is based on the compromise of a film thick enough to absorb as much light as possible, but thin enough to optimize carrier extraction. Instead, with nanowires geometry the junction can be designed radially, so that the full length of the nanowires is used to absorb light, and the carriers are extracted radially.

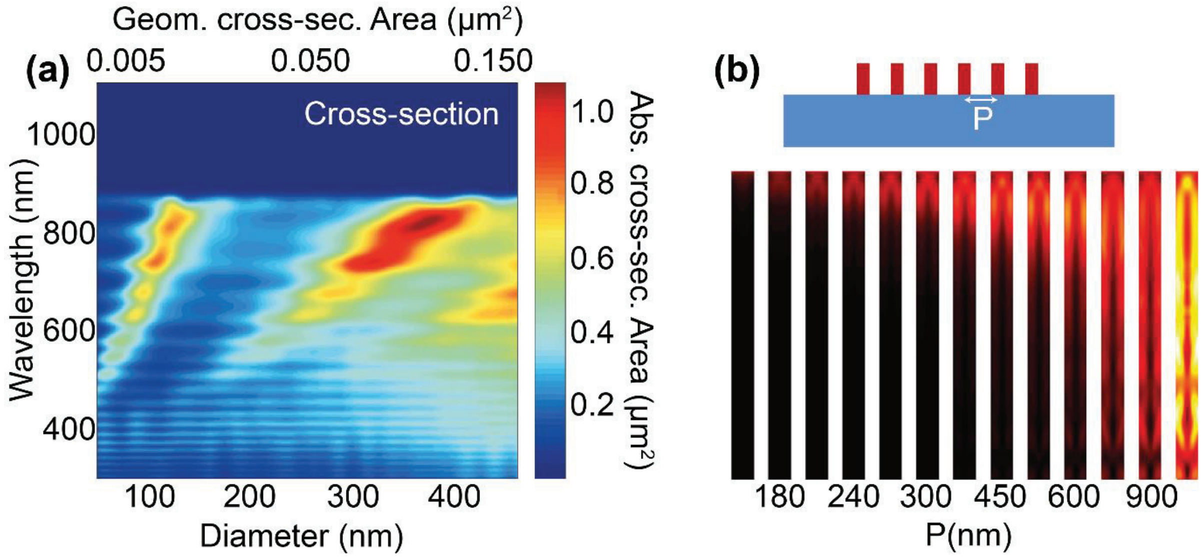

Figure 2 (a) Simulated light absorption of a GaAs nanowires perpendicular to the Si substrate. Reprinted by permission from Macmillan Publishers Ltd: Nature Photonics [15], copyright 2013. (b) Calculations of light absorption (average of the square of the electric field) in GaAs nanowires in an array for different pitches (i.e. nanowires spacing) [18]. © IOP Publishing. Reproduced with permission. All rights reserved.

Moreover the nanoscale dimensions of nanowires bring new properties which suite the PV application: they act as natural light concentrators. In other words, nanowires absorption cross-section strongly exceed their geometrical cross-section (see **Figure 2** (a)) [15], meaning that they can be spaced between each other and still absorb as a planar film, if not exceed it [19]. To better understand this concept we have to consider that light absorption in nanowires is not simply function of the material, but also of the specific nanowires geometry, namely diameter and density [18] [15].

Another interesting consequence of their property for PV application is observed by tuning the nanowires density: the full length of the nanowires can be used to generate and extract carriers (see **Figure 2** (b)), while dramatically reducing the material consumption. This is another advantage for PV application, since it allows to minimize the usage of GaAs, which is an expansive semiconductor (~1000x the price of Si [20]).

It is important to remark that all the above mentioned properties hold only for nanowires perpendicular to the Si surface, and (unfortunately) this is not the only possible growth direction for GaAs nanowires on Si. This makes orientation a key property to control, together with density and diameter. To better understand the origin of these different possible orientations we have to consider the fundamentals of growth and the nature of GaAs and Si.

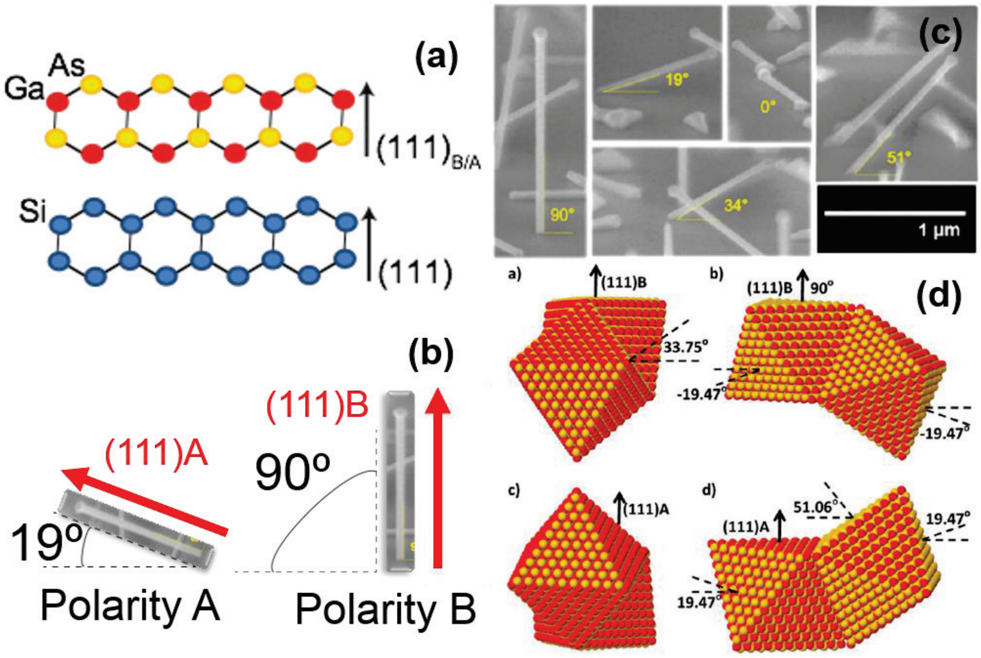

Figure 3 (a) Schematic of the Si lattice and GaAs lattice. (b) nanowires orientation based on the polarity of the first layer of atoms at the interface with Si. (c) Cross-section scanning electron micrographs of GaAs nanowires growing in different angles with respect to the substrate surface [21]. (d) 3D atomistic models that explains with 3D twinning the multiple observed orientations [21]. (c)-(d) Reprinted (adapted) with permission from [21]. Copyright 2016 American Chemical Society.

The direction of growth is determined by the energy minimization principle. Since the process we are considering is liquid catalyst driven, the catalytic droplet positions on the facet with the largest surface free energy to drive growth in that direction. For a Zinc-Blende crystal the (111) facet is the one with the largest surface energy since it has the highest atom-density/packing-density.

However another element has to be considered for GaAs: it is a polar semiconductor, meaning that it is formed from Ga atoms of the group III elements, and As atoms of group V elements. This binary composition has consequences at the crystal structure level: the two face centered cubic (fcc) primitive lattices that forms the Zinc Blende structure are one occupied by Ga atoms, and the other by As atoms.

In the case of the (111) plane, the surface is either Ga terminated (also called A-polar) or As terminated (B-polar) (see **Figure 3** (a)). As a consequence, the <111>

direction can be distinguished into <111>A and <111>B depending on the surface termination. In the case of growth on Si (111) substrates, depending on the polarity of the layer the nanowires will be either oriented perpendicularly to the surface (B-polar), or be tilted of 19° (see **Figure 3** (b)). To further complicate the scenario, the presence of defects or twins allow an even wider variety of possible orientations, such as 34°, 51° or even horizontally, as shown in **Figure 3** (c)-(d) [21]. Our group studied in detail the crystal orientation of the grain to understand the root cause of the different orientation of the nanowires. Evidences of multiple grains separated by twins in the case 34° and 51° tilted nanowires explained the appearance of these otherwise inconsistent orientation with the crystallography of a single grain.

1.4 Objectives and Outline

To recapitulate, the successful integration of GaAs on Si would pave the way to the development of high efficiency dual junction solar cells. In this frame of ideas the nanowire geometry is the most promising approach in terms of performances and potential cost saving opportunities. A Schematic of the aimed device is represented in **Figure 4**.

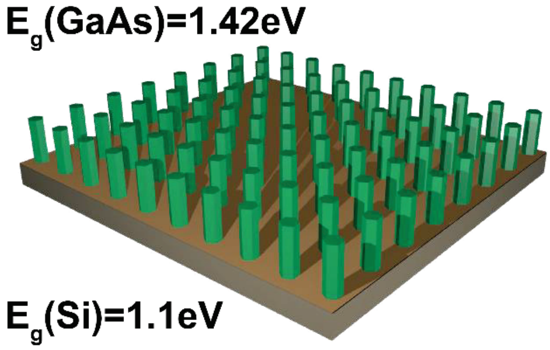

Figure 4 Schematic of the GaAs/Si dual junction monolitically integrated solar cell. In green the GaAs nanowires are represented, whereas in brown Si.

To work towards the development of this technology the following milestones have to be accomplished from the crystal growth side:

- The control of the nanowires diameter to tune light absorption.
- The control of density to minimize material usage.
- The control over orientation to enable the above mentioned properties.

All the above have to be accomplished reproducibly on a wide scale. These issues are of uttermost importance to advance in the development of GaAs nanowires solar cells on Si, and are therefore the main focus of this thesis.

In chapter 2 a general overview of GaAs nanowires growth is provided to place our research into context with the advances and with the open challenges in the field.

In chapter 3 we investigate in detail the role of the silicon oxide in the growth process, demonstrating it as a key parameter to achieve the desired nanostructures, control their orientation and their density.

Chapter 4 is dedicated to the study of the influence of the growth conditions over diameter and density. The understanding of the growth mechanism is used to grow tailored diameter density distributions of nanowires forests, demonstrating their influence over the reflectivity of the array.

2 State of the art of growth of GaAs Nanowires

2.1 Nanowires

Nanowires are filamentary crystals with high aspect ratio (see **Figure 5**), which can be grown out of many different materials, by means of different techniques.

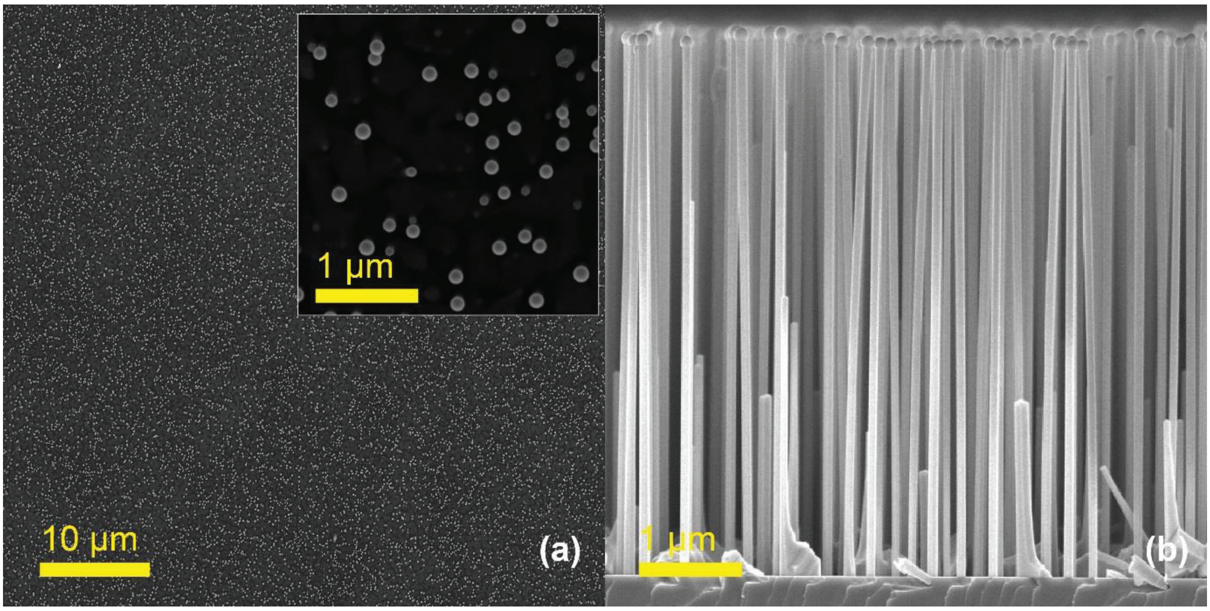

Figure 5 Electron micrographs of self-catalyzed GaAs nanowires grown on a Si(111) substrate via MBE technique. (a) shows the top view of the nanowires: vertically elongated crystal. The inset show a closer look at the catalytic droplet on top of the nanowires. (b) reports a cross section image of the nanowires to show the extended aspect ratio.

The first example of these filamentary crystals dates back to 1951, with low melting point metals [22]. Few years later Barns and Ellis reported the first example for GaAs [23]. To experience a renewal in interest, their exploratory work needed to wait more than 30 years to be fully appreciated. The interest in these highly anisotropic structures was renewed in the early 1990 by Hiruma et al. [24] [25], but only around the 2000 the pioneering work of the Lieber group (Harvard University) triggered the interest of a vast community, as they demonstrated the interest of these structures fir a wide variety of applications [16] [17]. From there on, the field experienced an exponential growth of publications per year. Among the most influential groups that demonstrated the high potential of nanowires very early on for optoelectronic applications are the Yang group (University of California Berkeley) [26], the Samuelson group (Lund University) [27], and Bakkers group (Eindhoven University) [28].

Since the exploratory work of Wagner and Ellis several synthesis methods have been developed; the more established are Molecular Beam Epitaxy (MBE), Metal Organic Chemical Vapor Deposition (MOCVD), Metal Organic Vapor Phase Epitaxy

(MOVPE), Chemical Beam Epitaxy and Gas Source-Molecular Beam Epitaxy. The technique of our choice is MBE.

All the above mentioned techniques have in common the possible mechanisms with which Nanowires can grow: the vapor liquid solid (VLS) mechanism and the vapor solid mechanism (VS). The VLS method was discovered in 1964 by Wagner and Ellis for Si whiskers [29], and from there on it got applied to different material systems.

2.2 Vapor Liquid Solid (VLS) & Vapor Solid (VS) Growth mechanisms

The VLS mechanism, as the name suggests, involves three different phases: liquid, solid and vapor. The liquid forms droplets on the surface by diffusion (see **Figure 6**), and act as catalyst. These droplets adsorb the atoms impinging onto its surface, which start to diffuse towards the inside of the catalyst due to a concentration gradient. Once the adsorbed atoms reach supersaturation, the material precipitates underneath the droplet in solid form (see **Figure 6**). It is worth mentioning that, since the solid phase precipitate underneath the droplet, the size of the latter will determine the nanowire diameter. In the case of a crystalline substrate, the seed crystal nucleated in the droplet is formed epitaxial to the substrate.

The continuous precipitation drives the growth of the nanowires along the direction of the largest surface free energy (e.g. in the case of a ZB crystal is (111)).

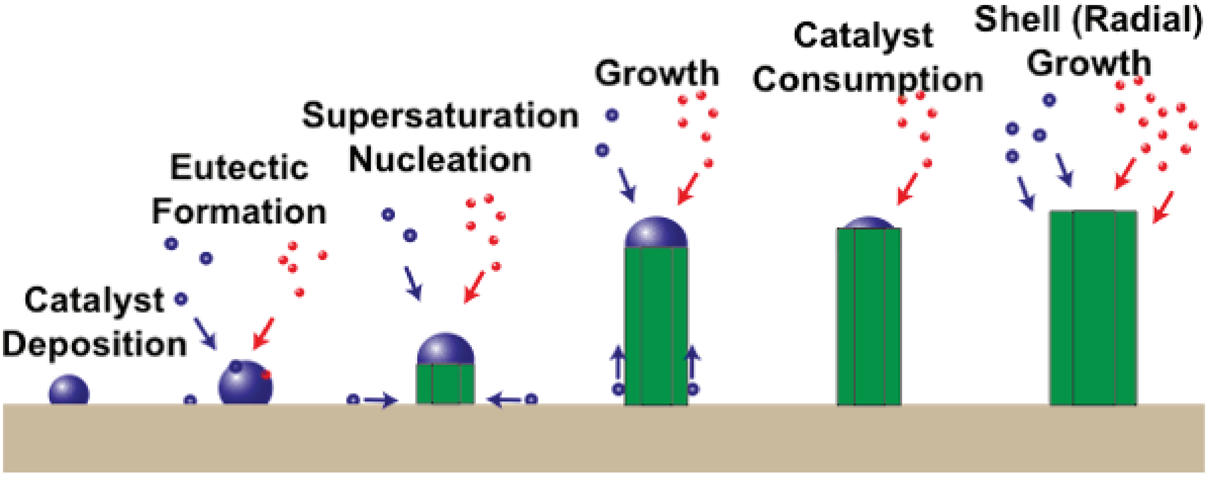

Figure 6 From left to right schematic of the evolution steps of the VLS mechanism. The catalyst is pictured in blue, the vapor phase in red and solid phase in green. The last two steps illustrate the termination of vertical growth and shell growth by VS mechanism.

The nanowires keep growing as long as both the liquid and the vapor phase are fed into the system. To terminate the process, in the case of self-catalyzed growth, the catalyst supply is interrupted, so that the liquid phase gets "consumed" (see **Figure 6** "Catalyst Consumption"). The practice described heretofore is also called "core growth". A variation of this method is the vapor solid solid (VSS), where the catalyst is in solid phase [30].

In the specific case of nanowire based solar cells or any other radial heterostructures, this core growth is followed by vapor solid (VS) growth to form the shells. The VS method differ from the VLS since it does not involve liquid. The elimination of the latter is achieved by a combination of lower growth temperatures than VLS and higher vapor phase supply. These different conditions lower Ga mobility, which cannot reach anymore the more energetic (111) facet, producing epitaxial growth uniformly in all the directions. This result in a uniform shell around the nanowires (which is used as "template").

To recapitulate, the main variables in the VLS growth process are the catalyst, the vapor flux and the solid substrate. In the following sections we review the current knowledge on the effect of these variables onto the nanowire properties in the case of GaAs.

2.2.1 Liquid Catalyst

The main catalysts that have been investigated for GaAs nanowire growth are Au and Ga (the latter also called self-catalyzed, or catalyst free). The main difference between the two metal catalysts is that they have different surface tensions, which lead to a change of the nanowires crystal structure: for Ga, which has lower surface tension than Au, the preferred crystal phase is Zinc Blende (ZB), whereas for Au Wurtzite (WZ) [31] [32]. It is important to note that WZ is never observed in the bulk phase because it is energetically more costly than ZB. Another difference between the two catalysts is that Au present disadvantages for the fabrication of both radial and axial heterostructures.

For axial heterostructures the sharpness of the interface depends on the type of material change that is performed. In the case of change of material of group V sharp interfaces can be achieved, since group V elements have generally low solubility into Au. This may not be the case for group III materials, since they have high solubility into Au. This problem is originates from the ternary alloy in the catalyst, where Ga has higher solubility than As into Au. In other words, even at complete As consumption Ga will still be in the droplet. This effect is called reservoir effect, and impedes the formation of sharp axial interfaces between different materials [33] [34]. To circumvent the problem Dick and coworkers developed a technique that involves pulsing fluxes to control the abruptness of the interface [35].

In the case of radial heterostructures the Au-catalytic droplet cannot be consumed in situ, increasing the complexity of the process. Moreover Au present the disadvantage of getting incorporated at the impurity level into the nanowires [36], although the effective incorporation in III/Vs is still controversial. From a more fundamental standpoint the Au catalyzed approach provide helpful insight into the mechanisms of growth. In our case we decided to focus on the self-catalyzed option, being the most promising candidate. Nevertheless, we will also review the Au catalyzed achievements. In the following sections the state of the art of GaAs growth is presented, divided in Au catalyzed and self-catalyzed.

2.2.1.1 Au

Historically Au catalyzed growth was first studied [23]. Among its advantages is the simple formation of nano-droplets by evaporation and annealing of a thin film, lack of oxidation, and the ease of control of their size by simply tuning annealing time and temperature. The majority of the investigations for Au catalyzed nanowire growth has been performed on GaAs substrates.

In the case of Au-catalyzed growth on GaAs substrates the research has mainly focused on the control of the crystal phase, and on the fundamental understanding of the kinetic processes:

- Control of the crystal phase: nanowires exhibit high density of stacking faults in the <111>B growth direction (see Figure 7), leading to the coexistence of WZ and ZB.

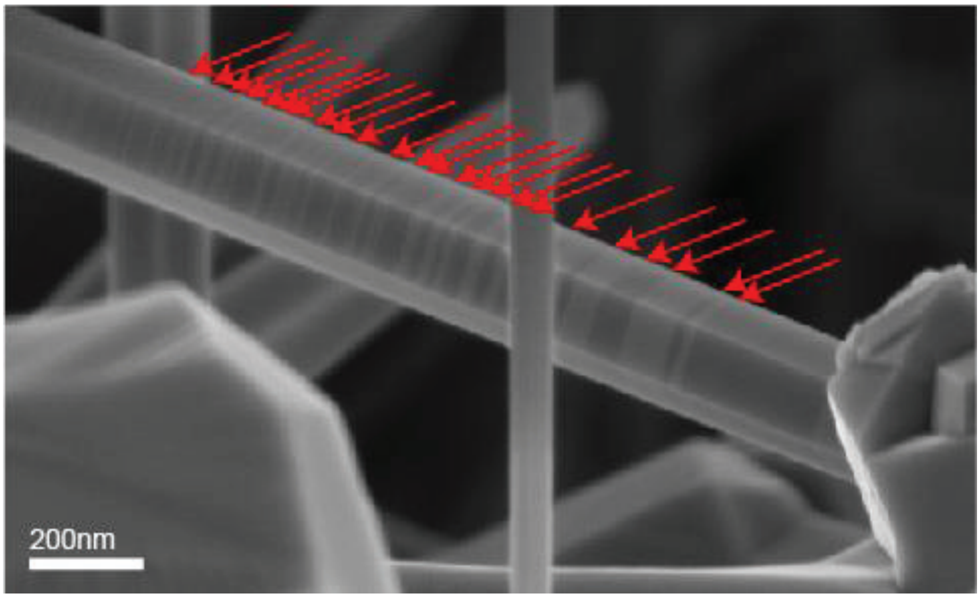

Figure 7 Scanning Electron Micrograph of a GaAs nanowire. The red arrows points at where the stacking faults can be observed along the length of the nanowire.

  The control over the crystal structure is crucial for PV application because defects affects the electronic and optical properties of the Nanowires. Therefore many studies focused on the occurrence of wurtzite and zinc-blende, and the relative growth conditions to control their appearance [38] [39] [40] [41] [42] [43]. However, only recently an experimental proof of the crystal phase change has been reported by in-situ technique: the droplet volume, chemical potential and associate contact angle change the nucleation of the new bilayer from the triple phase line (line of contact between vapor, solid and liquid) to inside the droplet [44].

- Fundamental understanding of the kinetic processes: comprehension of the adatom diffusion contribution to nanowires growth in terms of length and diameter distribution [45] [46], and how process parameters influence it [47] [48] [49] [50] [51].

To date, few studies of Au-catalyzed GaAs nanowires have been performed on Si(111), since Au-Si form an eutectic, which favors the incorporation of Au impurities in the nanowires. Nevertheless, from a fundamental standpoint the investigation of GaAs nanowire growth on Si provides insightful information on the influence of the substrate over the process. Different results have been achieved by changing the surface preparation [52] [53] [54] [55], suggesting an influence of the surface properties on the process. This topic will be investigated in depth in the Chapter 3.

2.2.1.2 Ga

The Ga catalyzed process was introduced to circumvent the drawbacks of using Au (see 2.2.1 and 2.2.1.1). It involves the use of Ga droplet as catalyst, which avoids any potential contamination by foreign metals, and allows the consumption of the catalytic droplet to form heterostructures (see 2.2.1). This is yet another advantage for the Ga catalyzed approach.

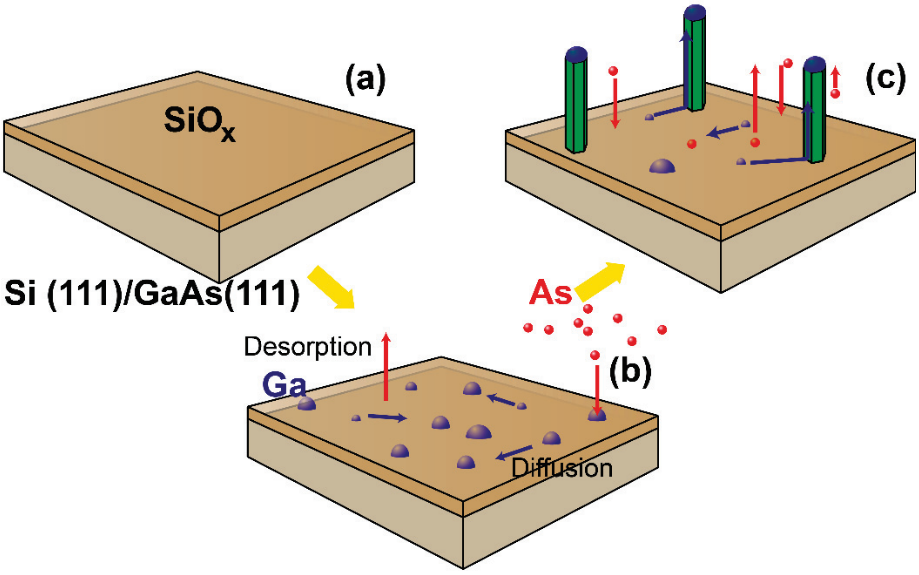

Figure 8 Illustration of the VLS mechanism for self-catalyzed nanowires growth. Section (a) shows the initial step, a GaAs(111) or Si(111) surface coated with silicon oxide. (b) When the material fluxes are started Ga will form droplet on the surface. Instead As, which has higher vapor pressure than Ga, will tend to stay in the vapor phase through adsorption and desorption. Section (c) pictures when the Ga droplet supersaturation has already been achieved, and the nanowires growth started. In this stage the material feed to the catalytic droplet is by diffusion for Ga, and via adsorption of directly impingent and secondary flux for As.

The Ga droplet can be formed during the growth process in Ga rich conditions, where the accumulation of Ga on the surface is promoted, without the need of predeposition (see **Figure 8**). In other words, Ga droplets are naturally formed on the surface even though both Ga and As fluxes are supplied at the same time. This happens because at the nanowire growth temperature (~630°C) the As vapor pressure is higher than the Ga, favoring As to stay in the vapor phase and Ga in the liquid phase [56] [57]. Nevertheless, the Ga droplet formation is a necessary but not sufficient condition to grow nanowires: a thin layer of oxidized Si was observed to be necessary, both in the case of Si or GaAs substrate [58]. Our group reported a critical oxide thickness for sputtered oxide of 30nm on GaAs (111): below that thickness pinhole were formed, allowing epitaxial connection of the nanowires to the substrate (see Figure 9 (a)). Instead, above 30nm only randomly oriented nanowires were observed (see Figure 9 (b)) [59]. To date, the role of the oxide in the growth process was not understood. A detailed investigation on how oxide influences nanowires formation is presented in Chapter 3.

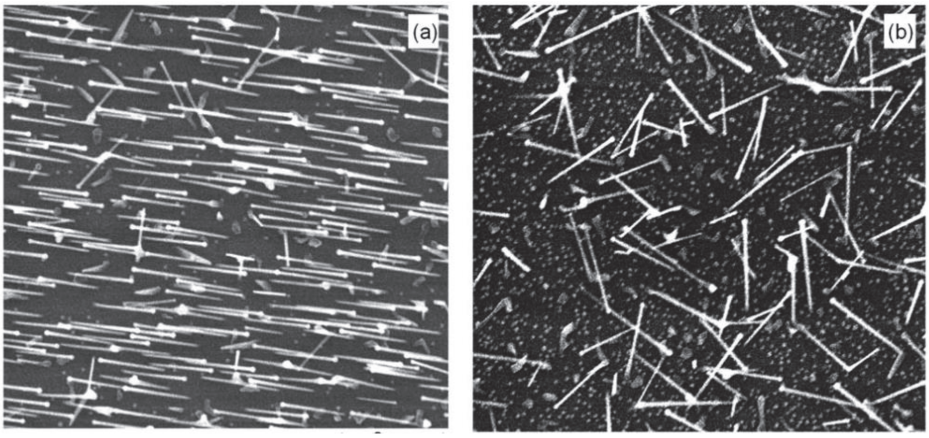

Figure 9 Scanning electron micrographs of self catalyzed growth of GaAs nanowires on Si(100) on GaAs substrate coated with a (a) 6 nm and (b) 90nm thick layer of sputtered silicon oxide layer. Reproduced from [59], with the permission of AIP Publishing.

As in the case of Au catalyzed, the GaAs substrate was the first one on which growth was achieved also for the self-catalyzed process. The topics that have been first investigated are also similar to the case of Au catalyzed: the influence of the process parameters over radial and axial growth rate [60], and the control of crystal structure [61]. Differently from the Au-catalyzed, the number of the catalytic droplets per unit area and the size are not trivial to control in the self-catalyzed approach. This challenge triggered the development of two main approaches to control nanowires density: by self-assembly (tuning the thickness of the oxide) [62], or by patterning the oxide surface with holes to control the nanowires position [63].

The first reports of self-catalyzed growth of GaAs nanowires on Si substrate were performed on cleaved Si(100) and on Si(111) by respectively Jabeen et al. [64] and Paek et al. [9]. In the latter the Si surface was covered by silicon oxide, whereas Jabeen et al reported no oxide (sample was loaded directly after cleaving). This work, together with the report of Plissard et al. [65], are the only reported cases of nanowire growth without silicon oxide.

The first reports of self-catalyzed growth on Si were also devoted to the understanding of the kinetic processes, as in the other cases. The nanowire diameter was observed to increase with the Ga flux, and shrink at raising As fluxes [55], coherently with what was observed for Au catalyzed. These influences can be understood considering the effect of the Ga and As flux to the catalytic droplet: the group V flux shrinks the droplet volume by increasing the precipitation of the solid, whereas the group III increases it. Differently from Au catalyzed, the Ga flux was also observed to affect, together with temperature, the density of the nanowires and of 2D polycrystalline islands growth, also called parasitic material [66] [67] [68]. This trend is understood in terms of increased diffusion of Ga on the surface, which favors the formation of more nucleation sites. Alternative approaches to control nanowires density have been explored, both by self-assembly and by patterning the oxide with holes. In the first case the well-established droplet epitaxy was used to form catalytic droplets with the desired density and diameter. The droplet properties were controlled by temperature and Ga flux, and then converted into nanowires in a second step [69]. A similar approach has been used to achieve lithography free patterning: in this case the droplets were also supersaturated to form GaAs crystals, and then exposed to air to define the nucleation sites. By doing so an oxide mask is formed around the crystals, which are evaporated once reinserted in the growth chamber, leaving empty holes in the oxide mask. These sites are used as nucleation sites for GaAs [70]. However both approaches present limitations over the yield of conversion of droplet into nanowires. A more common approach to control nanowire density is by controlling the density of the nucleation sites via lithographic patterning. In this case thermally grown SiO_2 is used as a mask, which is then patterned by e-beam lithography to define the nucleation sites. Many groups attempted this approach, however the reproducibility over the yield of vertical nanowires is still an unresolved issue [65] [71] [72] [73] [18] [74] [75].

Moreover, beyond the challenges of controlling nanowire density, it has to be kept in mind that with Si substrates GaAs nanowires can have multiple different orientations (see Section 1.3). Uccelli et al. investigated the origin of these multiple orientations and discovered that is determined both by the polarity of the nucleation seed, together with the multiple twinning formation [21]. Russo et al. used this understanding to develop a technique to control the nanowire orientation by increasing the V/III ratio, namely the the ratio of the flux of As over Ga. They suggested that the observed effect was produced by the shrinking of the droplet on just the (111) orientation of the orthorhombic seed crystal [76]. However no comparison between the size of the droplet and the size of the seed was reported. Also Krogstrup et al reported on the influence of the V/III ratio over the orientation: the lack of homogeneity over the substrate was associated to a gradient in temperature that affects the local V/III ratio [66]. We attempted the same approach to achieve control over nanowire orientation on a series of batches of wafers, but unsuccessfully. Aside of these approaches, several others have been developed to control nanowires orientation: Paek tried to induce the B polarity by exposing the Si substrate at high temperature to As overpressure, but no effect was observed [55]. Jabeen et al attempted predeposition of Ga previous to growth, and compared it with no predeposition, but no difference was observed [64]. Therefore the control over orientation of the nanowire is still an open question.

2.2.2 Vapor Fluxes and other process parameters

The process parameters that control nanowire growth are the As beam flux, Ga beam flux and temperature. Their influence over the nanowire properties have been widely investigated to gain insights in to the growth mechanism. For instance the growth rate was found to be proportional to the arsenic flux, exceeding the thin film growth rates. In other words, the observed growth rate could not be explained only by direct impingement of Ga and As atoms, but a diffusion/re-evaporation/multiple-impingement induced contribution had to be considered as the major supplier, providing a major insight onto the growth mechanism. In the case of Ga, the atoms are expected to diffuse to the liquid droplet from the substrate to the nanowire sidewalls [60] [77] [51]. However this is not the case for As, since it has higher vapor pressure than Ga (i.e. more volatile). As a consequence arsenic is expected to get adsorbed and desorbed from the surface, acting as a second source of material feed to the catalytic droplet [78].

A strong effect of the ratio between the Ga and As flux over the nanowire properties was observed. In the case of low V/III ratio, namely a stronger feed of Ga to the system, the catalytic droplet tends to increase in volume, leading to an increase in diameter of the nanowires [55] [79] [80]. Vice-versa, in the case of high V/III ratio the higher feed of As promote the shrinking of the catalytic droplet, leading to thinner and longer nanowires, boosting the growth rate [60] [55] [79] [80] [81]. Moreover the V/III ratio was also observed to influence the yield of vertical nanowires [76], as mentioned above. The modulation of the V/III ratio was also reported to affect the crystal phase formation and the density of defects, since the incoming fluxes modify the liquid droplet shape, which determines the crystal phase underneath. A deep theoretical understanding of the mechanism that lead to the control of the crystal phase has been developed [32] [82] [83], and very recently the first in situ observation of the transition mechanism was reported [44]. However, to date, the experimental attempts reported so far succeeded only partially in the control of the crystal phase in self-assembled nanowires. Researchers demonstrated only partially defect free nanowires [68] [66] [68], or crystal phase control from ZB to WZ only through highly defective transition regions [84] [79] [61].

On a different note the effect of temperature over GaAs nanowires growth reported are quite diverse: control nanowires orientation by modifying the V/III ratio [66], increase nanowires number density [68], decrease length [68] [41] [80] and increase diameter [85] [86].

2.2.3 Solid Substrate

The most widely investigated substrates for GaAs nanowire growth are Si and GaAs. It is worth mentioning that a wide variety of substrates has actually been investigated, such as graphene [87], glass [88] [89], sapphire [90] and even without the need of a substrate [91]. However, for simplicity, we focus only on reviewing the most commonly used. GaAs was the first substrate on which GaAs nanowire growth has been demonstrated, and then Si. In both cases the crystalline orientation of the substrate plays a major role, determining the direction of growth of the nanowires compared to the substrate. In other words, if GaAs nanowires are grown on a GaAs(111)B wafer, they will grow perpendicular to the substrate (see Figure 10 (a)), whereas on a GaAs(001) wafer they are tilted by 34.5° with respect to the substrate (the tilt affects the growth rate because of a stronger contribution of the adatoms having diffused, rather than direct adsorption [21, 20]. Details on how the tilting of the nanowires affect their growth process can be found in [92]).

The root cause of the influence of the crystal orientation of the substrate over the nanowires tilt is the preferential growth direction of the nanowires, (111)B, which corresponds to the crystalline facet with higher surface energy (see Section 1.3).

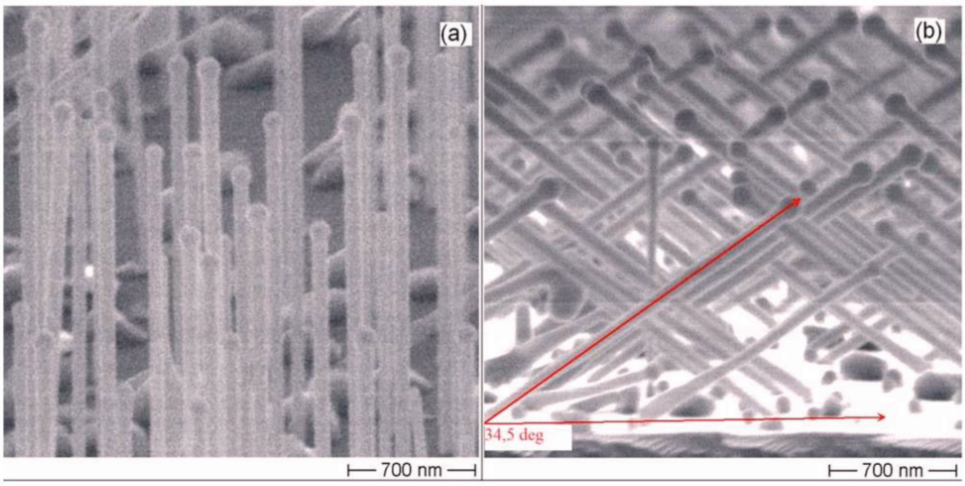

Figure 10 Scanning electron micrographs of self-catalyzed growth of GaAs nanowires on (a) GaAs (111) and (b) GaAs (100) substrates coated with a silicon oxide layer. Reproduced from [59], with the permission of AIP Publishing.

In the case of the Au catalyzed process, the substrate role is only limited to provide the epitaxial orientation to the nanowires in order to grow them in the desired direction. Instead, since the achievement of the first self-catalyzed growth, the solid substrate acquired further importance in the process to allow the formation of the catalytic droplets. The technique used consisted in depositing an oxide layer on top of the substrate to favor the formation of Ga droplets. A growth without the oxide layer does not result in nanowire growth, but only 2D polycrystalline growth. However, despite the importance of the oxide in the growth process few works investigated the influence of its characteristics (stoichiometry, porosity, thickness), and its preparation methods [93]. Several groups have suffered of lack of reproducibility by changing wafer batches for native oxide use and oxide types. In the following chapter a detailed investigation of the influence of the different types of oxides on the growth process is presented.

2.3 Nanowire Properties and Applications

As introduced in Section 1.3, nanowires present novel properties that would not be possible with bulk materials. The new engineering possibilities attracted the interest of a wide community of researchers for a broad range of applications.

An example of these novel properties is the possibility of combining materials with different lattice constant, without forming defects at the interface. The confined diameters allow elastic relaxation instead of plastic, enhancing the materials design freedom beyond the possibilities of bulk phase. A good example is the case of Ge and Si: they have a 4.2% lattice mismatch and different thermal expansion coefficient which causes high density of dislocations at the interface. These misfits act as recombination centers, which in a case of a device severely compromise its performances. However, by combining the two materials in nanowires geometry Falub and workers demonstrated epitaxial growth of Ge on Si micrometer pillars free of defects [94].

Another new possibility generated by the novel geometry is bandgap engineering using the strain at the interface of the materials. For instance, in the case of Si it could be used to transform Si into a direct bandgap semiconductor, a holy grail for Si based photonic devices [95]. Nolan and coworkers studied the nanowire band-gap modification, showing band structure modulation with lattice strain [96], specifically with tensile strain enhancing the direct band-gap characteristic. A successful example of bandgap engineering was demonstrated with GaP, where Assali and coworkers demonstrated the conversion from indirect bandgap to direct by controlling the crystal structure [97].

The range of applications where nanowires have demonstrated potential is broad and in continuous expansion. Here we report few examples (shown in Figure 11), such as (i) solar cells, (ii) LED, laser, photodetectors, (iii) transistors, (iv) chemical/biological sensors, photocatalyst and (v) thermoelectrics [98]:

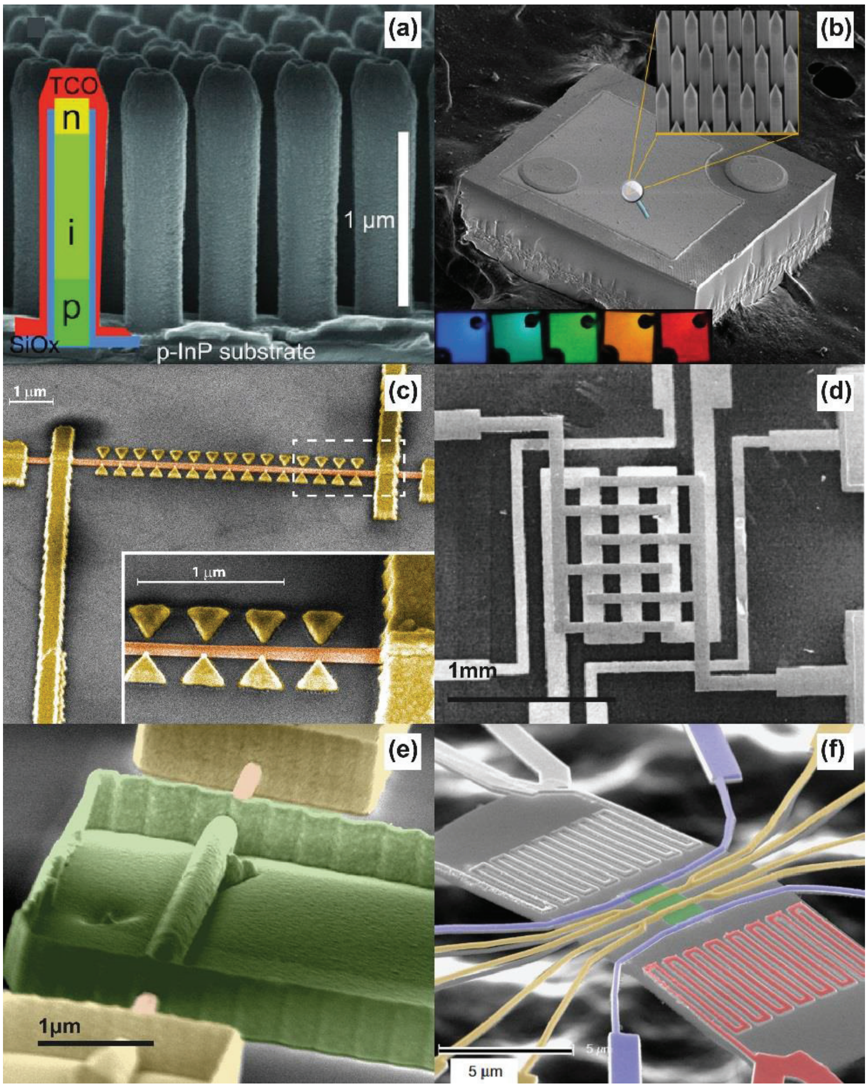

Figure 11 Scanning Electron Micrographs of different nanowire applications: (a) InP axial nanowire solar cells. Adapted from [99], with the permission of Science/AAAS. (b) GaN nanowire LED of glō® [100]. (c) Example of a GaAs nanowire used as photodetector [101]. ZnO nanowire used as ethanol sensor. Adapted from [102], with the permission of AIP Publishing. (e) GaAs nanowire wrap gate transistor [103]. (f) Example of Si nanowires employed as thermoelectric device. Adapted from [104], with the permission of Nature Publishing Group.

(i) The solar cell is one of the potential application that attracted interest in our group. As mentioned in Section 1.3, the enhanced absorption, the new degree of freedom of radial heterostructures and the minimization of material usage are all very appealing properties for PV. Atwater and coworkers were the first to investigate the opportunities of nanowires in this field in 2005 [105]. The first device demonstrations were achieved few years later with axial and radial p-i-n Si nanowires, reporting efficiencies of respectively 0.5% and 4.8% [106] [107]. GaAs followed few years later [108]. Since then much progress has been made, as demonstrated by the 13.8% of efficiency for InP axial nanowires p-i-n junction array from J. Wallentin and coworkers demonstrates (see Figure

11 (a)) [99]. The potential of nanowires for PV applications goes beyond the classical thermodynamic limits (Shockley–Queisser limit [8]), as the work from P. Krogstrup and coworkers demonstrated [15]: the enhanced light absorption is produced by the light-concentrating property of the standing nanowire, which implies new limits for the maximum efficiency obtainable.

(ii) The range of applications that involve the control of light emission find in nanowire' geometry promising characteristics. To mention a few, nanowires have a high difference in refractive index with respect to air and dimensions which confine light into smaller dimensions than dielectrics. Moreover the elongated geometry acts as waveguide, which leads to very high radiative quantum yield (~90-100%), a very important property for both LED, photodetectors and laser (see Figure 11 (b)-(c)). For the latter the nanowire offers a simplified design, since it acts as both gain medium and cavity. Additionally, the shape of the tip can be adapted to improve photon extraction and low spatial dispersion, easing the collection by common optics [109]. As in the case of the photovoltaic application, the possibility to combine materials with different lattice constant enhances the design freedom. In the case of laser the first example of optically driven laser was reported by Huang et al. in 2001 for zinc oxide (ZnO) nanowires [110], which set the ground for the development of the electrically driven nanowire lasers in 2003 [111]. However, to date, no electrically driven laser for axial or radial junction has been realized. Among the reasons are the doping and the electrode design challenges. On a different note, Heiss and coworkers demonstrated the self-assembly of a high-quality bright quantum-dot in nanowires using two basic components, GaAs and AlAs [112].

(iii) For sensing application the large surface area of the nanowires is an interesting property for both chemical and biological sensing, as well as catalytic surface, providing potential enhanced/extended sensitivity/reactivity [113] [102] [114]. An example of chemical sensor is shown in Figure 11 (d).

(iv) In the case of transistors the geometry again plays an important role, allowing a uniform gate (wrap gate, as shown in Figure 11 (e)) that avoid any potential leakage at the nanoscale, which is an issue with other geometries. The first example of a nanowires transistor was reported for the case of core shell geometry by Xiang and coworkers, with a field-effect transistors [115].

(v) In the case of thermoelectrics, nanowires can combine poor thermal conductivity and high electrical conductivity, key factor in maximizing thermopower to have efficient thermo-electric devices [116] [104]. An Example of a Si nanowire employed in a thermoelectric device is reported in Figure 11 (f).

2.4 2.4 Molecular Beam Epitaxy

Molecular Beam Epitaxy (MBE) is the technique of our choice to fabricate nanowires. It was invented in the 1960s at Bell Labs by John R. Arthur Jr. and Alfred Y. Cho as epitaxial thin film deposition. The peculiarities of the technique are the Ultra-High-Vacuum, low deposition rates (~3μm/h), and extreme purity of elemental sources. These characteristics make MBE grown films the best in purity and crystal structure.

The underlying physics which govern the process is rather simple: the elemental sources in ultra-pure form (~99.999999%) are evaporated or sublimed to generate a flux of materials going towards the targeted surface. The latter is heated to allow the mobility of the incoming atoms on the surface, so that they can re-arrange epitaxially. By changing the material fluxes, heterostructures with sharp interfaces can also be formed.

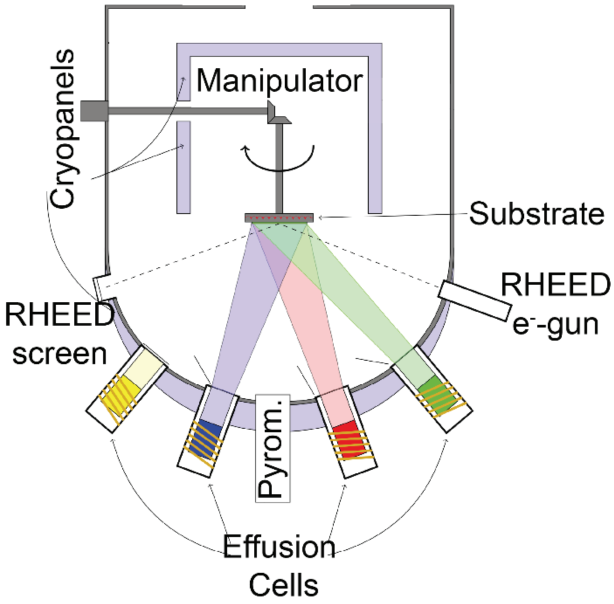

Figure 12 Schematic drawing of an MBE system

Such a simplicity is achieved thanks to sophisticated technologies: Knudsen effusion cells to finely tune the atomic fluxes of materials (see **Figure 12**), cryogenic pumps and cryopanels to keep the UHV conditions and reflection high energy electron diffraction (RHEED) to monitor the crystal layer growth rate. This technological effort is necessary to keep the extreme conditions at which the system operates, such as effusion cells at >~1000°C and pumps at -259°C. These conditions are needed to achieve the high quality structures. For instance, the UHV conditions are fundamental to fulfill the molecular beam conditions, since the atoms' mean free path has to be bigger than the growth chamber. Such a design avoid potential contamination of the substrate: all atoms that are not impinging on the substrate directly from the effusion cells diffuse until trapped from the cryopanels (cold traps).

The main components that forms an MBE machine are:

- A UHV system as the one shown in **Figure 13**, which is sequence of stainless steel chambers with different functions, all connected via a robot arm but separated by gate valves to avoid cross contamination. The main chambers in our system are:
    - A central distribution chamber (CDC), from which the robot arm control the transfer to all the other cluster of chambers.
    - A load lock chamber, where the samples are loaded. It is the only chamber that reaches atmospheric pressure.
    - A degassing chamber, used for the only purpose of heating the substrate after loading to remove potential impurities from the surface.
    - A hydrogen chamber to further clean the surface under H flux.
    - A storage chamber where the samples sits after degassing or growth.
    - Two growth chambers where the effusion cells are located, in which growth is performed.

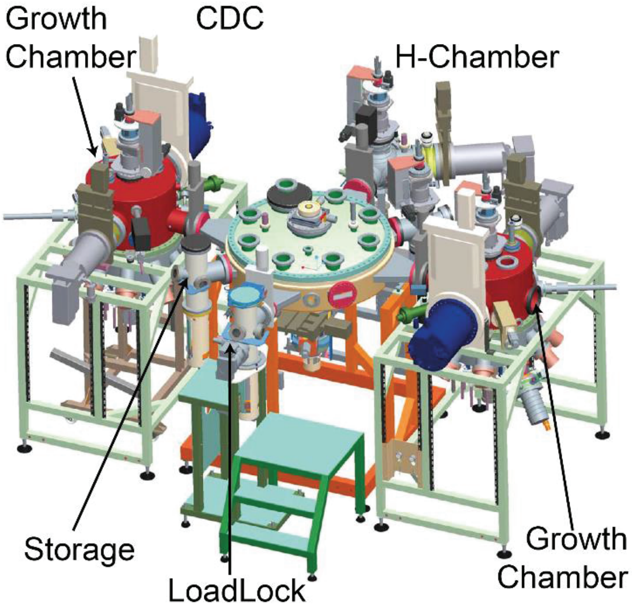

Figure 13 Schematic of the DCA P600 MBE machine, with all the UHV components.

  All the above mentioned components need to be able to withstand bake-out temperatures of 200°C for extended periods of time. This process is used whenever a component is exposed to air, to reduce the internal walls desorption (or outgassing) of material.

- Knudsen cells, or effusion cells, where the elemental sources sits (see **Figure 12**). In our system the elemental sources installed were Ga, As, In, Al, Sb and Si and C for doping. The key component of the cells are:
    - A heating unit, which is controlled by a proportional-integral-derivative controller (PID) to improve temperature stability.

    - A shutter, which allows abrupt interruption or start of fluxes, crucial for sharp heterostructure interfaces.
- The substrate manipulator, which rotate the substrate smoothly to have homogeneous material distribution over the surface of the substrate (see **Figure 12**). At the same time, the manipulator is equipped with a heater to control the growth temperature.
- A pyrometer to measure the temperature on the surface of the substrate during growth (see **Figure 12**).
- A RHEED system, to measure the growth rate of the thin film. The system is composed by:
    - An electron gun that generates the beam of electrons (see **Figure 12**).
    - A photo-luminescent screen to observe the diffraction patterns.

  The electrons collide at small angle on the surface, and a small part of them interferes constructively at specific angles, generating a diffraction pattern on the photo-luminescent screen. The interference depends on the location of the atoms on the sample surface. The spots of the diffraction pattern fluctuate in intensity periodically, following the formation of a single atomic layer. Therefore the frequency of oscillation over a period of time are used to calculate the number of monolayers grown.
- Cooling system, composed from a cascade of different pumps: scroll pump, turbo pump, cryopumps and cryopanels. This extensive set of pumps is needed to maintain UHV (10^{-10} torr) since each type has a different range of pumping capabilities. The system is crucial for MBE to avoid cross-contamination of the cells, and desorption from the walls.

2.5 Summary

In this chapter the VLS formation mechanism of the nanowires has been explained in general, and for the specific case of the self-catalyzed GaAs nanowires growth. The influence of each one of the three different phases, vapor, liquid and solid over the nanowires growth has been presented. The inter-play between each other have been explained: the vapor fluxes control the dimension of the droplet, and the contact angle of the droplet control the crystal phase formation. The solid control the orientation of growth of the nanowires, and determine its morphology and feasibility. However, within the influence of the solid phase, the role of the oxide has not been yet clarified.

3 Role of the silicon oxide in the growth of GaAs nanowires on Si

In the previous chapter we have reviewed the VLS growth mechanism of nanowires. The influence of each phase onto the growth process has been outlined: given a catalyst, the vapor fluxes control the volume of the droplet, its supersaturation and contact angle, determining the crystal structure. The liquid phase influences the nanowire' aspect ratio, and plays an important role in the sharpness of heterostructures' interfaces. For the solid phase more complex considerations has to be taken into account, since it changes over time: at the early stages of growth the solid phase is the substrate, but when nanowire growth is already initiated the solid phase is the nanowire. In the latter case, the shape of the nanowire-catalytic droplet interface was observed to control the crystal phase purity of the nanowire [44]. On the other hand, in the case of the early stages of growth, the substrate influence was not widely investigated. Apart from the influence of the wafer crystal orientation onto nanowire orientation, no other surface properties influence on the growth process had been studied. The need of a silicon oxide layer to achieve nanowire growth had been reported from several groups with different oxides, thicknesses and growth conditions, but no comparison study has been done. The goal of this chapter is to compare the influence of oxide physical characteristics on the nanowire growth, to achieve reproducible and uniform results over the full wafer. The information gathered brings new elements to unveil the role of the oxide in the growth process.

3.1 Introduction

Since the first self-catalyzed growth was achieved, silicon oxide became an important parameter in nanowires growth. To date, few reports show successful growth without oxide [86] [64] [65], and the only works that aimed to understand the role of oxide in the growth process were performed on GaAs substrate [59], or for InAs nanowires on III/V substrates [117]. In both cases a layer of sputtered oxide was used, and no vertical nanowire growth was observed above a certain thickness. Nevertheless, these "critical" thicknesses reported were different (5nm for [117] and 30nm for [59]), even though the same type of silicon oxide was employed (sputtered oxide). The mechanism proposed to explain the role of the silicon oxide in nanowire growth involves the opening of "craters" in the oxide layer above 500°C. However no dependence on the silicon oxide nanoscale characteristics (i.e. chemical composition, roughness) was reported. Moreover silicon oxide can be produced by a wide variety of techniques, such as sputtering, thermal oxidation and chemical deposition. Rieger and coworkers investigated the influence of the thickness of a resist produced oxide (Hydrogen Silsequioxane HSQ) on the nanowire density for

GaAs substrates, and reported an increase in nanowire density when thinning oxide layer [62]. In this case the thinning of the oxide was associated to an increase in density of the pinholes.

In the case of Si substrates, few works compared the influence of different oxide preparation techniques in nanowire growth [86] [65]. Despite that, little surface characterization had been performed to understand the influence of the surface properties on the growth process. One should note that successful nanowire growth have been achieved with a wide variety of silicon oxides, but no direct comparison between them has been done to understand their effect. At the same time in our group we were experiencing lack of reproducibility when using bare Si wafers directly from the boxes, lack of uniformity over the wafer scale, and dependence of growth conditions upon wafer batches. We therefore made the hypothesis that the oxide properties and the lack of reproducibility were correlated. To verify whether or not the oxide was responsible of these reproducibility and uniformity problems we characterized the chemical composition by means of attenuated total reflection (ATR) FT-IR spectroscopy, surface roughness by Atomic Force Microscopy (AFM), and thickness via ellipsometry for the different types of oxides, in order to understand the difference in properties between each other's.

3.2 Types of Silicon Oxide

The most common types of silicon oxide are:

- Native oxide, naturally formed on the "fresh" silicon surface exposed to air, therefore to oxygen.
- Thermal oxide, achieved by oxidation at high temperature (800°C-1200°C) under controlled flux of oxygen or water (also called "wet oxide").
- Sputtered oxide, which is obtained by a physical vapor deposition method. Silicon oxide is ejected from a target onto the desired Si substrate. The oxide ejection can be performed by a wide variety of techniques (e.g. ion or reactive sputtering).
- HSQ oxide, obtained by annealing Hydrogen Silsesquioxane resin, previously spun on the substrate, annealed under Nitrogen flux at low temperature (200°C-400°C) for ~2h [118] [119].

All these different silicon oxides have different physical and chemical properties. Even though many of them have been known for more than 50 years, only recently their mechanism of formation was understood. In the case of native oxide the growth of the oxide is monolayer by monolayer triggered from a radical propagation mechanism [120] [121], without increasing surface roughness. The thickness of the oxide layer formed is affected by oxygen and water content in air, and also by the type and level of doping of the substrates [122]. An example of the oxidation process of Si which leads to the growth of the native oxide is shown in Figure 14 (a), for Si (111) substrates (10-20 Ω·cm), under controlled conditions (21°C±0.5, 44% humidity). The initial steps of oxidation result in a fast growth of the native oxide thickness, which progressively slows down, to saturate at ~1.6-1.7nm. The native oxide SiO_x present a gradient of composition from the surface to the Si interface: the closer to the surface the more x is close to 2 (i.e. stoichiometric), whereas by the Si interface x is less than 2 (sub-stoichiometric) [123], as shown in Figure 14 (b).

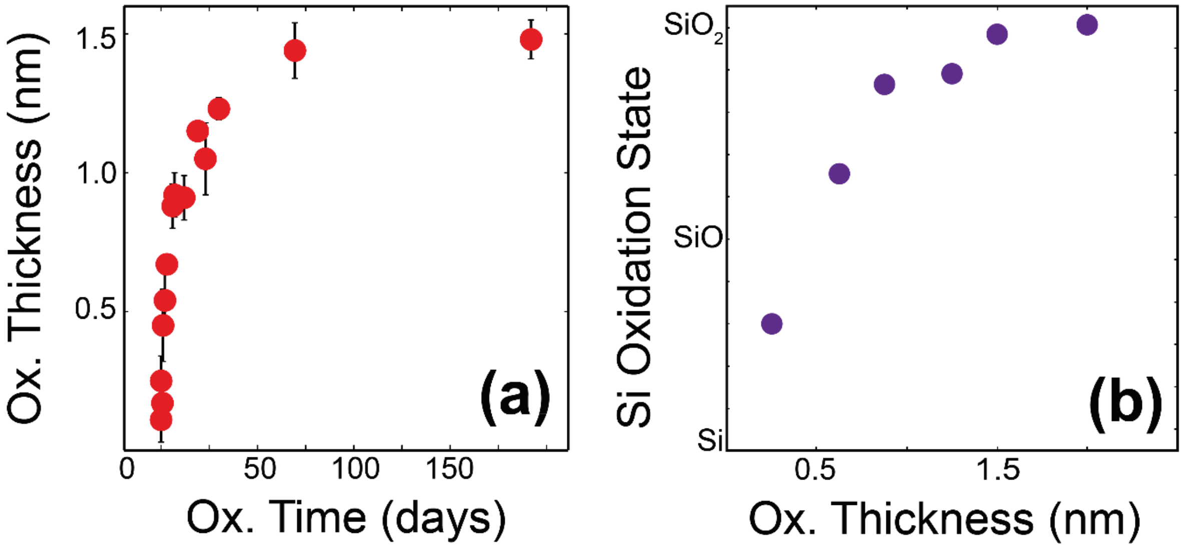

Figure 14 (a) Native oxide thickness evolution as a function of time. (b) Chemical composition evolution as a function of oxide thickness.

Thermal oxide growth is driven by a chemical reaction [64] that follows the Deal-Grove model [124]. The latter includes a first diffusion step of the oxygen to the solid interface, a second diffusion through the existing oxide layer to the silicon oxide/silicon interface, and the reaction of the oxygen with Silicon. Each step proceed at a rate that is proportional to the oxygen concentration. This oxide is the more chemically stable since it is mainly formed by SiO_2, and the compositional gradient of suboxide to the interface with Si decay extremely rapidly [125]; the oxide also presents also extremely low roughness [126].

Sputtered oxide and includes a variety of different techniques such as plasma or ion. The morphology and stoichiometry of the oxide are determined by the processing parameters such as temperature, rate of evaporation and vacuum quality. If the process is performed at low temperature and poor vacuum the oxide structure can be more porous and with lower oxygen content (SiO_x where $x<2$), whereas if the temperature and vacuum is high, higher O content is obtained, with low porosity.

HSQ oxide is obtained by a transformation of a cage structure to a network in the range of $200°C – 400°C$, while SiH_4 is released in gas phase generating porosity in the surface [119] [118]; in such a process temperature is the most important parameters for the morphology of the surface.

3.3 Outlook

In a first place, given the variety of types of silicon oxides with which successful nanowire growth had been achieved, we chose a representative selection of them, which included thermal oxide, native oxide and HSQ oxide. We characterized their chemical composition by IR Spectroscopy, the surface morphology by AFM and the thickness by ellipsometry. The different oxides presented different chemical compositions, and different critical thicknesses for nanowire growth, which were observed to be correlated to the characteristic roughness. For instance thermal oxide, the most stoichiometric oxide, presented a critical thickness of 1-2nm and a comparable roughness (see Figure 15).

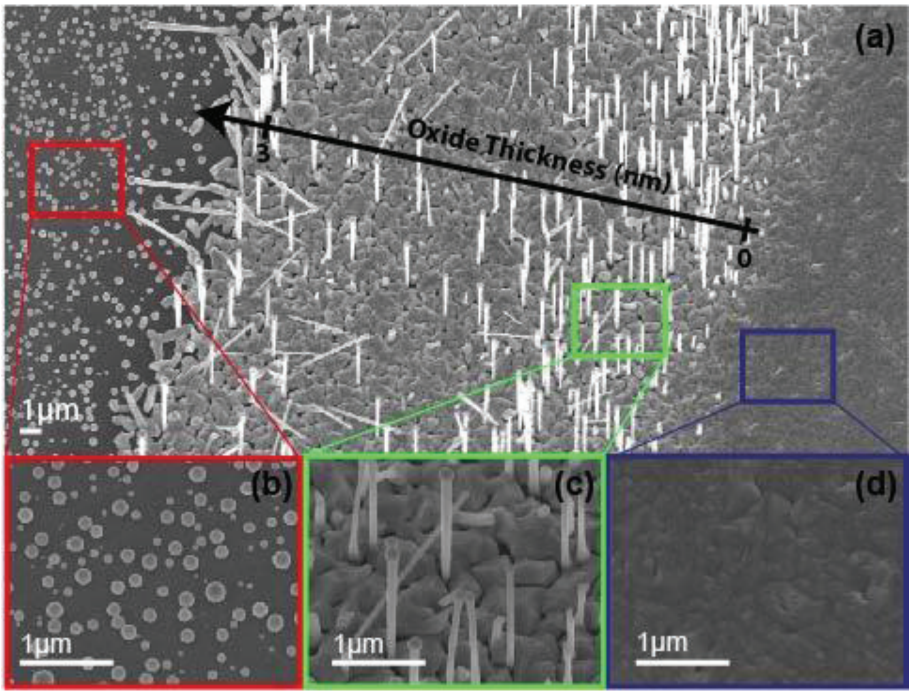

Figure 15 Scanning Electron Micrographs of self-catalyzed growth of GaAs nanowires on Si (111) coated with a layer of thermal oxide with a varying thickness from 0 to 3nm (from left to right). The inset (b)-(d) presents magnified sections at different oxide thickness.

When using lower oxygen content oxides such as HSQ growth of vertical nanowires was achieved at higher oxide thickness, 4-5nm, and comparable roughness. We then explored the parameter space (i.e. T, Ga flux and As flux) to achieve similar nanowire properties in terms of number density and diameter, and correlated the change in growth conditions to the surface properties such as roughness, stoichiometry and oxide thickness. We observed lower temperature and Ga rate growth conditions for more sub-stoichiometric rougher oxides than for instance thermal oxide.

This first work was also instrumental for us to optimize nanowire growth and its reproducibility: controlled native oxide demonstrated reproducible and uniform results over the full wafer. However, we showed that the native oxide properties changed depending on time and conditions of storage of the substrates before delivery. To circumvent this problem we developed an in-house technique to fabricate reproducibly and consistently the oxide layer. The process developed was formed by two steps:

- Etch away the original oxide layer from the wafer with an HF etch.
- Let the wafer oxidize in cleanroom conditions of humidity and temperature (21°C±0.5, 44%Humidity).

Once we could consistently control the native oxide thickness at the sub-nanometer level we investigated the influence of the oxide thickness on the GaAs nanowire growth. The outcome was surprising: by tuning the oxide layer thickness between $0<x<2$nm, the growth morphologies changed from 2D polycrystalline, to high density high yield of vertical nanowires, to low density low yield (see Figure 16 (a)-(g)). The change in nanowire density was of more than 2 orders of magnitude, and the diameter more than doubled.

The outcome of this study was to identify a simple reproducible method to grow high yield high density of vertical nanowires. At the same time it also raised questions on the causes of this abrupt change in behavior for a variation of oxide thicknesses of less than a nanometer. To shed some light on this question we characterized the oxide surface properties by depositing Ga in identical growth conditions. For constant deposition times we observed a change of the contact angle of the Ga droplet from 50° up to 116° for oxide thicknesses from 0.3nm up to 1.5nm, as shown in see Figure 16 (h)-(n). At the same time, also the Ga droplet dimensions changed with the oxide thickness, as shown in see Figure 16 (o)-(u): they went from 2μm in diameter for 0.3nm oxide, to 60nm for the case of 1.5nm oxide. These results suggested a change in the surface properties with oxide thickness. To probe the changes in surface energy (i.e. wettability) and chemical compositions at different oxide thicknesses, we performed microscopic contact angle measurements and XPS measurements. This allowed us to correlate the changes in wetting properties to a variations in oxide stoichiometry, which also corresponded to different oxide thicknesses. The next logical step was to evaluate the influence of these parameters on the growth process. To assess the influence of the oxide stoichiometry on thermal stability we performed annealing experiments with different oxide thicknesses. We observed a correlation with thickness: the thinner the layer, the more prone to local evaporation and holes formation, and vice-versa. At the same time, Ga collection was observed to be selective to the oxide layer openings where the bare Si(111) was exposed, meaning that Ga could not be stably collected on the oxide, but only in the holes. This confirmed that the holes generated in the oxide films by annealing are the only nucleation sites for Ga, and their formation is dependent on the chemical composition. **These insights may explain the dramatic change in nanowire density** observed at different oxide thicknesses: thin native oxides (<1nm) are less stoichiometric, consequently less thermodynamically stable and more prone to evaporate. Upon annealing, more holes are generated on the surface, collecting more Ga and nucleating more droplets than thicker oxides (>1nm), where less holes are formed.

Nevertheless, the increase of tilted nanowires observed between 1nm to 1.5nm was still not well understood. We therefore assumed that the different surface properties would influence the droplet positioning, and that the latter could determine the growth morphology and nanowire orientation. To verify such a hypothesis we approached the problem from a computational standpoint: we used a software (surface evolver [127]) to calculate the energy cost of allocating the Ga droplet in different positions, at different wetting properties (which corresponded to the different oxide thicknesses). Then, to be able to predict the droplet behavior, we assumed that the system would adopt the more energetically favorable configuration (i.e. the less costly). As a result we observed that, depending on the wetting properties of the surface, which were observed to change with oxide thickness, the droplet assumed different configurations at constant volume. More in detail, the model developed showed that the surface properties of a thicker oxide allowed different droplet configurations. The latter were demonstrated to lead to multiple growth morphologies, as observed experimentally. On the other hand, in the case of a thinner oxide (~1nm), the energy distinction between the different configurations was much larger, allowing only the ones that lead to vertical nanowire growth (as experimentally observed).

The outcome of this study was of having developed a model, which is capable of bringing new insights on all the different growth morphologies simply by taking into account the changes in surface properties observed at the different oxide thicknesses.

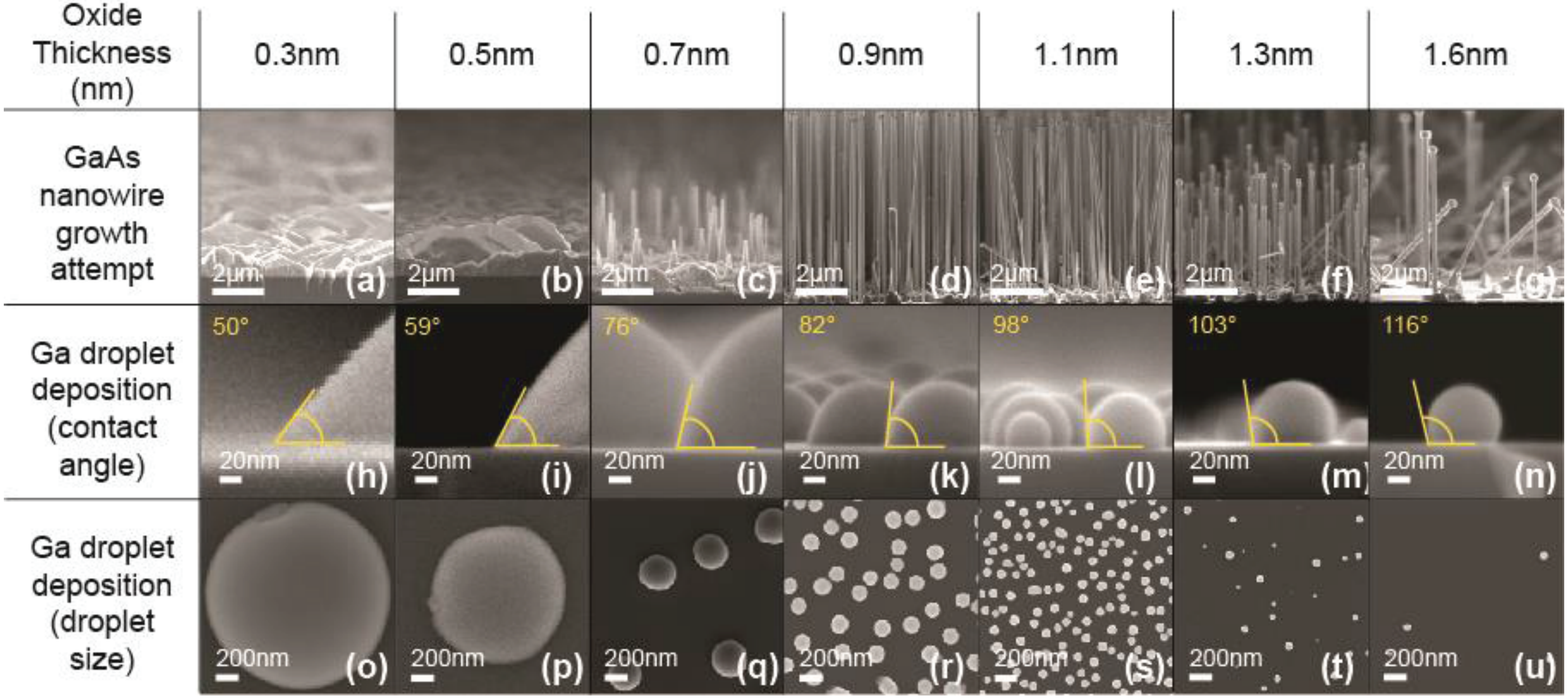

Figure 16 Graphic table of Scanning Electron Micrographs of: from (a) to (g) growth of self-catalyzed GaAs nanowires on Si (111) substrates coated with different oxide thicknesses. The growth conditions in terms of temperature, time and Ga and As fluxes were identical in all the experiments. From (h) to (n) the contact angle of the droplets (cross-section images), and (o) to (u) the dimensions (top-view images), formed by Ga deposition experiments are shown.

3.4 Papers Included in the chapter

I. **Ga-assisted growth of GaAs nanowires on silicon, comparison of surface SiO_x of different nature**
F. Matteini, G. Tütüncüoglu, D. Rüffer, E. Alarcón-Lladó and A. Fontcuberta i Morral
Journal of Crystal Growth 404 (2014) 246

II. **Wetting of Ga on SiOx and Its Impact on GaAs Nanowire Growth**
F. Matteini, G. Tütüncüoglu, H. Potts, F. Jabeen and A. Fontcuberta i Morral
Crystal Growth and Design 15 (2015) 3105

III. **Impact of the Ga droplet wetting and spilling pinholes on the orientation of GaAs nanowire growth**
F. Matteini, G. Tütüncüoglu, D. Mikulik, J. Vukajlovic-Plestina, H. Potts, J.-B. Leran, W. C. Carter and A. Fontcuberta i Morral
Submitted.

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Ga-assisted growth of GaAs nanowires on silicon, comparison of surface SiOx of different nature

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ABSTRACT

Physical properties of surfaces are extremely important for initiation and nucleation of crystal growth, including nanowires. In recent years, fluctuations in surface characteristics have often been related to unreproducible growth of GaAs nanowires on Si by the Ga-assisted method. We report on a systematic study of the occurrence of GaAs nanowire growth on silicon by the Ga-assisted method for different kinds of silicon oxides: native, thermal and hydrogen silsesquioxane (HSQ). We find that success in achieving nanowires and the growth conditions such as gallium rate and substrate temperature depend mainly on the physical properties of the surface: oxide stoichiometry, oxide thickness and surface roughness. These results constitute a step further towards the integration of GaAs technology on the Si platform.

1. Introduction

Semiconducting nanowires provide a wide range of possibilities both in applied and fundamental science [1–3]. Within the range of possible applications III–V semiconductors are among the most promising materials. The small footprint of nanowires allows for virtually defect-free integration of mismatched materials, which would not be possible in the thin film form [4,5]. Moreover, III–V nanowires can be obtained on Si [6–11], providing a path for combining the III–V and Si platforms. As nanowires start growing generally in a single nucleation event followed by a layer-by-layer mode, III–V nanowires grown on silicon appear also free from anti-phase boundaries otherwise often found in thin film counterparts [12–14]. Still, the lack of polarity of the silicon substrate leads to non-perpendicular growth nanowires grown on Si(111) due to the existence of three-dimensional twinning under certain growth conditions [13,15].

One of the most successful ways of growing nanowires is the vapor–liquid–solid method (VLS) in which a liquid droplet (denominated as catalyst) is used for the gathering and preferential decomposition of growth precursors [16,17]. Upon supersaturation of the droplet, precipitation occurs at the interface with the substrate in the form of a nanowire. One of the most successful catalysts used for VLS is gold. However, when heating a Si substrate with gold on top, the gold droplets incorporate a significant amount of silicon by the formation of an eutectic alloy. The presence of Si in the Au interferes with the decomposition and precipitation of precursors. As a consequence, growth of III–V nanowires on Si using gold as a catalyst is quite more challenging than on III–Vs. Many groups working on the growth of III–V nanowires on silicon have looked for alternative methods, including the selective area epitaxy and Ga-assisted growth of GaAs nanowires [6–8,13,18–21]. In the latter, it was found that the presence of an oxide at the surface was necessary for the formation of the liquid droplet necessary for VLS.

The physical characteristics of the silicon oxide have always been an important parameter in Ga-assisted nanowire growth [9–11]. It was observed that the oxide thickness plays a role in achieving nanowires with an epitaxial relation to the substrate [22]. Interestingly, the critical thicknesses reported by the various groups are significantly different depending on the preparation method of the oxide: 5 nm for Hydrogen Silsesquioxane (HSQ), 0.9–2 nm for thermal oxide and 30 nm for sputtered oxide [22,23]. In these works, the existence of a critical oxide thickness on a GaAs substrate was discussed in terms of the opening of craters in the oxide, either by the reaction of Ga with the substoichiometric oxide and/or due to the desorption of As at GaAs surface temperatures above 500 °C. Few works report on successful growth without the presence of an oxide on the silicon surface [24,7,10]. One should note that in all of these cases, there was a non-negligible time lapse between substrate preparation and loading in the ultra-high-vacuum environment. It is well established that

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Si surfaces naturally undergo oxidation even at room temperature, simply by exposing them to air. The same oxidation process takes place also in the case of hydrogen passivated surfaces [25–27]. As a consequence, what was claimed as oxide-free surface had most probably oxidized to Si +1 (i.e. Si–O–Si) as shown from X-Ray photoelectron spectroscopy data of refs [10,28].

Most of the works discussing the role of the oxide in the growth of GaAs nanowires by the Ga-assisted method were performed on GaAs substrates [22,7,9–11]. To the best of our knowledge, there are no reports on the role of oxide in Ga-assisted growth of GaAs nanowires on silicon. Different groups have used different types of surface preparation, but no systematic comparison between different types of oxide has been realized. Additionally, it is generally accepted that growth conditions for obtaining GaAs nanowires can strongly depend on the wafer batches and providers used, despite identical nominal properties. There is a clear need for finding out the physical origin of this in order to deduce a reproducible preparation method of the silicon surface. In this work, we address the following unanswered questions on the Ga-assisted growth of GaAs nanowires on silicon: is the presence of an oxide needed? What is the ideal oxide stoichiometry for reproducible growth? What is the ideal critical oxide thickness? Is it possible to relate the physical characteristics of the surface with the ideal growth conditions? For this, we analyze the physical characteristics of different types of oxides and relate them to the optimized GaAs nanowires growth conditions. This work constitutes a step towards systematic use of silicon as a substrate for Ga-assisted growth of GaAs nanowires and could be potentially extended to other materials systems.

2. Experimental details

GaAs nanowires have been grown by Ga-assisted self-catalyzed method on Si(111) 2-inch wafers RCA treated (ended with an HF etch) from different providers (Virginia and Siltronix, p-doped Boron, 10–20 Ω cm) from now on named Batch A and B respectively. The growth was performed in a Molecular Beam Epitaxy machine (MBE) with solid state sources (DCA P600). Previous to growth and in order to ensure a clean surface, all substrates were annealed at 500 °C in a separate UHV chamber for 2 h; from now on we will refer to this process as degassing. The effect of this step on oxide chemistry, thickness and roughness is reported in the Supplementary Information. All the values of roughness, thickness and chemistry characterization reported in the manuscript have been performed after degassing, unless differently specified. After this step, the samples were moved to the growth chamber, always in UHV.

The silicon substrates were prepared with different types of oxides: thermal, native and Hydrogen Silsesquioxane (HSQ). Thermal oxide was produced by means of dry oxidation of the wafer of batch B in a Centrotherm furnace at 950 °C in a cleanroom environment. The native oxide was obtained by natural exposure of the Si wafers (of batch A and B) to air in cleanroom environment (21 ± 0.5 °C, humidity 44%). HSQ oxide was obtained by spinning a HSQ:MIBK solution (XR-1541-002, Dow Corning) on wafers of batch B at 6000 rpm with subsequent annealing for 5 min at 180 °C for removal of the solvent. Without diluting the solution, the oxide thickness achieved was of 28–30 nm. By diluting it (1:4–1:8), thinner oxides were obtained (8–4 nm). The films were transformed into silicon oxide by annealing them at 475 °C in N_2 atmosphere for 1 h. The solutions were spun right after exposing the Si wafers to an HF solution, in order to avoid the presence of the native oxide. The oxide thickness was controllably reduced by chemical etching with a NH_4F:HF (500:1) solution. The etching rate was calibrated independently for every type of oxide used. The oxide thickness was measured with spectroscopic ellipsometry (Sopra GES 5E) and confirmed by Atomic Force Microscopy (AFM) on etched steps. Each thickness value obtained by ellipsometry is the result of the average of five measurements in different points on the wafer. Attenuated total reflection (ATR) IR spectroscopy (Jasco FT/IR 6300 with Pike MIRacle holder with single reflection diamond crystal) was realized for the characterization of the oxide stoichiometry, by scanning in the 650–4000 cm^{-1} range with 100 accumulations. Although, since the intensity of the signal-to-noise ratio above 1500 cm^{-1} is extremely low, only the low range (650–1500 cm^{-1}) is considered and reported. Each ATR-FTIR measurement was repeated 3 times on each sample in different points. Finally, AFM (Bruker) was also used for the determination of the surface roughness: each surface roughness value is the result of the average of three measurements of 5 × 5 μm, 1 × 1 μm and 500 × 500 nm areas. It is important to remark that the reported values of roughness have been measured after the degassing. The roughness before degassing are reported in the Supplementary Information. In the case of completely etched oxides, the substrates were immersed in an isopropanol bath immediately after etching, and then dried under Nitrogen flow just before loading in the UHV environment. We used the following range of growth conditions:

- the substrate temperature between 580 °C and 660 °C, as measured by means of a calibrated pyrometer;
- Ga rates between 0.25 A/s and 1.25 A/s, as calibrated on planar growth on GaAs (111) by means of Reflection High Energy Electron Diffraction (RHEED);
- As_4 fluxes were from 2.5×10^{-6} torr to 4.9×10^{-6} torr; as calibrated by means of a beam flux monitor gauge.

Scanning Electron Microscopy (SEM) (Zeiss Merlin) was used for the morphological characterization of the samples.

3. Experimental results

3.1. *Chemical composition of the oxides*

We start by presenting the nature of the various oxides used in this work. Thermal oxide is a mostly stoichiometric oxide (SiO_2), which can be produced by oxidation of Silicon at 800–1200 °C under a controlled oxygen flux; it exhibits low as-grown roughness ($\sim > 0.6$ nm) [34].

Native oxide is a thin layer of oxide formed by the natural exposure of a Si wafer to air; it follows the surface roughness of the underlying silicon substrate and it grows monolayer by monolayer [25,35,27]. The chemical composition of native oxide depends on its thickness. For thicknesses of few monolayers, it mainly consists of Si–O–Si [36]. The oxygen content increases for larger thicknesses, though it remains sub-stoichiometric with respect to thermal oxide.

HSQ oxide is obtained by annealing a Hydrogen Silsesquioxane resin on a silicon wafer previously etched with HF. The thickness can be tuned by the dilution of the resin solution and the spinning rate [37,38]. Annealing the HSQ resin at 450 °C transforms the cage structure of HSQ monomer into a network, whose chemical composition is SiO_x with $1 < x < 2$, depending on the annealing temperature [37,38].

By investigating these three types of oxides, we can understand the influence of the stoichiometry in the nucleation and growth mechanism of GaAs nanowires. The stoichiometry of silicon oxide can be characterized with Fourier Transform Infrared Spectroscopy (FTIR). The main absorption bands characteristic of silicon oxide are the interstitial oxygen band (Si–O–Si), centered at 1107 cm^{-1}, [29,31,32] the transverse optical phonon (TO) of SiO_2 around 1075 cm^{-1} [33], as well as the longitudinal optical phonon (LO) around 1250 cm^{-1} [33], as reported in Table 1. Suboxides of the form SiO_x with $1 \leq x < 2$ are characterized by an absorption band downshifted and broadened with respect to the TO SiO_2. The shift can be directly related to the stoichiometry [33]. Examples of ATR-FTIR spectra obtained from the different oxides are shown in Fig. 1.

In Fig. 1 the Si–O–Si absorption band is observed for all the oxides (thermal, native and HSQ), albeit with different intensities. The spectra at higher wavenumbers depend on the oxide type:

- Thermal oxide shows a clear LO-SiO_2 positioned at 1250 cm^{-1}, indicating it being stoichiometric oxide.
- HSQ oxide shows an absorption band (1226 cm^{-1}), indicating that it is substoichiometric oxide SiO_x with $(1 \leq x < 2)$ [33].
- Native oxide does not show any additional absorption band than the already described Si-O-Si related, consistently with reported results on films of similar thickness [29].

Table 1
Characteristic phononic modes of silicon oxide.

Phononic mode	Position (cm^{-1})	Ref.
Si–O–Si	1107	[29–32]
TO SiO_2	1075	[33]
LO SiO_2	1250	[33]

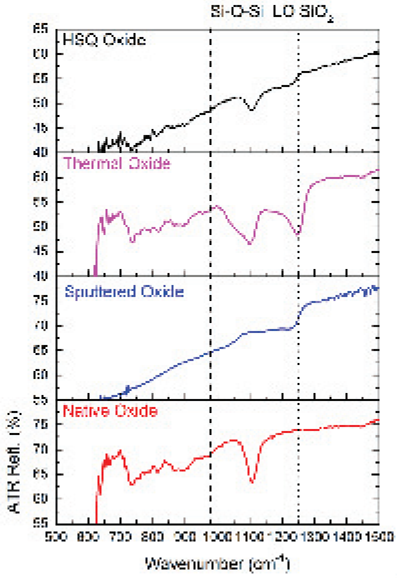

Fig. 1. ATR FTIR spectroscopy of different oxides. The peak at 1250 cm^{-1} corresponds to the LO mode of SiO_2, whereas the peak at 1107 cm^{-1} is related to the presence of interstitial oxide Si–O–Si. The TO mode of SiO_2 is located around 1075 cm^{-1}. Thermal oxide is the only oxide that shows TO and LO modes of SiO_2. HSQ presents a downshifted broad peak around 1225 cm^{-1} correspondent to non-stoichiometric oxide SiO_x with $x < 2$. All the oxides show the interstitial oxide peak (1107 cm^{-1}) but not the sputtered oxide on GaAs; this proves that Si–O–Si is peculiar of Si/SiO_2-interface. A similar result was obtained with HSQ oxide on GaAs substrate (see Supplementary Information).

In order to demonstrate that the interstitial oxide is characteristic only of the interface between the silicon and the silicon oxide, the spectra of sputtered oxide on GaAs is also shown (see Fig. 1); the same result has been achieved with HSQ on GaAs (see Supplementary Information). No absorption band is observed at 1107 cm^{-1}, showing that no interstitial oxide is present. On the other hand a broad absorption is observed around 1226 cm^{-1}, characteristic of sub-stoichiometric oxide. As a remark, interstitial oxide is present in every type of oxides on silicon since it represent the initial step of oxidation of every silicon surface, being followed by oxide of different composition, depending on the processing [27]. In the following, FTIR spectrum of Si substrate is used as a tool to investigate the physical properties that influence the early stages of growth of self-catalyzed GaAs nanowires.

3.2. Thermal oxide

We first present our results on thermally oxidized silicon substrates. As introduced earlier in this manuscript, three physical properties of the substrates will be considered: thickness, roughness and chemical composition. First we investigate substrates with four different thicknesses of the same oxide, by a combination of optical lithography and etching (see supplementary information). This allowed us to investigate simultaneously several oxide thicknesses under identical experimental conditions.

Fig. 2 shows SEM micrographs of oxidized substrates with varying oxide thicknesses after performing the same growth process. The growth conditions were substrate temperature $T = 600$ °C, Gallium rate Ga = 1.25 Å/s and Arsenic beam flux pressure $As = 2.5 \times 10^{-6}$ torr. Under these conditions nanowire growth was observed only for an oxide thickness between 1 and 2 nm (Fig. 2(c)). Similar thickness selectivity results were obtained under other conditions (T=590–630 °C, Gallium rate 0.5–1.25 Å/s) leading to nanowire growth. In the case of thicker oxides, Ga droplets were always observed on the surface (see Fig. 2(a) and (b)). Oppositely, for oxide-free silicon surfaces, textured two-dimensional growth was found (see Fig. 2(d)). Such a change in growth mechanism could be related to the difference in surface energy of the SiO_2 compared to the bare Si and thereby influence the initial Ga droplet formation and pinning on the surface. The question here is what makes 1–2 nm thermal oxide so prone for Ga-assisted nanowire growth. In order to shed some light to this question, we show the ATR-FTIR spectra of the thermal oxide of different thickness (see Fig. 2 (e)), with comparable pre-degassing roughness (~0.3 nm). It is interesting to note that the intensity of the LO SiO_2 is proportional to the thickness, while the Si–O–Si mode exhibits the identical amplitude for all. This corroborates the interface nature of Si–O–Si. Moreover, when the oxide thickness is around 1–2 nm, roughness was comparable to thickness (see Table 2) and only the Si–O–Si band is observed. These results are in good agreement with the results obtained by Muller et al. [34]: stoichiometric silicon dioxide is formed only for thicknesses higher than 2 nm.

3.3. Native oxide

From our study on thermal oxide we understand that when roughness is comparable to thickness, nanowire growth can be achieved. In other words, this condition corresponds to the exposure of Si/SiO_2-interface (i.e. Si–O–Si) Based on the thermal oxide results, we also speculate that the substoichiometric composition of the oxide might help in the achievement of nanowire growth. As described in the first section, native oxide appears naturally upon exposing silicon wafers to air. This would supposedly make native oxide a reliable candidate. Still, one observes an extreme variation within batches and providers on the success in nanowire growth, which to date is not understood. In order to

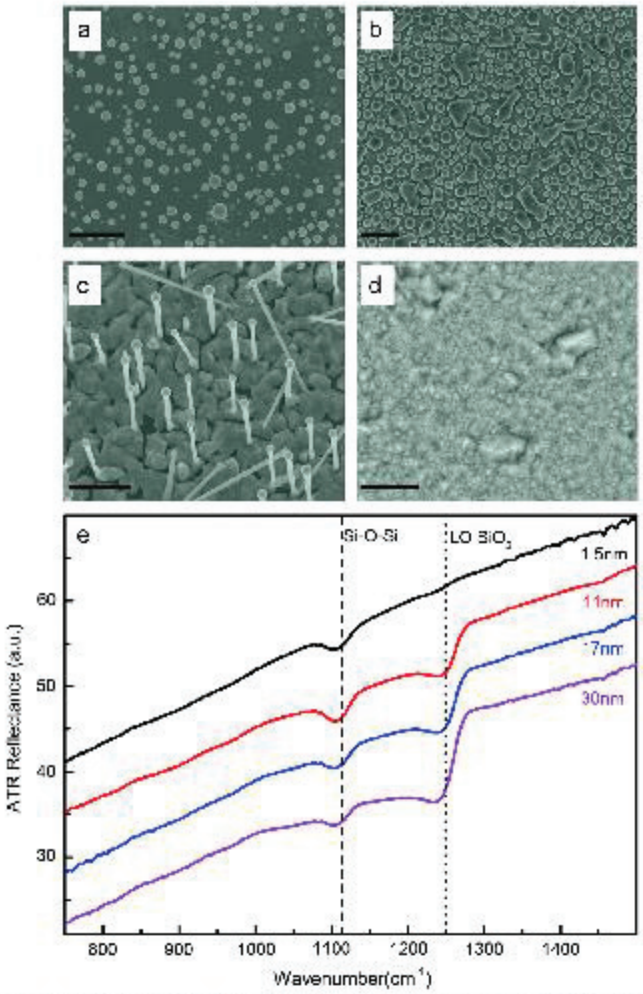

Fig. 2. Growth of GaAs nanowires on Si (111) substrates covered by thermal oxide. The same substrate has been etched with NH_4F:HF (500:1). SEM micrographs of GaAs nanowires growth attempt on (a) 24 nm, (b) 10 nm and (c) 1.5 nm thick thermal oxide. In (d) growth without oxide is reported. Growth has been performed simultaneously for all the different oxide thicknesses. In (e) ATR-FTIR spectra of thermal oxides with different thicknesses and comparable roughness pre-degassing (~0.3 nm) are reported. By decreasing the oxide thickness the LO–SiO$_2$ is decreasing in intensity, whereas the Si–O–Si remain unchanged. The scale-bar corresponds to 1 μm.

Table 2
Thickness and roughness of different types of oxides after degassing. The measurements have been performed by ellipsometry.

Oxide type	Annealing (°C)	Thickness (nm)	Roughness RMS (nm)
Native oxide (Batch A)	500	0.8 ± 0.6	0.5 ± 0.5
Native oxide (Batch B)	500	2.1 ± 0.6	5.3 ± 0.5
Thermal oxide	500	1.2 ± 0.6	1.3 ± 0.5
HSQ etched	300	8.8 ± 0.9	3.1 ± 0.5
HSQ as spun	300	8.1 ± 0.6	1.2 ± 0.5

demonstrate that this variability is not a provider issue, we take a closer look at the physical properties of the native oxide of substrates coming from different providers that, despite having identical specifications, gave rise to different growths. One should note that the characteristics may not be specific of a certain company and may vary from batch to batch. As a first observation we find that at comparable roughness pre-degassing (0.3–0.8 nm, see supplementary information) the oxide is slightly thicker in the case of batch B than batch A (see Table 2). Secondly, the ATR-FTIR spectra (Fig. 3 (a)) show that the intensity of the Si–O–Si peak is much higher for Batch B wafers, pointing out a rougher Si/SiO$_2$-interface. This is in accordance with the post degassing roughness measurements (see Table 2). Finally, we show the SEM micrographs of the growth performed on the two type of substrates (see Fig. 3 (b) and (c)). The two growths were performed under identical conditions (T=610 °C, Ga=0.27 A/s, As=2.5 × 10^{-6} torr). However, while a forest of nanowires is obtained on batch B wafers

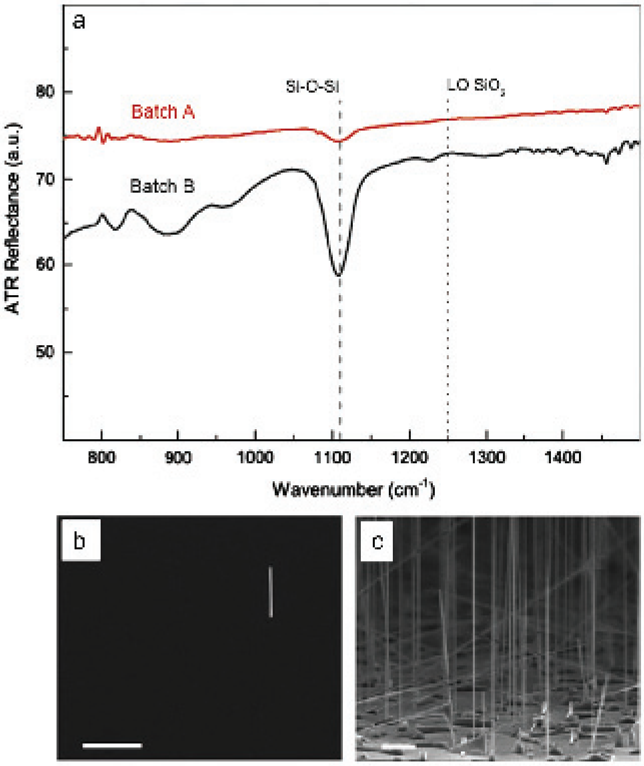

Fig. 3. Native oxide grown on wafers of different providers (batch A and B) with same doping concentration and same surface treatment (see Section 2). In (a) the ATR-FTIR spectra of batch A and B native oxides are shown. Batch B shows stronger absorption band of Si–O–Si compared to batch A, at higher thickness (see Table 2) and comparable roughness (0.3–0.8 nm, see Supplementary Information). Growth has been performed with same process parameters (T=610 °C, Ga=0.27 A/s, As=2.5 × 10^{-6} torr), and in the case of Batch A extremely low nanowire density (< 10^6 cm^{-2}) was achieved (b), whereas in the case of batch B higher nanowire density (~1.5 × 10^7 cm^{-2}) was achieved (c). The scale-bar corresponds to 2 μm.

(roughest surface), an extremely low density of nanowires is observed on the batch A (smoothest surface). The different nanowire density can be understood in terms of changes in surface diffusion: a lower roughness results in an augmented surface diffusion, that lead to a lower nanowire density [39]. Vice versa, a rougher substrate (i.e. batch B) leads to a higher nanowire density, as shown in Fig. 3 (c). In a nutshell, the Si/SiO$_2$-interface seems to be a key parameter in the GaAs nanowire growth on Si. Further studies should involve the intentional modification of this roughness for engineering the nanowire density in a reproducible manner.

3.4. *HSQ oxide*

So far we have evaluated the growth on SiO$_2$ and interstitial oxide (Si–O–Si) exposed to the surface. Now we want to evaluate the possibility of growth on an oxide with intermediate composition. For this purpose we used silicon substrates covered with silicon oxide from HSQ processing. Further information about the processing of HSQ can be found in the Supplementary Information. Analogously to the thermal oxide investigation, several growths were performed simultaneously on oxide thicknesses ranging from 2 nm up to 24 nm. Representative SEM images of samples grown under at a substrate temperature of 595 °C, Ga rate of 1.1 A/s and As flux of 2.5 × 10^{-6} torr are reported in Fig. 4. As the SEM micrographs show, growth of vertical nanowires was only achieved for thin oxide layers (< 5–6 nm). This value is higher than in the case of thermal oxide, and comparable to what has been reported for HSQ on GaAs substrates [40]. Similar to what was observed for thermal oxide, the Si–O–Si band is the most dominant feature in the FTIR spectra of HSQ oxide of around the critical thickness and below. We note that the IR spectrum of 4 nm thick HSQ presents a non-negligible SiO$_x$-related absorption band.

For this reason we performed the following experiment; we prepared two substrates with the same HSQ oxide thickness, achieved by

- Spinning HSQ from a MIBK diluted solution (1:8) to form directly a film with a thickness of 4–5 nm. This type of sample will be called "as spun".
- Spinning HSQ from non-diluted solution, and etched it down to a similar thickness. In the following, this type of sample will be called "etched".

The IR spectra are virtually identical (see Fig. 5 (a)), indicating the same composition of Si–O–Si and SiO$_x$. Interestingly, successful

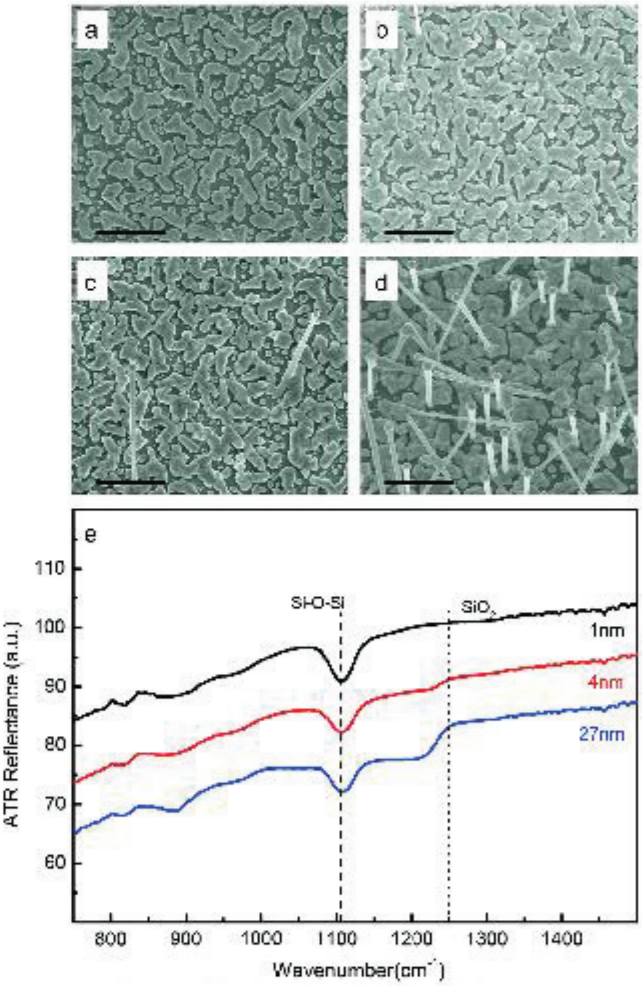

Fig. 4. Growth of GaAs nanowires on Si(111) substrates covered with HSQ oxide. Thickness was controlled by etching down the oxide with NH_4F:HF diluted 500:1. In (a)-(b)-(c) and (d) the SEM micrographs show the growth attempts on respectively 19-15-8 and 5 nm oxide thicknesses. Only in the latter case growth was performed successfully; the growth conditions were substrate temperature 595 °C, Ga rate of 1.1 Å/s and As flux of 2.5×10^{-6} torr. (e) ATR-FTIR spectra of HSQ oxides with different thicknesses: the absorption band of SiO_x decreases in intensity by decreasing oxide thickness. On the other hand the absorption band of Si–O–Si does not decrease in intensity, showing that it is related to the Si/SiO_2-interface. The scale-bar corresponds to 2 μm.

growth had been achieved only in the case of etched HSQ (see Fig. 5). Even though the substrates seemed to be identical, the AFM analysis revealed a difference in surface roughness (see Table 2). In the case of low roughness (as spun) only Ga droplets were obtained, whereas for roughness of the order of the oxide thickness (etched), vertical nanowires were observed. We believe that, as schematically depicted in inset of Fig. 5, the Ga droplet cannot reach the Si/SiO_2-interface and no growth is observed in the case of a smooth and compact oxide layer. On the other hand, for large surface roughness (i.e. comparable to thickness), the Si/SiO_2-interface can be exposed to the precursors, allowing vertical nanowire growth.

4. Discussion

We discuss now the results in views of generalizing our findings for nanowire growth. We first review the impact of stoichiometry and roughness of the oxide on nanowire growth. We have varied the composition of the silicon oxide SiO_x with x ranging from 0 to 2. For simplicity's sake, we start considering growth on the two extreme cases: stoichiometric SiO_2 ($x=2$), namely thermal oxide thicker than 2 nm, and oxide-free silicon ($x=0$), see for example Fig. 2. In both cases it was not possible to obtain GaAs nanowire growth in any of the conditions used. Instead, we observe a droplet-like deposit on the SiO_2, while a

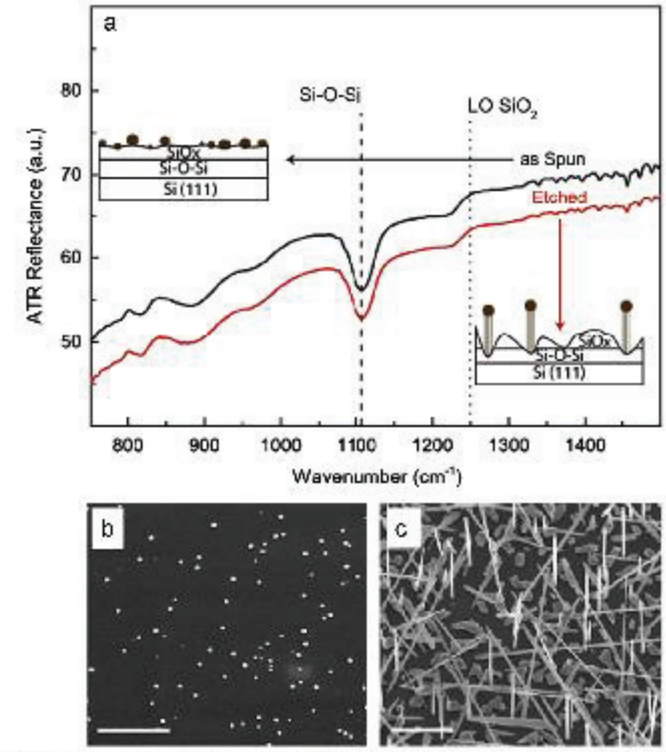

Fig. 5. (a) ATR-FTIR spectra of HSQ oxides with identical thickness but different preparation method: the as spun was prepared by direct dilution, whereas the etched was prepared by a more concentrated solution and then etched down. In (b) and (c) the SEM micrographs report the growth attempts on respectively the as spun and etched HSQ. Nanowires growth was successful only in the case of the etched HSQ. The insets in (a) show the proposed mechanisms for etched and as spun HSQ: the latter present a lower roughness compared to the etched HSQ (see Table 2), that did not allow Si/SiO$_2$–interface exposure to the surface, leading to no nanowire growth. Differently, successful growth was achieved for the etched HSQ since the roughness allowed Si/SiO$_2$–interface exposure to the surface (see Table 2). The scale-bar corresponds to 2 μm.

polycrystalline growth is observed in the oxide-free surface. The droplet-like deposit suggests that the diffusion coefficient of Ga-adatoms on the oxide is higher than on the silicon surface. It is interesting to note that in the case of growth on Si substrates covered with oxide thickness comparable to roughness, nanowires were always obtained. This condition suggests a nucleation model based on the formation of a pin-hole that provides the epitaxial relation with the substrate, coherently with what reported from other researchers [41,22]. The conditions of roughness comparable to thickness that allow the pin-hole formation, necessary to achieve nanowire growth can be obtained in various manners: thermal oxide thinner than 2 nm, HSQ etched thinner than 4–5 nm and native oxide. A clear proof of the importance of roughness vs thickness is shown in Fig. 5 (b) and (c), where two substrates were prepared with HSQ with identical thickness and composition, but different roughness. We have also seen that the roughness/thickness conditions that lead to successful growth seems to be correlated to Si/SiO$_2$-interface (i.e. Si–O–Si), as shown in Fig. 6. The recurrent observation of such an interface layer has been described in other works, where though successful growth of GaAs nanowires on patterned silicon dioxide is not related to the presence of interstitial oxide at the SiO$_2$ hole opening [42–44]. However the role of Si/SiO$_2$-interface in the growth mechanism is still not fully understood and requires further investigation.

In parallel, we explored growth on smooth surfaces (batch A substrates) to understand if nanowire density could be controlled by the "processing parameters", as Ga rate or substrate temperature. We varied both Ga rate and substrate temperature respectively from 0.3 A/s to 1.1 A/s, and from 600 °C to 660 °C, as shown in Fig. 6. At low Ga flux and substrate temperatures ((a) and (b)) extremely low density of vertical nanowires is observed, as already reported in Fig. 3. On the other hand the higher the Ga flux ((c)-(e)-(g)), the more material is deposited on the surface, resulting in an increased nanowire density and polycrystalline parasitic islands density. By increasing temperature, the polycrystalline parasitic layer decreases ((g)-(h)-(i)). Coherently with what mentioned before, the diffusion length of Ga atoms augment with increasing temperature, decreasing the polycrystalline islands density.

In order to generalize these results, we have correlated the surface characteristics with the conditions needed to achieve growth with comparable density number of vertical nanowires ($(1.5 \pm 0.5) \times 10^7$ cm^{-2}). Fig. 7 depicts the general conditions for obtaining comparable nanowire density as a function of surface roughness and Si–O–Si content. In general, a lower surface roughness requires higher substrate temperature and Ga rate to achieve

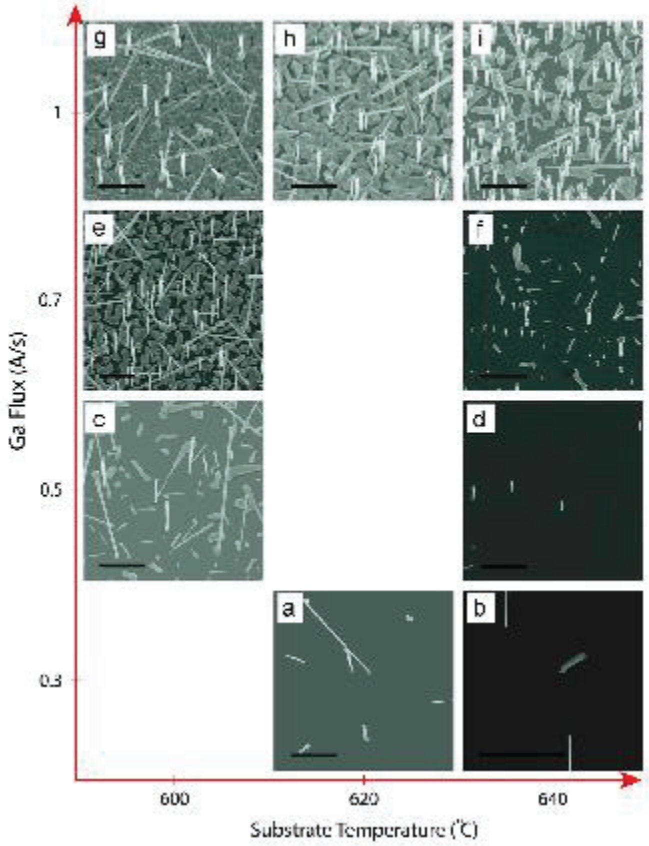

Fig. 6. SEM micrographs of GaAs nanowires grown on batch A wafers covered with native oxide. The as flux used in all the growths shown is constant at 2.5×10^{-6} torr. By moving from bottom to top Ga rate increases, whereas from left to right the substrate temperature increases. At low Ga rate and substrate temperatures (a) and (b) low material depodition is observed. On the other hand the higher the Ga rate (c)–(e)–(g), the more material is deposited on the surface, increasing at the same time nanowire density and polycrystalline island density. If also temperature is increased, the density of vertical nanowire strongly increases (g)–(h)–(i), decreasing polycrystalline island density. Growth at temperature above 640 °C was also attempted, but no growth was observed anymore. The scale-bar corresponds to 2 μm.

comparable nanowire density. As an example, in the case of batch A Si wafers (smoothest surface), the conditions to achieve the desired nanowire density were of Ga=0.75 A/s and T_{sub}=640 °C.

Thermal oxide presented the second lowest surface roughness: the desired nanowire density was achieved with Ga=0.75 A/s and T_{sub}=625 °C. The trend is followed by HSQ for which the conditions for the desired nanowire density were Ga=0.45 A/s and T_{sub}=610 °C. In the case of the highest surface roughness, a comparable nanowire density was achieved at Ga=0.27 A/s and T_{sub}=610 °C.

We explain the change in Ga rate conditions for creating comparable nanowire density with surface diffusion: a decrease in roughness produce an increase in surface diffusion, forming less nanowires [39]. Therefore, to increase nanowire density for lower roughness substrates (i.e. native oxide batch A) Ga rate and substrate temperature have to be increased compared to rougher substrate (i.e. native oxide batch B).

As shown in Fig. 7, roughness and interstitial oxide content are directly correlated, suggesting that the sharpness of the Si/SiO_2-interface affects the characteristic roughness for the bottom up oxides (i.e. thermal oxide and native oxide). Presently, how to achieve control over interstitial oxide formation remains still open and it needs further investigation.

5. Conclusions

In conclusion, we have shown that roughness is a key parameter for forming pinholes necessary for successful GaAs nanowire growth. This explains the different optimal oxide thicknesses to achieve growth reported in literature: the critical oxide thickness depends on the surface roughness as it is related to the thickness leaving Si/SiO_2-interface exposed to the surface. For example, we found a critical thickness of 1–2 nm for thermal and native oxide, 5–6 nm for oxide from HSQ. The lower the roughness, the higher the temperature and the Ga rate needed for achieving the comparable nanowire density, and vice versa. Additionally, we have also shown that the "provider dependence"

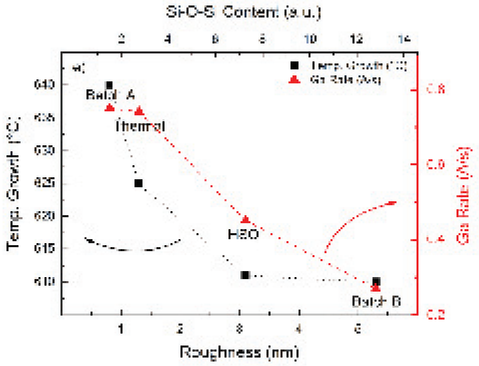

Fig. 7. The relation between optimal growth conditions (substrate temperature and Ga rate) at comparable density number of vertical nanowires ((1.5 ± 0.5)× 10^{8} cm^{-2}) with surface roughness and interstitial oxide content is shown. The higher the Si–O–Si content, the rougher the Si/SiO$_2$-interface. To achieve comparable nanowire density lower roughness lead to higher substrate temperature and Ga rate, and vice versa.

on growth conditions has physical reason, and it is related to the interface roughness of the substrates, that seems to be correlated to Si/SiO$_2$-interface. Still, to clarify the latter point further investigation is needed. Systematic AFM and FTIR on the received substrates might help in determining the conditions to achieve the desired nanowire density. This work opens new perspectives for the reproducible integration of GaAs nanowires on silicon.

Acknowledgments

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Appendix A. Supplementary data

Supplementary data associated with this article can be found in the online version at http://dx.doi.org/10.1016/j.jcrysgro.2014.07.034.

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Wetting of Ga on SiO_x and Its Impact on GaAs Nanowire Growth

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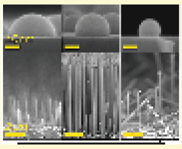
Supporting Information

ABSTRACT: Ga-assisted growth of GaAs nanowires on silicon provides a path for integrating high-purity III−Vs on silicon. The nature of the oxide on the silicon surface has been shown to impact the overall possibility of nanowire growth and their orientation with the substrate. In this work, we show that not only the exact thickness, but also the nature of the native oxide determines the feasibility of nanowire growth. During the course of formation of the native oxide, the surface energy varies and results in a different contact angle of Ga droplets. We find that, only for a contact angle around 90° (i.e., oxide thickness ~0.9 nm), nanowires grow perpendicularly to the silicon substrate. This native oxide engineering is the first step toward controlling the self-assembly process, determining mainly the nanowire density and orientation.



Semiconductor nanowires bring a wide range of new concepts for next generation optoelectronic and electronic technologies, as well as new platforms for fundamental science.[1−7] Among all the III/V semiconductors that can be used to form these structures, GaAs and InP are among the most promising for photovoltaic applications due to its ideal bandgap.[8,9] However, GaAs is technologically more relevant due to the wider availability of Ga in the Earth's crust with respect to In. Moreover, GaAs nanowire solar cells can also be obtained on silicon platforms, creating the possibility of a double junction.[10] Still (to date), no device with GaAs nanowires is commercially available. For several reasons, the fabrication challenges could be invoked. The most common mechanism used for the formation of nanowires is the so-called vapor liquid solid (VLS).[11] This technique requires a liquid droplet, often called a catalyst, which decomposes and/or preferentially gathers the growth precursors in vapor phase. Upon supersaturation of the liquid, a solid phase precipitates underneath. Au is the most widely used metal to induce VLS. Several studies show that Au atoms can get incorporated in the body of the nanowire and on the silicon substrate.[12−15] To circumvent the use of gold for nanowire growth, several groups have studied self-catalyzed or catalyst-free growth of nanowires on silicon.[16−23] Detailed understanding of this particular growth mechanism has led to a better control of the nanowire morphology and crystal phase.[18,19,24−30] However, to date, full control over nanowire orientation was observed to be dependent on the wafer batch.[31,32] Most studies focus on the comprehension of the growth at the steady state. To the best of our knowledge, very little work has targeted the understanding of the initial steps of growth. This phase is key in the heterogeneous integration of III−Vs on silicon as it influences all the subsequent stages.[19,33] In the present work we investigate the influence of the surface properties of the native silicon oxide on the initial growth stages of self-catalyzed GaAs nanowires obtained by molecular beam epitaxy (MBE). In particular, we show how the native oxide thickness is strictly related to nanowire orientation with respect to the substrate, and which conditions are needed to achieve only vertical growth.

We start by describing the preparation of the substrates. We use 2 in. Si(111) wafers with a nominal resistivity of 10−20-Ω*cm. The doping of the wafer only determines the kinetics of oxide formation. All wafers were initially immersed in a BHF solution (7:1) for 2 min to remove the native oxide, and subsequently exposed to air in a controlled cleanroom environment (21 ± 0.5 °C, 44% humidity) for a determined time. The native oxide thickness was monitored with a Sopra GES 5E spectroscopic ellipsometer. The thickness obtained by ellipsometry has been confirmed by AFM measurements on oxide steps (see SI). The temporal evolution of the native oxide thickness after the HF etching is shown in Figure 1a. The native oxide regrows at the fastest pace after the immediate removal of the native oxide. Within a week, a thickness of ~0.8 nm is achieved. After this initial period, the oxidation slows down, reaching a final thickness of ~1.5 nm in a much longer time frame, e.g., 20 weeks, as observed earlier in previous studies.[34,35]

After preparing the substrates with a native oxide of particular thickness, we introduce them in the ultra-high-vacuum environment of our MBE machine (DCA P600). For the sake of removing any remnant water or organic residues from the surface, the substrates undergo several degassing steps. First, a halogen lamp degasses the substrates and substrate holder at ~150 °C for 2 h in the MBE load-lock (between 10^{-6} and 10^{-8} Torr). After this, the wafers are heated to ~500 °C in a separate chamber for 2 h at a pressure ~10^{-10} Torr. A third and last degassing is performed in the growth chamber directly prior to growth at 750 °C for 20 min.

We compare the growth for different thicknesses of the native oxide (from 0 to 1.5 nm). All growth was performed

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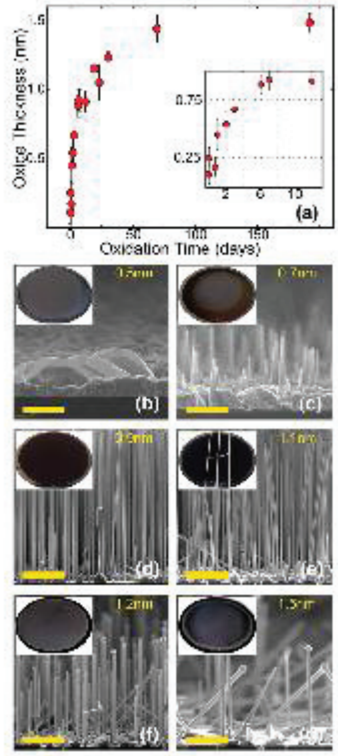

Figure 1. (a) Evolution of the thickness of native oxide as a function of time, as measured by ellipsometry. The inset shows the growth of the native oxide thickness in a smaller time frame (up to 12 days). (b−g) Optical images of the wafers after GaAs growth on the 2 in. wafers and corresponding SEM micrographs of the growth performed at the oxide thicknesses of 0.5, 0.7, 0.9, 1.1, 1.2, and 1.5 nm, respectively. The scale bar is 1 μm.

under identical conditions, which corresponds to a standard for Ga-assisted growth of GaAs nanowires: 640 °C substrate temperature, a Ga rate of 1.1 Å/s, As flux of 2.5×10^{-6} Torr, and growth time of 1 h.[32] Optical and scanning electron microscopy images (SEM) of the samples after growth are shown in Figure 1b−g. For thicknesses of ~0.5 nm or less, no nanowires are observed. In this case, only polycrystalline GaAs growth is observed (see Figure 1b). At an oxide thickness of around ~0.7 nm, elongated vertical structures start to form on the polycrystalline layer. Interestingly, these short nanowires mostly exhibit a perpendicular relation with the substrate surface and do not exhibit a droplet at their tip (see Figure 1c). This represents the transition from 2D growth toward Ga-assisted GaAs nanowire growth, which is achieved for oxides thicker than ~0.9 nm (see Figure 1d). As can be observed in the optical micrographs, the appearance of the samples is homogeneous over the 2 in. wafer. SEM investigations confirm that this is the case. For a native oxide thickness of 0.9 nm only vertical nanowires are observed. Growths performed at oxide thicknesses of 1.1, 1.2, and 1.5 nm present nanowires across the full 2″ wafer (see, respectively, Figure 1d−f). By increasing the native oxide thickness, we observe a progressive increase of nonvertical orientations, a broadening of length and diameter distributions, as well as a decrease of nanowire density.

A more detailed analysis of the nanowire morphology is given in Figure 2: in (a−d) tilted views of the nanowire forests grown on, respectively, 0.9, 1.1, 1.2, and 1.5 nm oxide thickness show a clear decrease in nanowire density and an increase of tilted wires for thicker oxides. The droplets will be discussed in the next paragraph. Quantitatively we observe that the nanowire density drops by 2 orders of magnitude (from 2.6×10^8 to $4.7 \times 10^6 \text{cm}^{-2}$), while the nanowire diameter increases from 90 to 180 nm, as the oxide thickness increases from 0.9 to

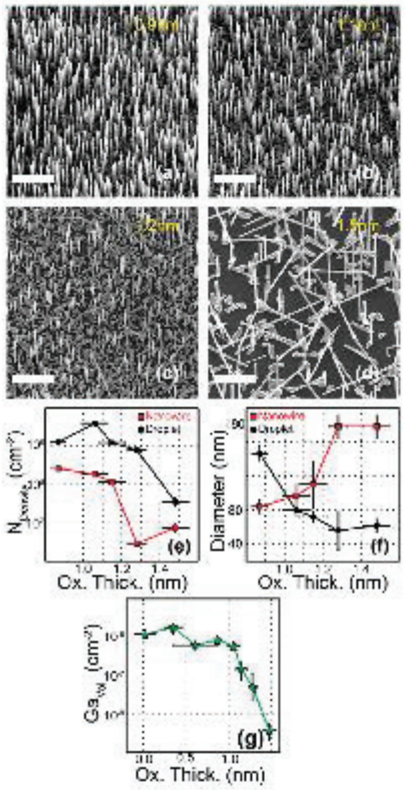

Figure 2. (a−d) SEM micrographs of GaAs nanowires grown on, respectively, 0.9, 1.1, 1.2, and 1.5 nm native oxide on Si (111) substrates. The scalebar is 3 μm. In (e) the density change of nanowires and Ga droplets at increasing oxide thickness is quantified: in both cases the decrease in density is 2 orders of magnitude, although the droplet density is 1 order of magnitude higher: nanowire density goes from $(2.6 \pm 0.03) \times 10^8$ to $(4.7 \pm 0.4) \times 10^6$ cm^{-2}, whereas droplet density goes from $(4.0 \pm 0.23) \times 10^9$ to $(3.6 \pm 1.0) \times 10^7$ cm^{-2}. In (f) the diameter evolution for nanowires and droplets at different oxide thicknesses is represented. Nanowire diameter rises by ~100 nm (from 84 ± 8 to 186 ± 12 nm), at increasing oxide thickness, whereas the droplet diameter diminishes (from 145 ± 9 to 62 ± 8 nm). In (g) the volume of Ga on the Si substrates after deposition as a function of oxide thickness is represented.

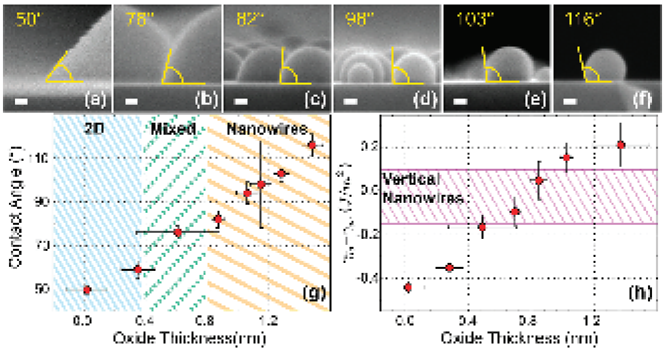

Figure 3. SEM micrographs of the wetting of the Ga droplets formed by Ga deposition at 640 °C for 5 min on oxide thicknesses of 0.1 (a), 0.6 (b), 0.9 (c), 1.1 (d), 1.3 (e), and 1.5 nm (f). The scale bar is 20 nm. In (g) the increase of the contact angle at increased oxide thicknesses is represented. The progress of the contact angle is correlated to the evolution from 2D growth, to mixed 2D-elongated structures without droplets, to nanowire growth. In (h) the surface energy of the different native oxide thicknesses calculated by Young's equation is shown. The range of surface energy at which only vertical nanowire growth was achieved is marked in purple.

1.5 nm. Nanowire populations of >100 were considered for the statistical study.

In order to explain our observations we looked at the initial stage of growth, namely, the formation of the Ga droplets. For this, we deposited Ga for 5 min at the growth temperature. Immediately after the deposition the substrate was cooled down to room temperature for observation. Representative SEM images of the sample surface are shown in the SI. The Ga droplet density and size vary dramatically as a function of the thickness of the native oxide. At ~0.1 nm of oxide thickness, droplets of diameter above 2 μm are found, while at increasing oxide thicknesses up to 1.5 nm, the droplet diameter progressively shrinks, down to ~60 nm (see SI).

In Figure 2e,f, the density and diameter of the Ga droplets are compared to the diameter and density of nanowires for oxide thicknesses above 0.8 nm. Ga droplet and nanowire density follow a similar trend. They decrease slightly for oxide thicknesses between 0.8 and 1.1 nm to strongly decrease at higher thickness. Still, there is an order of magnitude difference between the droplet and nanowire density. Unexpectedly, nanowire and droplet diameters evolve in opposite directions: nanowire diameter increases at raising oxide thickness, whereas droplet diameter obtained at a fixed time shrinks. To better understand these counterintuitive results we measured the time required for nanowire growth to start, for different oxide thicknesses. For the sake of simplicity, we will call this time the "incubation time". We monitored the substrate surface by reflection high energy electron diffraction (RHEED) and measured the time lapse until the diffraction peaks of crystalline GaAs nanowires appeared. For oxide thicknesses of 0.9 nm the incubation time was below 10 s, whereas at 1.3 nm it increased up to ~5 min (see SI). The fact that nanowires start to grow at an earlier time for thinner oxides could explain the smaller nanowire diameter (~80 nm) compared to the larger nanowire droplet (~150 nm) achieved with 5 min deposition. The difference in nanowire and Ga droplet diameter for thicker oxides is more difficult to explain, as the incubation time is close to the 5 min of deposition. In this case, the axial growth and nanowire density decrease, which favors the size increase of the Ga droplet during axial growth and thereby the nanowire diameter (further details in SI).

Figure 2g shows the evolution of the amount of Ga found on the surface as a function of the native oxide thickness, calculated by adding the average volume of the droplet times their areal density. The amount of Ga remains constant within the error bar to an oxide thickness of ~1.0 nm. For thicker oxides it is strongly reduced. This hints at a lower sticking coefficient of the Ga for thicker oxide at the growth temperature. It also indicates a change in the nature of the oxide.[36,37]

In order to further illustrate the change in the nature of the native oxide and to relate it to what one generally observes in nanowire growth,[32] we look at the contact angle of the Ga droplets, β (Figure 3). By progressively increasing the native oxide thickness (0.4, 0.6, 0.9, 1.1, 1.2, and 1.5 nm) the contact angle increases from 50° up to ~120° (see, respectively, Figure 3a−f). A summary of the contact angle as a function of the oxide thickness is reported in Figure 3g. Interestingly, nanowires form for $\beta > 80°$. The change in contact angle can also be related to the variation of the oxide surface energy through Young's equation:

$$\gamma_{sl} - \gamma_{sv} = \gamma_{lv}\cos(\beta)$$

where γ_{sl} is the liquid−solid surface energy, γ_{sv} is the solid−vapor surface energy, and γ_{lv} is the liquid−vapor surface energy. The latter was calculated by the empirical relation of Hardy.[38] The evolution of the term $\gamma_{sl} - \gamma_{sv}$ is illustrated in Figure 3h: it is negative for an oxide-free silicon surface, therefore energetically favoring the liquid/solid interface formation. The increase in surface thickness leads to an increase of the term $\gamma_{sl} - \gamma_{sv}$. At around 1 nm of oxide thickness $\gamma_{sl} - \gamma_{sv}$ becomes zero (see Figure 3d). From this critical value on, the formation of liquid−solid interface is not favorable, consistent with the high contact angle (>90°). The progressive change in contact angle should be explained by the gradient in the chemical composition of the native oxide. At the Si/SiO$_x$ interface the oxide is silicon-rich. When the distance to the interface (and thickness) is increased, the oxygen content progressively increases. For thick enough layers, typically obtained by thermal oxidation, the composition reaches the stoichiometric composition SiO$_2$ at ~1.3 nm off the Si interface.[39−42] Such a variation in chemical composition necessarily results in a change of surface energy.[16,40,42−49]

It is worth noting that a contact angle β between 50° and 70° is related to 2D growth. Instead, when the contact angle is larger than 80° nanowire growth becomes viable. Only for contact angles around 90° are a majority of vertical nanowires obtained. Higher contact angles favor the formation of tilted nanowires. This suggests that the initial wetting characteristics of the Ga droplet determine whether or not nanowires are formed, as well as their orientation with respect to the substrate. In principle, the change in nanowire orientation can be due to the following factors: (i) a change in polarity of the first layer nucleating on the silicon substrate or (ii) the existence of three-dimensional multiple twinning.[24] To understand which of the factors is more determining, we measured the tilting angles of the nanowires grown on thicker oxides (1.3 and 1.5 nm). If a change in polarity would be at the origin of the tilted angles, only nanowires with orientations of 19° and 90° would appear. Instead, we observe a wide range of tilting angles consistent with 19°, 34°, 41°, 58°, and 68°. This suggests that (ii) is triggering the formation of multiple orientations. Further work is needed to understand whether the surface energy or thickness of the oxide favors the three-dimensional multiple twinning. One should also consider that the change in surface energy at different oxide thicknesses might influences the Ga diffusion rate, leading to potentially different growth kinetics (e.g., formation of larger Ga droplets). Finally, detailed work on the role of the interface energy between GaAs and the oxide in the initial stage of growth should be performed in the future. For example, one could determine the shape and localization of the initial nuclei as a function of the oxide thickness. One would gain deeper insight into the origin of three-dimensional twinning for thicker layers.

In conclusion, with the present work we have demonstrated the key role of the nature of the native oxide in the Ga-assisted growth process of GaAs nanowires. We have shown that a change in the native oxide thickness is accompanied by a variation of surface energy. This determines the contact angle of Ga droplets on the surface and the capability of forming nanowires as well as their orientation. We find that a contact angle of 90° is the most suitable for obtaining vertical nanowire growth. This work opens new possibilities in nanowire growth in terms of control and reproducibility, also being a step forward toward a realistic integration of compound semiconductor nanowires on the Si platform.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

Additional characterization. The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.cgd.5b00374.

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

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Impact of the Ga droplet wetting, morphology, and pinholes on the orientation of GaAs nanowires.

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Ga-catalyzed growth of GaAs nanowires on Si is a candidate process for achieving seamless III/V integration on IV. In this framework, the nature silicon's surface oxide is known to have a strong influence on nanowire growth and orientation and therefore important for GaAs nanowire technologies. We show that the chemistry and morphology of the silicon oxide film controls liquid Ga nucleation position and shape; these determine GaAs nanowire growth morphology. We calculate the energies of formation of Ga droplets as a function of their volume and the oxide composition in several nucleation configurations. The least energy Ga droplet shapes are then correlated to the orientation of nanowires with respect to the substrate. This work provides the understanding and the tools to control nanowire morphology in self-assembly and pattern growth.

In addition to InP, GaAs is well known to be among the most promising and best performing semiconductor materials for photovoltaic application because it has a direct bandgap [1] [2]. However, the high material cost has limited commercial applications. Direct integration of GaAs nanowires on Si is a potential solution to reduce material consumption and increase cost competitiveness [3].To achieve a reliable and high-yield production method, several hurdles exist. Among the different techniques used to produce nanowires, the Vapor Liquid Solid (VLS) technique is the most established: it involves a liquid phase (the catalyst), a solid phase and a vapor phase. We choose self-catalyzed (i.e. Ga catalyzed) growth to avoid contamination of a foreign catalyst into the nanowire and consequent defect formation of deep trap impurities [4] [5] [6] [7]. Several groups have studied the adoption of the self-catalyzed or catalyst-free growth of GaAs nanowires from GaAs to silicon substrates [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [10] [11] [20] [21] [22] [23]. Most of these studies focus on steady-state growth and not the initial stages of Ga nucleation on the surface oxide.

Recently, we reported the influence of the native silicon oxide's surface energy on the yield and characteristics of nanowire growth morphology and orientation with respect to the substrate [23]. In this work, we identify the mechanisms that lead to the different growth orientations. First, we show that the composition of the SiO_x determines the wetting of Ga droplets as well as their localization via the formation of pinholes.

The SiO_x layers of different thicknesses were obtained by controlled exposure times of bare Si wafers in a controlled humidity ambient, as reported in [23]. In **Figure 17**, we report the SiO_x (a) wetting properties and (b) chemical composition as function of the oxide thickness. **Figure 17** (a) shows in green stars the surface energy that would be perceived by a polar liquid at different oxide thicknesses. In this case no trend is observed. However, if we consider Fowkes model [24], the surface energy γ_i of a substance is broken into independent components: a polar, γ_p, that includes Coulombic forces and any other type of dipole interaction, and the dispersive, γ_d, that derives from van der Waals forces and any other non-dipole related interactions. To assess the effect of the oxidation state the Ga/SiO_x interfacial energy, we are only interested in the dispersive component, because Ga is a non-polar liquid. Given the three unknown ($\gamma_i, \gamma_p, \gamma_d$), we performed macroscopic (~µl) contact angle measurements with polar (water and ethylene glycol) and non-polar (diiodomethane) liquids. These independent observations are used to calculate γ_d, which is reported in red squares in **Figure 17** (a). Only the dispersive component, γ_d , of the surface energy changes appreciably with thickness. γ_d decreases with increasing thickness and therefore the contact angle decreases with thickness as well. To confirm that the observed trend in contact angle corresponded to a change in γ_d and not to nanostructuring of the Si surface in islands of oxides we characterized the surface roughness of all the SiO_x layers by Atomic Force Microscopy (AFM). The surface roughness was very low (RMS=±0.2nm) for all layers, within AFM tolerance (±0.2nm) and no pinholes were observed at this stage. Therefore, the hypotheses of the cause of the change in γ_d are that the principle dispersive contribution derives from (i) the Ga/Si non-polar interaction across the SiO_x film, and from (ii) a change in chemical composition of the SiO_x which lead to different surface energies of the film. In case (i) the interaction energy derives from a $1/r^6$ body-body integration across the film thickness [25]. To verify the contribution of (ii) in the change of contact angle we measured the SiO_x oxygen composition by X-ray Photoelectron Spectroscopy (XPS) on the different films. The results are shown in **Figure 17** (b) as function of SiO_x film thickness. The Si oxygen content has been calculated with the method presented in [26] (the Si 2s, 2p and O XPS data and interpretation are available in the SI). The oxidation state of silicon increases with the oxide thickness and becomes stoichiometric SiO_2 beyond 1.4-1.5 nm thickness. These results are consistent with literature [23]. In summary, 1) we observe that increasing oxide thickness the chemical composition of the oxide changes towards SiO_2, the thermodynamically more stable form of oxidized silicon; 2) the change in chemical composition correlates with decreased wetting (i.e., increased contact angle) of Ga droplets on the SiO_x film.

Since the first publications on Ga-assisted growth of GaAs nanowires, it has been recognized that pinholes have a central role in nucleating and fixing the droplets on the substrate [27] . Furthermore, pinholes that protrude to the underlying Si substrate produce an epitaxial relation between the nanowire and the substrate layer during the growth process [27] [28]. However the pinhole formation mechanism is uncertain. To understand whether or not pinholes are formed in the oxide and if Ga plays a causal role in pinhole formation, we investigated the surface of thermally treated Si wafers after the thermal cycling used for growth (same procedure presented in [23]). We used a Si wafer with a 1.5 nm oxide. **Figure 18** (a) shows the AFM characterization performed right after the thermal cycle: pinholes of sizes of ~30nm are observed in the oxide layer. Insets A & B in **Figure 18** (a) show the hole profiles. The depth is comparable to the oxide thickness. Because we did not observe any surface nano-structuring before the thermal cycling, we conclude that form upon heating at 750°C in UHV (as already reported by [29] [30] [31] [32]): Ga is not necessary to form pinholes.

We turn now to the role of pinholes in the nanowire growth. We would like to understand if both nanowires and polycrystalline growth, which we will call parasitic growth, start from a pinhole, or whether only nanowires start from pinholes and parasitic growth nucleates on the oxide. With this purpose, we repeated the thermal cycling prior to growth with the addition of Ga deposition for different time periods, comparing the density of Ga droplets and the density of pinholes. The droplet density was measured by Scanning Electron Microscopy (SEM), and the pinhole density has been measured via AFM after removing the Ga droplets with chemical etching (HCl 37% Vol, 25 min). The results are reported in **Figure 18** (b): the density of droplets and pinholes is plotted as a function of different Ga deposition times: these densites are perfectly correlated. This observation leads to the conclusion that oxide pinholes are the nucleation points for Ga droplets. The selectivity of Ga deposition on bare Si agrees with previous reports [33] [34]. Both pinhole and droplet density increase with deposition time. Because the deposition is performed at high temperature, additional pinholes are formed during the process. Further information on the characterization of pinholes and their formation process can be found in the supplementary information.

To summarize, the SiO_x film's oxygen content increases with film thickness and saturates at x=2 around 1.5 nm. Ga becomes increasingly non-wetting as the SiO_x film's thickness increases. Ga is not necessary for pinhole formation because form during thermal treatment in UHV.

These surficial film observations are used to model nucleation and growth of nanowires. The experimental observation of the evolution of the shape of small liquid Ga clusters in nanometer size holes is extremely challenging. Here we use a numerical approach to compute the three dimensional wetting configurations. We assume the liquid droplets adopt their energy-minimizing shape at any given volume. Furthermore, we consider several possible wetting configurations and compute their volume-dependent minimal energy. For this purpose we used Surface Evolver, a program for minimizing energy of surfaces [35].

As a first step in modeling we considered all different possible catalyst droplet configuration in the pinholes and for the different observed contact angles [23], as illustrated in **Figure 19**. Figure (a) represents the case of a droplet sitting inside the center of a hole, (b) of a droplet sitting in a corner inside a hole, (c) of a droplet wetting the walls of a hole, (d) a "spilled" droplet wetting the inside of a hole and also spilled one of the abutting SiO_x surfaces, and (e) a droplet symmetrically spilled onto both SiO_x surfaces abutting the pinhole (the computations were performed in three-dimensions, the two dimensional graphics in Figure 3 are for illustrative purposes). The energy difference between configurations are expected to influence the nucleation and growth morphologies. The Ga(l)/GaAs(s) equilibrium contact angle is observed and reported [36] [37] to be bigger than 116°, whereas the Ga/SiO_x ($1<x<2$) equilibrium contact angles are always smaller than 116° ($50°<\theta<116°$). In other words, when supersaturation is reached and the first layer of GaAs is formed, the droplet tend to populate the energetically more favorable Ga(l)/SiO_x interface (if still existing).

In the cases of a droplet sitting inside the center of a hole (a) and sitting in the corner of a hole (b) (see **Figure 19**) in a supersaturated environment, nucleation is more likely at the more favorable Ga/Si(111) interface instead of Ga/GaAs; if the particle touches both surfaces, a Marangoni force will drive the droplet towards the Ga/Si(111) interface. This will lead the droplet to fill the hole, being therefore equivalent to the droplet wetting the walls of a hole (c). The latter will most likely lead to the formation of vertical nanowires (see **Figure 19** (c)), because there is no misbalance in the forces that would tend to tilt the droplet with respect to the substrate. This is not the case for a droplet that covers the inside of a hole and the spills assymetrically on the SiO_x (d), since the formation of Ga/GaAs interface will result in a net force to the droplet to spill out of the hole (see **Figure 19** (d)). The "crawling" of the droplet should then be more significant in the case of low oxide thickness (i.e. $\theta<90$; thick. $<\sim$1nm), since the difference in contact angles before and after the formation of a GaAs nucleus is higher compared to thicker oxides (i.e. $\theta>90$; thick. $>\sim$1nm). The abrupt change in droplet shape might lead to either the formation of polycrystalline material on the surface, or of tilted nanowires.

The homogeneously spilled droplet configuration (e) will behave differently depending on whether the Ga/SiO_x equilibrium contact angle is larger or smaller than 90°. The case $\theta>90°$ will lead to vertical nanowires, whereas in the case of $\theta<90°$, the Ga/SiO_x interface will be more favorable. In this case the droplet will spill towards the oxide, producing polycrystalline material on the SiO_x or horizontal nanowires. In conclusion, the initial droplet configuration determines the final growth morphologies.

We turn now to the calculation of the probability of finding each proposed configuration. This can be written as:

$$P_{nucl} \propto e^{-\frac{\Delta G}{k_b T}} \quad (1)$$

Where P_{nucl} is the nucleation probability of the droplet, ΔG is the Gibbs free energy, k_b is the Boltzmann constant and T is the temperature. The Gibbs free energy can be written as:

$$\Delta G = -\Delta gV + \sum_i A_i \gamma_i \quad (2)$$

Where ΔgV is the volumetric component and $\sum_i A_i \gamma_i$ is the interface component. The interfacial energy component is computed from the minimizing surface, and its value will depend on which surfaces the droplet contacts. In other words, the droplet configurations (a)-(e) will have different nucleation probabilities. Combining the two equations, we can see that the nucleation probability is higher for droplet configurations exhibiting a lower interface energy component for an equivalent droplet volume.

We calculated the energy associated for different droplet configurations at different volumes and for different oxide compositions and thicknesses (i.e. different Ga/SiO_x equilibrium contact angles θ= {59°, 76°, 82°, 94°, 98°, 106°, 116°}, as measured experimentally in [23]). Since we did not know the dimensions of the holes at nucleation, we performed the calculation for a range of hole width to height ratio from $2<w/h<20$. For simplicity we report here only the w/h=2, the other results, including a detailed discussion of the influence of the aspect ratio of the hole are available in the supplementary information. The results are summarized in **Figure 20** : (a), (b) and (c) show the energy cost as a function of volume for the Ga/SiO_x equilibrium contact angles θ of 59°, 94° and 116°. The units of the axes are dimensionless, so that the results can be generalized to different material systems. On the x-axis we plot the filling percentage of the holes (e.g. when $V_{liq}/V_{hole}=1$, the hole is full of liquid), whereas the y-axis has the total surface energy normalized by the liquid surface energy multiplied by the squared hole height. Each curve corresponds to a different droplet configuration, and the color background corresponds to the lower energy configuration in each volume range (see sketch above **Figure 20** (c)). In (a) we observe that at low volume ratios ($0< V_{liq}/V_{hole} <0.64$), the lowest energy configuration is the droplet sitting in a corner of the hole. Whereas in the range of volume ratios up to 1.28, the minimal energy droplet wets the walls of the hole and stay pinned to the edges of the hole. Beyond that volume, the droplet will tend to spill symmetrically. However, the non-homogeneous spill is energetically very close (see **Figure 20** (a)). We expect the statistical differences between the symmetric and non-symmetric spilled cases to be small.

A similar trend of transition from droplet sitting in the corner of a hole to wet the walls is also observed in the case of θ=94° and θ=116°, but the transitions from bottom corner, to wetting the walls happens at respectively larger volume ratios compared to the θ=59° (for θ=94°; V_{trans}=0.7, whereas for θ=116°; V_{trans}=0.74). For the transition from wetting the walls to spilled, the transition volumes are similarly increased (for θ=94°; V_{trans}=1.64, whereas for θ=116°; V_{trans}=2.08). Consideration of the simulation results of the energy transitions (**Figure 20**) for the different wetting configurations (**Figure 19**), we conclude and experimentally observe the following:

- In the case of θ=59°, the Ga/SiO_x interface is more favorable to form than the Ga/GaAs, therefore leading either to nanowires or to 2D polycrystalline growth, depending on the volume (i.e., minimizing droplet configuration) at which the nanowire nucleation occurs (see **Figure 20**(a) and **Figure 21** (a)). To verify this, we performed a 15 sec GaAs growth on Si(111) coated with a SiO_x layer of 0.5nm (which give the 59° Ga/SiO_x contact angle), for 15 sec, in order to be able to observe the early stages. The result is shown in **Figure 21** (c): the growth morphologies attained were vertical nanowires and 2D growth VLS driven, consistent with the prediction. **Figure 21** (e) show a growth performed under identical conditions but for 1h growth time, to illustrate the evolution of the process.
- In the case of θ=94°, the energetically favorable configurations (see **Figure 20** (b)) are either wetting the pinhole walls or symmetrically spilled (respectively the configuration in **Figure 19** (c) and the configuration in **Figure 19** (e)), depending on

when the solid GaAs nucleation will happen (i.e. Ga droplet volume). For this equilibrium contact angle both the configuration, wetting the walls and symmetrically spilled, would lead to vertical nanowire formation, as illustrated in **Figure 21** (b)—there is no tilting of the droplet with respect to the substrate. However, in the volume range > 1.64 the non-symmetric spill of the droplet (configuration in **Figure 19** (d)) is energetically close to the homogeneously spilled droplet, potentially leading to significant amount of 2D polycrystalline growth. Also in this case we attempted to verify experimentally the prediction by growing GaAs nanowires on a 0.9nm oxide layer for 15 sec to observe the early stages of growth (the incubation time had been previously measured to be ~10 sec [23]). The results in **Figure 21** (d) show vertical nanowires of different lengths and diameter, which may reflect that GaAs nucleation occurred both in the prior and post-spilling scenarios presented above. **Figure 21** (g) illustrate the growth after 1 hour, yielding to a high-density forest of vertical nanowires.

- In the case of θ=116°, all the configurations have very similar energies (see **Figure 20** (c)), which would not tend to select a particular droplet configuration, and therefore different growth morphologies (2D polycrystalline growth, vertical and tilted nanowires). These potential scenarios are drawn in **Figure 21** (c). The GaAs nanowire growth attempt on oxide thicknesses of ~1.6nm (i.e. θ=116°) for 6 min (the incubation time had been previously measured to be ~5min [23]) is shown in **Figure 21** (e). A combination of vertical and tilted nanowires was observed, consistent with the simulation results. Their evolution after 1h is shown in **Figure 21** (h).

Our calculations are consistent with the observations that correlate the oxide properties, equilibrium configuration of the Ga droplets and growth orientation of the nanowires, the combination of the hole dimensions, droplet volume, and surface energy condition the growth morphology (i.e. vertical nanowire, tilted, or polycrystalline). Nevertheless, since hole formation in the self-assembled growth is distributed over time and so far cannot be controlled, the achievement of only vertical nanowire will depend on controlling the pinhole geometry and evolution.

In conclusion, the native oxide thickness determines the chemical composition of the surface, its thermodynamic stability at high temperature and its wetting properties. These changes influence formation of holes in the oxide film, which determine Ga droplet volume and curvatures, and the droplet configurations within the pinhole. The latter determines the nanowire nucleation time and the growth morphology. The engineering of the wetting properties of the oxide can control the orientation of the nanowires. These results can be generalized for the case of patterned growth, as preliminary results in the SI point out, and can be extended to different material systems.

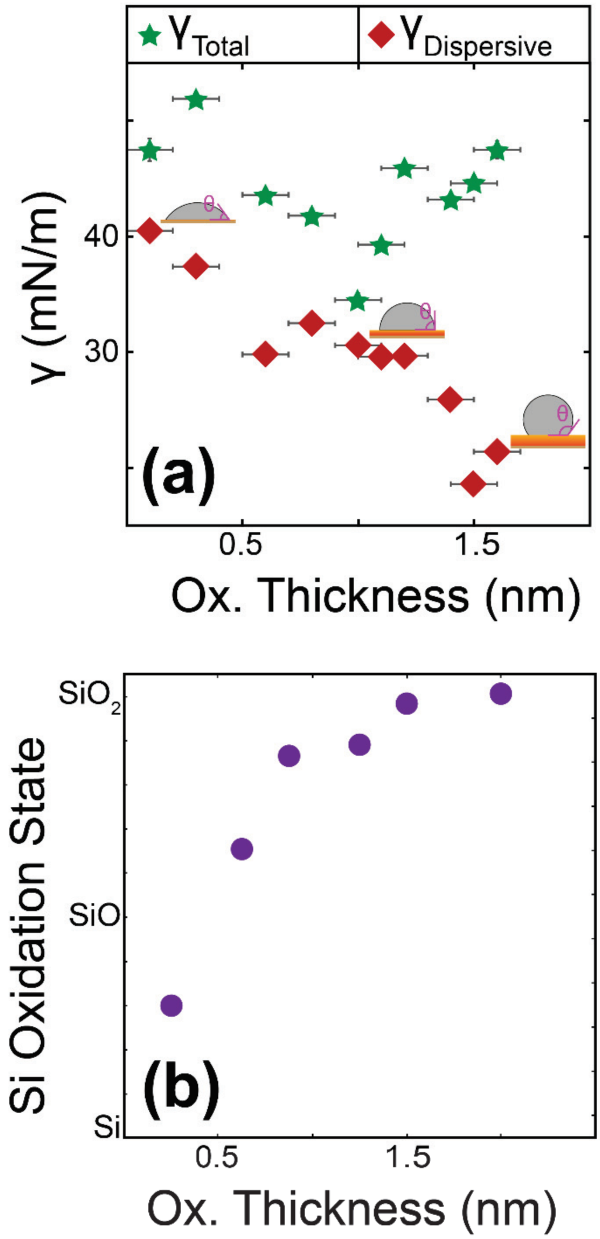

Figure 17 (a) Evolution of the surface energy as a function of native oxide thickness. The dispersive surface energy was calculated with Fowkes method from the contact angle measurements performed with polar (water and ethilen glycol) and non-polar (diiodomethane) liquids. (b) Evolution of the Silicon oxidation state as a function of the native oxide thickness. The oxidation state of Si has been calculated with the method described in [26] using XPS measurements on different native oxide thicknesses.

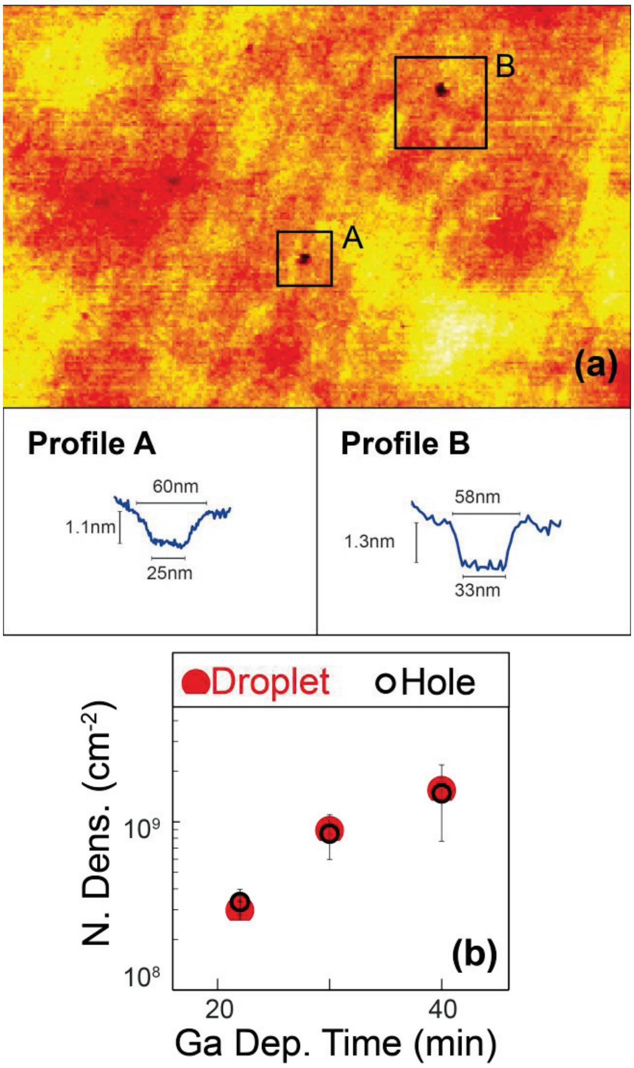

Figure 18 (a) AFM scan of a 1.5 nm native oxide on Si (111) substrates after thermal annealing at 750C for 45min. The insets A & B show the profile of holes in the oxide that were not observed before the thermal annealing. (b) The area density of holes and of Ga droplets at different deposition times. The oxide thickness was 1.5nm. The hole density and diameters were measured by AFM after etching Ga with 25 min HCl etch. The plot shows that the density correlate perfectly and that holes are formed during the process.

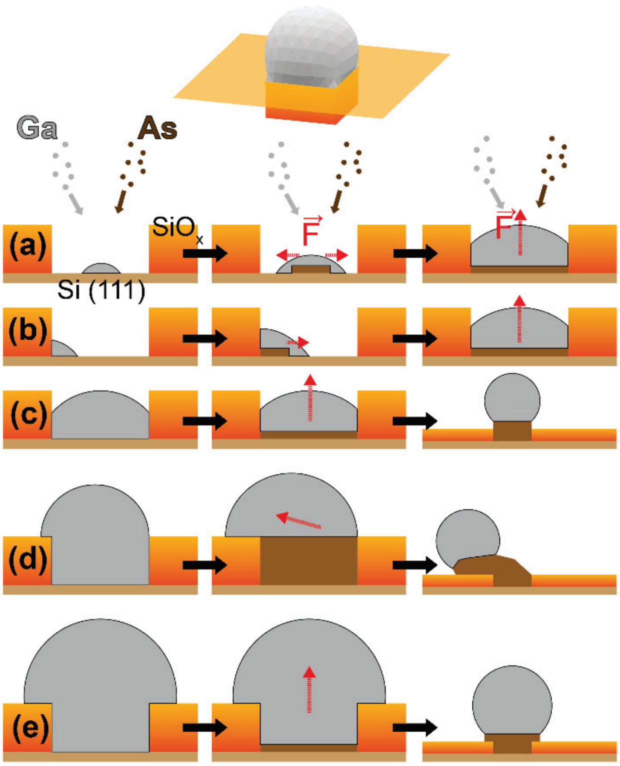

Figure 19 Diagrams of hypothetical droplet configurations prior to nanowire nucleation. The computations presented in this paper were three dimensional, as shown at the top. The diagrams are used to illustrate the various configurations for simplicity. In orange to yellow the SiO_x ($1<x<2$) layer is represented, whereas bare Si is beige and liquid Ga in grey and GaAs is brown. The first column presents the droplet configurations before nucleation of the GaAs, the second column the early stages of growth, and in the third column the consequent nanowire configuration. In (a) the droplet is formed in the center of the hole, where the liquid phase form an interface only with bare Si (111). (b) Shows the bottom corner droplet configuration, where the liquid form an interface with bare Si (111) on the horizontal plane, and with SiO_x on the vertical wall of the hole. In (c) the droplet is in contact with both sides of the pinhole. (d) Shows the configuration of an assymetrically "spilled" droplet which wets only one side of the abutting SiO_x film. In (e) the case of symmetric spill of the droplet is represented. Its evolution towards a nanowire depends on the contact angle: if $\theta>90°$ we observe nanowires (as shown here), whereas $\theta<90°$ leads to parasitic growth (not shown).

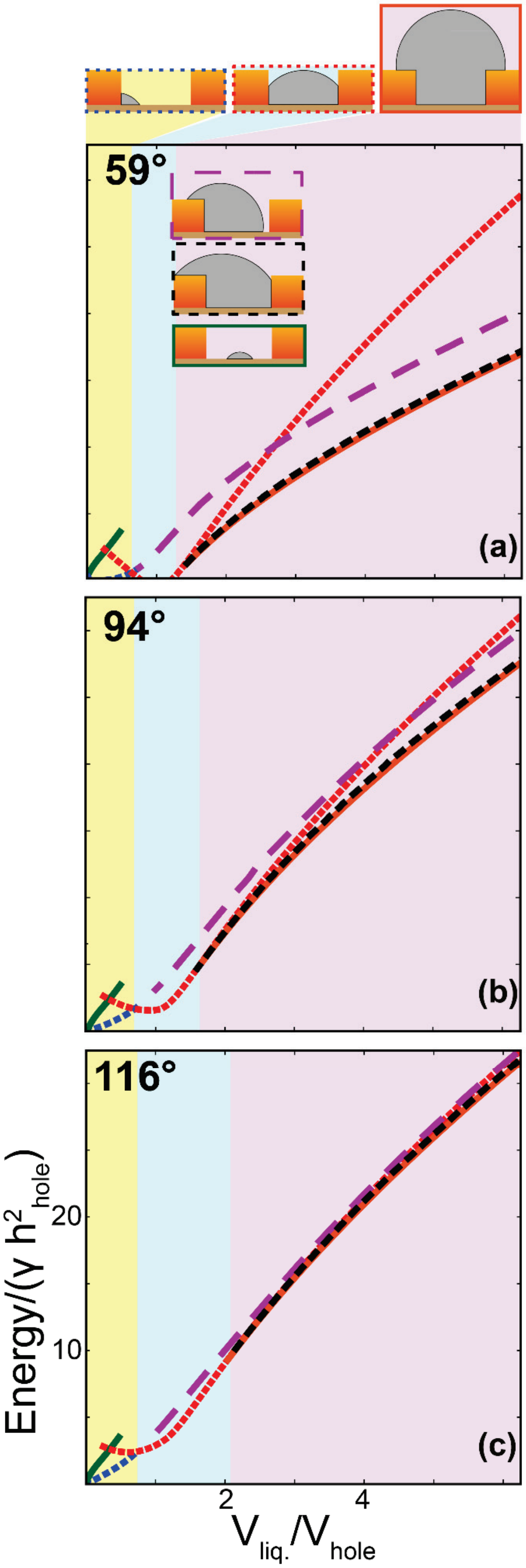
59°
(a)
94°
(b)
116°
(c)
Energy/(γ h²_hole)
10
20
2
4
V_liq./V_hole

Figure 20 Representation of the energy vs volume curves of the different droplet configurations with (a) 59°, (b) 94° and (c) 116° degrees of Ga to SiO_x contact angles. The green curve represents the droplet at the center of the hole configuration, the blue curve the bottom corner droplet, the red curve the droplet wetting the walls of the hole. The orange curve the symmetrically spilled droplet, the black curve is for the non-uniform spilled droplet, and the purple curve the assymetrically spilled droplet wetting the bottom of the hole and not one of the pinhole sides. The background colors refer to the energetically most favorable configuration as function of the volume, as sketched above (c).

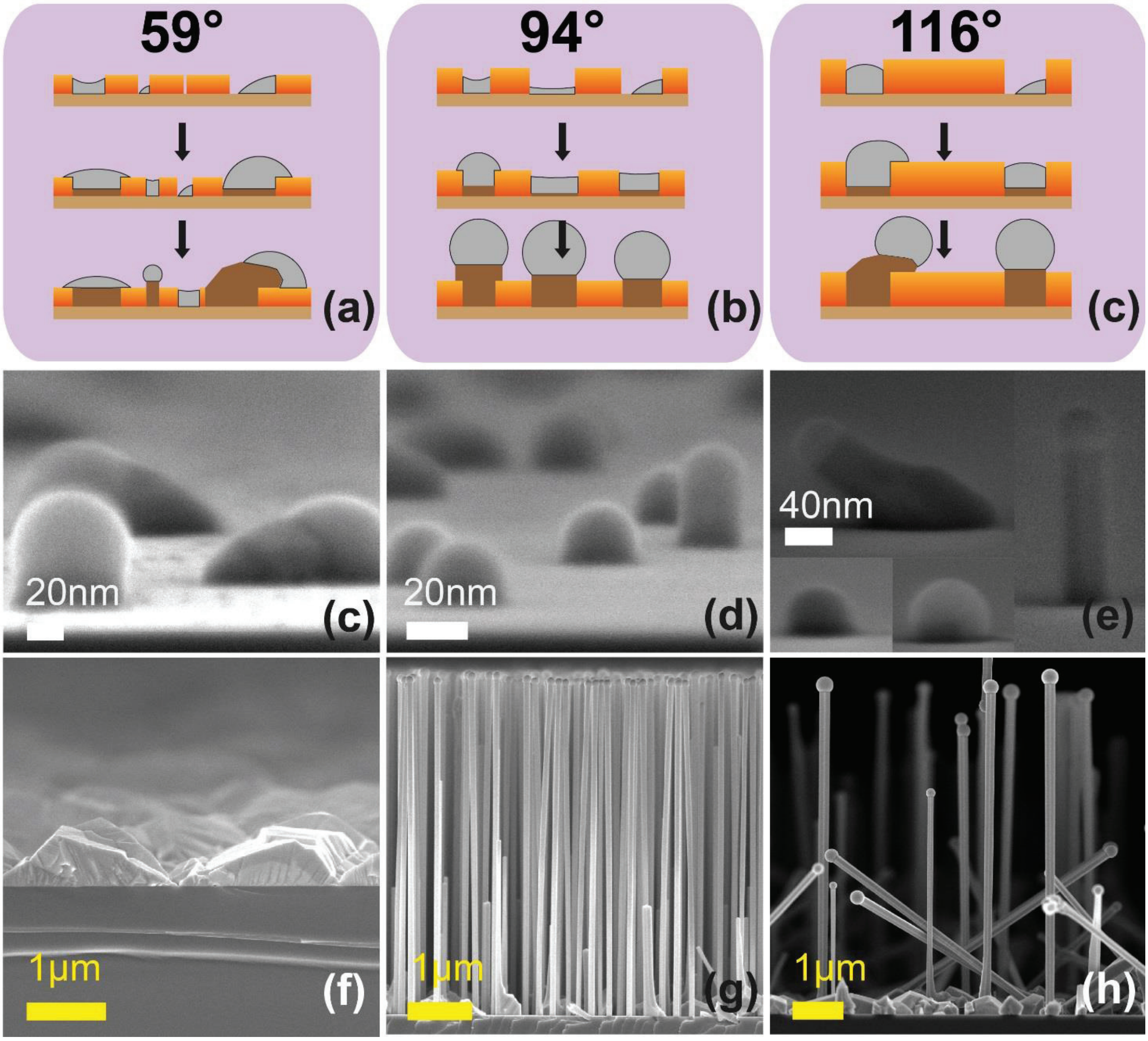

Figure 21 (a) - (c) illustrate the energetically most favourable droplet configurations and their evolution upon nucleation of the GaAs, for Ga/SiO$_x$ equilibrium contact angles of 59°,94° and 116° respectively. In (c) -(e) the SEM micrographs of GaAs nanowire grown on Si (111) coated with 0.5nm, 0.9nm and 1.6nm of native oxide are shown. The growth times of (c) - (e) correspond to the characteristic incubation time of each oxide thickness, which is ~15 sec for 0.5nm and 0.9nm oxides, and ~6 min for the 1.6nm oxide (the incubation times were determined in [23]). (f) - (h) Show the nanowires grown under the same conditions of (c) - (e) after 1 hour.

ASSOCIATED CONTENT

Additional characterization. This material is available free of charge via the Internet at http://pubs.acs.org

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

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3.5 Summary

In this chapter we have investigated the role of the silicon oxide in GaAs nanowire growth. We first have identified roughness, stoichiometry and thickness as key parameters for nanowire growth. Native oxide was further investigated for its simple fabrications steps and excellent results. The surface properties in terms of wetting and chemical composition were observed to be dependent on oxide thickness. The chemical composition was observed to be responsible of the thermal stability of the oxide, which determined nanowire density. The wetting properties determined the droplet positioning, which controlled the growth morphologies and nanowire orientations. These investigations provided valuable results both on an experimental and theoretical level. On the experimental level, it brought a simple reproducible method to have high density high yield of vertical nanowires, and on the theoretical level it provided the understanding of the role of the oxide layer in the growth process. The knowledge developed paves the way towards the possibility of having vertical nanowires independently on the oxide thickness. These results can also be extended in the case of patterned growth.

4 Mastering nanowire properties for light interaction

In the previous chapter we have investigated how the characteristics of of the silicon oxide affect the growth process. It was observed to influence growth morphology, nanowire orientation and density. More in detail, by controlling its thickness we could control nanowire orientation consistently. The latter, as presented in Section 1.4, is fundamental for photovoltaic applications. The other milestones for the development of GaAs nanowire solar cells that still had to be accomplished were the control over diameter and density. This chapter is dedicated to the investigation of the growth mechanisms that control nanowire diameters and density.

4.1 Introduction

The control of nanowire density and diameters has been demonstrated to be crucial to achieve the accurate design of the individual junction for nanowire-based solar cells [15] [18]. Despite its importance, the general approach to the topic consisted in individual studies of either one of the properties, instead of considering their relation.

Many works have investigated the influence of the process parameters, such as vapor fluxes and temperature in Ga-assisted growth of GaAs nanowires, on the nanowire diameter. The increase of Ga flux was observed to enlarge the catalytic droplet, leading to broader nanowire diameters [55] [79] [80]. Differently, an increase in the As flux was reported to shrink the Ga droplet, leading to smaller nanowire diameter [60] [55] [79] [80] [81]. The influence of temperature on the diameter is more complex: Tersoff demonstrated that, given a specific temperature and a combination of vapor fluxes, there is only one stable droplet diameter and volume [128]. On the experimental level, a temperature increase is expected to enhance diffusion up to a critical temperature, enlarging the nanowire diameters. Beyond the critical value, desorption is fostered, resulting in a diameter decrease. This critical temperature was observed to be ~620°C [129] [93]. A more exotic approach has been attempted by Kizu and coworkers: they employed an alternating supply of the fluxes to foster Ga migration and shrink the nanowire diameter [130]. In a different approach, in the case of patterned growth, where the number of nucleation sites is lithographically defined, the nanowire diameter was tuned by exploiting the shadowing effect: a smaller spacing between the nanowires shrinks the diameters, increasing the competitiveness of the growth process, where a Ga atoms can feed several nanowires. Vice-versa, when nanowires are more spaced, an incoming Ga atom can diffuse and feed only one nanowire, increasing the feed and therefore also the diameter [131].

In the case of nanowire density, several groups reported a dependence from temperature and Ga flux. From a qualitative standpoint, the increase of Ga flux resulted in a rise of nanowire density, since more material is available on the surface to form new droplets [67] [79]. Also an increase in temperature was observed to increase nanowire density, by fostered Ga mobility [68] [67]. More original approaches to control nanowire density have been attempted by means of droplet epitaxy related techniques. Somaschini and coworkers pre-deposited the catalytic droplets by means of droplet epitaxy on bare Si or Si coated with native oxide, and supersaturated them under As flux. In a second step they exposed the substrate to air to oxidize the rest of the surface, and used the supersaturated droplets as nanowire seeds [69]. A similar approach had been developed by Hakkarainen and coworkers: the supersaturated droplets were then used as sacrificial templates. These seeds were evaporated in the MBE to use their location as nucleation sites [132]. Bietti and coworkers simplified the whole process eliminating the need of an oxide layer and the exposure to air step, and directly using the supersaturated droplets as nanowire seeds [133]. The droplet to nanowire conversion process was also demonstrated to be efficient. The drawback of this approach was the high density of polycrystalline material formed at the bottom of the nanowires due to the high Ga collection, which is generated by the absence of a masking oxide.

4.2 Outlook

In our investigation we decided to focus on the self-assembly approach and study the behavior of diameter and density as an ensemble, to gather deeper understanding of the nanowire growth governing mechanisms. We first explored the effect of temperature and Ga flux over diameter and density. The results are shown in Figure 1Figure 22 (a): higher temperature lead to higher nanowire density, but also to broader diameters, and larger Ga flux lead to higher density but also larger diameters. These observations were coherent with what reported from other groups, as mentioned in Section 4.1. This preliminary experiments showed a clear correlation between diameter and density: the larger the density, the larger the diameters and vice-versa. However, in the case of the different Ga fluxes, we observed also a change in the breadth of the diameter distribution of the nanowires: the Ga flux increase resulted in a progressive narrowing of the distributions. We investigated the matter more in detail in collaboration with Professor V.G. Dubrovskii, and performed a kinetic model, where we considered nanowires nucleation to be time dependent. Nanowires were not considered to start growing at the same time, but to have a certain characteristic incubation time before starting to grow (see Figure 22 (b)). This model provided the insight of a Ga flux dependent incubation time: at higher Ga flux, all the nucleation events were verified in a narrow window of time, leading to finer length and diameter distributions. Instead, at low Ga flux, the nucleation events were more spread over time, leading to broad distributions.

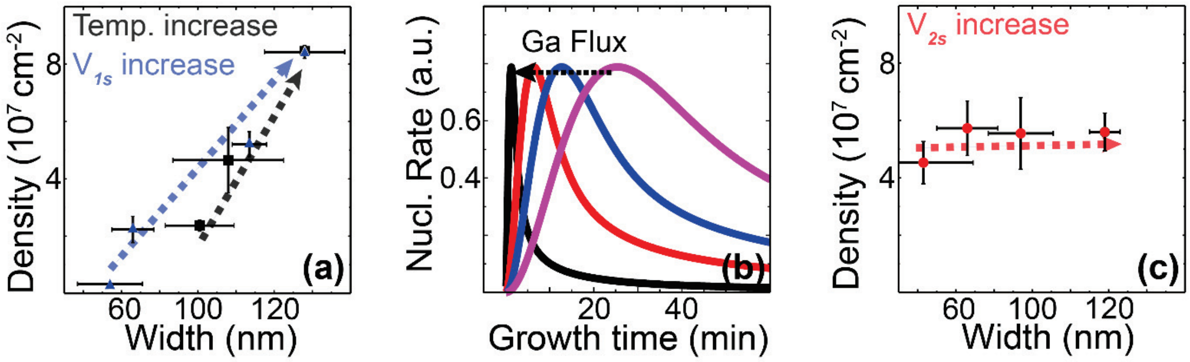

Figure 22 (a) Diameter-density relation of nanowires grown at (blue line) increasing Ga fluxes (0.5,0.75 and 1 A/s) and increasing temperature (604, 624 and 645°C). (b) Time dependence of the nucleation rate as a function of the Ga flux. (c) Diameter-density relation of the two step Ga fluxes growth.

This understanding of the initial stages of nanowire growth was instrumental to develop diameter-density combinations that were not possible with a classical approach (see Figure 22 (c)). We introduced a two-step Ga fluxes growth: the first Ga flux was used to tune the density and the distribution width, and the second step to tune the diameter. To demonstrate the effect of diameter tuning over the nanowire optical properties we measured the reflectivity of the nanowire's forests. The nanowire diameter demonstrated to affect the reflection of the ensemble, as expected from the theoretical predictions. The simulations predict a boost of light absorption around 800nm for nanowire diameters ~150nm. In a similar fashion, in Figure 23 (b) the reflectivity of the GaAs nanowires' ensembles grown with the two steps Ga approach show a decrease in reflectivity at ~800nm for nanowire diameters that approach the ~150nm.

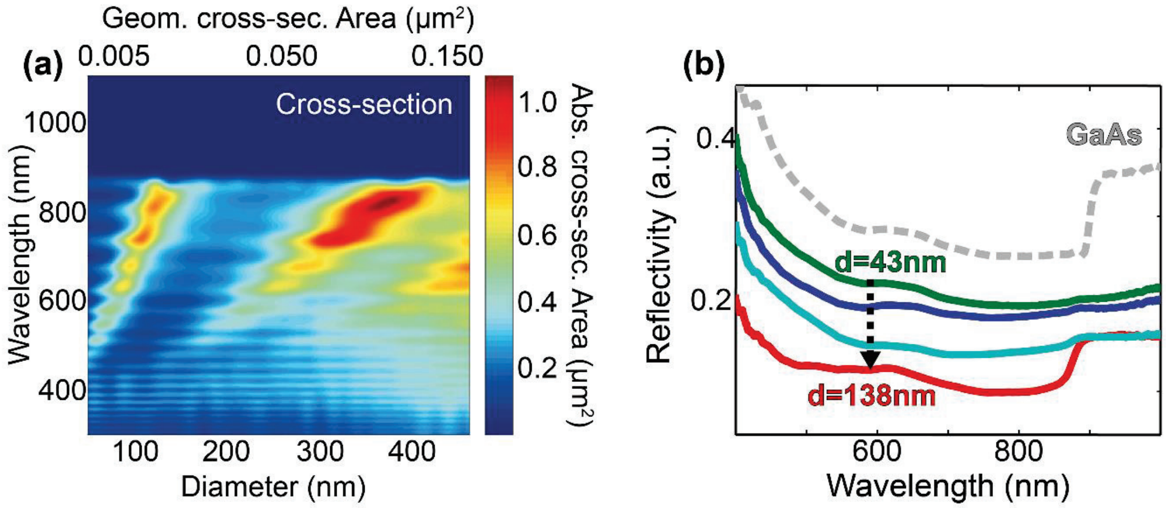

Figure 23 (a) Simulated light absorption of a GaAs nanowires perpendicular to the Si substrate. Reprinted by permission from Macmillan Publishers Ltd: Nature Photonics [15], copyright 2013. (b) Reflectivity of the GaAs nanowire forest grown with the two-step Ga, compared to the reflectivity of a GaAs wafer (dashed line). The increase of Ga flux at the second step progressively increases the diameters and enhances the light absorption.

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4.3 Papers included in the chapter

I. **Tailoring the diameter and density of self-catalyzed GaAs nanowires on silicon**
F. Matteini,V.G. Dubrovskii, D. Rüffer, G. Tütüncüoglu, Y. Fontana and A. Fontcuberta i Morral
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Tailoring the diameter and density of self-catalyzed GaAs nanowires on silicon

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Abstract

Nanowire diameter has a dramatic effect on the absorption cross-section in the optical domain. The maximum absorption is reached for ideal nanowire morphology within a solar cell device. As a consequence, understanding how to tailor the nanowire diameter and density is extremely important for high-efficient nanowire-based solar cells. In this work, we investigate mastering the diameter and density of self-catalyzed GaAs nanowires on Si(111) substrates by growth conditions using the self-assembly of Ga droplets. We introduce a new paradigm of the characteristic nucleation time controlled by group III flux and temperature that determine diameter and length distributions of GaAs nanowires. This insight into the growth mechanism is then used to grow nanowire forests with a completely tailored diameter-density distribution. We also show how the reflectivity of nanowire arrays can be minimized in this way. In general, this work opens new possibilities for the cost-effective and controlled fabrication of the ensembles of self-catalyzed III–V nanowires for different applications, in particular in next-generation photovoltaic devices.

S Online supplementary data available from stacks.iop.org/NANO/26/105603/mmedia

Keywords: GaAs nanowires, self-catalyzed growth, nucleation, growth modeling, light absorption

(Some figures may appear in colour only in the online journal)

1. Introduction

Semiconductor nanowires are interesting as building blocks for next-generation optoelectronic and electronic technologies [1–5]. Within a wide range of III–V compounds used to form these structures, GaAs is among the most promising materials for photovoltaic applications [6]. Furthermore, GaAs nanowire-based solar cells can be grown on Si, easily resulting in a dual-junction device [7]. Proof-of-concept radial p-i-n GaAs nanowire solar cells have been demonstrated in the past [8–13]. Recently, it has been shown that the achievement of high efficiencies can only be obtained after the accurate design of the individual junction, the nanowire diameter, and density so that light absorption and conversion are maximized [14, 15]. Pre-patterning the substrate would be an approach to control density. However, such a technique is technologically demanding and presents several open challenges [15–17]. Furthermore, a regular array would not work on all incident angles due to diffraction effects [18]. We propose here a more cost-effective alternative: the self-assembly of nanowires. We will show how understanding the initial stages of growth provides the tools to control the dimensions of the nanowires on the substrate.

To the best of our knowledge, relatively few works published so far report on the distribution of nanowire density and diameters [19–23]. An original approach for controlling

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the nanowire density makes use of droplet epitaxy techniques [19]. This method is very efficient for controlling the density and diameter of Ga droplets that initiate GaAs nanowires. However, when it comes to the transition from droplets to nanowires, the yield is not yet 100%. Additionally, uncontrolled secondary nucleation changes the predetermined nanowire density and diameter. Some groups have reported on the substrate temperature effect on the nanowire diameter and density [22, 24]. However, no comprehensive model was proposed to grasp the fundamental mechanism and thereby tailor the nanowire diameter and density in an effective manner.

Consequently, in this work we study the impact of the growth conditions on the morphology and density of self-assembled GaAs nanowires on Si (111). An understanding of the underlying mechanism is used to achieve diameter-density combinations 'à la carte', allowing one to tailor light absorption of the self-assembled nanowire arrays. We start by showing the general influence of the substrate temperature and Ga flux over the nanowire density, diameter and length distributions. This is followed by presenting a model that reveals the underlying mechanisms. The model is then used to develop an alternative growth approach based on two steps of Ga fluxes to tailor at will the nanowire diameter and density. Finally, we show how tailoring the nanowire diameter-density can be used to increase the overall solar light absorption.

2. Experimental details

Our samples were grown by molecular beam epitaxy (MBE) on Si(111) substrates covered with a native oxide layer. The surface roughness of the substrates was around 0.4 ± 0.2 nm as measured by atomic force microscopy. Growths were carried out with simultaneous deposition of Ga and As_4. The range of Ga fluxes extended from 0.03 nm s^{-1} to 0.11 nm s^{-1}, as calibrated by reflection high-energy electron diffraction (RHEED). The As flux was kept constant in all the experiments at 2.5×10^{-6} Torr, and was calibrated by a beam flux monitor gauge. The range of temperatures used went from ~600 °C to 645 °C, calibrated by a pyrometer that measures the emissivity of the Si substrate.

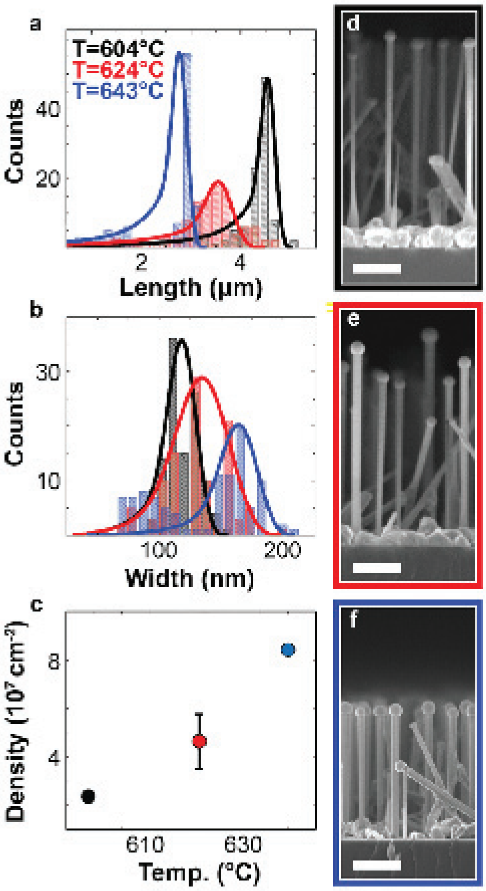

Figure 1. Length (a) and width ($d = 2R$) (b) distributions of self-catalyzed GaAs nanowires grown at a fixed Ga flux of 0.11 nm s^{-1} and three different temperatures (T = 604 °C, T = 624 °C and T = 643 °C) for 60 min. The lines in (a) and (b) are the fits obtained from the model presented in the text (for further details, see the supplementary information), with the parameters summarized in table 1. In (c) the evolution of nanowire density over different substrate temperatures is reported. The scanning electron micrographs of the nanowires grown at the three different temperatures are, respectively, shown in (d), (e) and (f). The scalebar is 1 micrometer.

3. Results

3.1. Impact of growth conditions

In the first set of experiments, the substrate temperature was varied from 604 °C up to $T = 643$ °C, whereas the Ga growth rate was kept constant at $V = 0.11$ nm s^{-1}.

Figures 1(a)–(b) show the distribution of nanowire length and diameter for three different temperatures. The statistics are the result of measuring a total of at least 100 nanowires. The lines show theoretical fits by the model presented hereafter. The increase of temperature decreases the nanowire length from ~4.5 μm to ~2.8 μm (see figure 1(a)), and increases the diameters from ~100 nm up to ~160 nm, (see figure 1(b)).

Figure 1(c) shows the density dependence over temperature (from 2.4×10^7 nanowires/cm^2 to 8.4×10^7 nanowires/cm^2), and figures 1(d)–(f) show typical scanning electron micrographs of the samples. In general, higher substrate temperatures result in a reduction of the length and an increase in the diameter. Higher substrate temperatures also result in a reduction of polycrystalline GaAs islands, also

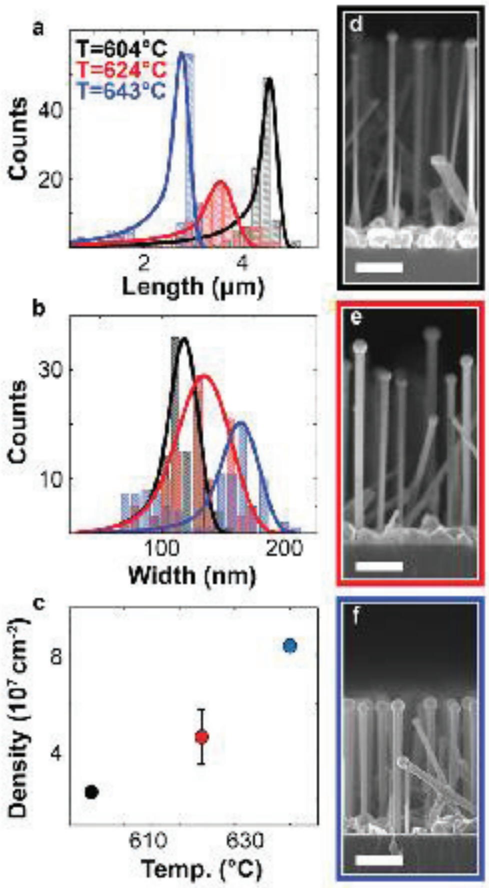

Figure 2. Length (a) and width (b) distributions of self-catalyzed GaAs nanowires grown at a fixed substrate temperature of 643 °C and three different Ga fluxes (V_{III} = 0.11 nm s^{-1}, V_{III} = 0.075 nm s^{-1} and V_{III} = 0.05 nm s^{-1}) for 60 min. In (c) the evolution of nanowire density over different Ga fluxes is reported. The lines in (a) and (b) are the fits obtained from the model, with the parameters summarized in table 1. (d), (e) and (f) show the respective scanning electron micrographs of the nanowires grown at the three different Ga fluxes. The scalebar is 1 micrometer.

called parasitic growth, while the nanowire density increases. In the second experiment, we looked at the nanowire diameter and length distribution under varying Ga flux. We chose the substrate temperature of 643 °C, which was found to minimize the parasitic growth. The Ga flux was varied from 0.11 nm s^{-1} to 0.05 nm s^{-1}. The results are shown in figure 2, which displays the corresponding length and diameter distributions. The decrease of Ga flux produces a drop in nanowire length, broadening its distribution (see figure 2(a)), although without presenting a clear trend. The diameter distribution is very sensitive to the Ga flux: the mean diameter shrinks from ~160 nm to ~50 nm as the Ga flux is decreased (see figure 2(b)). Figure 2(c) shows the nanowire density at different Ga fluxes. The decrease of Ga flux results in a broadening of the length distributions and reduction of the mean diameter, as well as a fall in density. Figures 2(d)–(f) show the typical scanning electron micrographs of as-grown GaAs nanowire samples. A pronounced decrease in nanowire diameter and density at decreasing Ga fluxes is observed. While the increase of the nanowire diameter with the Ga flux is expected and was reported earlier in [9], narrowing of the diameter distribution has not been discussed before.

3.2. The model

A common feature of the nanowire morphologies presented here is rather broad distributions of length and diameter. The nanowire density seems to be directly linked to the growth temperature and Ga flux. In contrast to the standard vapor-liquid-solid (VLS) growth procedures where metal catalyst particles are prepared before the material deposition [23, 25–28], our self-assembled approach makes use of Ga droplets that form concomitantly with nanowires [29]. Therefore, rather than having all nanowires emerging instantly at $t = 0$, different nanowires nucleate and start growing vertically at different moments of time $0 \leqslant t_0 \leqslant t$, where t is the total deposition time. This important feature requires a careful investigation of time-dependent nucleation of nanowires and nanowire statistics, a problem that, to the best of our knowledge, has not been addressed so far. On the other hand, self-catalyzed III–V nanowires usually grow not only vertically, but also extend radially [30, 31]. This is due to an excessive group III influx into the reservoir in the Ga droplet. Without accounting for different starting times for growth as well as the radial extension, the deterministic length-radius, length-time and radius-time correlations (which usually assume instantaneous nucleation from preexisting catalyst particles and a time-independent nanowire radius, defined by the size of these particles [23, 26, 27]) would not give the adequate description of self-catalyzed growth in our experimental conditions.

Consequently, in our modeling we consider the random nucleation of Ga droplets (which then act as nanowire growth seeds with a certain yield coefficient [32]) occurring alongside the nanowire growth itself. The model is illustrated in figure 3(a) and described in the following. The gallium and arsenic species arrive onto the substrate surface, and the Ga droplet surfaces at the rates I_3 and I_5, respectively, measured in atoms per unit time per unit area. When Ga and As adatoms meet on the surface, they form the parasitic (polycrystalline) GaAs islands at the rate K_{35}(nm^2 s^{-1}). Dimerization of two Ga adatoms at the rate K_3 will subsequently lead (with a certain probability) to the nucleation of Ga nanodroplets and ultimately nanowires. Both processes are expected to be associated with the formation of 'craters' or even the openings penetrating through the oxide toward the substrate surface [29, 33, 34]. Therefore, the rate constants K_3 and K_{35} should be orders of magnitude lower than that given by the effective

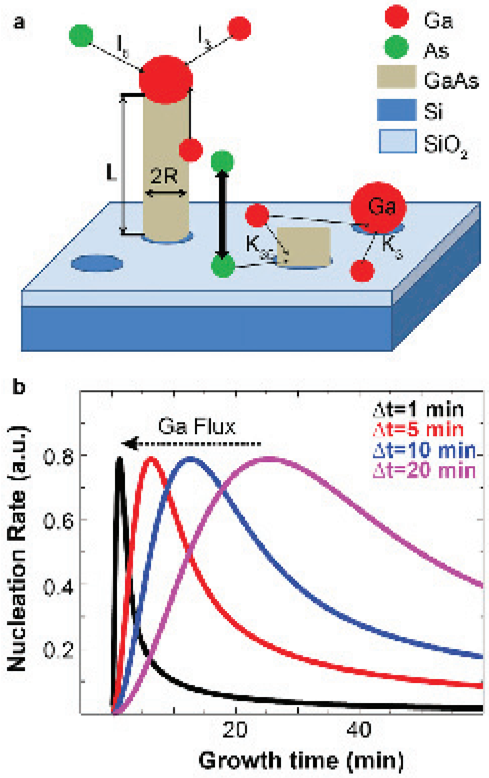

Figure 3. (a) Schematics of different kinetic processes considered within the growth model: (i) formation of Ga droplets from two Ga adatoms in the 'craters'; (ii) formation of parasitic GaAs islands from Ga and As atoms in the craters and (iii) nanowire growth catalyzed by Ga droplets, with the model parameters described in the text. In (b) the time dependence of the nucleation rate of Ga droplets at different nucleation times Δt is shown.

Ga diffusivities ($\sigma_3 D_3$ and $\sigma_{35} D_3$, with σ as the corresponding capture coefficients [35–37]).

Within the frame of the irreversible growth model, that is, with neglect of decay of both Ga-Ga and Ga-As surface dimers [35–37], the set of kinetic equations for the surface density of Ga droplets (N_3), parasitic GaAs islands (N_{35}) and Ga adatoms (n_3) can be written as

$$\frac{dN_3}{dt} = K_3 n_3^2;$$
$$\frac{dN_{35}}{dt} = K_{35} n_3 n_5 \cong K_{35} n_3 I_5 \tau_5;$$
$$\frac{dn_3}{dt} = I_3 - K_3 n_3 N_3 - K_{35} n_3 N_{35}. \tag{1}$$

Here, we assume that the kinetic growth constants are the same for differently sized surface clusters, as in [36] and [37]. The first equation shows that the number of Ga droplets increases due to the Ga-Ga dimerization, with $K_3 n_3^2$ as the nucleation rate in irreversible growth [37]. The second equation gives the nucleation rate of parasitic GaAs islands, where we assume that the unknown concentration of As adatoms quickly equilibrates with the vapor atomic flux I_5: $n_5 \cong I_5 \tau_5$, with τ_5 being the characteristic lifetime of As. This τ_5 is expected to decrease very steeply with increasing surface temperature due to enhanced desorption of As. The third equation gives the time dependence of the Ga adatom concentration, which increases due to the vapor influx and decreases when the Ga adatoms attach to either the Ga droplets or GaAs islands.

In the large time limit where $dn_3/dt \to 0$, the Ga adatom concentration is given by the dynamic balance between the vapor flux and the adatom consumption by the growing islands and droplets:

$$n_3 = \frac{I_3}{K_3 N_3 + K_{35} N_{35}} \cong \frac{I_3}{K_{35} N_{35}}. \tag{2}$$

In all our samples, the surface area covered by parasitic GaAs is much larger than that covered by the nanowires (and hence the Ga droplets). Thus, the limiting case of $K_3 N_3 \ll K_{35} N_{35}$ should apply uniformly in these conditions. Using this n_3 in equation (1) for N_3 and N_{35}, and integrating over, we obtain the large time asymptotes of the island and droplet densities:

$$N_{35} = \left(2 I_3 I_5 \tau_5 t\right)^{1/2}; \; N_3 = \frac{K_3 I_3}{2 K_{35}^2 I_5 \tau_5} \ln\left(t/t_0\right). \tag{3}$$

We can see that the concentration of parasitic GaAs islands scales with time as $t^{1/2}$, whereas the Ga droplet concentration increases with time only logarithmically (i.e., almost saturates at large enough t). As mentioned earlier, each Ga droplet gives rise to a newly formed nanowire with the probability χ. The nanowire surface density is thus given by

$$N_{nw} = \chi N_3, \tag{4}$$

where the yield χ may depend on temperature and the Ga flux.

Despite its simplicity, our nucleation model is capable of explaining the major experimental trends:

(i). Since the leading temperature dependence of the prefactors in equation (3) should be determined by a rapidly decreasing As lifetime τ_5, parasitic growth decreases and nanowire density increases when the surface temperature is raised, as experimentally observed in figure 1.

(ii). Both N_{35} and N_{nw} increase at higher Ga flux, as experimentally observed in figure 2. Since the theoretical dependence of the Ga droplet density on I_3 is linear and the observed experimental correlation $N_{nw}(I_3)$ is superlinear, it can be concluded that the yield coefficient increases with Ga flux.

By further developing the model based on some earlier results for the growth kinetics of GaAs nanowires [31, 38, 39] and the nucleation equations [26, 40] (all the details are provided in the supplementary information), we get the

Table 1. Theoretical parameters used for fitting the length and width distributions for different samples.

T (°C)	V (nm s^{-1})	$L_{\max}$ (nm)	ΔL (nm)	Δt (min)	$2R_{\max}$ (nm)	$2\Delta R$ (nm)	C (nm min^{-1})	A (nm min^{-1})	$2R_c$(nm)
604	0.11	5050	380	4.5	145	35	84	−2.76	200
624	0.11	4500	710	9.5	195	65	75	−2.41	205
643	0.11	3400	450	7.9	210	48	57	−1.45	—
643	0.075	3200	1550	29	129	42	53	−1.55	210
643	0.05	3700	1550	25	105	38	62	−1.73	130
643	0.11/0.075	2500	650	15.5	145	42	42	−1.45/−1.69	190
643	0.11/0.05	2500	650	15.5	140	50	42	−1.45/−1.86	190
643	0.11/0.027	2500	650	15.5	135	60	42	−1.45/−2.03	190

corresponding nanowire nucleation rate in the form

$$J_{nw} = \frac{dN_{nw}}{dt} = \chi J_0 g^2\left[(t/\Delta t)^{3/2}\right]. \tag{5}$$

Here, J_0 is the known normalization constant and $\Delta t = 4^{4/3}/[3(K_3 I_3)^{1/2}]$ is the characteristic nucleation time interval for Ga droplets. The universal function $g(y)$ is given by

$$g(y) = e^{-y}\int_0^y dx\frac{e^x}{x^{1/3}}. \tag{6}$$

Hence, the nanowire nucleation rate varies at different characteristic nucleation times, as shown in figure 3(b): the larger the Δt, the more spread in time and the more delayed is the nucleation rate. The variations in the characteristic nucleation time is controlled by I_3, the group III flux. In other words, the initial Ga flux I_3 determines the distribution of diameter and lengths: a larger Ga flux yields a narrower diameter and length distributions (i.e., more uniform), since the nucleation rate over time is narrower for smaller Δt (see figure 3(b)). Instead, a lower Ga flux produces an upturn in Δt that broadens the nucleation pulse over time, resulting in wider diameter and length distributions. The model presented earlier explains very well the results of the Ga flux set of experiments, where broader distributions are observed at diminishing Ga flux.

In order to understand the length and radius distributions of self-catalyzed nanowires and to describe their evolution with the growth time, we now consider the nanowire growth itself. According to the model described in detail in [31], the nanowire elongation rate is proportional to the difference between the impinging atomic As flux and desorption flux, while the surface diffusion of As can be neglected [38, 39]. In contrast, Ga is not expected to desorb from the droplet at temperatures below 650 °C, but can easily migrate from the nanowire sidewalls to the droplet. The increase of the droplet volume is determined by the effective Ga-to-As imbalance. In fact, the decrease of Ga flux leads to smaller diameters, as already reported in figure 2(b), whereas a temperature increase produces a diameter expansion (see figure 1(b)), related to the decrease in As lifetime τ_5.

These considerations yield our main results for the length (L) and radius (R) distributions of self-induced nanowires given by

$$f(L,\ L_{\max}) = const\ \times\ g^2\left[\left(\frac{L_{\max} - L}{\Delta L}\right)^{3/2}\right]; \tag{7}$$

$$F(R,\ R_{\max}) = const\ \times\ \frac{1}{B/R - |A|}g^2\left[\left(\frac{R_{\max} - R}{\Delta R}\right)^{3/2}\right]. \tag{8}$$

Here, g is the same function as in equation (6), whereas $L_{\max}$ and $R_{\max}$ are the maximum length and the maximum radius of the nanowires having nucleated at the very beginning of GaAs deposition. The parameters ΔL and ΔR describe the widths of the length and radius distributions. Both ΔL and ΔR are proportional to Δt. The A and B in equation (8) are the kinetic coefficients that can be obtained by fitting the time dependences of the mean length and diameter (see supplementary information). As usual in the deterministic growth theories [26, 37, 40], the size distributions reflect the shape of the time-dependent nucleation rate, inverted in such a way that zero moment of time corresponds to the maximum size of nanowires. Full details of derivation of the key in equations (7) and (8) are given in the supplementary information. Clearly, with the measured $L_{\max}$, $R_{\max}$, A and B, theoretical length and diameter distributions of nanowires contain only one fitting parameter: the corresponding distribution width (ΔL or ΔR), which is determined by the random character of nucleation. The parameters used for fitting the experimental length and diameter histograms in figures 1, 2 and 6 are listed in table 1, in which the critical radius R_c is defined as $R_c = B/|A|$, $V = \Omega_{35} I_3 \cos\alpha_3$ is the Ga deposition rate, $\Omega_{35} = 0.0452\ \text{nm}^3$ is the elementary volume per GaAs pair in the solid state and $\alpha_3 = 45°$ is the incidence angle of the Ga beam with respect to the substrate. The parameter C is obtained from $L_{\max} = Ct$ for the total growth time $t = 60$ min and the characteristic nucleation time Δt from $\Delta L = C\Delta t$ (see the supplementary information for the details).

Figure 4 summarizes the effect of Ga flux variations at a constant temperature and the effect of temperature variations at a constant Ga flux over the nanowire diameter and density. By augmenting Ga flux, diameter and density increase (figure 4, blue arrow); a similar behavior is observed in the case of temperature increase (figure 4, black arrow). Therefore, within the classic growth approach where the Ga flux is kept constant during growth, small nanowires (<100 nm) can

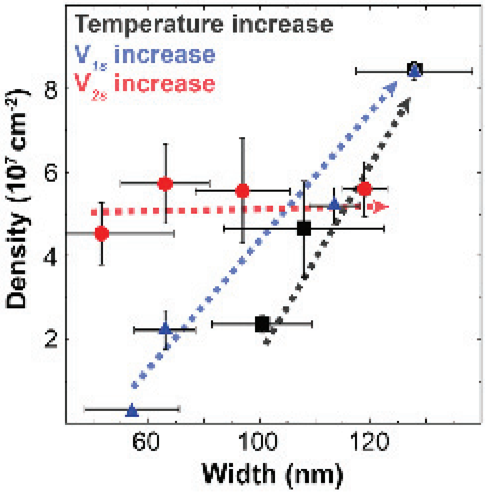

Figure 4. Diameter-density correlation of (i) one-step Ga series (blue triangles), (ii) temperature series (black squares) and (iii) two-step Ga series (red circles). (i) The increase in Ga flux (blue arrow) results in larger diameters and denser nanowire forests. In a similar fashion, (ii) higher growth temperature increases diameter and density (black arrow). (iii) In the case of two-step Ga flux series, the decrease of the Ga flux at the second step (red arrow) lowers down the nanowire diameters without changing the density values.

be achieved only at the compromise of low density, and vice versa (see figure 4).

3.3. Alternative two-step approach

We now turn to the implementation of our model for the reverse engineering of diameter, length and density. In order to combine a high density of nanowires with small diameters, we grew nanowires in a two-step fashion. We initiated the growth at a high Ga rate (0.11 nm s^{-1}) in view of achieving a high nucleation rate (i.e., high nanowire density). Then after 30 min of growth, we decreased the Ga rate in order to suppress supplementary nanowire initiation and to decrease the nanowire diameter by consuming some additional Ga from the droplet.

Figures 5(a) and (b) show the corresponding length and diameter distribution, respectively. The nanowire length does not seem to be affected by decreasing the Ga flux at the second growth step. Conversely, the diameter progressively diminishes as the Ga flux at the second step is decreased (from ~90 nm to ~40 nm). Figure 5(c) displays the nanowire densities at different Ga fluxes at the second step, showing that density is not affected by the Ga flux variations. Figures 5(d)–(f) show the typical scanning electron micrographs of the as-grown samples, where the diameter decreases at diminishing Ga flux at the second step is clearly observed.

The diameter-density results for the two-step Ga fluxes are also shown in figure 4 (red arrow) in comparison with the single-step Ga flux series and with the temperature series. Very importantly, the decrease of the Ga flux at the second step yields much smaller nanowire diameters, while the nanowire density remains relatively constant. Such a result could not be achieved by simply varying the Ga flux or temperature in the one-step procedure. The two-step Ga approach is thus very useful for tailoring the nanowire diameter and obtaining the predefined diameter-density combinations: the diameter is controlled by the Ga flux at the

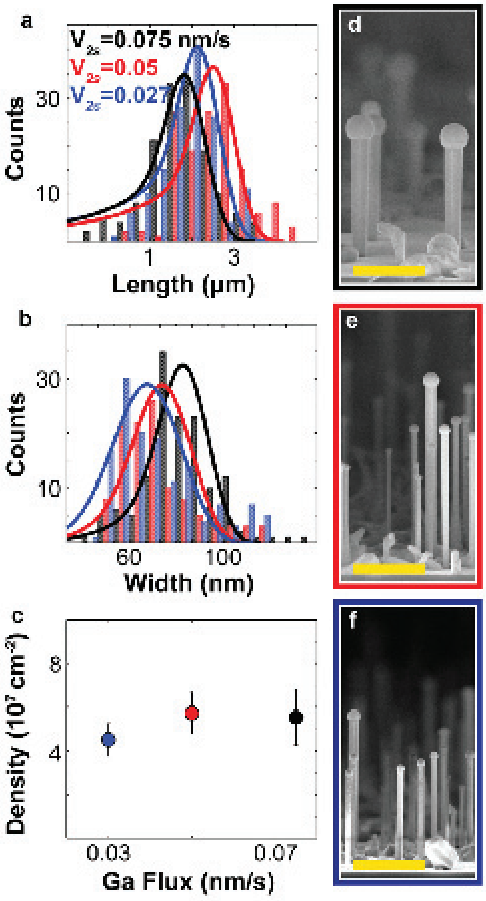

Figure 5. Length (a) and diameter (b) distributions of self-catalyzed GaAs nanowires grown at a fixed temperature of 643 °C and initial Ga flux (V_{1s} = 0.11 nm s^{-1}) for the first 30 min, but different Ga fluxes (V_{2s} = 0.075 nm s^{-1}, V_{2s} = 0.05 nm s^{-1} and V_{2s} = 0.027 nm s^{-1}) for the second 30 min. The lines in (a) and (b) are the fits obtained from the model, with the parameters summarized in table 1. In (c) the evolution of nanowire density over different Ga fluxes is reported. (d), (e) and (f) show the scanning electron micrographs of the nanowires grown, respectively, at the three different Ga fluxes for the second 30 min. The scalebar is 1 micrometer.

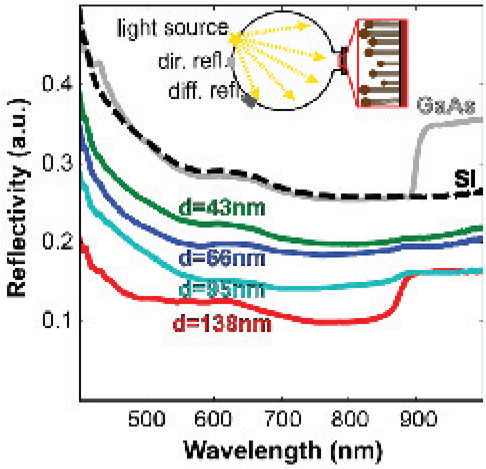

Figure 6. Reflectivity of the GaAs nanowire ensembles grown on Si (111) with different Ga fluxes at the second step (relating to different mean diameters *d*), compared to the reflectivity of Si and GaAs wafers. The nanowires grown at low Ga flux ($V = 0.03\ \mathrm{nm\ s^{-1}}$, $d = 43$ nm) present reflectivity around 25%. The increase of Ga flux at the second step progressively enhances the light absorption, which is greater than 85% for the highest Ga flux due to the increased nanowire diameter ($d = 138$ nm). Around 900 nm, the absorption decrease is observed, related to the GaAs band gap and is more pronounced for GaAs wafer and the widest nanowires with $d = 138$ nm. The inset illustrates schematics of the setup used for the reflectance measurements.

second step, while the density is determined by the growth parameters during nucleation.

3.4. Absorption measurements

The control of nanowire diameter and density is important for the application of nanowires in solar cells. In particular, it has been shown previously that the absorption rate is only enhanced for certain diameters [13–15]. In order to extrapolate the potential of these nanowire ensembles for solar cell applications, we assess their reflectivity properties in the experiments with an integrating sphere. Figure 6 shows the results of the spectral reflectivity measurements of the GaAs nanowire ensembles with similar density and different diameter, obtained by changing the Ga rate at the second step as described earlier. The reflectivity of the nanowire samples is shown in comparison with the measured reflectivity of Si and GaAs wafers. The nanowires obtained at the Ga rate of 0.027 at the second step (with smaller diameters, $d = 43$ nm) have a reflectivity ~0.25 in the entire spectral range. These relatively high values are expected because of the low density of nanowires and the diameter outside the absorption resonance range [14, 15]. Interestingly, the reflectivity is reduced below 0.15 for the nanowire ensemble with the largest mean diameter ($d = 138$ nm), the one obtained with a $0.085\ \mathrm{nm\ s^{-1}}$ Ga flux at the second stage. This enhancement is obtained by just increasing the diameter of the nanowires for the same surface density.

4. Conclusion

We have shown that the nanowire length and diameter distributions are the consequence of a time-dependent nucleation process, which is controlled by group III flux and temperature. Within this kinetic approach involving random nucleation of Ga droplets and consequently GaAs nanowires, the nanowire density is established at the initial nucleation step, while the diameter can be tuned by the Ga flux at a later growth stage. As a result, we have demonstrated an independent control of the nanowire density and diameter over time. This method allows one to circumvent the challenge of cost-ineffective lithography for organizing the Ga growth seeds and to control the nanowire diameter just by the Ga flux. We have shown how the control of nanowire diameter and density determines the reflectivity, with the best values below 0.15. This result may constitute the first step towards obtaining a nanowire-based solar cell using the fully self-assembled process. The self-assembled approach is very attractive for applications where the broad length and diameter distributions do not degenerate the required properties. More generally, our procedure combines features of the deterministic VLS growth of nanowires and random self-assembly of surface islands. We have shown that the usual assumption, an instantaneous nucleation of nanowires [17, 25, 31–33] does not work for Ga-catalyzed growth of GaAs nanowires, and could significantly change the deterministic growth picture of VLS nanowires in general.

Acknowledgments

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4.4 Summary

In this chapter we have investigated the underlying mechanisms in GaAs nanowire growth that control the density-diameter relations. We have studied the effect of Ga flux and temperature on the nanowire properties. These observations lead to the development of a kinetic model that consider the characteristic nucleation time controlled by group III flux and temperature, which controls the diameter and density distributions of GaAs nanowires. This understanding was leveraged to grow nanowire forests with tailored diameter-density distribution. We also measured the optical properties of nanowire forests as a function of their diameters and density and compared them to what is expected from the theoretical predictions, showing the coherent behavior between them.

5 Conclusions

In this thesis we have investigated the **growth related aspects of GaAs nanowire growth on Si for photovoltaic applications**. Our **approach** was **VLS** mechanism driven, **Ga-catalyzed**, via **self-assembly**, by means of **MBE** technique. We first identified the **key properties** to pave the way for the development of nanowire based photovoltaic technologies: the nanowires **diameter** needed to be controlled to optimize **light absorption**, nanowire **density** to **minimize material utilization** and nanowire **orientation** to build **symmetric junctions**. The control of these properties and the understanding of the underlying mechanisms that influences them were the objective of this work.

We investigated the steps before nanowire growth and the early stages of it. A particular focus was given to the influence of the silicon oxide in the growth process, since its role was not yet clarified. We first characterized oxides produced via different fabrication techniques, such as native oxide, thermal oxide and Hydrogen Silsesquioxane. The different processes resulted in oxide films with different chemical composition, roughness, and critical thickness to achieve nanowire growth. **With this first work we identified surface roughness, oxide stoichiometry and thickness as key parameters in nanowire growth**. This preliminary study was also instrumental to choose to further investigate native oxide for its uniform properties and simple fabrication steps.

By **controlling the native oxide thickness on the sub-nanometer level**, resulted in subtle **changes in wettability and chemical composition as** function of oxide **thickness**. We demonstrated a correlation between **oxide** chemical **composition and** its **thermal stability**. This insight together with the selective collection of Ga in the holes formed into the oxide film, **explain**ed the change in density of nucleation sites, **material collection** and **nanowire density** at different oxide thicknesses. **The wetting properties and the aspect ratio of the holes in the oxide film** determined the droplet positioning, which **controlled the growth morphologies and nanowire orientations**. Achieved control over the latter, the nanowire properties left to be mastered were diameter and density. We studied the underlying mechanisms that control them via **Ga flux and temperature**. We discovered them to **influence the start of nanowire growth**, and described the mechanism with a kinetic model. The latter considers the characteristic nucleation time to be controlled by Ga flux and temperature, **which control the diameter and density distributions** of the nanowires. The insight was **instrumental to develop a novel approach** to grow nanowire forests with **tailor**ed **diameter-density distribution**. To **demonstrate** the modification of the **optical properties of the nanowire**

ensembles as a function of their diameters and density we measured the reflectivity of arrays with comparable density but different diameters.

On the experimental level this work lead to a simple reproducible method to have high density high yield of vertical nanowires, and provide the tools to tune their diameters to tune light absorption. On the theoretical level it provided the **understanding of the role of the native oxide layer in the growth process**: upon **exposure to high temperature in UHV** it locally evaporates, **lead**ing **to the formation of holes in the film**. These discontinuities are the nucleation sites **where Ga gets collected**. The **wetting properties** of the film, together with the **aspect ratio of the holes** play a major role in **controll**ing the **growth morphology**. Large aspect ratio holes produce either tilted nanowires or polycrystalline material, depending on the wetting properties. The knowledge developed can also be extended to the case of patterned growth and paves the way towards the control of nanowire orientation independently on the oxide thickness.

To summarize, in this thesis we have demonstrated the importance and the role of the oxide layer in nanowire growth as key parameter to control nanowire orientation and density. We have also proven the relevance of the early steps of growth to tune nanowire properties, which need to be mastered for high performance photovoltaic. We believe this work provides fundamental insights from both a fundamental and application point of view, paving the way for the development of GaAs nanowire photovoltaic technologies.

5.1 Future Outlook

The work described in this thesis contributes to the continuing trend of understanding the fundamental aspects involved in nanowires growth to better achieve control other their properties. The novelty presented here consist in the consideration of the surface properties' influence in the VLS growth. The detailed investigation of the chemical composition, wetting properties and thickness of the oxide layer showed the variation of its surface properties. The tailoring of them demonstrated their influence over the growth process resulting in different morphologies. The responsibility of the oxide' chemical composition in the pinhole formation, in the wetting and in the droplet positioning had been identified. These findings put in a different light the growth process: surface properties have to be considered to achieve reproducible high yield of vertical nanowires, on top of the other process parameters (e.g. Ga flux, As flux and growth temperature). At the same time this work open new challenges.

Achieve control of the wetting properties independently of the native oxide thickness is one of them. A successful outcome would allow high yield of vertical nanowires with narrow diameter and length distributions, independently on nanowire density and oxide thickness. In this direction, surface treatments to engineer the wetting is worth to be investigated, as well as the catalytic droplet alloying to tune the surface tension.

Specifically for the self-assembly case, an ultimate challenge lays in controlling holes' formation in order to remove any polycrystalline formation from the surface and have exclusively vertical nanowire. To explore this opportunity, localized doping of the bare Si surface to then regrow the oxide layer on top is one of the possibilities to deepen the understanding of the hole formation and its localization.

Nevertheless, the present work also impacts the pattern growth. In this field the exploration of new hole geometries from a modeling standpoint, and their influence over droplet positioning can potentially lead to new designs which can tune growth morphology independently of oxide thickness and wetting properties.

On a more fundamental note, given the change of surface properties at different oxide thicknesses, it is reasonable to expect different Ga diffusion lengths depending on the oxide. The measurements of those would supply valuable inputs for the modeling, where so far only constant diffusion lengths had been considered. A deeper grasp of the fundamental steps of growth would also provide useful insights in a device perspective, to better understand doping incorporation in nanowires and structures of different size and geometries. Finally, from an application standpoint the optimization of the junction design, the development of the effective surface passivation methods and contacts are crucial to open the way to the development of nanowire technology for photovoltaic applications. In this mindset, the transfer of the MBE developed knowledge to more scalable techniques such as MOCVD technique would further pave the way to the technology price-competitiveness.

Appendix

In this appendix the Supplementary Information of the publications I, II, III, and IV are reported.

SI Publication I

Supplementary Information of: Ga-assisted growth of GaAs nanowires on silicon, comparison of surface SiOx of different nature

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1 Annealing effect

In this section the annealing effect over oxide thickness and roughness is investigated. The different substrates have been annealed (called "degas") in a first place in UHV for 2 hours at 500 ($^{\circ}C$) (unless differently specified) in a separate chamber. The characterization by means of ellipsometry and AFM to determine thickness and roughness was performed within a day after unloading. The results reported in Table 1 show a different effect of annealing over thickness and roughness of the different oxides:

- In the case of native oxide a different behavior is observed for Siltronix and Virginia. For the latter roughness and thickness are not affected by degassing. This is not the case for Siltronix, where an increase of roughness (from 0.8±0.5 nm to 5.3±0.5 nm) is observed. Such a different behavior might be related to the different Si/SiO_2-interface.
- Thermal oxide's thickness is not affected by degassing, whereas roughness decreases from 3.4±0.5 nm to 1.3±0.5 nm. The high roughness reported before degassing is due to the wet etching process that is not homogeneous over the wafer. The degassing seems to rehomogenize the surface morphology.
- The HSQ oxides investigated have been prepared with different techniques, as reported in section 4. The HSQ etched show a decrease in thickness (from 9.4±0.9 nm to 8.8±0.9 nm) an increase in surface roughness after degassing (from 1.1±0.5 nm to 3.1±0.5 nm), differently for the as spun roughness decreases (from 3.6±0.5 nm to 1.2±0.5 nm). The different behaviors of of the HSQs upon degassing is explained with the preparation technique (see section 4).

Table 1: Thickness and roughness of different types of oxides before and after the pre-growth annealing of 2 hours. The measurements have been performed by ellipsometry and AFM.

Oxide Type	Annealing ($^{\circ}C$)	Thickness (nm)		Roughness RMS (nm)	
		Before	After	Before	After
Native Oxide (Virginia)	500	0.9±0.6	0.8±0.6	0.3±0.5	0.5±0.5
Native Oxide (Siltronix)	500	2.3±0.6	2.1±0.6	0.8±0.5	5.3±0.5
Thermal Oxide	500	1.4±0.6	1.2±0.6	3.4±0.5	1.3±0.5
HSQ Etched	300	9.4±0.9	8.8±0.9	1.1±0.5	3.1±0.5
HSQ As Spun	300	8.1±0.6	8.1±0.6	3.6±0.5	1.2±0.5

2 Interfacial nature of interstitial oxide

In this section is shown that the $Si-O-Si$ absorption band is characteristic of Silicon-Silicon Oxide interface. In Fig. 1 the normalized FTIR spectra of HSQ and sputtered oxide on GaAs (111) substrates show a main absorption band is at $1226cm^{-1}$, but no characteristic absorption of $Si-O-Si$ is observed.

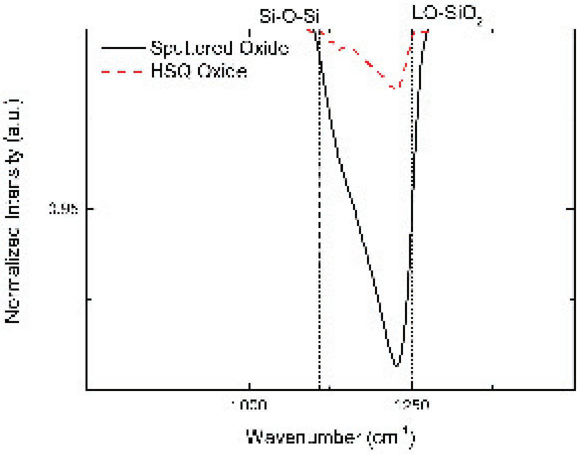

Figure 1: ATR-FTIR spectra of $6nm$ HSQ oxide "as Spun" (red) and 20nm sputtered oxide (black) on GaAs (111) substrate. In both the spectras a main absorption band is observed at $1226cm^{-1}$, corresponding to substoichiometric Silicon oxide. No characteristic $Si-O-Si$ absorption band ($1107cm^{-1}$)is observed; this suggest that the Si-O-Si formation is characteristic of the Silicon-Silicon oxide interface. The spectra has been normalized to better show the absorption bands.

3 Photolitography technique to achieve different oxide thicknesses

In this section a photolithographic technique to achieve different oxide thicknesses on the same wafer is presented. A 4-fold symmetry mask has been prepared, as shown in Fig. 2, to open sequentially windows in the photoresist to etch the oxide below. If the windows are not open the oxide is not etched, being covered by the photoresist. The sequential opening of the windows in the photoresist allow the etching to start at different oxide thicknesses. The coupling of such a technique together with a low etch rate solution (1 nm/min) allow a fine control of the oxide thickness.

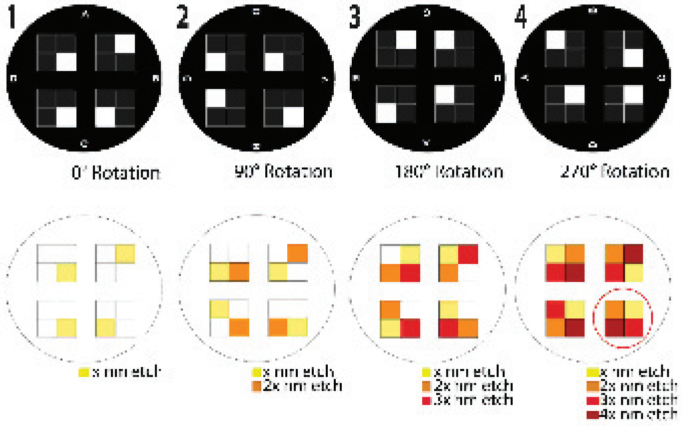

Figure 2: Photolithography steps to obtain different thicknesses of oxide on the same wafer. In the upper line the mask is represented, and below the wafer is shown. Before the first exposure the wafer with oxide is covered by photoresist. As shown in (1) by exposing and developing a window is formed in the photoresist; through such window the oxide in the area is etched down by wet etching with buffered HF solution ($NH_4F : HF$ 500 : 1) with low etch rate ($\sim 1 nm/min$). (2)Then the mask is rotated of 90°and the wafer is exposed and developed again to open a second window in the photoresist, in order to etch down the oxide in the "new" window and the "old" window. By repeating other two times the rotation of the mask of 90°C steps the result shown in (4) is obtained: four different thicknesses of oxides in the same wafer (red circled) on which growth will be performed. The color scale from yellow to red show the increase of etched thickness.

4 HSQ processing effects

Prior to growth and in order to ensure desorption of all volatile components from HSQ, all substrates were degassed in UHV at 400 °C for 2h. The as spun and etched HSQ substrates have been characterized before and after pre annealing-growth, in terms of roughness (see Tab. 1) and chemical composition (see Fig. 3).

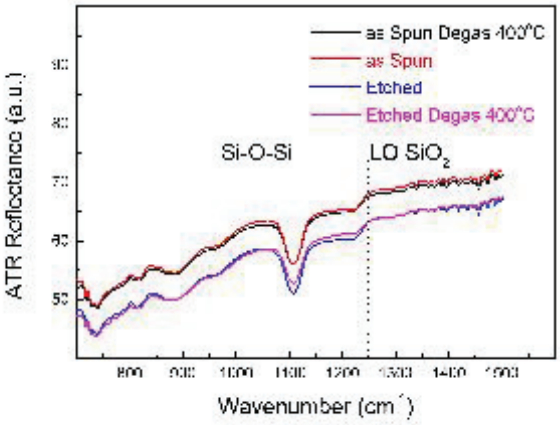

Figure 3: (Color Online) The evolution of the ATR-FTIR spectra before and after the annealing step previous to growth is shown. In the case of the *as spun* no variation is observed, whereas in the case of the *etched* a decrease of intensity of the absorption bands of $LO\ SiO_2$ and of $Si-O-Si$ was observed. Such a decrease observed in the IR spectra is supported by an observed decrease in oxide thickness (see Tab. 1).

It is interesting to note that the as spun HSQ has initially higher roughness (3.6nm) than the etched HSQ (1.1nm). On the other hand after the pre-growth annealing the trend is reversed: the etched HSQ is rougher (3.1nm) than the as spun (1.2nm). This behavior is due to the intrinsic nature of HSQ: if initially a thinner film is prepared, more volatile components leave the oxide compared to a thicker oxide.[1, 2] The effect of more volatile components leaving the oxide is higher roughness in the case of as spun HSQ, compared to etched HSQ. Then, during pre-growth annealing the as spun HSQ homogenize and decrease roughness (from 3.6nm to 1.2), leaving its thickness unchanged (8.1nm). On the other hand the roughness of the etched down HSQ increases after annealing (from 1.1nm to 3.1nm), and decreases its thickness (from 9.4nm to 8.8nm), due to the release of volatile components.

References

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SI Publication II

Supporting Information Available

Oxide Thickness

The reliability of the ellipsometry measurements was assessed by AFM. The oxide thickness of the oxidized Si (111) wafer was first measured by ellipsometry, then patterned with a periodic array of microdots and etched with a BHF solution (7:1) for 2 minutes. The result of this process was an array of equally spaced microdots of native silicon oxide on Si (see **Figure *24*** (a),(b)). The measured oxide thickness by ellipsometry was 1.2±0.2 nm. The AFM scans (***Figure 24*** (a),(b)) report a step height of ~1.3±0.2 nm (see **Figure *24*** (c)), confirming the reliability of the ellipsometry measurements.

Nucleation time and native oxide thickness

In order to investigate the influence of the native oxide thickness on nanowire nucleation we performed Reflection High Energy Electron Diffraction (RHEED) experiments. In the case of 1.0nm oxide thickness we observed nucleation (i.e. the characteristic diffraction pattern of ZB) below 10 seconds, whereas at 1.1,1.2 and 1.7nm the measured nucleation time was respectively 34, 140 and 400 seconds (see ***Figure* 25** (a)). For comparison purposes, the samples, on which the RHEED experiments were performed, were grown for 5min (excluded the

1.7nm sample which was grown for 7min). The SEM micrographs are reported in ***Figure* 25** (b)-(e): (b) at 1nm of oxide a high density of nanowires with diameter below 40nm and length ~500nm is observed. (c) Already at 1.1 nm a decrease in nanowire length is observed. The same trend is observed at 1.2 and 1.7nm, together with a decrease in nanowire density. The SEM micrographs are in agreement with the delay of the nucleation time induced by the native oxide thickness. The small nanowire diameter obtained at 1.7nm of oxide thickness after 5min (see ***Figure* 25** (e)) are in agreement with the small droplet diameter (~60nm) observed at 1.5nm oxide. Therefore the apparent contradiction of the increasing nanowire diameter and shrinking droplet diameter at raising oxide thickness is understood as follows: for high oxide thickness (>1.3nm), the nanowire diameter is small at the early steps of growth due to the small Ga droplets given by the poor wetting of the oxide. However, the nanowire diameter dramatically increases during growth, because of the high material feed related to the low density of nanowires.

Ga droplets and pin-hole formation

The result of the Ga deposition at different oxide thicknesses is shown in **Figure *26***. Even though the Ga deposition conditions were kept identical, a dramatically different droplet dimension was observed: at ~0.1nm of oxide thickness, droplets of diameter above 2μm were observed (see **Figure *26*** (a)), whereas at oxide thicknesses of 0.4, 0.6, 0.9, 1.1, 1.2 and 1.5nm the droplets showed a progressively decreasing diameter, down to ~60nm (see **Figure *26*** (b),(c),(d),(e),(f) and (g) respectively). The trend in droplet diameter also corresponds to a trend in volume of Ga observed on the Si substrate, as shown in Figure 2 (g) of the manuscript.

To proof the selective Ga droplet formation in the holes of the native oxide produced by heating, we removed the droplet and scanned the surface by Atomic Force Microscopy (AFM). The Ga was selectively removed by a 20 min dip in 37% HCl, which does not etch Si or SiO_2. In ***Figure 27*** (a)-(c) the SEM micrographs of the Ga deposited on respectively 1.1, 1.3 and 1.7nm of native oxide are shown. In ***Figure 27*** (d)-(f) the AFM scans of the 1.1, 1.3 and 1.7nm samples after Ga removal are reported: they show they show the presence of holes of size smaller or equal to the size of the droplets, with a density comparable to the droplet density. The outcome of this experiment is supported by previous observations about holes nucleation in native oxide of Watanabe and co-workers,[1,2] and of selective Ga deposition on Si (111) of Shibata and co-workers.[3,4]

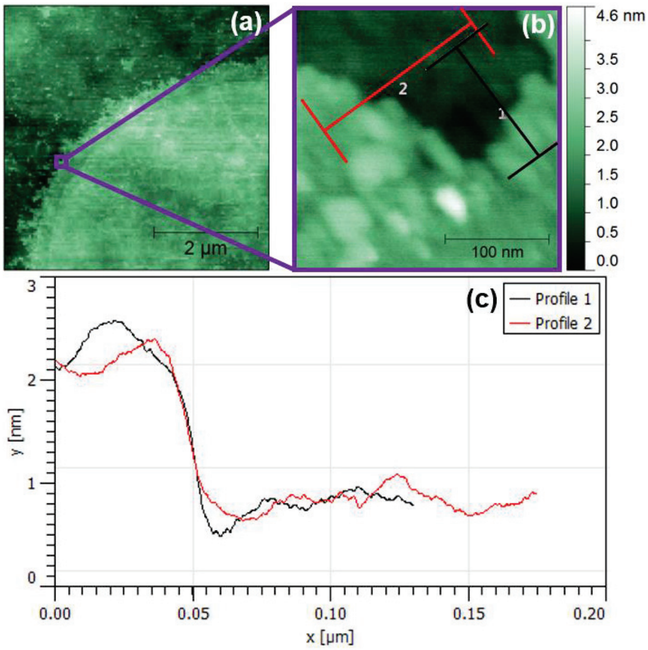

Figure 24 (a-b) AFM scan of the edge of a microdot of native oxide on Si (111) obtained by photolithography and BHF etching. (c) Height profile of the scanlines.

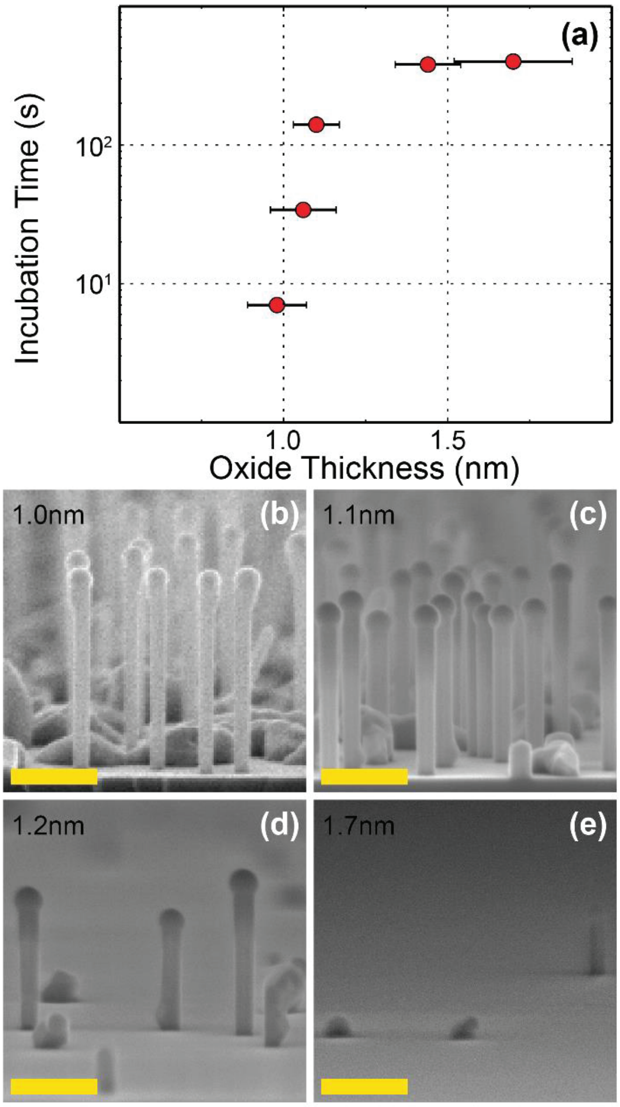

Figure 25 GaAs nanowire nucleation time measured by RHEED at different native oxide thicknesses on Si(111) substrates. SEM micrographs of the grown nanowires on 1.0, 1.0 and 1.2nm of oxide after 5min, and on 1.7nm of oxide after 7min. (respectively (b),(c),(d) and (e)). The scalebar is 200nm.

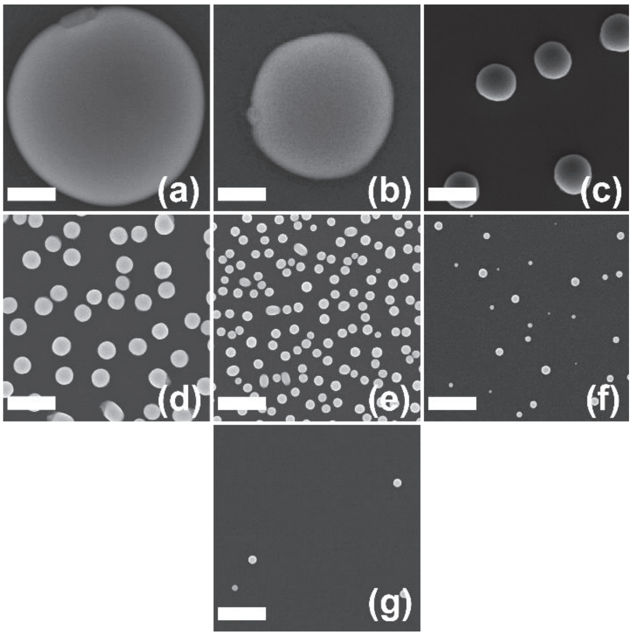

Figure 26 SEM micrographs of Ga deposition at 640°C for 5 minutes on Si (111) substrates. The latter were covered by a native oxide thickness of 0.1 (a), 0.4 (b), 0.6 (c), 0.9 (d), 1.1 (e), 1.3 (f) and 1.5nm (g). The scalebar is 200nm.

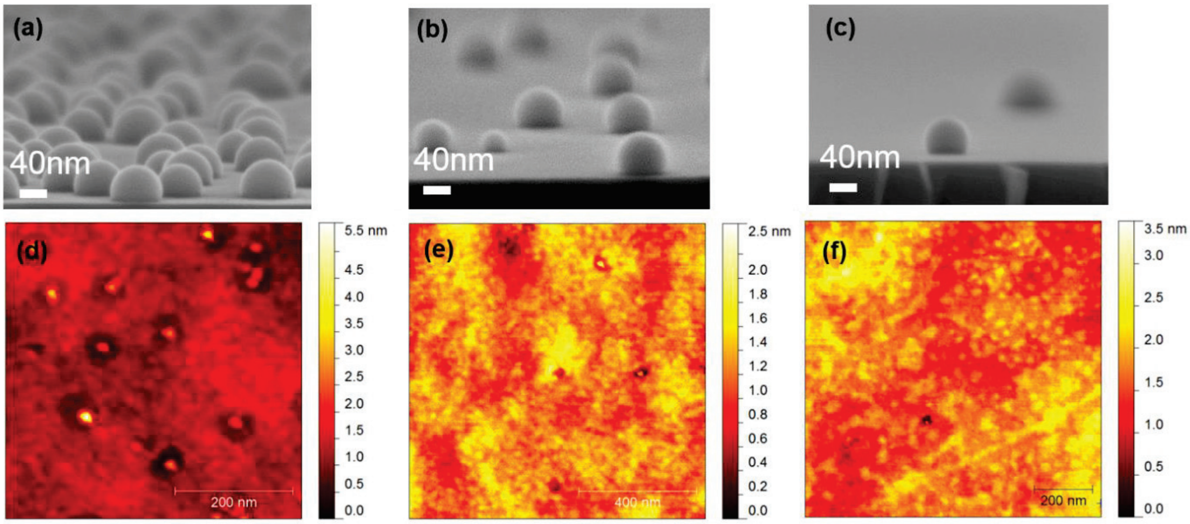

Figure 27 SEM micrographs of Ga droplets formed with 5 minutes Ga deposition at 640°C after on Si(111) substrates after the degassing step. The native oxide thickness was 1.1nm (a), 1.3nm (b) and 1.7nm (c). AFM scans of the surface of the respective different samples ((d) 1.1nm, (e) 1.3nm and (f) 1.7nm) after selective Ga etch (37% HCl, 20min) are shown.

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SI Publication III

Supporting Information Available

XPS on different native oxide thicknesses

To characterize the chemical composition of the native silicon oxide at different thicknesses we performed X-ray Photoelectron Spectroscopy (XPS). Via this technique we determined the oxidation state of Si from its binding energy. As references of no oxide we used a Si(111) wafer etched with HF on which we directly performed XPS (0.1nm); as fully oxidized stoichiometric SiO_2 we took a Si(111) coated with 17nm of thermal oxide, produced in an oxidizing furnace at ~1000°C. The different native oxide thicknesses were prepared with the method presented in [1]. The results reported in **Figure 28** (a), (b) and (c) show respectively the binding energy spectra for Si2s, Si2p and Oxygen for native oxide thicknesses of 0.1, 0.5, 0.7, 1.0, 1.2, 1.6nm and 17nm thermal oxide. In **Figure 28** (a) the Si2s metallic peak is centered at 150.5eV, whereas the oxidized Si peak progressively grow in intensity at thicker oxide, and also shift its position towards higher binding energy (SiO_2 is centered in 155.3eV). This suggest a gradual increase in Silicon oxidation by increasing oxide thickness.

Figure 28 (b) shows the Si2p metallic peak centered in 99.2eV, and the oxidized Si peak progressively increase in intensity and shift towards higher binding energy (103.2eV) (see inset expanded view). Also the observation of the Si2p bands behavior suggest an increase in Si oxidation with increased oxide thickness.

In **Figure 28** (c) the oxygen binding energy spectra is reported. The peak grow in intensity by increasing the native oxide thickness. The observations of the shifts in binding energy for Si2s, Si2p, and the increased intensity for Si2s,Si2p and O are coherent and support the interpretation of a change of chemical composition at different native oxide thickness.

Influence of oxide thickness over holes behavior at high T

In the section above we have demonstrated that the native oxide chemical composition changes with thickness. At the same time, in the main text, holes are observed to be formed upon annealing at high temperature in UHV. These two observations raise the question of the influence of the oxide's chemical composition on holes formation. Intuitively, we would expect that the chemical composition of the oxide, strongly linked to its thermodynamic stability, would influence the holes formation. However the experimental verification of such a hypothesis is challenging for oxide thicknesses below 1nm (demanding to observe randomly distributed holes of thickness <1nm via AFM). To overcome the technical hurdle and investigate the influence of oxide thickness (i.e. chemical composition) over holes formation at high temperature we first studied the correlation between droplets and holes at different deposition times (see **Figure** *24* (a)). The droplet and hole diameters were measured on the same samples but in different locations with respectively AFM and SEM. Both holes' and droplets' diameters were observed to grow at increased deposition time, but droplets were always observed to be bigger. Since droplets and holes have shown to behave coherently at different deposition time, we can assume that investigating droplet behavior is equivalent to holes. We therefore performed several Ga deposition experiments on different oxide thicknesses at different deposition times to understand on the influence of oxide thickness (i.e. chemical composition) over holes. The diameter measurements are reported in **Figure** *24* (b) as a function of the Ga deposition time for oxide thicknesses of 0.5nm, 0.9nm and 1.6nm. In all the three cases droplets' (i.e. holes) diameters were observed to increase, but at radically different rates: the thinner the oxide, the faster the growth rate, and vice-versa. These different behaviors can be understood in light of the oxide properties dependence on oxide thickness: thin oxides have low stoichiometric composition (i.e. thermodynamically more unstable) than the thicker ones. Therefore the thin oxides (<~1nm), since they are thermodynamically less stable and have less material tend to evaporate faster, resulting in a faster holes' diameter growth than the thick oxides (>1nm).

The latter have more material and are more thermally stable, therefore resulting in slow holes' diameter growth rate.

Figure ***24*** (c) shows the droplet number density as a function of deposition time for different oxide thicknesses (0.5, 0.9 and 1.6nm). Three completely different behaviors are observed: the droplets density (i.e. holes) at 0.5nm diminishes at increased deposition times, whereas at 0.9nm it first grows, peak, and decrease. Differently, at 1.6nm the droplets' (i.e. holes) density show a low but steady increase.

These apparently uncoherent results can be understood considering the different chemical compositions (i.e. thermodynamic stability) associated to the oxide thickness. When the oxide thickness is at 0.5nm the silicon oxide has lower stoichiometry than 0.9nm, and 1.6nm (i.e. lower thermal stability), leading to a more rapid oxide evaporation and hole formation. This interpretation is supported by the time series growth performed for 0.5nm oxide of 15sec and 1h reported in **Figure 30** (a)-(c). The red arrows in (a) and (b) point at small Ga droplet which start to form already after 15 sec of growth. The widespread accumulation of Ga lead to the formation of a 2D polycrystalline film, as shown in (c). In view of these observations, together with the selective deposition of Ga on Si(111), thin oxide layers (<1nm) sub-stoichiometric oxides are demonstrated to evaporate faster than thick oxides (>1nm), forming holes more easily. Above a certain holes' density they merge, leading to a density decrease and to the formation of oxide islands. This transition is well observed in the case of the 0.9nm, where density increase, peaks and decrease. In other words, the lower oxide thickness (0.5nm) is at more advanced oxide evaporation stage, where holes merge and only a decrease in density is observed. Instead, the higher oxide thickness (1.6nm), being thermally more stable, needs more time to evaporate, leading to a uniform increase of density over time. Similar behavior of oxide evaporation in thin silicon oxide films were reported by other groups [2] [3] [4], supporting our interpretation of droplets diameter and density as a function of oxide composition (i.e. thickness).

The current observations can also explain the nanowire density behavior at different oxide thicknesses reported in [1]: nanowire density was observed to drop progressively, increasing oxide thickness. If we consider that holes are the nucleation sites for droplets formation, and thus also for nanowires, the current holes' behavior at different oxide thicknesses explain those observations. At increasing oxide thickness (>~1nm) its thermal stability raise, leading to a diminished holes' nucleation rate, leading to less droplets, and therefore to less nanowires.

Vice-versa, decreasing oxide thickness, the oxide thermal stability deplete, leading to higher holes' density formation, more droplets, and thus more nanowires.

Influence of the hole aspect ratio over droplet configuration

In the main text the energy vs volume curves of droplets in different configurations for different Ga/SiOx contact angles with a hole aspect ratio (width over height w/h) of 2 were presented. In this section we investigate the influence of the aspect ratio of the holes over droplet positioning. In other words, we calculated the energy cost of each droplet configuration at different volumes in holes with different geometries, with a w/h of 2, 5 and 20. The results for 116° and 94° Ga/SiOx contact angle are presented in **Figure 31** (a)-(c) and (d)-(e) respectively. Each curve correspond to a different droplet configuration, and the background color refers to the lowest droplet energy configuration for a specific range of volumes, illustrated on top of each plot. For (a) the transitions are from a droplet sitting in a corner, to a droplet wetting the walls of the hole (V/Vhole=0.74), to a uniformly spilled droplet (V/Vhole=2.08). From a qualitative standpoint, the energy curve of each different configuration is similar, suggesting the possible presence of also other configurations. However, increasing the w/h ratio to 5 and 20 (see **Figure 31** (b),(c)) the scenario changes dramatically. The energy cost of the configurations of a droplet wetting the walls (red dashed), the spilled uniformly and non-uniformly (orange and black dashed) increase radically with respect to the droplet sitting in a corner (blue dashed), or non-uniformly spilled touching the bottom of the hole (purple dashed). It is important to bear in mind that the latter non-symmetric configuration lead to the formation of either tilted nanowires or polycrystalline growth. It is also interesting to note that increasing the w/h ratio to 20, the stability of a droplet sitting in a corner is extended up to 10 times the volume of the hole (in the case of w/h=2 the volume was 0.74 V_{hole}). A similar trend is observed also for the 94° Ga/SiOx contact angle, shown in **Figure 31** (d)-(f). Differently, the transitions from droplet sitting in a corner to non-uniformly spilled touching the bottom of the hole are verified at lower volume with compared to the

116°, as already observed in the main text. The results obtained suggest an influence of the aspect ratio of the hole over the yield of vertical nanowires: the broader the holes, the lower the yield of vertical nanowires. Since this trend could not be verified in the case of growth by self-assembly because we have no information of the hole aspect ratio at nucleation, we compared the results to the case of pattern growth. In the latter, the holes are defined by e-beam lithography into a thick (>10nm) layer of thermal oxide. In each pattern, the distance between the holes (called pitch) and the dimensions of the holes were changed. Interestingly, the most successful results were always achieved in the case of low aspect ratio (nominally w/h=1.5, measured w/h=~5), whereas an increase of the latter resulted in a dramatic decrease of the yield of vertical nanowires, as shown in **Figure 32** (a) and (b).

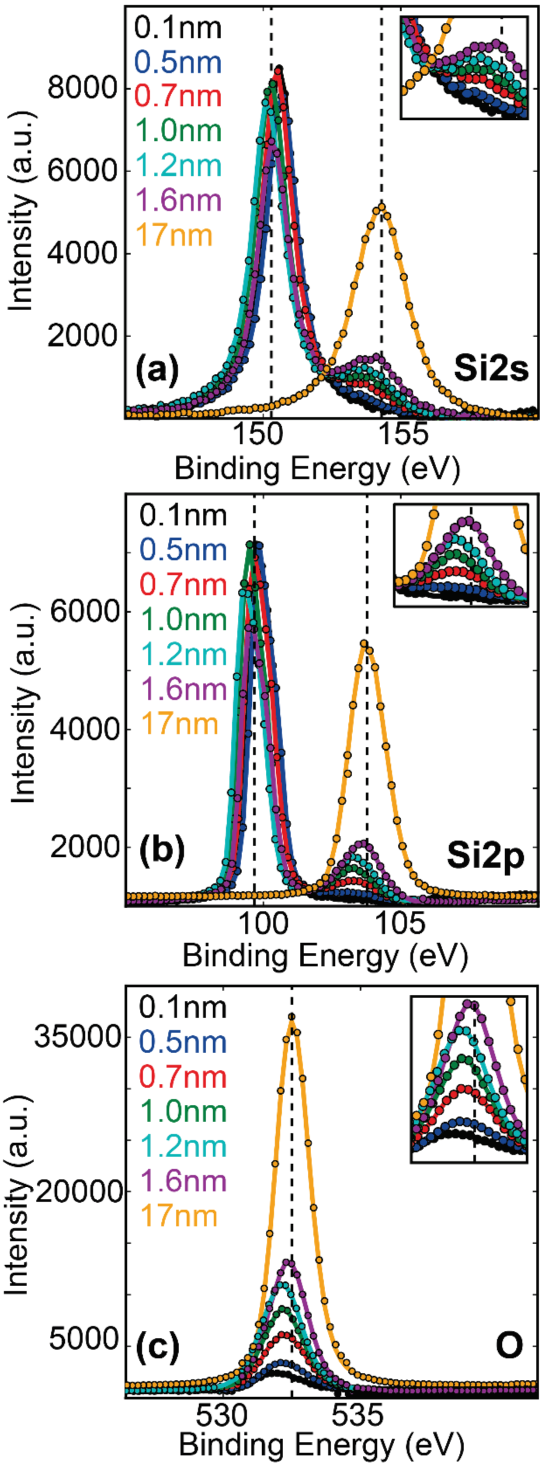

Figure 28 XPS spectra of native oxide layers of different thicknesses on Si (111) wafers. (a), (b) and (c) show respectively the Si2s, Si2p and Oxygen peaks.

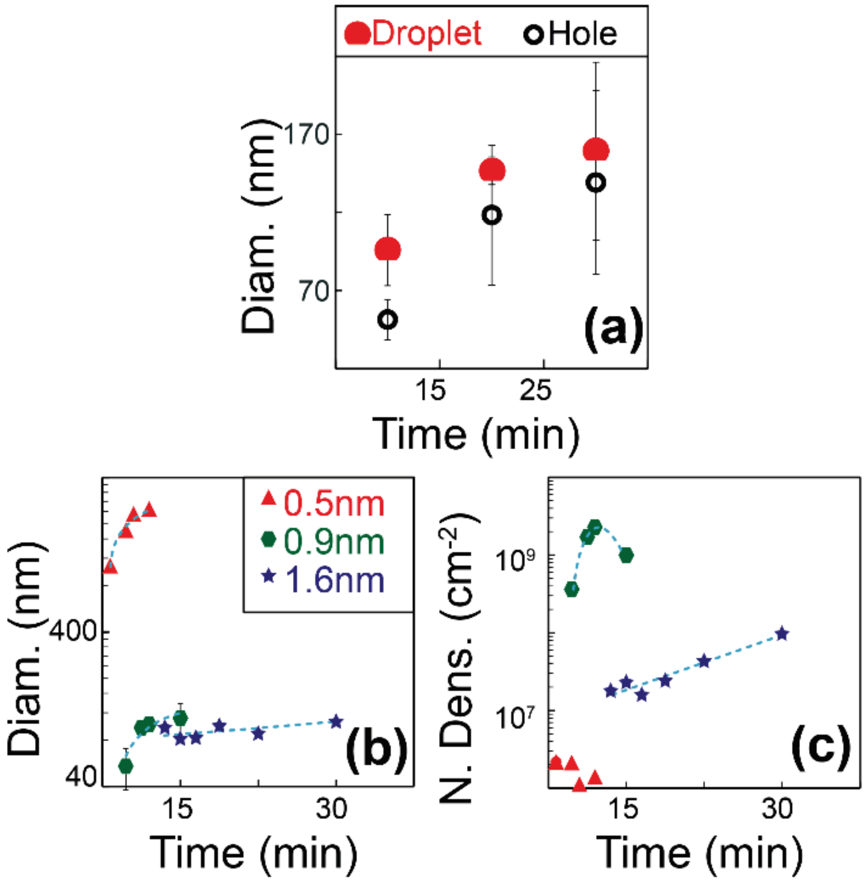

Figure 29 (a) Diameter evolution at different Ga deposition time for droplets and holes. The oxide thickness was ~1.5nm. (b) Droplet diameter and (c) density evolution at different deposition time for three different oxide thicknesses (0.5nm, 0.9nm and 1.6nm).

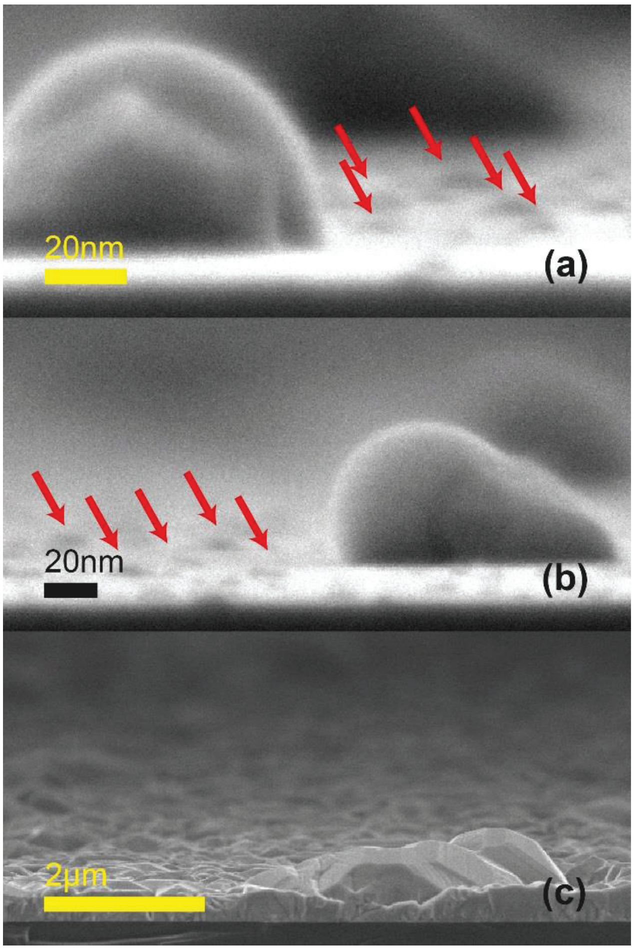

Figure 30 SEM micrographs of GaAs growth on Si(111) coated with 0.5nm oxide thickness for 15 sec (a),(b) and 1h (c).

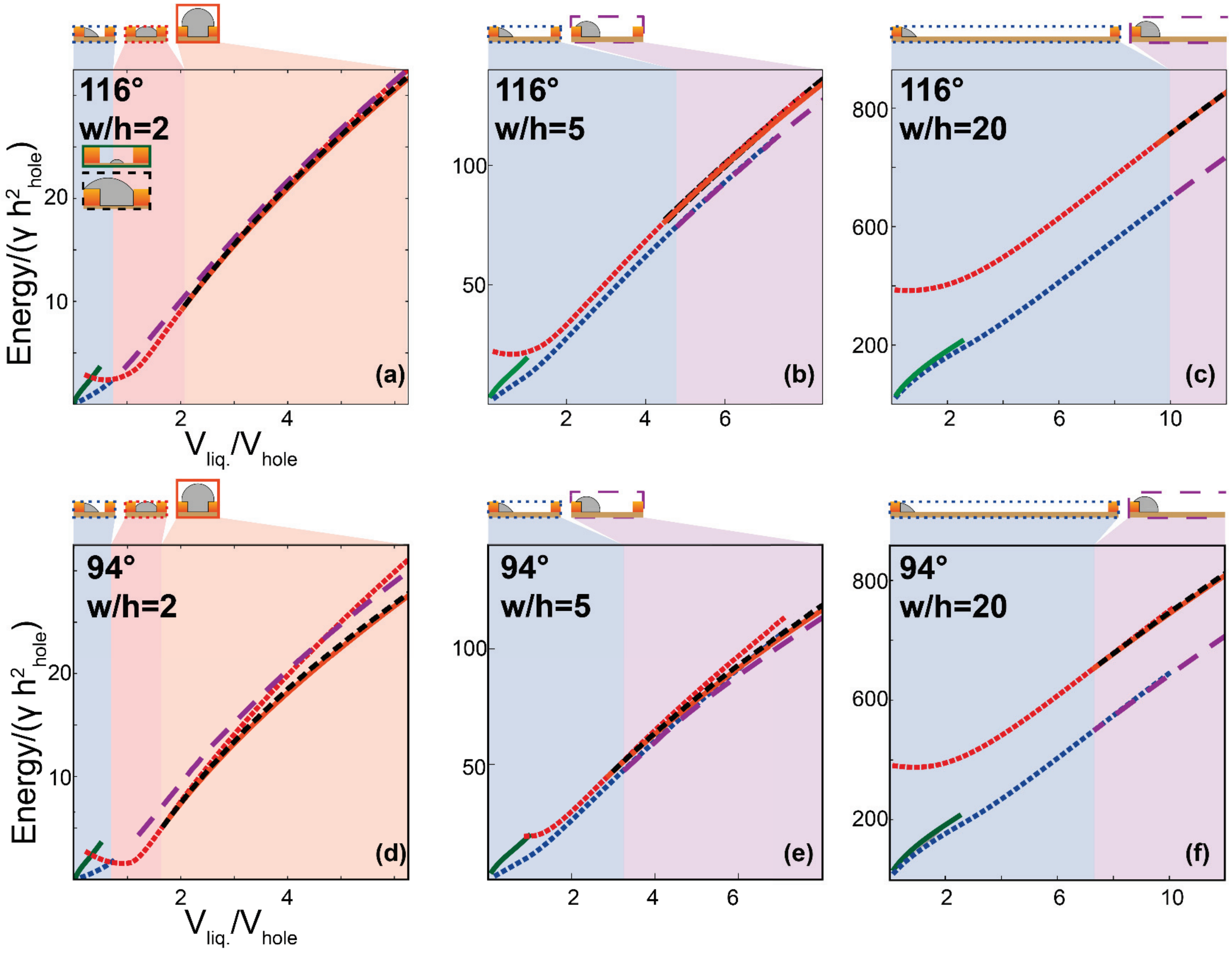
116°
w/h=2
(a)
116°
w/h=5
(b)
116°
w/h=20
(c)
94°
w/h=2
(d)
94°
w/h=5
(e)
94°
w/h=20
(f)
Energy/(γ h^2_{hole})
$V_{liq.}/V_{hole}$
10
20
50
100
200
600
800
2
4
6
10

Figure 31 Representation of the energy vs volume curves of the different droplet configuration with (a)-(c) 116° and (d)-(e) 94° of Ga/SiO_x contact angles for different holes width to height (w/h) aspect ratio, 2,5 and 20. The green curve represent the droplet at the center of the hole configuration, the blue curve the bottom corner droplet, the red curve the droplet wetting the walls of the hole. The orange curve the uniformly spilled droplet, the black droplet the non-uniform spilled droplet, and the purple curve the un-homogeneously spilled droplet wetting the bottom of the hole. The background colors refer to the energetically most favorable configuration as function of the volume, as sketched above each plot.

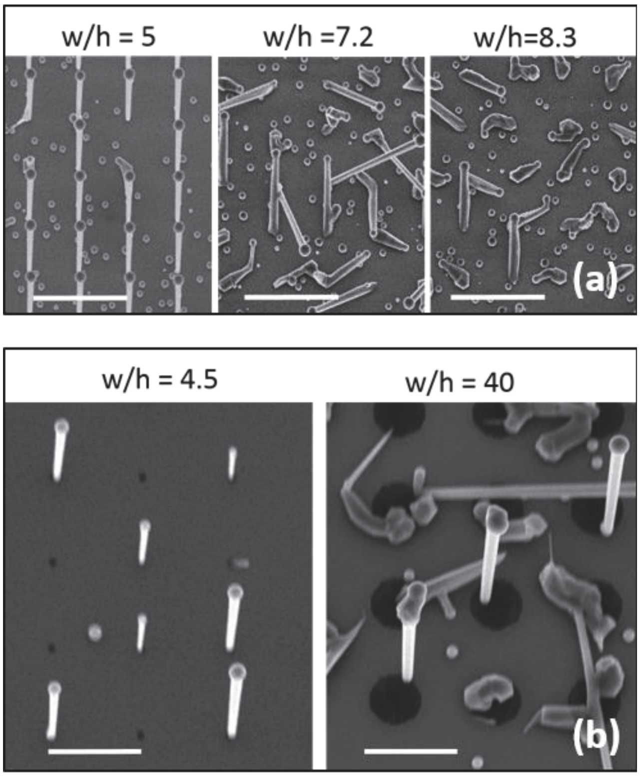

Figure 32 Representative SEM images of GaAs NW growth on the patterned samples demonstrating the influence of the aspect ratio of the hole over the yield of vertical nanowires. The oxide thickness, determined by ellipsometry, is 18 nm for both samples. Pitch is 1000 µm and 2000 µm for (a) and (b) respectively. The scale bar and tilt angle are 2µm and 20° for both images.

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SI Publication IV

Supplementary information: Details of calculations of the nucleation rate and size distributions of self-catalyzed GaAs nanowires

Here, we present the details of the growth model and the derivation of the time-dependent nucleation rate, length and radius distributions of self-induced GaAs nanowires, based upon Eqs. (1) to (5) given in the main text.

Applying the asymptotic Eq. (3) (from the main text) for N_{35} uniformly for all t in Eq. (1) for n_1 and using again the strong inequality $K_3 N_3 << K_{35} N_{35}$, which is a good approximation with our accuracy [S1], we arrive at

$$\frac{dn_3}{dt} + K_{35}(2I_3 I_5 \tau_5 t)^{1/2} n_3 = I_3 .$$

(S1)

Solving this differential equation with the initial condition $n_3(t=0)=0$, we obtain

$$n_3(t) = \frac{2}{3} I_3 \Delta t g\left[(t/\Delta t)^{3/2}\right],$$

(S2)

with the function $g(y)$ given by

$$g(y)=e^{-y}\int_0^y dx\frac{e^x}{x^{1/3}}.$$

(S3)

Here, $\Delta t=4^{4/3}/[3(K_3I_3)^{1/2}]$ is the characteristic nucleation time interval for Ga droplets. It is seen that $g(y)$ increases with y as $(3/2)y^{2/3}$ for small y and decreases as $y^{-1/3}$ at large y. According to the first equation in Eq. (1) and Eq. (4) of the main text, the corresponding nanowire nucleation rate has the form

$$J_{nw}=\frac{dN_{nw}}{dt}=\chi J_0g^2\left[(t/\Delta t)^{3/2}\right];\quad g(y)=e^{-y}\int_0^y dx\frac{e^x}{x^{1/3}},$$

(S4)

which is Eq. (5) of the main text. This solution describes the nucleation pulse whose duration increases for larger Δt, with the shape given by the universal function g^2.

We now consider the nanowire growth itself. According to the model described in detail in Ref. [S2], the nanowire elongation rate is proportional to the difference between the impinging atomic As flux and desorption flux, while surface diffusion of As can be neglected [S3,S4]. In contrast, Ga is not expected to desorb from the droplet at temperatures below 650°C, but can easily migrate from the nanowire sidewalls to the droplet. The increase of the droplet volume is determined by the effective Ga to As imbalance. These considerations yield the nanowire elongation rate and the radial growth rate in the form [S2]

$$\frac{dL}{dt} = C\,; \quad \frac{dR}{dt} = A + \frac{B}{R},$$

(S5)

with coefficients

$$C = \Omega_{35}(I_{5,eff} - I_{5,des})\,;$$

$$A = \frac{\Omega_3}{f(\beta)}(I_{3,eff} - I_{5,eff} + I_{5,des})\,;$$

$$B = \frac{\Omega_3}{f(\beta)}\frac{2}{\pi}\Lambda_3 I_3 \sin\alpha_3\,.$$

(S6)

Here, $I_{eff} \cong I/\sin^2\beta$ are the effective droplet fluxes for both Ga and As beams, β is the contact angle of the droplet at the nanowire top ($\beta \cong 135^o$ according to our post-growth measurements), assumed as being time-independent, $f(\beta) = [(1-\cos\beta)(2+\cos\beta)]/[(1+\cos\beta)\sin\beta]$ is the geometrical function which determines the droplet volume at a given nanowire radius R, Ω_{35}= 0.0452 nm^3 is the elementary volume per GaAs pair in the solid state [S5], $\Omega_3 = 0.02$ nm^3 is the atomic volume of Ga in the liquid [S6], $I_{5,des}$ is the As desorption flux from the droplet, Λ_3 is the effective diffusion length of Ga on the nanowire sidewalls, and $\alpha_3 = 45^{\circ}$ is the incidence angle of the Ga beam. The Ga adatom diffusion flux is taken here in the simplest form $const \times I_3 \Lambda_3 R$. More complex diffusion scenarios can be mastered in line with the approach of Refs. [S5].

Our analysis (see below) shows that the coefficient A is always negative in these growth conditions. Therefore, the length of a nanowire which has emerged at the moment of time t_0 increases linearly with the growth time, while the nanowire radius starts from a small initial value R_0 at $t = t_0$ and then saturates to the critical radius $R_c = B/|A|$:

$$L = C(t - t_0);$$

(S7)

$$t - t_0 = \frac{1}{|A|}\left[R_c \ln\left(\frac{R_c - R_0}{R_c - R} \right) - (R - R_0) \right].$$

(S8)

Obviously, the maximum length and the radius in the size distributions correspond to the nanowires having emerged at $t_0 = 0$, i.e., $L_{\max} = Ct$ and $R_{\max} = R(t_0 = 0)$.

We now turn to the analysis of the length and radius distributions of self-induced nanowires assuming that the nucleation of each Ga droplet immediately starts the nanowire growth (with probability χ). According to general nucleation theory [S5,S7], when nanowires grow vertically at a length-independent rate $dL/dt = C$, their deterministic distribution over lengths obeys the first-order equation

$$\frac{\partial f(L, L_{\max})}{\partial L_{\max}} = -\frac{\partial f(L, L_{\max})}{\partial L}.$$

(S9)

Therefore, the distribution must be a function of $L_{\max} - L$, where the maximum length $L_{\max} = Ct$ (corresponding to the nanowires that have emerged right at the beginning of growth) gives the linear measure of time. At the beginning of growth where $L = 0$, the distribution must equal the nanowire nucleation rate divided by the growth velocity, i.e.: $f(L = 0, L_{\max}) = J_{nw}(L_{\max})/C$ [S5,S7]. This yields our main result for the length distribution

$$f(L, L_{\max}) = const \times g^2\left[\left(\frac{L_{\max} - L}{\Delta L}\right)^{3/2}\right],$$

(S10)

with g given by Eq. (S4) and $\Delta L = C\Delta t$ as the measure of the distribution width.

We note that Eq. (S10) does not account for kinetic fluctuations (described by the second derivative with respect to size) since, in mononuclear nanowire growth, this fluctuation-induced broadening should be suppressed by temporal anti-correlation of successive nucleation events, as discussed in depth in Refs. [S8,S9]. Even in this Poissonian spectrum broadening was enabled, its width ($\sqrt{2<L>}$) would be much less than the nucleation dispersion, as follows from the numerical analysis given below.

As for the width (radius) distribution, Eqs. (S8) show that, while the length is the invariant size variable (for which the corresponding growth rate is $L-$independent), the radius is not (because the radius growth rate dR/dt depends on R). From Eqs. (S7), (S8) it follows that $dL/dR = C/(B/R-|A|)$. Using the normalization condition for the length and radius distributions [S5]

$$f(L)dL = F(R)dR,$$

(S11)

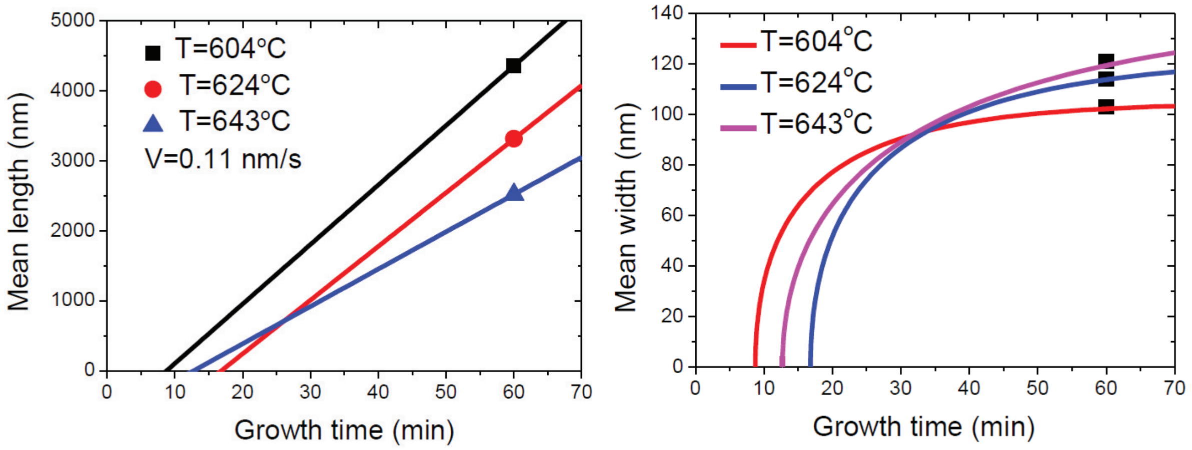
the $F(R)$ has the same form as $f(L)$ with the re-normalization factor dL/dR, i.e.

$$F(R,R_{\max}) = const\times\frac{1}{B/R-|A|}g^2\left[\left(\frac{R_{\max}-R}{\Delta R}\right)^{3/2}\right].$$

(S12)

with ΔR as the measure of width dispersion. Very importantly, the maximum length $L_{\max}$ and radius $R_{\max}$ can be directly measured since they correspond to the longest and thickest nanowires present in the histograms. The kinetic coefficients C, A and B can be estimated from the fits of the representative length and radius in the distributions at a given growth time (or, more accurately, from the time-dependent measurements). Therefore, our distribution shapes contain only one control parameter, the distribution width, which is related to the nucleation time of Ga droplets.

Let us now discuss the time-dependent growth kinetics of the self-catalyzed GaAs nanowires grown by the one-step and two-step growth procedures described in the main text. The proposed growth kinetics of the imaginary nanowire having the mean length and radius at given growth conditions is shown in Figs. S1 and S2. Here, the moment of nanowire nucleation is defined as $<t>=t-<L>/C$, where $<L>$ is the mean length for a given sample. Figure S1 (a) shows the linear increase of the mean length with time for the temperature series, as given by Eq. (S7). Figure S1 (b) shows the strongly nonlinear time dependences of the mean widths, obtained from Eq. (S8) at $R_0 = 0$ and the B values given in the figure caption. The typical values of B (of the order of 100) yield the effective Ga diffusion lengths of the order of 500 nm.



(a) **(b)**

Figure S1 Linear increase of the mean nanowire length with time (a) and time dependences of the mean width $2R$ (b) at $B = 145$ nm^2/s at 604ºC, 148 nm^2/s at 624ºC, and 104 nm^2/s at 643ºC. The starting times for growth of nanowires having the mean length are obtained from the experimental data of Table S1.

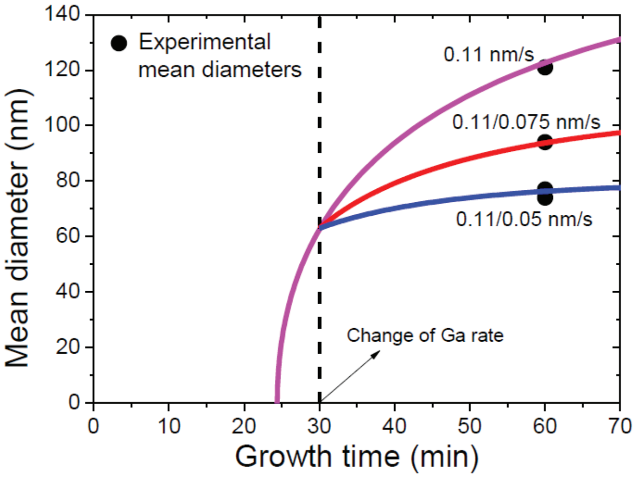


FIG S2. Time evolutions of the mean nanowire width in the two-step growth at 643ºC, obtained from Eq. (S8) with different A and B for different Ga rates: $A =$ -1.45 nm/s, $B = 119$ nm^2/s for the constant Ga flux, $A =$ -1.45/-1.69, $B =$ 119/90 for the 0.11/0.075 nm/s Ga fluxes and $A =$ -1.45/-1.86, $B =$ 119/74 for the 0.11/0.05 nm/s Ga fluxes. Further decrease of Ga flux to 0.027 nm/s does not lead to a significant decrease of width, since the critical width is almost reached already at the first growth step.

Table S1. Statistical parameters of the measured length and width histograms

Temperature	Ga flux	Mean length	Standard deviation	Mean width	Standard deviation	Maximum length
T (ºC)	V (nm/s)	$< L >$ (nm)	σ_L (nm)	$< 2R >$ (nm)	σ_D	$L_{\max}$ (nm)

604	0.11	4357	328	103	14.5	5161
624	0.11	3316	716	114	29	4619
643	0.11	2521	733	121	45.5	3091
643	0.075	1037	605	84	31	2685
643	0.05	1642	632	58.5	16	2907
643	0.11/0.075	1389	404	94	23	2380
643	0.11/0.05	1734	400	77	24	2645
643	0.11/0.027	1433	343	74	28	2185

Graphs shown in Fig. S2 were also obtained from Eq. (S8). This equation was solved for the two different sets of parameters A and B reflecting the abrupt decrease of the Ga flux, and sewed together at $t =$ 30 min. Of course, a much better understanding could be achieved based on the time-dependent measurements. This study will be presented elsewhere.

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Curriculum Vitae

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EDUCATION

03/12 – 03/16 PhD, Ecole Polytechnique Fédérale de Lausanne, EPFL (Lausanne, CH)
(4 years) Material Science and Engineering Doctoral School, LMSC lab.

09/15 – 02/16 Massachusetts Institute of Technology, MIT (Cambridge, MA, USA)
(6 months) Visiting researcher.

09/09 – 09/11 MSc, University of Bologna (Bologna, IT) & Universidad Politécnica de Valencia (Valencia, ES)
Chemical Engineering double degree, “International Master in Materials and Sensor System for Environmental Technologies”, Erasmus Mundus Master.
GPA: 110/110, Summa Cum Laude.

03/11 – 09/11 Rice University (Houston, TX, USA)
(6 months) MSc Thesis on “Alignment in 100% Carbon Nanotube wet spun Fibers”.

09/10 – 02/11 Universidad Politécnica de Valencia (Valencia, ES)
(5 months) Semester abroad as part of the double degree program.
GPA: 9.2/10.

09/06 – 07/09 BSc, University of Genova (Genova, IT)
(3 years) Material Science degree, Department of Physics.
***GPA:* 108/110.**

09/08 – 06/09 Dublin Institute of Technology (Dublin, IRL)
(10 months) Applied Physics Department. BSc thesis on the characterization of a nanopolymer for drug delivery.
***GPA:* 82.2/100.**

TRAINING

09/14 – 12/14 “Venture Challenge”, Venturelab (Lausanne, CH)
(5 months) National program for startup training supported by the Swiss Commission for Technology and Innovation.

06/14 – 06/14 “Lean, Kaizen, Six Sigma” (Lausanne, CH)
(1 week) EPFL introductory course to the principles of Lean Management, Six Sigma and Kaizen.

04/13 – 04/13 “Management of Innovation and Technology Transfer”
(1 week) EPFL Tech Transfer Office course for management of innovation, from the invention through Intellectual-Property protection, to license negotiation.

PROFESSIONAL EXPERIENCE

11/11–03/12 **DSM Ahead (Geleen, NL)**
(5 months) Intern in the R&D department of DSM, developing electrospinning polymeric fibers for filtration application.

ACHIEVEMENTS & AWARDS

04/15-04-16 **Best Nano-Tera.ch Entrepreneurship Presentation Award** Entrepreneurial program to transfer research to market, which included coaching, impact event participation, customer segmentation and market evaluation. Public's award for the best pitch.

09/15–02/16 **DocMobility Fellowship (Lausanne, CH)** Awarded twice a year by the Swiss National Science Foundation to promote young scientists in their careers to conduct research abroad.

02/15 **Startup Weekend (Lausanne, CH)** 3rd Classified.

11/11 **Best Thesis Award (Bologna, IT)** Awarded yearly by IMMSSET.

03/11–09/11 **International Graduate Fellowship (Bologna, IT)** Awarded yearly from the University of Bologna to students based on academic excellence to conduct research abroad.

SKILLS & COMPETENCES

Critical thinking: Developed during my PhD, this skill kept me focused on the objective, regardless the high uncertainty of scientific research and has since become my default mindset.

Problem solving: Advancing in scientific research continuously drove me to face new problems. My determination and analytical skills were keys in generating solutions.

Communicating: Effectively communicating the results and the impact of my research to a broad audience through technical writing and speaking.

Coding: Python, Surface Evolver.

ACTIVITIES & HOBBIES

Activities:
- Alumni Director of MIT Clean Energy Prize (~200'000$) (2015-16).
- Committee member of EDMX at EPFL (2014-16).
- Board member of ACIDE at EPFL (2013-14).

Hobbies:
- Rock climbing, in all its varieties (sport climb up to 7b+, bouldering up to 7a and traditional climbing up to E1).
- Hiking and travelling with my wife.

PUBLICATIONS LIST

1. F. Matteini, G. Tütüncüoğlu, H. Potts, D. Mikulik, F. Jabeen, W.C. Carter, and A. Fontcuberta i Morral, "Impact of the Ga droplet wetting and spilling pinholes on the orientation of GaAs nanowire growth" submitted, 2016.
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3. F. Matteini, V. G. Dubrovskii, D. Rüffer, G. Tütüncüoğlu, Y. Fontana and A. Fontcuberta i Morral "Tailoring the diameter and density of self-catalyzed GaAs nanowires on silicon", Nanotechnology, vol. 26, p. 105603, 2015.
4. F. Matteini, G. Tütüncüoğlu, D. Rüffer, E. Alarcón-Lladó and A. Fontcuberta i Morral, "Ga-assisted growth of GaAs nanowires on silicon, comparison of surface SiOx of different nature", Journal of Crystal Growth, vol. 404, p. 246, 2014.
5. F. Amaduzzi, E. Alarcón-Lladó, H. Hautmann, R.Tanta, F. Matteini, G. Tütüncüoğlu, T. Vosch, J. Nygård, T. Jespersen, E. Uccelli, A. Fontcuberta i Morral, "Tuning the response of non-allowed Raman modes in GaAs nanowires", Journal of Physics D: Applied Physics, vol. 49, p. 095103, 2016.
6. D. Cadeddu, F. Braakman, G. Tütüncüoglu, F. Matteini, D. Rüffer, A. Fontcuberta I Morral, M. Poggio, "Time-Resolved Nonlinear Coupling between Orthogonal Flexural Modes of a Pristine GaAs Nanowire", Nano Letters, vol. 16, p. 926, 2016
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8. G. Tutuncuoglu, M. De La Mata, D. Deiana, H. Potts, F. Matteini, J. Arbiol, A. Fontcuberta I. Morral, "Towards defect-free 1-D GaAs/AlGaAs heterostructures based on GaAs nanomembranes ", Nanoscale, vol. 7, p. 19453, 2015.
9. A. Diaz, T. Xu, G. Tutuncuoglu, T. Demonchaux, J. Nys, Maxime Berthe, F. Matteini, H. A. Potts, David Troadec, Gilles Patriarche, Jean-François Lampin, Christophe Coinon, A. Fontcuberta I Morral, Rafal E. Dunin-Borkowski,

Philipp Ebert, Bruno Grandidier "Nonstoichiometric Low-Temperature Grown GaAs Nanowires " Nano Letters, vol. 15, pp 6440, 2015.

10. L.Francaviglia, Y. Fontana, S. Conesa-Boj, G. Tütüncüoglu, L. Duchêne, M. B. Tanasescu, F. Matteini, A. Fontcuberta i Morral "Quantum dots in the GaAs/AlxGa1−xAs core-shell nanowires: Statistical occurrence as a function of the shell thickness", Appl. Phys. Lett., vol. 107, p. 033106, 2015.
11. M. Ramezani, A. Casadei, G. Grzela, F. Matteini, G. Tütüncüoğlu, D. Rüffer, A. Fontcuberta i Morral, and J. Gómez-Rivas "Hybrid semiconductor nanowire-metallic Yagi-Uda antennas", Nano Letters, vol.15, p. 4889, 2015.
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14. F. Amaduzzi, E. Alarcón-Lladó, E. Russo-Averchi, F. Matteini, M. Heiß, G. Tütüncüoğlu, Conesa-Boj, M. de la Mata, J. Arbiol, A. Fontcuberta i Morral, "Probing inhomogeneous composition in core/shell nanowires by Raman spectroscopy", Journal of Applied Physics, vol. 116, p.184303, 2014.
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16. D. Rüffer, M. Slot, R. Huber, T. Schwarze, F. Heimbach, G. Tütüncüoğlu, F. Matteini, E. Russo-Averchi, A. Kovács, R. Dunin-Borkowski, R. R. Zamani, J. R. Morante[5], J. Arbiol, A. Fontcuberta i Morral and D. Grundler, "Anisotropic magnetoresistance of individual CoFeB and Ni nanotubes with values of up to 1.4% at room temperature", APL Materials, vol. 2, p. 076112, 2014.
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