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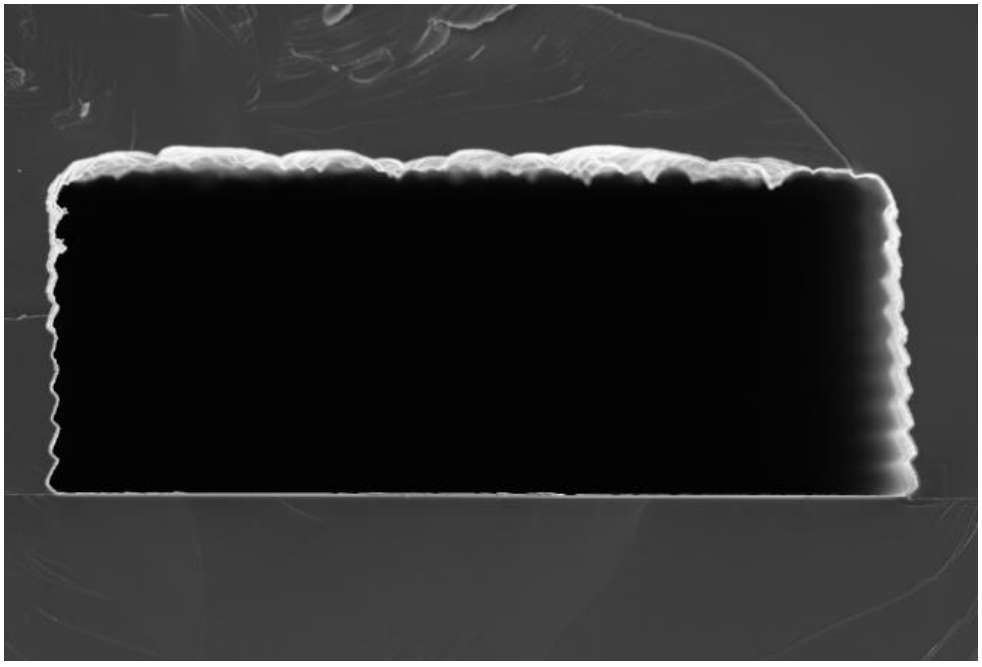
ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Master 2015/2016

Semester Project

Silicon Fusion Bonding for Microfluidic application



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Abstract

The aim of this project was to study the feasibility of Silicon Fusion Bonding for fabrication of capillaries to cool down some gas. This project was conducted in collaboration with a start up called Bright Sensors.

The first step of this project was to carry out an exhaustive review of the bonding techniques in literature. Considering this study and the advices from CMi staff, we developed our own recipe for fusion bonding, consisting of four steps:

1) RCA
2) O_2 plasma treatment and rehydration
3) Manual pre-bonding
4) Annealing

This process led to good results on patterned and non-patterned wafers. An infrared (IR) picture of the bonded patterned wafers is available below:

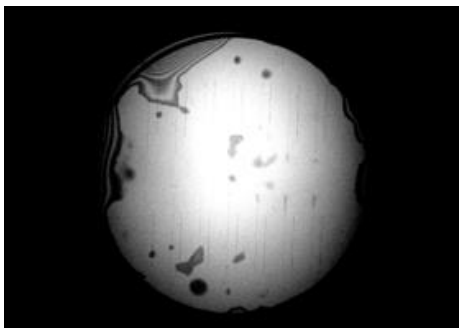


Figure 1: IR picture of patterned wafers bonded (slow annealing)

To study the influence of the annealing speed we decided to compare 2 recipes with slow or fast annealing. The results are summarized in the table below:

	Slow annealing	Fast annealing
Non patterned	Success	Failure
Patterned	Success	Success

As expected, and according to theoretical studies, the bonding was successful with a slow annealing for both non-patterned and patterned wafers. The failure observed for fast annealing and non-patterned wafers seems also logical since we assumed that this fast annealing involves a bad gas evacuation that prevents the bonding from happening. What is more surprising is the success for the patterned wafers, which is probably due to an enhancement of gas evacuation by the presence of channels and holes on the wafers' surface.

Once the wafer bonding was mastered we finished our process flow by adding outlets at the backside of our wafers, taking care of the alignment of existing inlets and future outlets. After the end of the process we diced and cleaved the wafer to observe the channels with SEM:

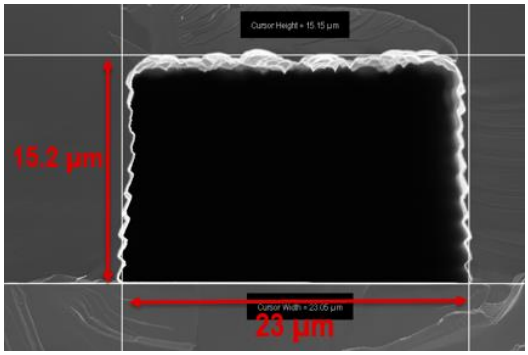


Figure 2: SEM picture of a 20 um wide channel

It is interesting to note that this channel is well defined according to specifications and properly opened. We noticed the growth of 120 nm of SiO_2 on the walls of the microchannels, due to O_2 atmosphere and high temperature annealing (up to 1000°C). The presence of a very thin layer of oxide at the interface between both wafers due to the bonding reaction itself is also quite remarkable.

We finally did a trial on low stress Silicon Nitride wafers ($300\ \text{nm}\ ls - Si_3N_x$), using the same recipe which succeeded for Silicon fusion bonding. The result was a failure, mainly because of roughness of the $ls - Si_3N_x$ layer we used and because the process needs to be adapted for silicon nitride bonding.

Introduction

This project, supervised by Annalisa De Pastina and Prof. Guillermo Villanueva, should have been focused on the bonding of Silicon Nitride. A direct application for this technology was A. De Pastina doctoral work on silicon nitride hollow micro resonator for biomolecular detection. The silicon nitride direct bonding indeed allows a substantial gain of steps in the fabrication of suspended micro channels, for example avoiding long wet etchings.

However, this technology quickly seemed a bit too ambitious for a semester project since the silicon nitride fusion bonding is a very challenging process. Furthermore a start-up called Bright Sensors contacted us and asked us to study the feasibility of the microfabrication of Silicon micro channels through silicon direct bonding. Since the technology of silicon bonding seemed to be easier to master than silicon nitride, we decided to first focus on this request and, in case of success, to come back to silicon nitride bonding.

The commonly used method for encapsulating micro channels etched in silicon is anodic bonding, which consists in the bonding of a glass plate on the silicon wafer by applying a very high voltage. The reason why Bright Sensors needs to bond silicon onto silicon is the thermal properties of silicon. Since they want to use the channels to cool down gas, they need to use materials that have good thermal conduction properties, and silicon has much higher thermal conductivity than glass ($149\ W \cdot m^{-1} \cdot K^{-1}$for silicon against $1\ W \cdot m^{-1} \cdot K^{-1}$).

This report will be separated in 3 main parts which correspond to the 3 main activities that I have been conducting during this project:

- A study of the State of the art about Silicon Fusion Bonding. Several techniques can be used to bond silicon wafers. We will describe them, focusing on the one we chose and justifying our choice. Then we will try understand what is chemically happening during the bonding process we chose. Finally we will have an overview of the existing techniques for characterization of the bonding strength.

- We will then precisely describe our process flow, focusing on the problems we encountered and on the non-common processes we used.

- Finally we will discuss the results of the bonding through observation of the bonding quality at IR microscope and with a study of diced channels through SEM pictures.

State of the art and theoretical aspects

Comparison of methods for wafer bonding

Silicon wafer bonding has been used for long for packaging of microelectronics devices. One of the first method we found in literature is the use of gold at eutectic temperature[1]. This method is based on the introduction of a thin layer of gold between the 2 wafers[2]. The gold is deposited by e-beam evaporation with a thin layer of titanium to promote adhesion. By annealing up to a temperature of 350°C the adhesion of the two wafers is made possible. This method is well-known and efficient, but for cost reasons and preference for techniques using no extra materials we focused on simpler and cheaper process.

The best paper we found on silicon fusion bonding without intermediate layer was published by Z.Liu[3]. This paper compares three pre-treatments we could use for wafer bonding:

- RCA activation of the surface
- HF treatment
- O_2 plasma activation

The results are shown in the following graph :

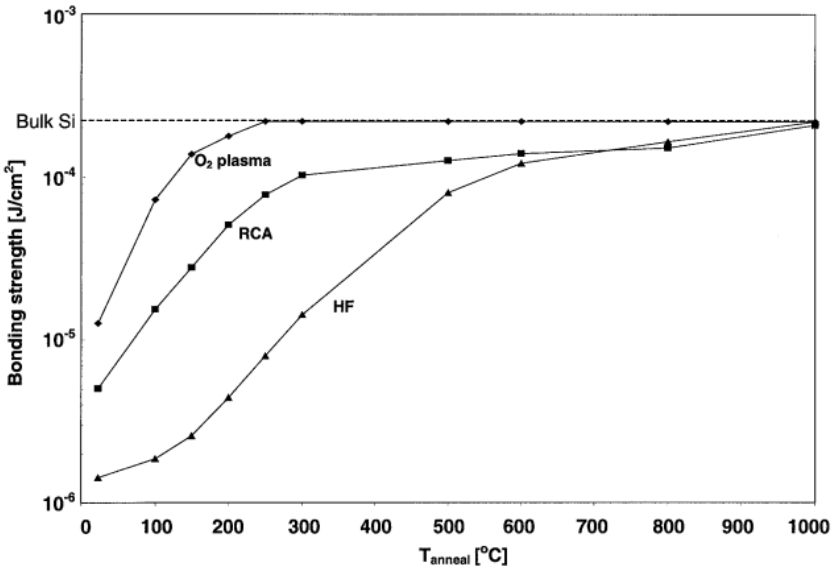


Figure 1: Surface energy of bonded wafers with different pretreatments as function of annealing temperature (Z. Liu and Al. [3])

[1] Wolffenbuttel and Al
[2] M. Schmidt et Al.
[3] Z.Liu and Al.

It is clear from this graph that the best pretreatment is O_2 plasma, with a very good bonding strength starting from 300°C. Furthermore it is relevant to notice that when the annealing temperature is high, around 1000°C, all these pretreatment allow a perfect bonding with at the end the same bonding strength than bulk silicon.

It is also described in the paper that we can use both O_2 plasma and RCA activation in order to get even better values of bonding strength for low temperatures. It has been decided to try first the following process in concertation with the CMi's staff:

1. RCA
2. O_2 plasma treatment and rehydration
3. Prebonding
4. Annealing

The chemical mechanisms happening during this bonding are described in the following paragraph.

Bonding chemical mechanisms

The main results presented in this part are extracted from a seminar on Bonding given by Tony Rogers of Applied Microengineering Ltd held at EPFL in April 2016[4].

Our bonding procedure is realized according to 4 main steps:

- The first step is a cleaning of the wafer by **RCA** to have surfaces as clean as possible for the bonding. **RCA** is a chemical cleaning process including four main steps. First the wafers are cleaned to remove residual photoresist or dust, then they are put in a bath to remove organic compounds, next in another bath of HF to dissolve the native oxide which could have grown during the previous step. Finally wafers are placed in a HCl bath to remove metallic compounds.

- The following step is an activation of the surfaces to get hydroxyl groups on them. This is done first by an **O_2 plasma** exposure followed by a **re-hydration** of the wafers. The idea is to have, before the pre-bonding, the kind of interface shown in the picture below:

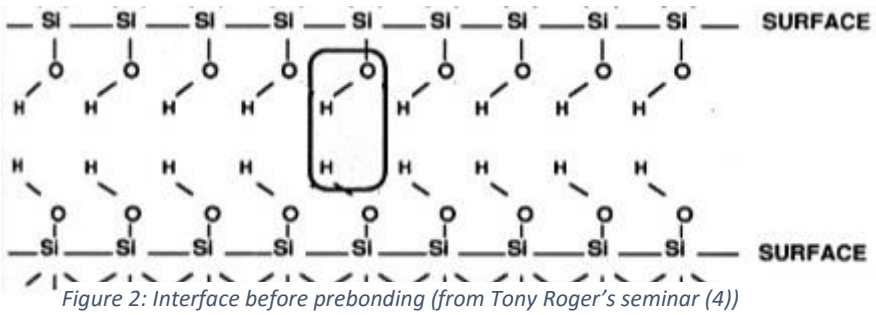


Figure 2: Interface before prebonding (from Tony Roger's seminar (4))

[4] T. Rogers seminar, April 2016

- The third step is the **<u>pre-bonding</u>**: the two wafers are placed in close vicinity and they spontaneously get in contact if pressed together, due to hydrogen bonds appearing at the interface, as we can see in the following picture:

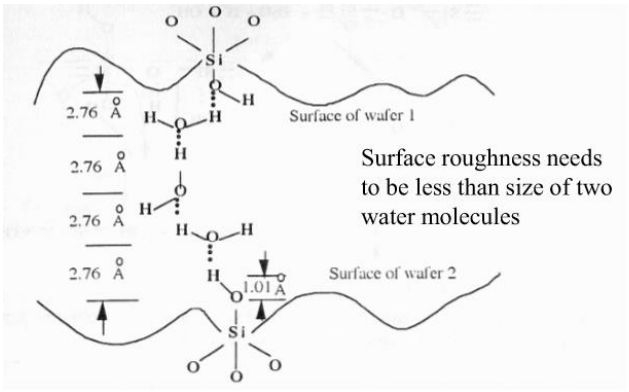


Figure 3: Hydrogen bonds after pre-bonding(from Tony Rogers seminar)

As it is shown in the above picture the wafers have to be extremely flat and clean for the bonding to happen, this explains the use of double side polished wafer for our process. The mean roughness for our wafer should thus be less than 1 nm (4). The pre-bonding is reversible: it results from the competition between attractive hydrogen and Van Der Waals forces and repulsive forces coming from the strain energy of the wafer bow. The bonding is initiate at a contact point and then propagates on all the wafers. In our process flow the water necessary for the creation of hydrogen bonds is provided by the rehydration step.

- The last step is necessary to enhance the bonding quality. It is composed of an annealing up to 1000°C. During this step several reactions happen:

  - From 110°C to 200°C:

$$Si + 2H_2O = SiO_2 + 2H_2$$

This reaction produces H_2 that needs to be evacuated to avoid formation of voids.

  - From 200°C to 400°C:

$$Si - OH + HO - Si = Si - O - Si + H_2O$$

This reaction is responsible for the enhancement of the bonding strength with the formation of covalent bonds, it produces H_2O that will then be dissociated in oxygen (used for the bonding) and hydrogen (gas that needs to be evacuated).

  - From 700°C to 1000°C, there is no special reaction happening, but we will increase the bonded surface and then the bonding strength. Another important aspect of this step is that it allows the evacuation of gas through the bulk silicon, reducing the issue of voids.

We can also think that that the presence of channels will have two opposite effects on the bonding quality. The first is a better evacuation of gas produced during the chemical reactions that should enhance the bonding quality, the other one is the decrease of the bonded area that will logically reduce the bonding strength.

To summarize, in our case the majority of the voids come from the existing microdefect on the wafer's surface and from an excess of chemical reaction byproducts, mainly water and dihydrogen that are liberated during the 2 reactions we gave above.[5]

We should thus pay close attention not to expose our wafers too long to the O_2 plasma to avoid a too large quantity of water in the bond that could lead to voids formation.

We also studied in this report the influence of the annealing speed on the quality of the bonding, we tried to see if a fast annealing will lead to a bad evacuation of gas and formation of large voids.

Finally we would like to get an interface looking like the one on the picture below:

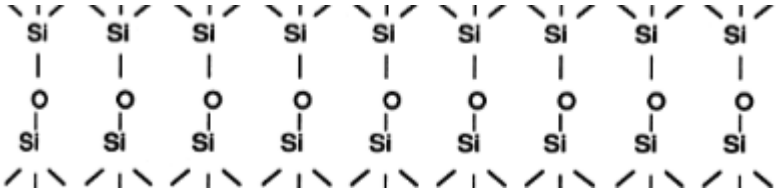


Figure 4: Interface of the 2 wafers after bonding (from Tony Roger's seminar)

[5] X.X. Zhang et Al.

Bonding strength characterization

Once both wafers are bonded, a critical point is to determine the strength of the bonding. One main issue is the opacity of silicon, which is only transparent in the infrared (IR) region. Several solutions have been found in the literature or advised by the CMi staff.

- The first and more used method is often called the **razor blade method**, it is described in the paper of L.Chen and AL.[6] and used in the paper of Z.Liu^3). The idea is to insert a razor between the 2 wafers and to measure with an IR microscope the crack length. The bonding strength can then be deduced with this formula:

$$\gamma = \frac{3Et_w^3 t_b^2}{32L^4}$$

Where E is the Young modulus of the wafer, t_w and t_b the thickness of the wafer and of the razor blade respectively and L the length of crack.

The scheme represented below illustrates the set-up used for this measurement:

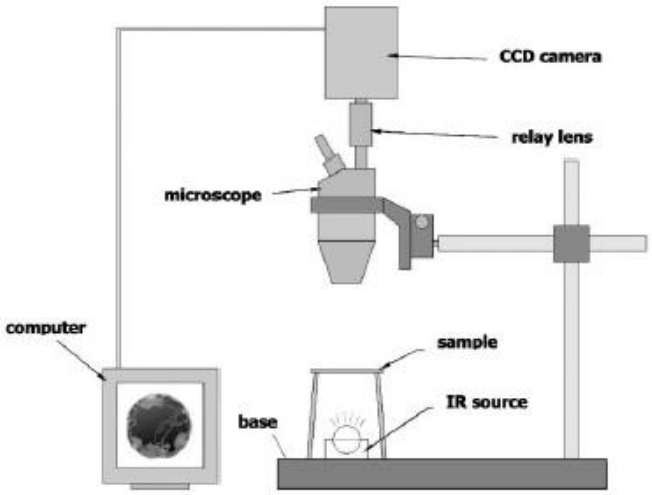


Figure 5: Set-up used in Liu's paper (3) for bonding strength determination (razor blade method)

Unfortunately our labs at EPFL do not have the set-up and the IR microscope to measure the crack propagation length, so we had to find other ways to characterize the bonding quality.

[6] L.Chen and Al.

- Another interesting way of measuring the bonding strength is to use the so called **"Micro-chevron" method**[7]. This method is more complicated because it requires an etching step during the process to get a special chevron shape at the interface of the 2 wafers where we can apply force to measure the bonding strength. Some pictures of this chevron shape are represented on figure 6:

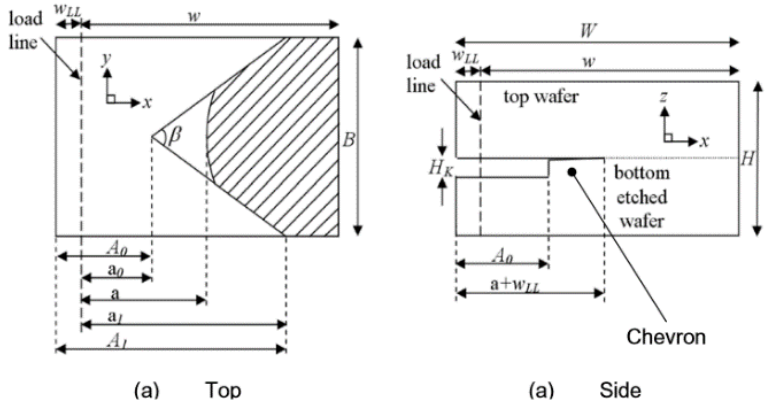


Figure 6: Geometrical schemes representing the chevron at the interface of both wafers

This method seems to be more complicated since it needs additional steps during the microfabrication process, special equipment for applying pressure and there are not many details in literature about how we can finally calculate the bonding strength.

- The CMi staff advised us another method based on **grinding**. The idea is to grind the backside until we arrive to the interface of the two wafers, and here we can have an idea of the quality of the bonding by observing the bonding and the voids. No literature was found on this technique, that is more a handmade method to get an idea of the interface's quality.

- Another idea we had is not to really determine the bonding strength of our wafers but rather to see if the bonding is strong enough for the final application of our device, i.e. to cool down liquid or gas. One proper way of qualifying the bonding strength could be to pass liquid through and to observe the **pressure** the channel is able to withstand without leaks or destruction.

- Something we could do pretty simply was to use an **IR microscope** for observation of the bonding interface. Since silicon is opaque in visible light and is transparent in infrared we decided to use an IR microscope located in CSEM in Neuchâtel. The pictures have been taken by Prof. Villanueva after packaging in vacuum of the samples to avoid them to be contaminated.

- The last idea was, if the bonding was successful, to **dice** the bonded wafers and cleave them so that we could take pictures of the interface and of the channels directly at SEM in the EPFL cleanroom.

[7] R.A. Allena and Al.

Experimental aspects

First part of the process flow for Bright Sensors

After receiving the specification from the start-up Bright sensors about the channel geometry, we decided to start the bonding with their design. We thus conceived the following process flow with a patterned wafer and a simple clean wafer just used for the last step with the bonding. The complete process flow can be found in Appendix 1 and the runcard in Appendix 2 for more details.

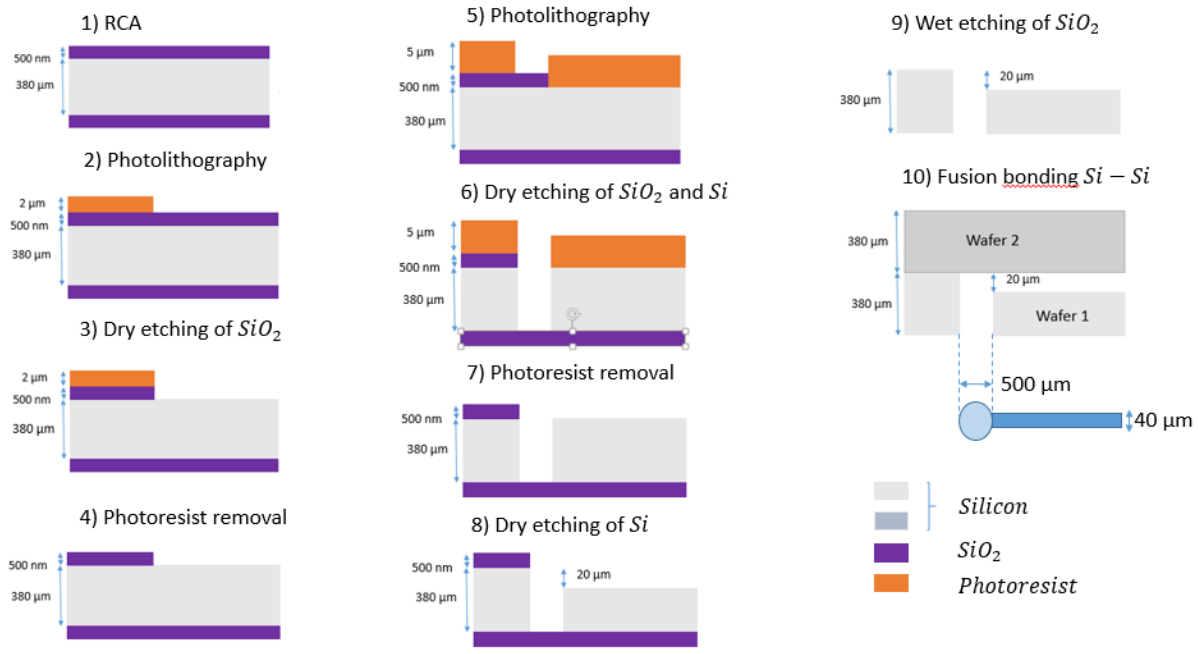


Figure 7 : First process flow for Bright Sensors

We will here quickly describe the relevant points on each step of the process flow :

1. The RCA is the first step, used to clean the surface of the wafer and followed by an oxidation of each side of the wafer.

2. The first lithography is made with a mask corresponding to the channel we would like to etch using positive photoresist AZ ECI with a thickness of 2 microns.

3. Then we etched SiO_2 with a dry etching process. Considering that we wanted to etch 500 nm and that we measured an etching rate of 340 nm/min, we etched the oxide for 1'30''.

4. We removed the photoresist by combining O_2 plasma and wet removing by solvents. At this point we could see this on the wafer surface:

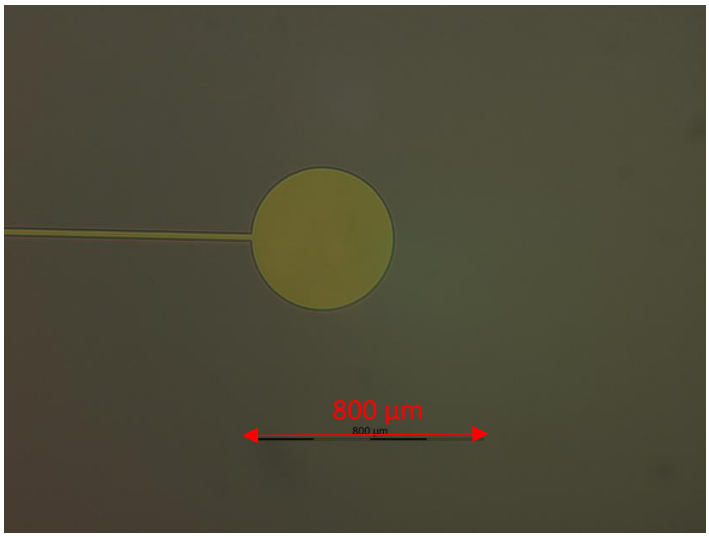


Figure 8: Picture of the wafer after the first photoresist strip

5. Then we did a second photolithography focusing on the inlets. It was really important for the alignment to be very precise as shown in the following pictures where we can see on the right hand side the alignment for the channels and on the left side the alignment for the marks dedicated to it. Since we wanted to realize a deep etching of silicon, for this second lithography we used a thick layer of photoresist (5 microns).

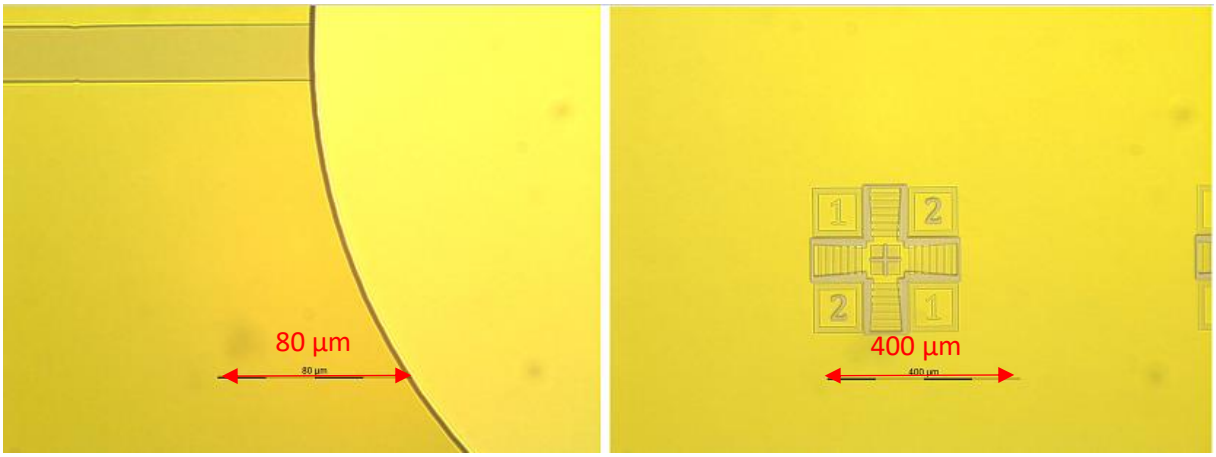


Figure 9 : Observation of the alignment marks

6. We etched the SiO_2 at the inlets part exactly as previously using a 1'30'' etching step.

7. Then we could etch all the silicon through all the wafer. This step was quite tricky because we shall take care of the edges of the wafer to not be destroyed by this long etching. We did the test and, although the edges are very fragile, they were not broken and could mechanically withstand careful manipulation and even automatical dryer. The etching wass done with a Bosch process, we measured an etching rate of 7.5 microns/min, so to etch 380 microns we deduced an etching duration of 50 minutes.

8. Next the photoresist was removed by O_2 plasma.

9. Afterwards we etched the channel itself by Silicon dry etching. As the depth of the channel was about $20\mu m$, an interesting point to note is that for this etching SiO_2 is used as hard mask so that we didn't need another photolithography. The etching of the channels was done by a Bosch process for 2'30.

10. Finally we removed all the SiO_2 remaining by a wet etching in B-HF for 10 minutes. We obtained a wafer with holes through it corresponding to the inlets for the gas that will be delivered in the channels. A picture of the wafer is available below. If the channel is very well defined, we can see roughness at the level of the inlet. This comes probably from the deep etching of Silicon that also corrodes the mask.

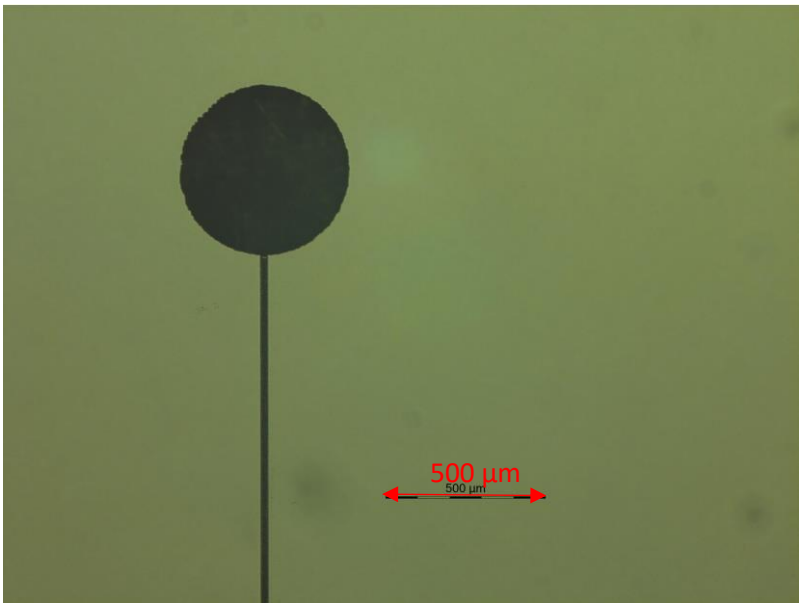


Figure 10: Surface of the patterned wafer before fusion bonding

11. The last step is the bonding of this wafer with a non-patterned wafer. First we did a RCA cleaning in order to have a surface as clean as possible. Then we did a O_2 plasma surface activation and a re-hydration immediately followed by the prebonding realized with vacuum tweezers. Finally we annealed the pre-bonded wafer to enhance the bonding.

Here is the picture of a whole wafer just before the bonding step:

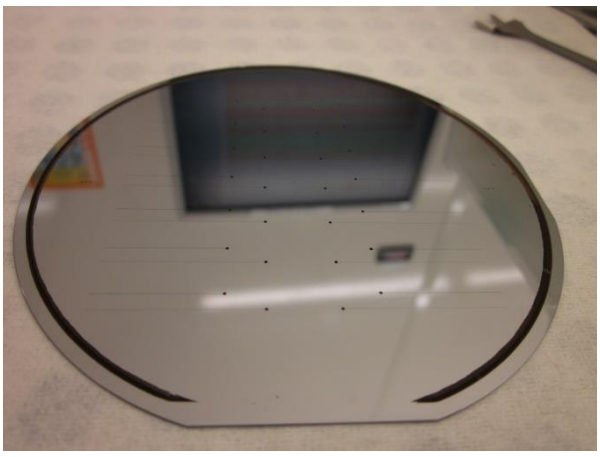


Figure 11: Photography of a patterned wafer before bonding

The wafer was weakened on the edges by the deep etching that damaged it near the EBR. This explains this black circle around the wafer. We were afraid this could prevent the wafers from pre-bonding but as we will see in the next part it was not a problem for the bonding.

Silicon Fusion Bonding: Experimentally

The fusion bonding is the most challenging step of our process flow, this is the reason why we decided to focus mainly on this step. There are four main steps that need to be performed in order to obtain direct bonding of silicon wafers:

1. **RCA** cleaning, done by the CMi staff on Wednesday every week. After this step we usually waited between 1 to 3 days to do the next step. If we were not able to do it before this delay we considered the cleanness lost and waited the next week to repeat RCA cleaning.

2. The **surface activation** to add hydroxyl groups on the wafer's surface was done in 2 steps. First we used the Surfx Atomflow Plasma to activate the surface with O_2 and then we did a rehydration by immersing the wafers for 10 minutes in deionized water. A picture of the Surfx Atomflow we used for plasma activation is shown below:

Figure 12: Surfx Atmosphere plasma used for surface activation (source: CMi website)

3. The **prebonding** was one of the most critical step of the process since it had to be done manually with a by-eye alignment. This step was done immediately after the re-hydration, in order to get the best surface activation. The two wafers were delicately placed on a chuck, at this point we could observe levitation due to electrostatic forces. To trigger the pre-bonding we have to push strongly at one point and then the bonding will be propagated to all the surface. The pressure was applied with a plastic pipette pushing at the center of the wafers. Some pictures of the chuck and of the manual prebonding are available below

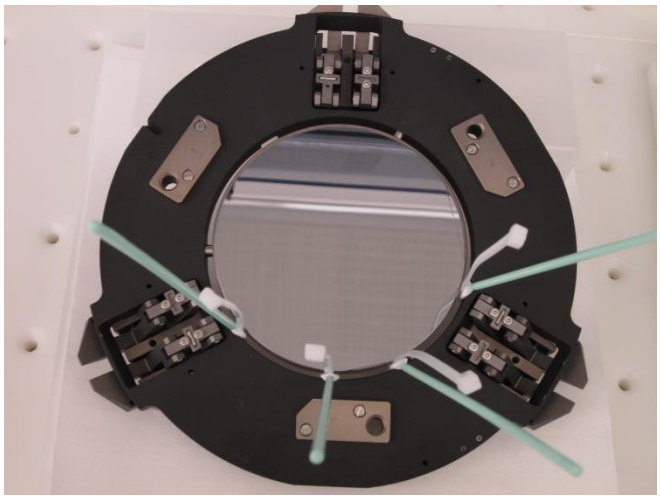


Figure 13: Chuck used for prebonding

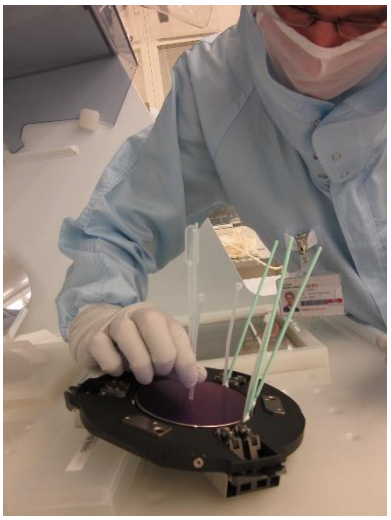


Figure 14: Prebonding by applying strong force on the levitating wafers

4. The last step is **annealing** to enhance the bonding through chemical reactions already described in the state of the art paragraph. We waited not more than 10 minutes before pre-bonding and annealing, even if according to CMi staff we could have waited a few days. So we had to plan the pre-bonding considering the furnace availability to do all these step consecutively, from the O_2 plasma to the final annealing. We decided to compare two recipes for annealing: one with faster annealing (100°C/s ramp up) and another with slower annealing (10°C/min ramp up). The idea is to see whether the wafers bonded with fast annealing will show more voids due to a bad evacuation of gas. The fast annealing was in the RTA (Rapid Thermal Annealing) and the slower one in a furnace. Both recipes are summarized in the following table:

Method for annealing	**Furnace**	**RTA (Rapid Thermal Annealing)**
Annealing duration	3 hours	30 minutes
Annealing's speed	10°C/min	100°C/sec
Temperature range	700-1000°C	100-900°C

A picture of the RTA machine loaded with bonded wafers is represented below:

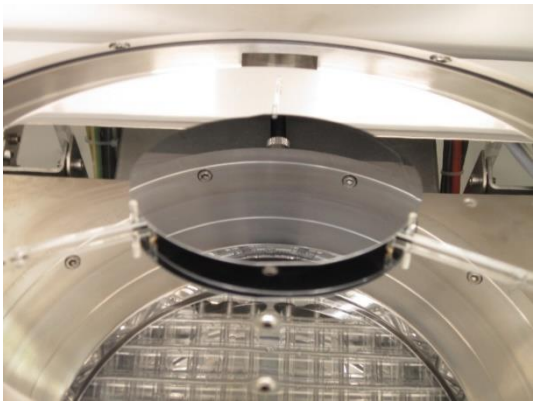


Figure 15: Pre-bonded wafer before annealing in RTA

First results: Comparison of both annealing methods

Slow annealing with furnace

The first bonding has been realized with the support of Dr. G. A. Racine, head of photolithography section of CMi at EPFL, who gave us many useful advices, as he already experimented silicon fusion bonding a few years ago. We annealed the pre-bonded wafers from 700°C to 1000°C in a 100% O_2 atmosphere.

In order to study the influence of the patterning and fabrication processes on the bonding process, we have always compared the bonding of two patterned wafers to the bonding of two non patterned wafers, adopting exactly the same conditions of annealing and surface activation.

The pre-bonding occurred successfully in both cases, even if the pre-bonding of the patterned wafer was more complicated, maybe because it was my first bonding realized in total autonomy.

Since silicon is opaque for visible wavelength we have to use special observation tools to look at the interface. These observations have been done in Neuchâtel at CSEM with an IR microscope and kindly conducted by Prof. G. Villanueva. The pictures for the bonding after annealing are available below:

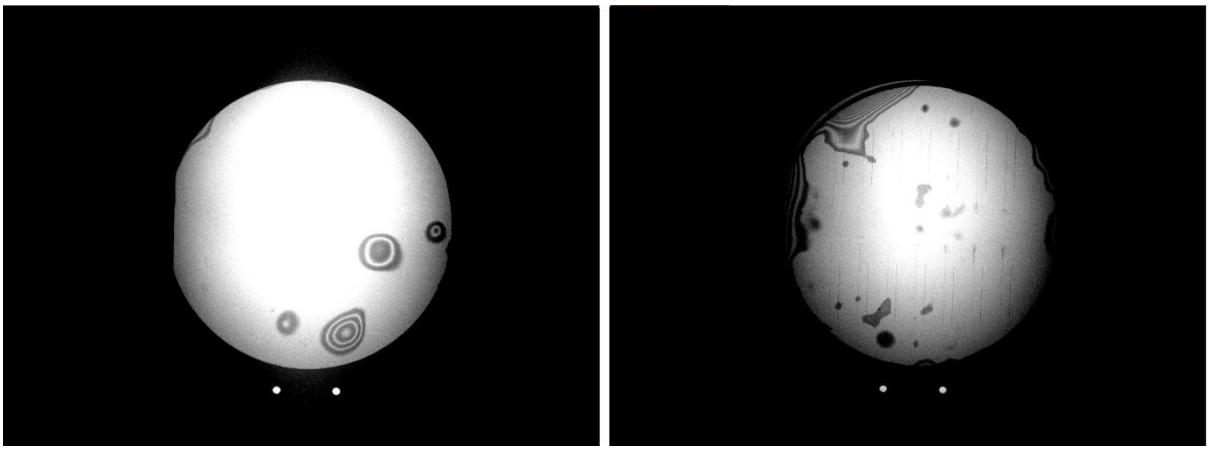


Figure 16: IR pictures of the bonded interfaces for non patterned (left) and patterned (right) wafers.

For the non-patterned wafers we observe a good result withonly few voids, just four spots. These voids come from small defects on the surface that prevent the bonding from happening properly. This is the reason why silicon fusion bonding has to be done in an extremely clean environment. In the literature we can read that a class 10 clean room is required (4). Since we don't have it in CMi we worked in Zone 3, that is the less frequented and the cleanest part of the clean room. We also tried to do the prebonding while this zone was empty.

For the patterned wafer the result looks pretty good also, even if there are more voids visible. This is logical and comes from the fact that during the microchannel fabrication we created some defects on the surface, which increased the surface roughness and led to a less clean bonding. It is remarkable to see that the bonding is worst near the flat part of the wafer, i.e. the part we used to manipulate it with tweezers, that makes sense after what we said above. The weak number of voids lets us think that the

annealing is slow enough for the gas to escape from the interface between both wafers. The channels, visible on the patterned wafer, may have helped this gas evacuation.

Considering the bonding of these 2 wafers good enough, we used them for the second part of our process flow, patterning the other face of the wafer to make the channels fully operational, as will be described later in this report.

Rapid annealing with RTA

To do this additional test we used other two pairs of wafers, one with pattern and another without. The pre-bonding was really good, both for patterned wafers and for non-patterned ones. Later the annealing was realized with a fast ramp of temperature (100°C/sec).

The results of the annealing were not so good. For the non-patterned wafer the bonding did not resist to a test with tweezers, which proves that the bonding was weak. This can furthermore come from the fact that we had to abort the first annealing of these wafers because of an issue with a thermocouple in the machine and with the loop control of temperature in the RTA. The graph below presents the evolution of set temperature and measured temperature as a function of time.

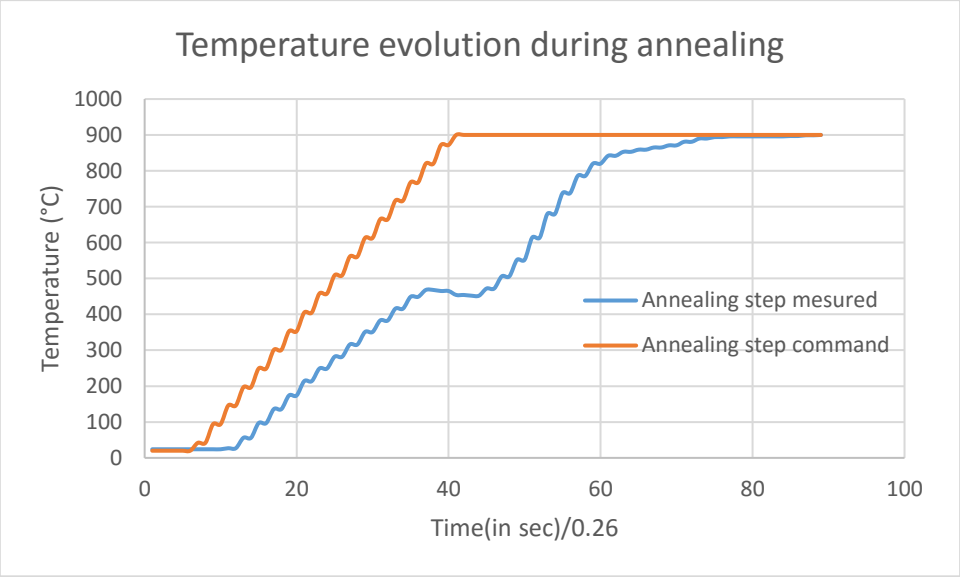


Figure 17: Graph showing evolution of temperature during annealing

On this step it is pretty clear that the closed loop control is bad, because the measured temperature doesn't follow properly the command curve. To understand this we have to understand how the machine implements the temperature control. After entering the recipe the machine automatically computes the optimal parameters of a PID controller to get a good servo-control. The problem is that these calculations are done for a single wafer and not for 2 pre-bonded wafers, which induces bad values of thermal dissipation and thermal inertia in the PID parameters calculation. This can explain the fact that the measured temperature doesn't follow properly the command. Another point that could explain the plateau we get around 400°C is the triggering of several reactions that produce gas

(mainly H_2). Because of the speed of the annealing the gas doesn't have time to diffuse through bulk silicon and stays at the interface. This can explain why we observed a movement of the wafers one respect to another: the pre-bonding is broken by the forces applied by gas and then the bonding occurs again when we stay for 30 minutes at 900°C after the diffusion of gas through silicon.

The second pair of patterned wafers was not tested with tweezers in order to keep them bonded and observe the quality of the interface with IR microscopy. The picture for the bonding is available below:

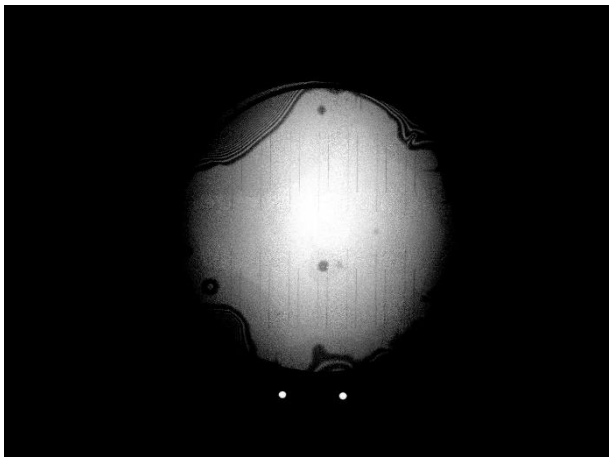


Figure 18: IR picture of bonded wafers with patterning after annealing in the RTA

It is pretty surprising to observe that this bonding looks the same than the one with the slow annealing recipe (see Figure 16), with maybe a bit more voids. Since the not patterned wafer, that should have been cleaner and less rough, did not survive to the annealing, we did not expect a better result with the patterned one. A possible explanation for this phenomena is the presence of channels at the wafers interface connected to holes through the wafers thickness, which could have helped the evacuation of gas at the interface, allowing thus the bonding to happen properly. It is also interesting to note that an annealing time of 30 minutes seems to be sufficient for the bonding to enhance. We tried to separate the patterned bonded wafers with tweezers without success, so the bonding seems to be really good mechanically. An additional step could be to see if they can resist patterning and dicing and then to observe the bonding at SEM, as we did for the slowly annealed wafers, as described in the following chapter.

End of the process flow and channels observation

Second part of the process flow for Bright Sensors

As the first steps of the process flow led to good results, we could add some steps to our design to pattern the bonded wafer with inlets and outlets so that we can really use these channels. We patterned the backside of slowly annealed wafers because they showed good mechanical properties when testing the bonding with tweezers and also good pictures at IR microscopy. We did not pattern the quickly annealed wafer mainly because of lack of time. The second wafer could have been patterned before the bonding, but we thought that this would have probably had a negative impact on the bonding, reducing the bonded area and the flatness of the wafer. The end of the process flow can be represented as follows:

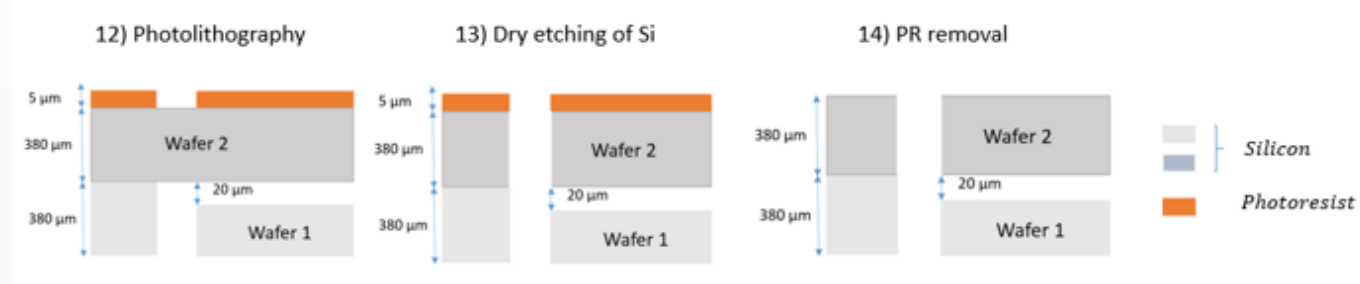


Figure 19: End of the process flow Bright Sensors

To align the outlets on the backside of the surface we performed a backside alignment photolithography. Since this technique was not available on the usual exposure tool (MaskLess Aligner 150), we had to fabricate a chromium mask in order to do it with another machine (MA6).

This step had a little drawback: at the end of the dry etching the plasma will go through the 2 wafers and eventually attack the chuck of the machine. This is the reason why the etching time needed to be precisely estimated with a calibration. Another possible problem we had to consider was that the process flow itself could have destroyed the bonding, for example during spin-coating, baking, dry and wet etching.

However, the bonded wafers (as a reminder those with slow annealing) survived to all these steps without issues and led to good results shown in the pictures below:

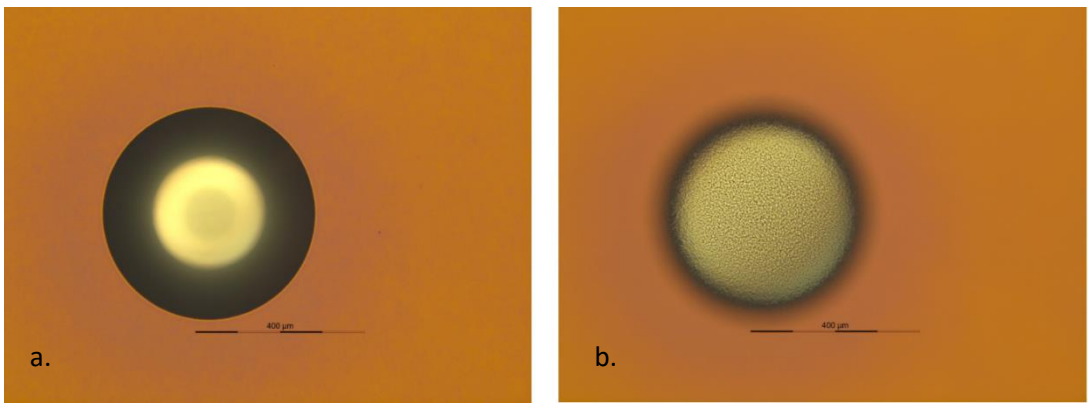


Figure 20: Holes etched through the back surface of the bonded wafers (top and bottom view)

Figure 20 (a and b) show the wafers at the end of the process after the inlets etching. We can see the top of the wafers (on the left: figure 20a.) and its bottom (on the right: figure 20b.). The bonded wafers were not perfectly aligned, because during the manual pre-bonding, when we pressed with the pipette the two wafers tended to slide one on each other. So we had to use the AMS 200 instead of the Alcatel 601 for the dry etching because the wafers did not fit into the AMS 200 chuck. The advantage of the AMS is that the clamping is realized electrostatically, and not by physical clamp as in the A601. This allowed us to process the two wafers even if they were a bit misaligned. The only modification that we had to do on the process flow was that, due to O_2 atmosphere and high temperature annealing, we observed the growth of a 120 nm thick layer of silicon oxide on the wafer surfaces. We just had to add a step for silicon oxide etching before deep silicon etching, as shown in the process flow in Appendix 2 (Step 12).

SEM channels observation

Preparation of the samples

Once our process flow was finished we wanted to check the quality of our bonding and our channels with SEM. This observation required first to dice the bonded wafers in small chips. This has been done by Dr. Y. Deillon of CMi staff. After the dicing we have been happy to notice that the wafers were still bonded and it was impossible to see the interface between them by eye. To get a picture of the channels we needed to have a clean crack along crystalline planes. This explains why we cleaved the wafer after we scratched the bonded wafers edge with a diamond pen. The results were good even if the cracks were not perfectly flat.

Observation of 40 µm wide channels

Observing with SEM microscope we quickly saw some channels at the interface. Figure 22 shows a panoramic view of the interface with a zoom on a channel.

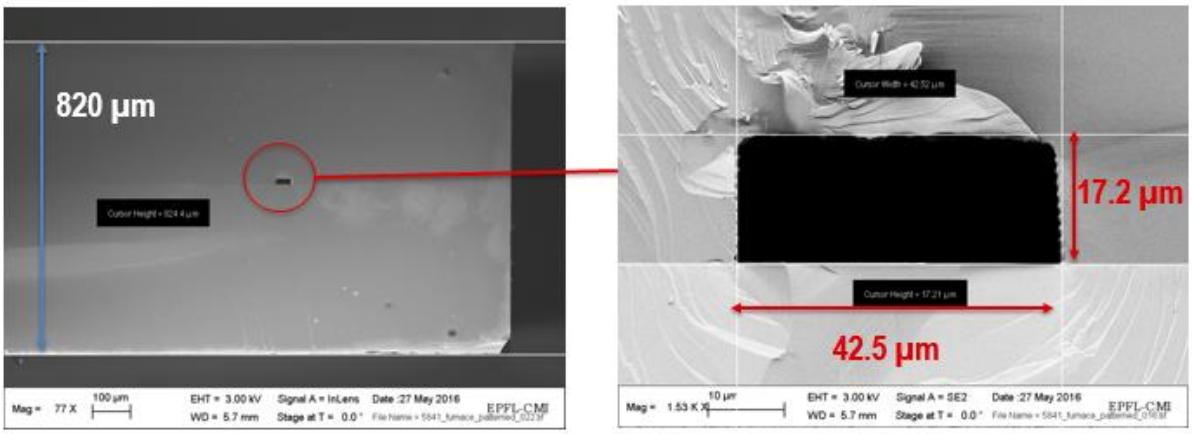


Figure 21: SEM panoramic observation of the 40 um wide channels

The picture on the left shows a view of the cross section of the bonded wafers and the picture on right shows a zoom on the channel with its dimensions. The channels are well defined according to the specification of the mask. The defects that are visible around the channel are due to the cleaving step, which did not create a very smooth and defect-free section. We took more pictures to see more precisely the channels and the interface between both wafers:

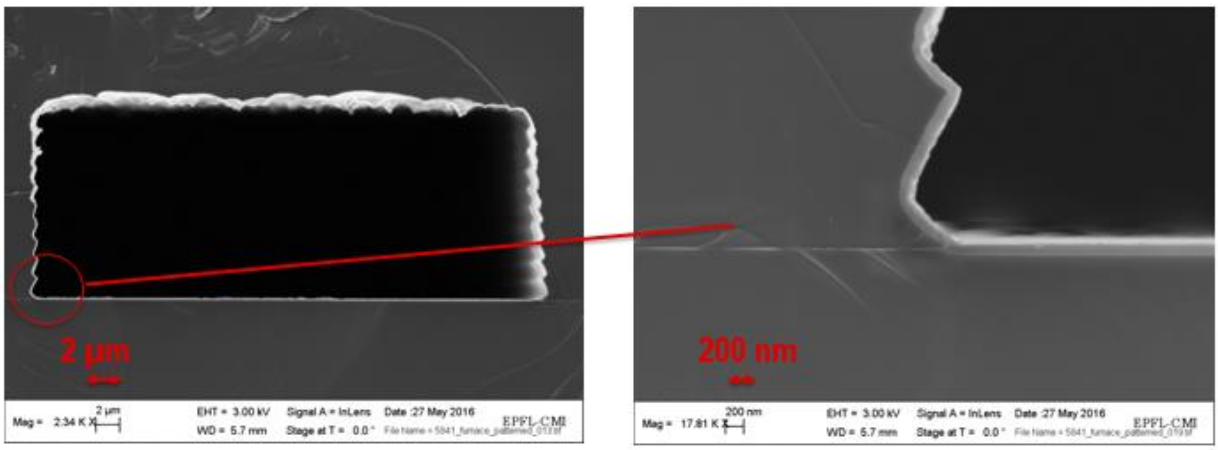


Figure 22: SEM pictures of interface and channel wall for 40 um wide channels

We can note the formation of SiO_2 on the channels walls during the annealing step with O_2 atmosphere. This layer was not only present on the wall but on the whole surface of the wafer where we could measure a thickness of about 120 nm, as described in the previous part. On the wall the layer seems to be around 100 nm thick, which is coherent with the thickness of oxide we measured on the wafers after annealing. This oxide can be useful if we want to pass aqueous liquid in the channels because it provides a hydrophilic coating. It could also have been simply removed by using HF wet etching.

At the interface between both wafers we can observe a thin oxide layer of a few nanometers that is coherent with the theory explained in the state of the art. It is also interesting to note that the shape of the channel walls makes perfectly visible the scalloping, typical of the Bosch etching process.

Observation of 20 µm wide channels

Following the specifications given by the start-up Bright Sensors we designed on the same wafer two different kind of channels with different widths: 20 µm and 40 µm. In the first paragraph we showed pictures of 40 µm wide channels and here we have some pictures of 20 µm wide channels:

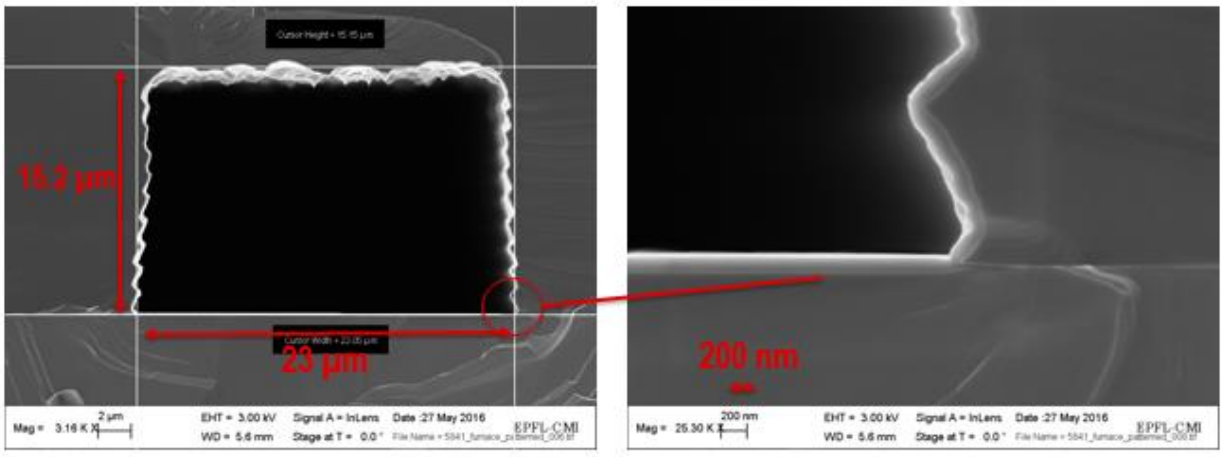


Figure 23: SEM pictures of interface and channel wall for 20 um wide channels

We can also notice the formation of SiO_2 on the wall and at the interface between the bonded wafers. An interesting point is the illustration of the aspect ratio dependent etching (A.R.D.E.) law that can be summarized as following: "the wider the aperture, the deeper the etching". We can thus remark that with a 40 µm wide opening the channel is 17.2 µm deep whereas with the 20 µm wide opening the channel is 15.2 µm deep. The difference is not huge but still not negligible.

Finally we can say that, on the 8 channels we observed with SEM, each of them was properly opened, which lets us think that our process flow is good for the creation of micro capillaries in silicon for microfluidic application.

The only point that needs to be improved is the backside alignment that requires two holes at the edge of the wafer for the second photolithography, so that we can get markers for the alignment.

Trial with Silicon Nitride

As a reminder our goal at the beginning was to bond 2 silicon nitride wafers. Since we succeeded in the fusion bonding for silicon with surface activation, manual pre-bonding and slow annealing in a furnace, we tried to use the same recipe for silicon nitride. It is interesting to specify that similar recipes have been reported by Reck and Al.[8] for silicon nitride fusion bonding, with promising results.

In our experience we observed a really weak pre-bonding: the first contact to overcome electrostatic forces had to be done several times before we could put the wafers in a furnace for 3 hours at 1000°C with a temperature ramp of 10°C/min. After the annealing we observed that the bonding totally failed, since the wafers appeared separated at the end of the annealing.

We can explain this by the roughness of our surface. The roughness of SiN layer is usually not good enough for allowing pre-bonding to happen. As we saw it in the state of the art, the roughness must be less than 1 nm. In the paper of K. Reck and Al. they succeed in bonding 2 silicon nitride wafers(with a thickness of silicon nitride layer of 75nm) but they had to use special deposition process to get very low roughness. The mean roughness R_a was indeed of 0.13 nm in the paper when the layers deposited at CMi exhibits a mean roughness R_a around 7 nm(H. Musard semester project, Fall 2015, GR-LVT). To realize SiN fusion bonding we should thus use special deposition process to get low roughness as studied by H. Musard last semester during his semester project at ANEMS group.

To follow in a more precise way the process flow they used in K. Reck paper, we should suppress the steps of O_2 plasma and rehydration, and anneal for 8 hours at 1150°C in N_2 atmosphere instead of O_2 atmosphere. Since we already have some theoretical and practical knowledge on fusion bonding this SiN fusion bonding is now much easier to achieve, compared to the beginning of the project. The goal will then be to get some pictures like the ones shown in K. Reck paper and visible below:

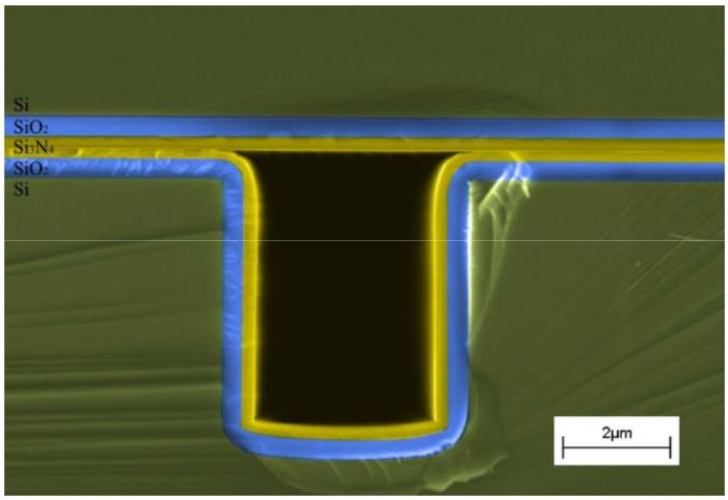


Figure 24: Picture of a channel obtained by Silicon Nitride Fusion Bonding in K. Reck Paper (8)

[8] Reck and Al.

Conclusion

During this semester we demonstrated the feasibility of micro-capillaries fabrication with the technology of Silicon Fusion Bonding. After an exhaustive review of silicon bonding existing technologies, we determined in collaboration with CMi staff an optimal recipe for Fusion Bonding with four steps: RCA, surface activation with O_2 plasma and rehydration, manual pre-bonding and annealing. Concerning this last step we compared the influence of the speed of annealing on the bonding strength. It seems than the annealing speed plays a significant role only if the wafer are bonded without patterning, since this patterning could help gas evacuation.

Using a slow annealing in a furnace we got good results with a good bonding quality for both patterned and non-patterned wafers. We did not measure quantitatively the bonding strength but we used different ways to characterize the bonding interface and strength:

- We observed the interface with an IR microscope to check the presence of voids due to bad gas evacuation.

- We finished the process flow on the bonded wafers: the fact that they survived the demanding remaining steps of the process flow, such as spin-coating, baking, dry and wet etching, dicing and cleaving, proved that the bonding is strong enough to withstand these steps.

- We observed the channels at SEM and the channels were well defined, with a very thin layer of Silicon oxide at the interface as predicted in the theoretical developments.

- We did not try fluid delivery into the channels because of misalignment issues and lack of time. The insertion of liquid in the channels would be useful to see if there are some leaks or not and to find the pressure the channels are able to withstand. By fabricating a new chip with inlets and outlets properly aligned this test could be conducted and give interesting results.

We briefly tried to transfer our results on silicon, to silicon nitride fusion bonding without success. Our failure is mainly due to the high roughness of the Silicon Nitride wafer we used, but the use of less rough surface and small changes in the bonding process should allow good results in SiN fusion bonding since we acquired some precious experience on bonding during this semester.

Acknowledgements

I would to like to thank especially my tutor Annalisa De Pastina for her help and support during all my semester. She answered to all my questions and proofread my runcard and process flow, giving me a lot of practical and useful advice on the life in cleanroom, because this project was one of my first experience in this environment.

I would also like to thank Professor Guillermo Villanueva who supervised this project for his involvement in it. By meeting A. De Pastina and myself once a week he really pushed the project in the right direction, preventing me from trying unrealistic things.

Finally I want to thank all the CMi's staff for the trainings and help in the cleanroom, especially Didier Bouvet for his availability concerning the use of furnaces and Georges-André Racine for teaching me his knowledge on Silicon Fusion Bonding.

References

1) Wolffenbuttel and Al., ''Low-temperature silicon wafer-to-wafer bonding using gold at eutectic temperature'', Sensors and actuators, 1994

2) M. A. Schmidt, "Wafer-to-wafer bonding for microstructure formation", Proceeding of the IEEE, 1998

3) Z. Liu and D.L. Devoe, "Micromechanism fabrication using silicon fusion bonding'', Robotics and computer integrated manufacturing, 2001

4) T. Rogers seminar given on silicon fusion bonding, Applied Microengineering Ltd, April 2016

5) X. X. Zhang and J-P Raskin, "Low-Temperature Wafer Bonding: A Study of Void Formation and Influence on Bonding Strength", Journal of micromechanicals Systems, 2005

6) L. Chen, T. Chen and L. Sun, "Measurement Method of Bond Strength for Silicon Direct Wafer Bonding", Proceeding of the IEEE, 2005

7) R. A. Allena, J. C. Marshalla, W. A. Bayliesb, D. T. Readc, F. DelRiod, K. T. Turnere, M. Bernaschf and J. Bagdahnf, '' A Standard Method for Measuring Wafer Bond Strength for MEMS Applications", ECS transactions, 2008

8) K. Reck, C. Østergaard, E. V. Thomsen and O. Hansen, "Fusion bonding of Silicon Nitride surfaces", Journal of Micromechanics and Micro engineering, 2011

Table of pictures

Appendix

Appendix 1: Complete process flow

- ☑ Semestral Project ☐ Master Project ☐ Thesis ☐ Other

Silicon surfaces bonding for suspended micro-channels

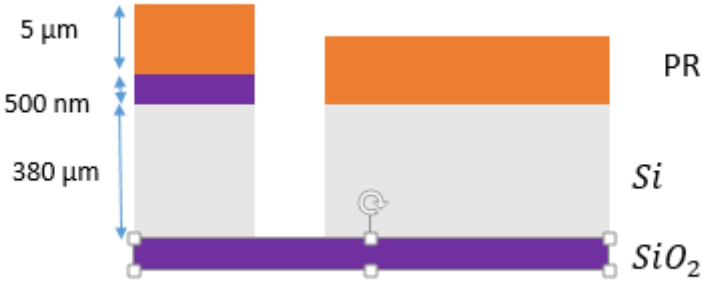
Description

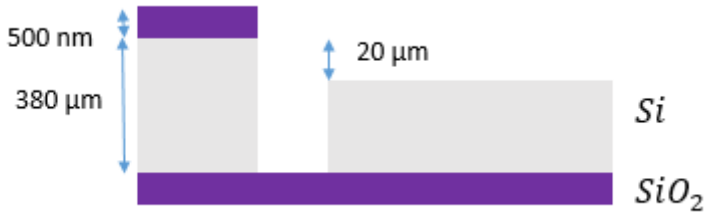
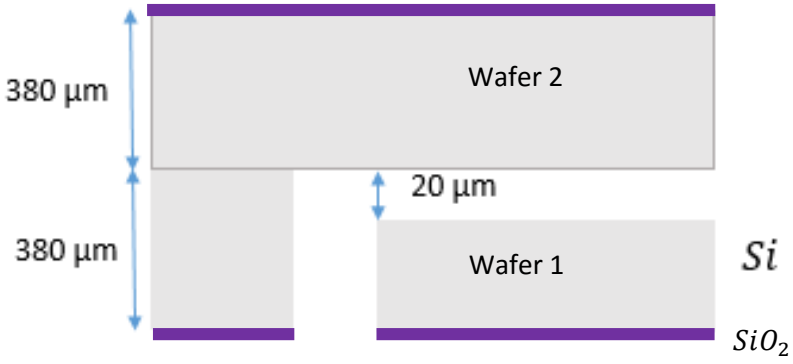
The goal of this manipulation is to create micro channels using 2 wafers that will be bonded together. The critical part of this manipulation is the bonding o the wafers.

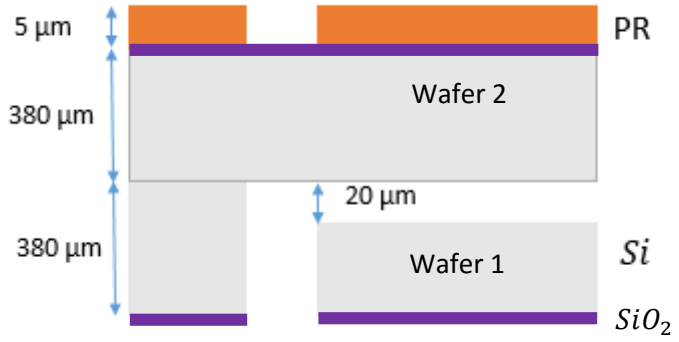
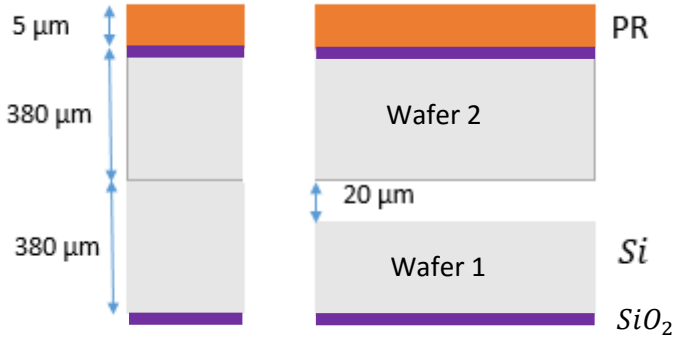
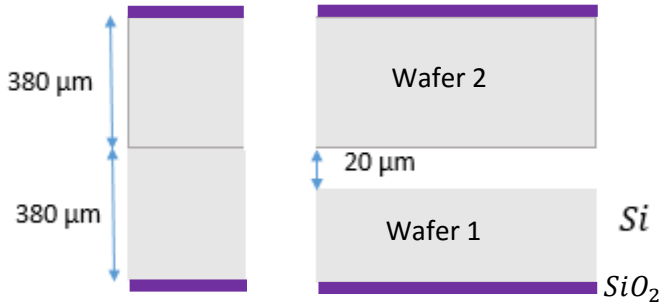
Technologies used			
Photolithography, dry etching, wet etching, wafer bonding, plasma, annealing.			
Photolith masks			
Mask #	**Critical** Dimension	Critical Alignment	Remarks
1	5um	First Mask	Channel definition
Substrate Type			
Silicon <100>, Ø100mm, 390um thick, Double Side polished, Prime, p type, 0.1-0.5 Ohm.cm			

Process outline

Step	Process description	Cross-section after process
01	*RCA* *500 nm of SiO2 each side*	
02	*Photolith* Machine: Rite track coater and developper,*MLA 150* PR : *AZ-ECI – 2µm* Mask : *CD = 20um*	
03	*Dry Etch* Material : *SiO2* Machine: *Alcatel 601E* Depth : *500nm*	

04	*Resist strip* Tepla Gigabatch UFT remover	
05	*Photolithography* Machine: Rite track coater and developper, *MLA 150* PR : *AZ-ECI – 5µm* Mask : *CD = 20um*	
06	*Dry Etch* Material : *SiO2* Machine: *Alcatel 601E* Depth : *500nm*	
07	*Dry Etch* Material : *Si* Machine: *Alcatel 601E* Depth : *390µm*	

08	*Resist strip* Tepla Gigabatch	
09	*Dry Etch* Material : *Si* Machine: *Alcatel 601E* Depth : *20 µm*	
10	*Wet etching of SiO2* Z2 Plade oxide wet bench	
11 **12** **13**	*Wafer bonding* Material : *Si-Si* *11.RCA treatement* *12.Plasma O2 treatement* Machine: Linear-beam atmospheric plasma system Surfx Atomflo 400L *13.Annealing :* Machine: Rapid Thermal	

	Processing/ *MEMS furnace*	
14	*Photolith* Machine: Rite track coater and developper, MA 6 (backside alignment) PR : *AZ-ECI – 5µm* Mask : *CD = 20um*	
15	*Dry Etch* Material : *Si* Machine: *AMS 200* Depth : *390µm*	
16	*Resist strip* Tepla Gigabatch	

Appendix 2: Runcard

Projet : Silicon Fusion Bonding for Bright Sensors
Operator : Pierre-Emmanuel
Created : 13.04.2016 **Last revision** : 06.06.2016
Substrates : silicon <100>, 100mm, 380um, double side, Prime, p type, 0.1-0.5 Ohmcm

Step N°	Description	Equipement	Program / Parameters	Target	Actual	Remarks
0	**WAFER PREPARATION**					
0,1	Stock out					10 wafers
0,2	500 nm Wet oxidation					
1	**PHOTOLITHOGRAPHY - Mask 1**					
1,1	HMDS		Prog. 0			
1,2	Coating	Z1/Ritetrack coater	AZ ECI EBR 2microns coating			
1,3	Exposure	Z5/ MLA	Mask 1 provided by ADP			Dose 215 mW/cm^2 Defocus -6
1,4	Development	Z1/ Developer	AZ ECI EBR 2microns dvt			
2	**OXIDE DRY ETCHING**					
2,1	Oxide Dry Etch	Z2/Alcatel	SiO2@A601, 1'30''	500nm		
2,2	Inspection	Z2/uScope				
3	**RESIST REMOVAL**					
3,1	Plasma removal	Z2/Gigabatch	Strip_High, 5'			
3,2	UFT removal	Z2/UFT remover	70°C			
3,3	Plasma removal	Z2/Gigabatch	Strip_Low, 3'			
3,4	Drying	Z2				
3,5	Inspection	Z2/uScope				
4	**PHOTOLITHOGRAPHY - Mask 2**					
4,1	HMDS		Prog. 0			
4,2	Coating	Z1/Ritetrack coater	AZ ECI EBR 5microns coating			
4,3	Exposure	Z5/ MLA	Mask 2 provided by ADP			Alignment Dose 500 mW/cm^2 Defocus -7
4,4	Development	Z1/ Developer	AZ ECI EBR 5microns dvt			
5	**Oxide DRY ETCHING**					
5,1	Oxide Dry Etch	Z2/Alcatel	SiO2@A601, 1'30''	500nm		
5,2	Inspection	Z2/uScope				
6	**DRY ETCHING SILICON**					
6,1	Dry Etch of silicon	Z2/Alcatel	Si_ambiant2@A601, 50'	380um		A bit too much
6,2	Inspection	Z2/uScope				
7	**RESIST REMOVAL**					
7,1	Plasma removal	Z2/Gigabatch	Strip_High, 5'			
7,2	UFT removal	Z2/UFT remover	70°C			
7,3	Drying	Z2				
7,4	Inspection	Z2/uScope				
8	**DRY ETCHING SILICON**					
8,1	Dry Etch of silicon	Z2/Alcatel	Si_ambiant2 A601, 3'	20 microns		SiO2 used as hard mask
8,2	Inspection	Z2/uScope				
9	**BHF SiO2 removal**					

9,1	Wet etching of SiO2	Z2/Wet Bench	BHF (7:1), 10'			
9,2	Inspection	Z2/uScope				
10	**Fusion bonding**					
10,1	RCA	Z3/Cmi staff	Full RCA			
10,2	O2 Plasma treatment	Z3/SurfAtomFlo	140 W, 30 L/min He, 0.4 L/min O2, 10 mm/s			
10,3	Rehydratation	Z3/WetBenchReclaim	10 min in Trickle Tank			
10,4	Drying	Z3/WetBenchReclaim/SRD	Full drying program 1			
10,5	Prebonding	Z3/WetBenchReclaim	Done manually			Critical step
10,6	Annealing	Z3/MEMS Furnace or RTA	Fast annealing or low annealing, O2 atmosphere			Growth of 120 nm oxide layer on wafer
10,7	Inspection	IR microscope CSEM				Done by Prof. Villanueva in Neuchâtel
11	**PHOTOLITHOGRAPHY - Mask 3**					
11,1	HMDS		Prog. 0			
11,2	Coating	Z1/Ritetrack coater	AZ ECI EBR 5microns coating			Difficulties to establish vacuum
11,3	Exposure	Z6/MA6-BA6	Mask 3 provided by ADP	21'' exposure, 20mW/cm^2		Backside Alignment, fabrication of a mask for this step, Done with ADP
11,4	Development	Z1/ Developer	AZ ECI EBR 5microns dvt			
12	**DRY ETCHING SILICON**					
12,1	Dry Etching of remanent SiO2	Z2/AMS200	SiO2PR AMS 200, 1'	121 nm		Etching of the small layer of SiO2 appeared during annealing
12,2	Dry Etch of silicon	Z2/AMS200	Si_ambient++ AMS 200, 62'	380um		A bit too much, On AMS 200 because not well aligned, etching of edge and SiO2 because no EBR
12,3	Inspection	Z2/uScope				
13	**RESIST REMOVAL**					
13,1	UFT removal	Z2/UFT remover	70°C			
13,2	Drying	Z2				
13,3	Inspection	Z2/uScope				
14	**DICING**					
14,1	Done by Yvan Deillon	Z2/UFT remover				
14,2	Eye inspection					Bonding survived dicing
15	**SEM observation**					
15,1	Cleaving	Z1/ Cleaving table				Done with ADP, bonding survived cleaving
15,2	SEM observation	Z1/ SEM microscope				Nice pictures, all channels visible and beautiful