Journal of ELECTRONIC MATERIALS, Vol. 45, No. 6, 2016 DOI: 10.1007/s11664-016-4449-x © 2016 The Minerals, Metals & Materials Society

Provided by Infoscience - École polytechnique fédérale de Lausann



# Performance of Indium Gallium Zinc Oxide Thin-Film Transistors in Saline Solution

# S. GUPTA<sup>1,2</sup> and S.P. LACOUR<sup>1,3</sup>

1.—Laboratory for Soft Bioelectronics Interface (LSBI), School of Engineering and Centre for Neuroprosthetics, École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland. 2.—e-mail: swati\_gupta@iith.ac.in. 3.—e-mail: stephanie.lacour@epfl.ch

Transistors are often envisioned as alternative transducing devices to microelectrodes to communicate with the nervous system. Independently of the selected technology, the transistors should have reliable performance when exposed to physiological conditions (37°C, 5% CO<sub>2</sub>). Here, we report on the reliable performance of parylene encapsulated indium gallium zinc oxide (IGZO) based thin-film transistors (TFTs) after prolonged exposure to phosphate buffer saline solution in an incubator. The encapsulated IGZO TFTs (W/ L = 500  $\mu$ m/20  $\mu$ m) have an ON/OFF current ratio of 10<sup>7</sup> and field effect mobility of 8.05 ± 0.78 cm<sup>2</sup>/Vs. The transistors operate within 4 V; their threshold voltages and subthreshold slope are ~1.9 V and 200 mV/decade, respectively. After weeks immersed in saline solution and at 37°C, we did not observe any significant deterioration in the transistors' performance. The long-term stability of IGZO transistors at physiological conditions is a promising result in the direction of metal oxide bioelectronics.

Key words: IGZO, encapsulation, phosphonate buffer solution, flexible substrate

### **INTRODUCTION**

Metal oxide semiconductor thin-film transistors (TFTs) have high electronic performance in terms of field-effect mobility ( $\sim 10 \text{ cm}^2/\text{Vs}$ ) and on/off current ratio ( $\sim 10^5 - 10^7$ ).<sup>1-4</sup> These characteristics motivate the development of large-area, transparent flexible displays,<sup>5</sup> thermal and pressure sensor networks,<sup>6</sup> and complementary metal oxide semiconductor (CMOS)-like technology on foil-based substrates.<sup>7</sup>

For neuronal recordings, field-effect transistors have advantages over microelectrode arrays (MEA) as they provide a higher signal to noise ratio.<sup>8</sup> Extracellular and intracellular recordings have been demonstrated using organic thin film transistors.<sup>8–10</sup> The signal to noise ratio can be further improved with higher field-effect mobility TFTs. Therefore, we have developed thin-film transistors based on an indium gallium zinc oxide (IGZO) semiconductor with fieldeffect mobility orders of magnitude larger than that of organic TFTs. The devices were further encapsulated with parylene, a biocompatible polymer with high resistance to moisture.<sup>11</sup> In this paper, we report on the technological steps to fabricate the encapsulated IGZO TFTs on a glass carrier substrate, their electrical performance, and stability over time, and after prolonged exposure to physiological conditions (immersion in phosphate buffer solution (PBS) at  $37^{\circ}$ C and a 5% CO<sub>2</sub> environment).

The TFT stack consists of chromium/gold (5 nm/ 30 nm) thin-film electrodes, a hafnium oxide (HfO<sub>2</sub>) dielectric layer, and an IGZO semiconducting film. The devices are annealed at 150°C in an ambient environment for 90 min, then subsequently encapsulated with a 1  $\mu$ m thick parylene C film. Next, the TFTs are soaked in phosphonate buffer saline solution and stored in an incubator. Their electrical characteristics are monitored at 1, 3, 7, 10, and 15 days. The TFTs display an on/off current ratio of 10<sup>7</sup>, field-effect mobility of >10 cm<sup>2</sup>/Vs, and subthreshold slope of 150 mV/decade. A stable performance of parylene

<sup>(</sup>Received August 24, 2015; accepted March 5, 2016; published online March 23, 2016)

encapsulated IGZO TFTs in physiological conditions was observed for 15 days.

### **EXPERIMENT DETAILS**

Bottom-gate and top-contact thin-film transistors were fabricated on a glass substrate. Prior to the fabrication, glass substrates were cleaned by the Piranha process. The cross-section of a TFT is shown in Fig. 1. Metallic gate contacts (5 nm of Cr and 25 nm of Au thermally evaporated) were patterned by lift-off photo-lithography. On top of gate contacts, 45 nm of hafnium oxide (HfO<sub>2</sub>) was deposited by atomic layer deposition at 200°C then patterned and etched by reactive ion-beam etching.

Next, a 30 nm thick IGZO was sputtered through a stainless steel shadow mask at room temperature by radio frequency (RF) magnetron sputtering (DP 650 sputterer, Alliance Concept) in the presence of argon (30 sccm) at a pressure of  $5 \times 10^{-3}$  mBar. Finally, source/drain contacts were prepared with the same process as for the gate contacts. Then, the transistors were annealed at a temperature of 150°C in an ambient environment for 90 min. This annealing step improves the transition metal oxide semiconductor thin-film transistors performance.<sup>2</sup> After annealing, the transistors were encapsulated



Fig. 1. Transistor cross-section.

with a 1  $\mu$ m thick film of parylene. To enable electrical probing, parylene was etched from the source, drained, and obtained gate contacts by oxygen plasma. During plasma exposure, all other areas were masked by photo-resist (AZ 9260). A range of devices was manufactured with channel widths of 200  $\mu$ m, 500  $\mu$ m, and 1000  $\mu$ m, and channel length varying between 10  $\mu$ m and 120  $\mu$ m.

The device characterization was performed with an Agilent 4155 B semiconductor device parameter analyzer. Field-effect mobility and threshold voltage in the linear and saturation regimes were calculated by the standard metal-oxide-semiconductor fieldeffect transistor (MOSFET) equations. The subthreshold slope was calculated as the inverse of slope of log ( $I_{\rm DS}$ ) versus  $V_{\rm GS}$ . Off-current was defined as the minimum current while the maximum current was the on-current.

## **RESULTS AND DISCUSSION**

In this section, the transistor characteristics on glass with and without encapsulation layer are presented. The transistor performance in physiological conditions is next shown for different immersion duration in PBS.

The transfer and output characteristics of TFTs fabricated on a glass wafer are shown Fig. 2. The drain-current is 6–7 orders of magnitude higher than the gate current, which shows  $HfO_2$  provides good electrical insulation. The transistor displays an on/off current ratio of  $4.5 \times 10^6$ , a threshold voltage of ~1.8 V, and a field-effect mobility of  $8.5 \text{ cm}^2/\text{Vs}$ . The field-effect mobility reported in this paper is slightly lower than that reported in the literature, <sup>1–4</sup> calling for further optimization of the IGZO-HfO<sub>2</sub> interface.

The characteristics of the parylene encapsulated TFTs are shown in Fig. 3. The increase in channel width from 200  $\mu$ m (Fig. 2) to 500  $\mu$ m (Fig. 3) leads to



Fig. 2. Transfer (a) and output (b) characteristics of a TFT of W/L = 200  $\mu$ m/10  $\mu$ m. In the transfer characteristics, red and black curves correspond to the linear ( $V_{DS} = 0.5$  V) and saturation ( $V_{DS} = 4$  V) regimes, respectively (Color figure online).



Fig. 3. Transfer (a) and output (b) characteristics of encapsulated TFT immersed in phosphonate buffer solution after 1, 7, and 15 days. The characteristics before immersion are shown in dashed lines (Color figure online).

a slight increase in leakage current density. The transfer and output characteristics of TFTs immersed in PBS solution were investigated at a regular time interval after washing the devices with deionized water. The dashed line in Fig. 3 corresponds to the response of the encapsulated transistor prior to immersion in PBS solution; all other curves are recorded at the indicated day. The TFT behavior remained nearly the same across the 15 days of immersion. TFTs without parylene encapsulation does not remain working after immersion in PBS solution. These results are encouraging in pursuing the development of IGZO-based TFT arrays for bioelectronic applications. Furthermore, the maximum fabrication temperature of the devices is 200°C, which opens them to their implementation on flexible substrates such as polyimide foil.

#### CONCLUSION

We have tested the stability of IGZO-based thin film transistors against exposure to physiological conditions. A parylene-based encapsulation offers a reliable insulation against moisture and salt compounds for at least 15 days in saline solution at  $37^{\circ}$ C. Transistor yields in fabrication were nearly 100%, all displaying similar transistor characteristics. The TFTs operated within 4 V and off-currents on the order of  $10^{-12}$  A. TFTs had high an on/off current ratio of  $10^7$  and a low subthreshold swing (150 mV/decade). All electrical characteristics remained stable over time. These results were a first but essential step towards the use of metal oxide transistors for bioelectronic circuitry.

#### ACKNOWLEDGEMENT

This work was supported by the Bertarelli Foundation, a European Research Council Starting Grant, ERC ESKIN, No. 259419.

#### REFERENCES

- C.J. Chiu, S.P. Chang, C.Y. Lu, P.Y. Su, S.J. Chang, J. Ihm, and H. Cheong, *AIP Conf. Proc.* 1399, 929 (2011).
- 2. H. Wu and C. Chien, *IEEE Electron Device Lett.* 35, 645 (2014).
- J.S. Lee, S. Chang, S. Koo, and S.Y. Lee, *IEEE Electron Device Lett.* 31, 225 (2010).
- J.-L. Wu, H.-Y. Lin, B.-Y. Su, Y.-C. Chen, S.-Y. Liu, C.-C. Chang, and C.-J. Wu, J. Alloy Compd. 592, 35 (2014).
- C.Y. Lin, C.W. Chien, H. Wu, H.H. Hsieh, C.C. Wu, Y.H. Yeh, C.C. Cheng, C.M. Lai, and M.J. Wu, *IEEE Trans. Electron Device* 59, 1701 (2012).
- I.-J. Park, C.-Y. Jeong, I.-T. Cho, J.-H. Lee, E.-S. Cho, S.J. Kwon, B. Kim, W.-S. Cheong, S.-H. Song, and H.-I. Lwon, Semicond. Sci. Technol. 27, 105019 (2012).
  T.C. Huang, K. Fukuda, C.M. Lo, Y.H. Yeh, T. Sekitani, T.
- T.C. Huang, K. Fukuda, C.M. Lo, Y.H. Yeh, T. Sekitani, T. Someya, and K.T. Cheng, *IEEE Trans. Electron Device* 58, 141 (2011).
- V. Benfenati, S. Toffanin, S. Bonetti, G. Turatti, A. Pistone, M. Chiappalone, A. Sagnella, A. Stefani, G. Generali, G. Ruani, D. Saguatti, R. Zamboni, and M. Muccini, *Nat. Mater.* 12, 672 (2013).
- A. Spanu, S. Lai, P. Cosseddu, M. Tedesco, S. Martinoia, and A. Bonfiglio, Sci. Rep. 5, 8807 (2015).
- D. Khodagholy, T. Doublet, P. Quilichini, M. Gurfinkel, P. Leleux, A. Ghestem, E. Ismailova, T. Hervé, S. Sanaur, C. Bernard, and G.G. Malliaras, *Nat. Commun.* 4, 1575 (2013).
- K. Alexandrou, N. Petrone, J. Hone, and I. Kymissis, Appl. Phys. Lett. 106, 113104 (2015).