IET Power Electronics, 2016

Galvanically Isolated Modular Converter

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POWER ELECTRONICS LABORATORY
ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

IET Power Electronics

Research Article

IET Journals
The Institution of Engineering and Technology

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ISSN 1755-4535
Received on 27th September 2015
Revised on 31st December 2015
Accepted on 9th February 2016
doi: 10.1049/iet-pel.2015.0747
www.ietdl.org

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Abstract: Direct current (DC) electrical grids are already a reality in low voltage (LV) telecom distribution systems and point-to-point high voltage DC transmission. Medium voltage (MV) domain, despite its big potential, still suffers from a lack of suitable conversion and protection technologies. This study presents a bidirectional, galvanically isolated, high power converter for interface of emerging MVDC grids with readily available LVAC grids. To achieve high conversion efficiency, the integration of a line frequency transformer into the structure of the modular multilevel converter (MMC) is analysed and described in a systematic manner. Two configurations of the galvanically isolated modular converter: (i) interleaved and (ii) stacked, are derived and presented. Differences and similarities, compared to the classical MMC, are presented on the system design level, while control performances are evaluated by means of simulations.

Nomenclature

P	positive terminal
N	negative terminal
M	DC-side star connection
M'	grid-side star connection
$\{a, b, c\}$	phase leg
$\{p, n\}$	positive/negative arm
$\{l, r\}$	left/right arm
m	modulation index
$e_{\{p,\ n\}/\{l,\ r\}}$	equivalent arm EMF voltage
v_{B}	bus-side voltage
v_L	grid-side voltage
e_{B}	equivalent EMF voltage on the DC bus side
e_L	equivalent EMF voltage on the AC grid side
V^{Σ}	summed capacitor voltages
i_{B}	bus-side current
i_{m}	magnetising current
i_L	grid-side current
i_{circ}	circulating current
i^{Σ}	average capacitor currents
N_{HV}	number of transformer turns – HV-side
N_{LV}	number of transformer turns – LV-side
n	transformer turns ratio
L_{m}	transformer magnetising inductance
L_{σ}	transformer leakage inductance
R_{σ}	transformer resistance
N_{sm}	number of submodules (SMs) per arm
C_{sm}	SM capacitance
R_{sm}	SM resistance
C_{arm}	arm equivalent capacitance
R_{eq}	equivalent SM resistance

1 Introduction

Power electronic technologies have not been available in the early days of electrification, leading to the development and widespread of AC infrastructures, with the exception of high voltage DC (HVDC) systems for bulk energy transmission over large distances. However, developments in semiconductor technology have enabled numerous converter topologies and wider penetration of power electronic technologies in the utility grid. Nowadays, the increased use of low voltage (LV) distributed energy resources (DERs) is in fact enabled by modern and highly efficient power electronics. When it comes to connecting large groups of LV DERs to distant medium voltage AC (MVAC) distribution grids, medium voltage DC (MVDC) collection and distribution grids are considered as a viable solution that could improve the overall distribution grid flexibility, efficiency, expansion opportunities and the operational or lifecycle cost.

Considering offshore wind farms, comparative analyses (AC versus DC) have been presented in [1, 2], highlighting techno-economical trade-offs between initial capital investment, cost of lost energy due to losses, unavailability due to scheduled maintenance or wind turbine failure and so on. While multiple advantages have been recognised (lower cost, increased availability, system expandability, smaller footprint, reduced filtering effort), a number of challenges still remain (protection, no standardised DC voltage level, no suitable converters), resulting in no large-scale MVDC distribution systems in use. Shipboard electrical distribution systems, usually realised with MVAC three-phase lines in the past, increasingly consider using DC distribution [3, 4]. Despite protection issues related to handling short circuit currents in DC applications, a number of ships already operate at oceans equipped with DC distribution systems. Yet, when it comes to MVDC, there are still many open issues [5]. The use of MVDC is foreseen for offshore wind energy collection [6, 7], and onshore renewable energy collection [8].

This paper presents a power electronic converter for the interconnection of an LVAC grid, or a large group of LVAC loads, and an MVDC grid. The application setting implies needs for galvanic isolation, high efficiency (>98%) and reliability, as well as power bi-directionality. While there are numerous power electronic topologies suitable for this kind of conversion, two prevailing research trends can be identified: (i) solid state transformer (SST) and (ii) modular multilevel converter (MMC).

The concept of the SST (originally proposed in [9, 10]) has attracted a lot of attention recently, with numerous topological variations for traction [11, 12] and utility [13] applications. The use of medium frequency transformers (MFTs) offers, in perspective, significant power density improvements, which are greatly counteracted by high insulation requirements due to MV. The majority of SST proposals are in essence multi-stage converter structures: at their core is a DC/DC converter with a

galvanic isolation, and multiple stages are cascaded for fractional power processing (input-series output-parallel). For an LVAC output, the SST efficiency is further reduced due to the LV inverter output stage that has to deal with large currents [14]. An SST concept similar to the dual-active-bridge, but based on an MMC, has been proposed in [15] or with an improved modulation concept in [16]. The use of high-voltage wide band-gap devices offers improved efficiency and complexity simplifications [17], but the future of these devices appears to be limited to niche applications, slowing down their development.

On the other hand, the MMC [18] has been quickly accepted as the new state-of-the-art technology for HVDC interconnects over the former line commutated inverters (LCIs) and voltage source converters (VSCs). The MMC offers increased efficiency due to the very low switching frequency, infinite voltage scalability, modularity and power electronics building block-based design, as well as reduced filtering needs thanks to the multilevel voltage waveform. This is especially true when one arm comprises several hundreds of submodules (SMs), as for HVDC applications. The control of the MMC for MV applications, with significantly less SMs, leads to modified modulation and balancing algorithms as in [19], if the objective is to keep the SM switching frequency low and to ensure an equal distribution of the losses across the SMs or as in [20], where the minimisation of the switching events is attained. The MMC has been considered for several different MV areas: grid inter-ties [21, 22], MV drives [23, 24], STATCOM [25] or EV charging station [26]. It is important to note that all proposals made on modified MMC topologies, namely: the hybrid modular multilevel VSC [27], the alternate arm converter [28], where for both direction switches were introduced, leading to an increased number of semiconductors (suboptimal semiconductor utilisation) and an additional DC filter for handling the six pulse ripple, the half-wave bridge AC/DC converter [29] or the open-end winding MMC [30–32], do not feature a circulating current component. It leads to the loss of a control degree of freedom compared to the classical MMC.

A judicious path is provided by the integration of the low-frequency transformer (LFT) at the arm level of the MMC, i.e. merging the function of the arm inductors and the AC side line filter into the LFT leakage inductance [30–35]. The combination of the MMC and the LFT offers a single-stage conversion, a bi-directional power flow capability and a high efficiency provided by the low switching frequency of the MMC. This is presented in details in this paper, providing comprehensive modelling and assessment of two variants of the galvanically isolated modular converter (GIMC), namely stacked GIMC and interleaved GIMC. The GIMC applies a particular transformer winding arrangement in order to resolve the DC bias issue found in some works [36]. To have a reference case for comparison, the modelling of the classical MMC, in combination with an external LFT, is presented as well.

The paper is organised as follows: Section 2 provides further details related to the integration of the LFT into the MMC. Section 3 presents the comprehensive modelling of the MMC and two variants of GIMC, while Section 4 describes a system-level design. In Section 5, the control structure is presented considering all cases. In Section 6, detailed time-domain simulations are presented to demonstrate the overall system performance for the considered variants. Finally, conclusions are provided in Section 7.

2 Galvanically isolated MMC

2.1 Classical MMC with external LFT

To adjust the voltage and provide galvanic isolation, an LFT can be simply connected between the MMC AC-side terminals and the LVAC grid connection. This solution, presented in Fig. 1, is considered as the reference case for both modelling and control. The addition of an LFT does not modify the behaviour of the MMC, thus usual definitions and equations apply. Each MMC phase leg is formed by two arms, with indices p for the positive

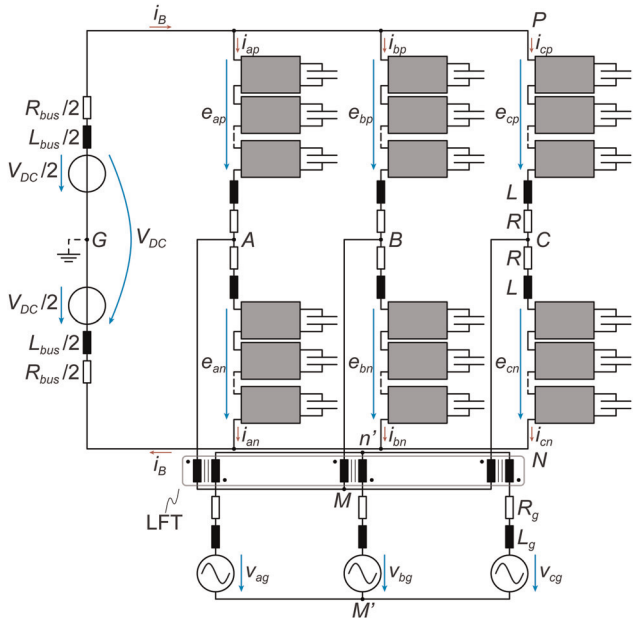

Fig. 1 *Classical MMC with external LFT*

one and n for the negative one. Each MMC arm comprises of N_{sm} series-connected SMs. In the scope of this paper, as the MV input is DC, only unipolar (half-bridge) cells are required. The possible output voltage levels of each cell are $\{0 \quad V_{sm}\}$. In the case of perfectly constant summed capacitor voltages, the modulation functions are given by

$$m_p(t) = \frac{1}{2}\left(1 - m\sin(\omega t)\right) \tag{1a}$$

$$m_n(t) = \frac{1}{2}\left(1 + m\sin(\omega t)\right) \tag{1b}$$

where $m \leq N_{sm}V_{sm}/(2V_{DC})$. The minimum required blocking voltage for each arm is V_{DC}; the midpoint out of each phase leg is allowed to swing between P and N.

2.2 MMC with integrated LFT

Several attempts have been made recently in the direction of the integration of the LFT windings [30, 31, 34] at the arm level of the MMC. They are presented shortly and general requirements for a DC free magnetic structure are derived. The closest proposal to the MMC was introduced by the authors [30, 31] and is presented in Fig. 2*a*. The LFT is connected to the p and n arms of one phase leg in an open-winding fashion, similar to the open-end winding configuration found in electrical drives. Therefore it is referenced as the open-end windings MMC (OEWMMC). The open-end windings connection implies a modification of the modulation functions and overall converter behaviour, as in order to prevent a DC voltage component across the windings of the LFT, an H-bridge alike operation has to be adopted, resulting in the following modulation functions

$$m_p(t) = m_n(t) = \frac{1}{2}\left(1 - m\sin(\omega t)\right) \tag{2}$$

where $m \leq N_{sm}V_{sm}/V_{dc}$. The blocking voltage capability of each arm is still V_{DC}. The output voltage on the HV-side of the transformer can have at most an amplitude of V_{PN}, which is twice the one of the classical MMC. It is important to notice that i_p and i_n are now identical, as there is no phase-leg midpoint present anymore. It has been shown in [36] that a DC current component, responsible for the power transfer between the DC and AC

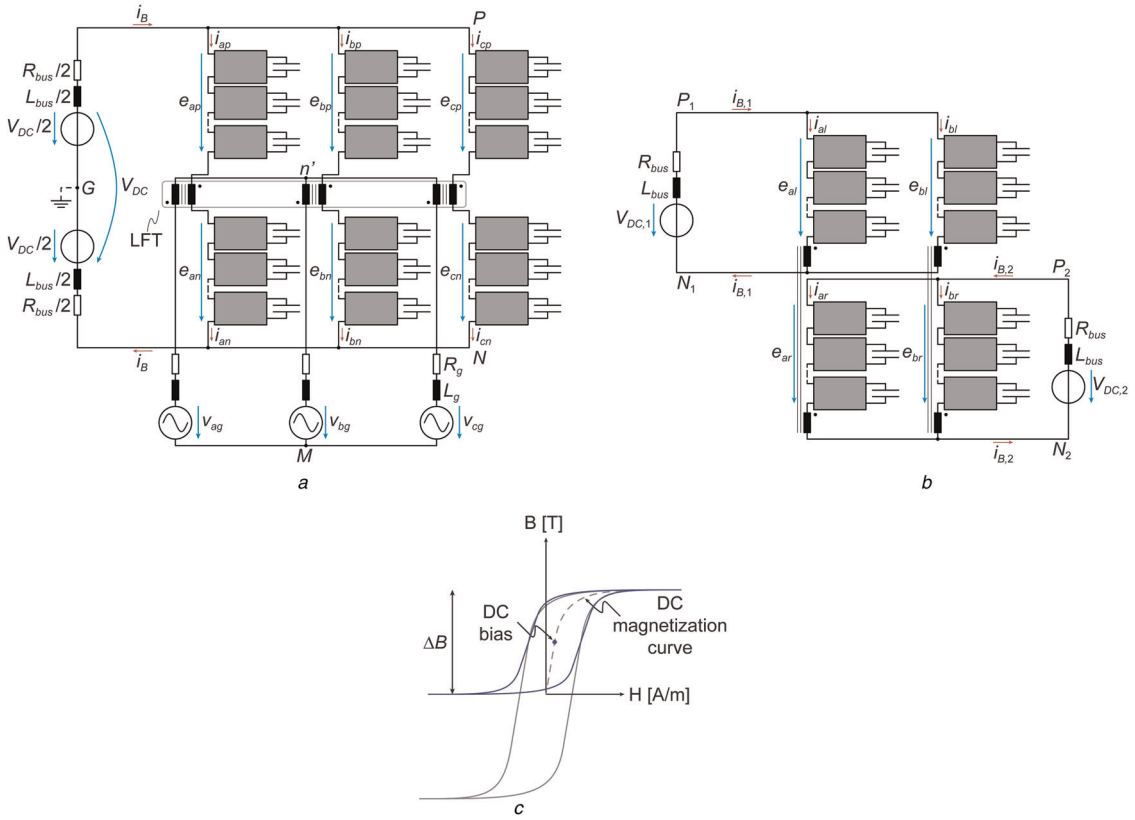

Fig. 2 *MMC topologies with transformer integration*

a Open-end windings MMC proposed in [31]
b Two ports isolated MMC proposed in [34]
c Reduction of the magnetic material utilisation (ΔB) for the OEWMMC due to the DC bias

terminals, flows through the HV windings. From that conclusion, the magnetic design would have to deal with this additional current component, resulting in a biased operation. Unfortunately, the DC current component is load dependent, and therefore its value moves between the first and third quadrants of the *BH* curve (Fig. 2*c*). Constructing this kind of transformer would result in significant over-sizing.

The second alternative was initially proposed in [34], more recently in [32], and is presented in Fig. 2*b*. While the proposal targets two ports isolated DC/DC converter for high power applications, it has relevance to the scope of the paper. Each LFT winding is series-connected with one MMC arm. The minimal configuration comprises of two phase legs per side (the magnetic coupling is indicated by thin double lines), so that an AC component can be circulated between phase legs without being reflected to any of the DC terminals. This translates into the following modulation functions, with the same additional condition of no DC voltage component across the LFT

$$m_{\mathrm{l}}(t) = m\sin(\omega t - \pi) \tag{3a}$$

$$m_{\mathrm{r}}(t) = m\sin(\omega t) \tag{3b}$$

where $m \leq N_{\mathrm{sm}}V_{\mathrm{sm}}/(2V_{\mathrm{DC}})$. The blocking capability of each arm is

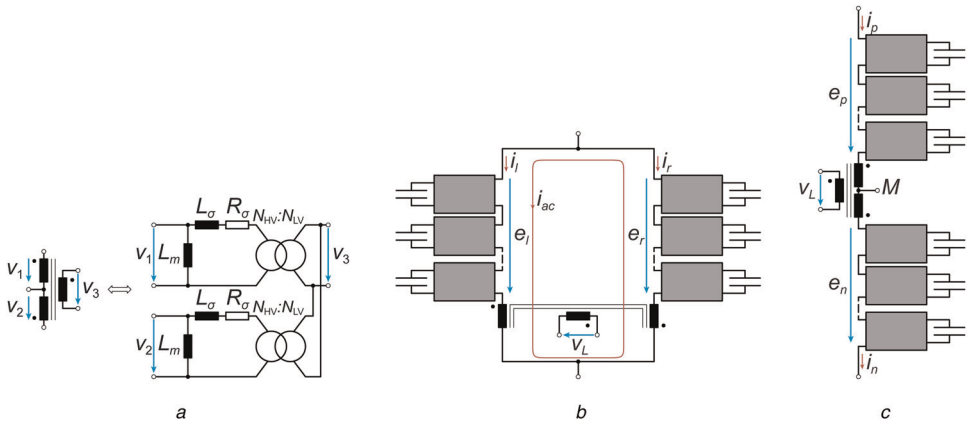

Fig. 3 *Elementary GIMC*

a Three-windings transformer with DC flux cancellation in the magnetic core as well as one of its equivalent circuit
b Interleaved GIMC
c Stacked GIMC

$2V_{dc}$. In this case, the DC cancellation inside the magnetic structure is achieved, as for any loading condition $i_{B,1}$ and $i_{B,2}$ have opposite signs.

2.3 Galvanically isolated modular converter

It is important to note that the phase leg structures presented in [31, 34] are in essence very similar, and positive and negative arms of [31] could be easily merged in one arm of [34]. This is also consistent with the total blocking capabilities of each phase leg. The DC cancellation cannot be achieved by control means, as the DC current flowing in each phase leg is load dependent and necessary for energy exchange (cf. [31]). However, a suitable windings configuration provides DC cancellation [34]. Based on these observations, it can be derived that the phase leg should comprise of at least two independent currents and if appropriate windings polarity of the LFT is provided, the DC component could be cancelled. The classical MMC features two different arm currents, whose difference forms the output current ($i_{AC} = i_p - i_n$) and pondered sum the circulating current ($i_{circ} = (i_p + i_n)/2$). This results in a need for a multi-winding transformer, as presented in Fig. 3*a*. A similar structure has already been introduced in [33, 35], but the systematic derivation of the two elementary stages of a GIMC has not been elaborated so far.

On the basis of the previous considerations, two fundamental structures can be generalised out of the same GIMC phase leg by either folding or unfolding. The folded one (pivot point is the midpoint out of the two windings HV-side) is referenced as interleaved GIMC, as shown in Fig. 3*b*, and the unfolded one as stacked GIMC, as shown in Fig. 3*c*. While only the interleaved GIMC can intrinsically handle DC/1-AC (single-phase conversion), two paralleled stacked GIMC phase legs are mandatory for the same conversion type. Each elementary GIMC is targeting different applications: the interleaved GIMC is more suitable for 'step-up' operation, as only half the DC-link voltage is necessary to obtain the same fundamental AC amplitude (compared to the classical MMC), while the stacked GIMC is much closer to the classical MMC. Similar configurations were reported under the names push-pull MMC [33] and three-windings MMC [35].

3 Modelling

To verify the impacts of the LFT integration on the overall converter characteristics, a model for each variant has been derived: (i) classical MMC with external LFT, (ii) interleaved GIMC and (iii) stacked GIMC. The modelling approach is similar to that proposed in [37].

3.1 Transformer model

A simplification of the classical T-shape transformer model is used (Fig. 3*a*), which is referred as the L-shaped transformer model in the literature. It is suitable as long as the modelling is aimed towards the control design, as it allows to reduce the number of state variables. Note that it is only valid if $L_{\sigma_{HV}} \ll L_m$ and $L_{\sigma_{LV}} \ll L_m$. Regarding conventions, the superscript prime indicates that a variable is referred to the HV-side. The following definitions apply

$$n = \frac{N_{LV}}{N_{HV}}, \quad V' = \frac{V}{n}, \quad I' = nI, \quad Z' = \frac{Z}{n^2} \tag{4}$$

where n is the transformer ratio, N_{HV} is the transformer HV-side number of turns, N_{LV} is the transformer LV-side number of turns, V is the voltage across transformer terminals on the LV side, I is a current on the LV-side and Z is an impedance on the LV-side. According to Fig. 3*a*, the following expressions describe the simplification

$$L_\sigma = L_{\sigma 1} + \frac{L_{\sigma 2}}{n^2}, \quad R_\sigma = R_{\sigma 1} + \frac{R_{\sigma 2}}{n^2} \tag{5}$$

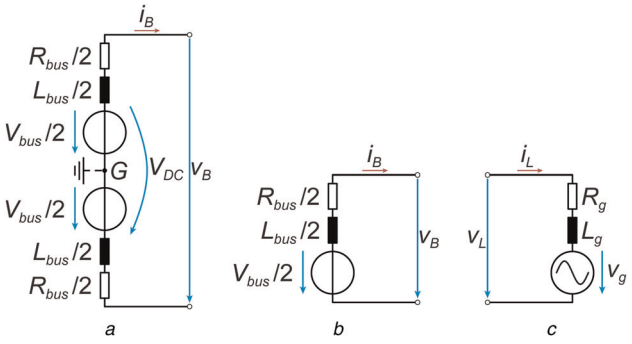

Fig. 4 *Circuit for external quantities*

a Bus side circuit for classical MMC and stacked GIMC
b Bus side circuit for interleaved GIMC
c Line side circuit

3.2 Common part of a model

The modelling of the external quantities related to the MVDC and LVAC terminals is identical to all three configurations and is done once to avoid repetition. The corresponding circuits are presented in Figs. 4*a–c*. Kirchhoff's voltage law (KVL) equations consider terminal voltages, namely v_B on the bus side and v_L on the line side

$$v_{bus} = R_{bus} i_B + L_{bus} \frac{d}{dt} i_B + v_B \tag{6a}$$

$$\frac{v_{bus}}{2} = \frac{R_{bus}}{2} i_B + \frac{L_{bus}}{2} \frac{d}{dt} i_B + v_B \tag{6b}$$

$$v_{L'} = \frac{R_g}{n} i_L + \frac{L_g}{b} \frac{d}{dt} i_L + \frac{v'_g}{n} \tag{6c}$$

3.3 Classical MMC modelling

The modelling of the MMC has been widely reported in the literature, and no unique tool exists. By contrast, some models fail to cover certain part such as the summed capacitor voltage ripple. In that perspective, the arm is modelled at a macroscopic level by a pair of controlled voltage and current sources, where $x \in \{p, n\}$

$$e_x = m_x V_x^\Sigma, \quad i_x^\Sigma = m_x i_x \tag{7}$$

The definition for the arm capacitance and arm resistance follows the usual definitions

$$C_{arm} = \frac{C_{sm}}{N_{sm}}, \quad R_{eq} = R_{sm} N_{sm} \tag{8}$$

The modelling highlights the decoupling between the bus side (v_B) and line side (v_L) terminals, a particular feature of the MMC compared to conventional topologies. For the sake of simplicity, only a single phase leg is modelled and the extension to three phases is straightforward. The equivalent model of a classical MMC phase leg is represented in Fig. 5*a*. For instance, the external bus and line circuits, modelled in the previous subsection, should be connected between the terminals forming v_B and v_L, respectively.

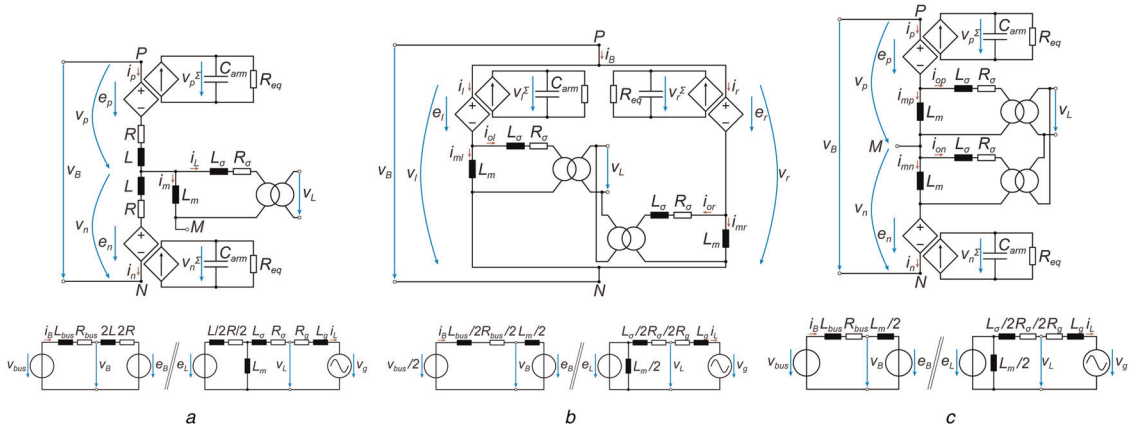

Fig. 5 *Modelling*

a Classical MMC phase leg with average arm model and its decoupled representation
b Interleaved GIMC phase leg with average arm model and its decoupled representation
c Stacked GIMC phase leg with average arm model and its decoupled representation

KVL is applied to both bus side and line side terminals, resulting into as many equations as state variables (i_B, i_L and i_m)

$$v_B = e_p + e_n + R(i_p + i_n) + L\left(\frac{d}{dt}i_p + \frac{d}{dt}i_n\right) \tag{9a}$$

$$v'_L = \frac{-e_p + e_n}{2} - \frac{R}{2}(i_p - i_n) - \frac{L}{2}\left(\frac{d}{dt}i_p - \frac{d}{dt}i_n\right) - R_\sigma i_L - L_\sigma \frac{d}{dt}i_L \tag{9b}$$

$$v'_L = -R_\sigma i_L - L_\sigma \frac{d}{dt}i_L + L_m \frac{d}{dt}i_m \tag{9c}$$

A more convenient set of variables are introduced to better reflect the dynamics of the model

$$\begin{aligned} v_B &= v_p + v_n, \quad e_B = e_p + e_n, \quad i_B = \frac{i_p + i_n}{2}, \\ v'_L &= \frac{-v_p + v_n}{2}, \quad e_L = \frac{-e_p + e_n}{2}, \quad i_L = i_p - i_n - i_m \end{aligned} \tag{10}$$

with all variables indicated in Fig. 5*a*. The decoupling between the bus side and line side terminals of the MMC can be effectively highlighted by the adoption of the following state-space representation

$$\begin{bmatrix} 2L & 0 & 0 \\ 0 & -L/2 - L_\sigma & -L/2 \\ 0 & -L_\sigma & L_m \end{bmatrix} \frac{d}{dt}\begin{bmatrix} i_B \\ i_L \\ i_m \end{bmatrix} + \begin{bmatrix} 2R & 0 & 0 \\ 0 & -R/2 - R_\sigma & -R/2 \\ 0 & -R_\sigma & 0 \end{bmatrix}\begin{bmatrix} i_B \\ i_L \\ i_m \end{bmatrix} = \begin{bmatrix} v_B - e_B \\ v'_L - e_L \\ v'_L \end{bmatrix} \tag{11}$$

In this representation, the bus current i_B and the pair of AC quantities (i_m and i_L) are decoupled, as shown by the zero elements in the coefficient matrices. This result might therefore be translated into the graphical representation of Fig. 5*a*. Please note that i_m is not multiplied with any resistive term, as the magnetising branch model does not include any resistive part.

3.4 GIMC modelling

Due to their close similarities, the modelling of the two GIMC structures is merged. Similar to the classical MMC case, the modelling follows the same path: the average arm model as well as the transformer equivalent circuit are the same, except that the HV-side is formed by two independent windings (cf. Figs. 5*b* and *c*).

KVL are once again applied to each GIMC phase leg, and the result is contained in the equations (12) and (13).

$$\text{Interleaved:} \begin{cases} v_B = \dfrac{e_l + e_r}{2} + \dfrac{L_m}{2}\left(\dfrac{d}{dt}i_{ml} + \dfrac{d}{dt}i_{mr}\right) \\ v_L = \dfrac{-e_l + e_r}{2} + \dfrac{R_\sigma}{2}(-i_{ol} + i_{or}) + \dfrac{L_\sigma}{2}\left(-\dfrac{d}{dt}i_{ol} + \dfrac{d}{dt}i_{or}\right) \\ v_L = \dfrac{R_\sigma}{2}(-i_{ol} + i_{or}) + \dfrac{L_\sigma}{2}\left(-\dfrac{d}{dt}i_{ol} + \dfrac{d}{dt}i_{or}\right) + \dfrac{L_m}{2}\left(\dfrac{d}{dt}i_{ml} - \dfrac{d}{dt}i_{mr}\right) \end{cases} \tag{12}$$

$$\text{Stacked:} \begin{cases} v_B = e_p + e_n + L_m\left(\dfrac{d}{dt}i_{mp} + \dfrac{d}{dt}i_{mn}\right) \\ v_L = \dfrac{-e_p + e_n}{2} + \dfrac{R_\sigma}{2}\left(-i_{op} + i_{on}\right) + \dfrac{L_\sigma}{2}\left(-\dfrac{d}{dt}i_{op} + \dfrac{d}{dt}i_{on}\right) \\ v_L = \dfrac{R_\sigma}{2}\left(-i_{op} + i_{on}\right) + \dfrac{L_\sigma}{2}\left(-\dfrac{d}{dt}i_{op} + \dfrac{d}{dt}i_{on}\right) + \dfrac{L_m}{2}\left(\dfrac{d}{dt}i_{mp} - \dfrac{d}{dt}i_{mn}\right) \end{cases} \tag{13}$$

As it can be seen, with the exception of the first rows of (12) and (13), the indices $\{l, r\}$ and $\{p, n\}$ can be seamlessly exchanged. This also implies a unique state-space representation, however, with different definitions for the bus variables

$$\text{Interleaved:}\begin{cases} v_{\mathrm{B}} = \dfrac{v_{\mathrm{l}} + v_{\mathrm{r}}}{2}, & v_{\mathrm{L}} = \dfrac{-v_{\mathrm{l}} + v_{\mathrm{r}}}{2} \\ e_{\mathrm{B}} = \dfrac{e_{\mathrm{l}} + e_{\mathrm{r}}}{2}, & e_{\mathrm{L}} = \dfrac{-e_{\mathrm{l}} + e_{\mathrm{r}}}{2} \\ i_{\mathrm{B}} = i_{\mathrm{l}} + i_{\mathrm{r}}, & i_{\mathrm{L}} = i_{\mathrm{l}} - i_{\mathrm{r}} - i_{\mathrm{m}} = i_{ol} - i_{or} \end{cases} \tag{14}$$

$$\text{Stacked:}\begin{cases} v_{\mathrm{B}} = v_p + v_n, & v_{\mathrm{L}} = \dfrac{-v_p + v_n}{2} \\ e_{\mathrm{B}} = e_p + e_n, & e_{\mathrm{L}} = \dfrac{-e_p + e_n}{2} \\ i_{\mathrm{B}} = \dfrac{i_p + i_n}{2}, & i_L = i_{\mathrm{p}} - i_n - i_{\mathrm{m}} = i_{op} - i_{on} \end{cases} \tag{15}$$

The following state-space representation stems from the introduction of (14) and (15):

$$\begin{bmatrix} L_{\mathrm{m}}/2 & 0 & 0 \\ 0 & -L_\sigma/2 & 0 \\ 0 & -L_\sigma/2 & L_{\mathrm{m}}/2 \end{bmatrix} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\mathrm{B}} \\ i_L \\ i_{\mathrm{m}} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & -R_\sigma/2 & 0 \\ 0 & -R_\sigma/2 & 0 \end{bmatrix} \begin{bmatrix} i_{\mathrm{B}} \\ i_L \\ i_{\mathrm{m}} \end{bmatrix} = \begin{bmatrix} v_{\mathrm{B}} - e_{\mathrm{B}} \\ v'_{\mathrm{L}} - e_{\mathrm{L}} \\ v'_{\mathrm{L}} \end{bmatrix} \tag{16}$$

The decoupling between the bus side and line side terminals is graphically presented in Figs. 5*b* and *c*. From (16), one may notice that to get the same filtering performances with GIMC as with the classical MMC, the leakage impedances have to be doubled since only half the grid current flows through each leakage winding.

4 System level design

To evaluate and compare the performances of all three topologies, a converter system with parameters as provided in Table 1 is analysed. The design has been done considering a 10 MVA conversion with 10 kV DC on the MV side and 400 V AC on the LV side. Section 3 has provided the demonstration that all three topologies are very similar from the control point of view, as it can be seen from the state-space representations in (11) and (16).

4.1 Arm inductor sizing

The selection of an arm inductance value is done considering the DC-link fault behaviour (current limitation). If the arm resistance is neglected, the current slope is given by $\alpha = V_{\mathrm{DC}}/(2L_{\mathrm{arm}})$. Given $L_{\mathrm{arm}} = 0.75$ mH, the corresponding value for the current slope under DC fault is $\alpha = 6.67$ kA/ms.

4.2 Capacitor sizing

The SM's capacitor sizing is tightly linked to the energy requirements (amount of energy buffered in the arm) and the allowed voltage ripple. Those two items would be the same as for any classical topology. However, the capacitor sizing is also affected by the control method selected for the circulating current and the operating condition (grid unbalance etc.). The sizing of the SM's capacitor has already been presented in [38–40].

The worst case for the SM's capacitor sizing occurs when there is neither a common mode voltage injection nor a double line frequency circulating current injection. It is assumed that the arm current is composed only of a DC circulating current and half of the grid current. In that scenario, the capacitive arm powers for the phase *a* are given by (note that an additional $\mp 2\pi/3$ phase shift gives the expressions for the two other phases)

$$\begin{aligned} p_{C,ap} = e_{ap} i_{ap} &= \frac{V_{\mathrm{B}}}{2}\left(1 - m\cos(\omega t)\right)\left(I_{\mathrm{circ},0} + \frac{1}{2}\hat{i}_{\mathrm{g}}\cos(\omega t + \phi)\right) \\ &= \frac{1}{2}V_{\mathrm{B}}I_{\mathrm{circ},0} + \frac{1}{4}V_{\mathrm{B}}\hat{i}_{\mathrm{g}}\cos(\omega t + \phi) - \frac{1}{2}mV_{\mathrm{B}}I_{\mathrm{circ},0}\cos(\omega t) \\ &\quad - \frac{1}{8}mV_{\mathrm{B}}\hat{i}_{\mathrm{g}}\left(\cos(\phi) + \cos(2\omega t + \phi)\right) \end{aligned} \tag{17a}$$

$$\begin{aligned} p_{C,an} = e_{an} i_{an} &= \frac{V_{\mathrm{B}}}{2}\left(1 + m\cos(\omega t)\right)\left(I_{\mathrm{circ},0} - \frac{1}{2}\hat{i}_{\mathrm{g}}\cos(\omega t + \phi)\right) \\ &= \frac{1}{2}V_{\mathrm{B}}I_{\mathrm{circ},0} - \frac{1}{4}V_{\mathrm{B}}\hat{i}_{\mathrm{g}}\cos(\omega t + \phi) + \frac{1}{2}mV_{\mathrm{B}}I_{\mathrm{circ},0}\cos(\omega t) \\ &\quad - \frac{1}{8}mV_{\mathrm{B}}\hat{i}_{\mathrm{g}}\left(\cos(\phi) + \cos(2\omega t + \phi)\right) \end{aligned} \tag{17b}$$

In steady state, the DC power balance has to be guaranteed. This means the terms $V_{\mathrm{B}}I_{\mathrm{circ},0}/2 - mV_{\mathrm{B}}\hat{i}_{\mathrm{g}}\cos(\phi)/8$ have to cancel each other, leading to a condition on $I_{\mathrm{circ},0}$

$$I_{\mathrm{circ},0} = \frac{m\hat{i}_{\mathrm{g}}\cos(\phi)}{4} \tag{18}$$

The time integration of the remaining terms gives the energy ripple at the arm level

$$\begin{aligned} \tilde{E}_{C,ap} &= \frac{V_{\mathrm{B}}\hat{i}_{\mathrm{g}}}{4\omega}\sin(\omega t + \phi) - \frac{mV_{\mathrm{B}}I_{\mathrm{circ},0}}{2\omega}\sin(\omega t) \\ &\quad - \frac{mV_{\mathrm{B}}\hat{i}_{\mathrm{g}}}{16\omega}\sin(2\omega t + \phi) \end{aligned} \tag{19a}$$

$$\begin{aligned} \tilde{E}_{C,an} &= -\frac{V_{\mathrm{B}}\hat{i}_{\mathrm{g}}}{4\omega}\sin(\omega t + \phi) + \frac{mV_{\mathrm{B}}I_{\mathrm{circ},0}}{2\omega}\sin(\omega t) \\ &\quad - \frac{mV_{\mathrm{B}}\hat{i}_{\mathrm{g}}}{16\omega}\sin(2\omega t + \phi) \end{aligned} \tag{19b}$$

From there, as $C_{\mathrm{arm}} = 2\Delta\tilde{E}/\left(V^2_{C_{\mathrm{arm,max}}} - V^2_{C_{\mathrm{arm,min}}}\right)$, it is found that the required equivalent arm capacitor is

$$C_{\mathrm{arm}} = \frac{\Delta\tilde{E}_{C,ap/n}}{2k_{\mathrm{r}}V^2_{C_{\mathrm{arm}}}} \tag{20}$$

where k_{r} is the capacitor voltage ripple factor, $V_{C_{\mathrm{arm,max}}} = (1 + k_{\mathrm{r}})V_{C_{\mathrm{arm}}}$, $V_{C_{\mathrm{arm,min}}} = (1 - k_{\mathrm{r}})V_{C_{\mathrm{arm}}}$, so that $\Delta V_{C_{\mathrm{arm}}} = 2k_{\mathrm{r}}V_{\mathrm{DC}}$. The comparison between the analytical method and PLECS simulation (with average model), where similar operating conditions where recreated (especially no second harmonic current) are presented in Fig. 6*a*. The reason for the acceptable error between the two is that R_{arm} and L_{arm} was neglected in the analytical expressions. The verification that the capacitor voltage ripple is within the bounds (black lines) is illustrated in Fig. 6*b*. It is finally found that $C_{\mathrm{sm}} = 13.3$ mF. This corresponds to an energy requirement of 45.3 kJ/MVA (with $k_{\mathrm{r}} = 0.1$).

5 Control system design

The control structure has to consider the so-called internal state variables, specific to MMC or GIMCs, and external state variables, common to any inverter topology. In addition, the arm balancing algorithm is briefly presented. The overall control scheme is shown in Fig. 7*a*. Due to the tight similarities in the derived state-space models (11) and (16), the same control strategy is applied to all three topologies.

Table 1 System parameters

V_{DC}	10 kV	L_{bus}	500 μH	R_{bus}	10 mΩ	N_{sm}	8	k_r	10%	C_{sm}	13.3 mF
L_{arm}	0.75 mH	R_{arm}	16.7 mΩ	L_m	172.5 mH[a]/345mH[b]	L_g	0 mH	R_g	0 mΩ	S	10 MVA
L_σ	1 μH	R_σ	1 mΩ	$f_{sw,app}$	3 kHz	n	0.0765				

[a]Classical MMC and [b]GIMC

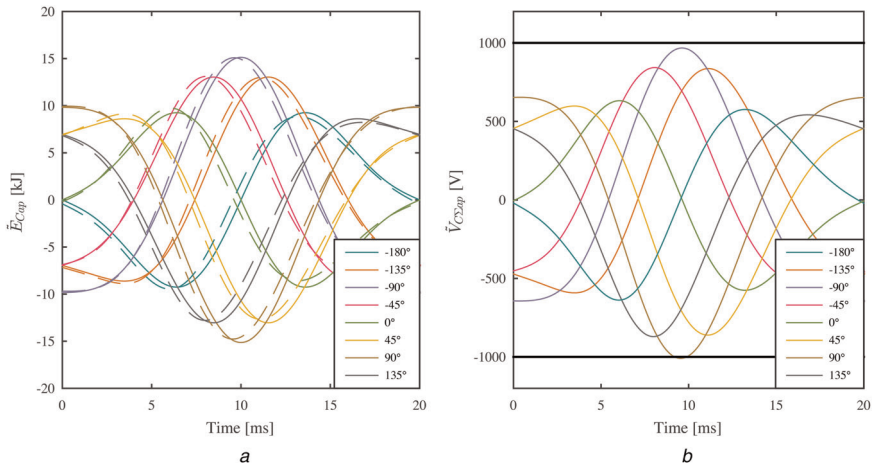

Fig. 6 *Verification of the SM capacitor sizing method (analytical and PLECS average model simulations) over one fundamental period as function of the load angle ϕ, owing the fact that the analytical expressions do not take into account R_{arm} and C_{arm}*

a Comparison of the energy ripple waveforms (solid: analytical and dashed: simulation)
b Verification that the summed capacitor voltage ripples are within the bounds. The difference in (a) comes from the fact that the analytical expression does not account for the arm impedance (L_{arm} and R_{arm})

5.1 Internal state variables control

The selected control method is based on the state-of-the-art control structure for MMC [41]: both the sum and difference of the summed capacitor voltages are controlled. The former ensures the horizontal balance via the total energy control [Fig. 7*b* (top left)], while the latter ensures the vertical balance via the differential energy control [Fig. 7*b* (top right)]. Following this coordinate transformation, the corresponding modulation indices are estimated by

$$m_\Sigma = m_p + m_n \Rightarrow m_{\Sigma,\text{est}} = \frac{1}{2}\left(\frac{v_B}{v_{C\Sigma p}} + \frac{v_B}{v_{C\Sigma n}}\right) \tag{21a}$$

$$m_\Delta = -\frac{1}{2}m_p + \frac{1}{2}m_n \Rightarrow m_{\Delta,\text{est}} = \frac{1}{2}\left(\frac{v_L}{v_{C\Sigma p}} + \frac{v_L}{v_{C\Sigma n}}\right) \tag{21b}$$

Each component has dominant double and fundamental grid frequency components, respectively, that are filtered out by notch filters. The current reference from the total energy controller has to be transformed ($2/m_{\Sigma,\text{est}}$ factor). The current reference from the differential energy controller is mapped in the fundamental frequency referential by using the following matrix, initially proposed in [42] see (22)
where θ_L is the angle of e_L. The idea behind this matrix is to induce reactive power flows in the adjacent phases to compensate for the active power flow in one phase that is required to compensate for a vertical unbalance. This means no grid frequency current component is present on the DC link.

The current references are summed up and a circulating current controller [PI + R Fig. 7*b* (bottom left)] controls the DC, fundamental and second harmonic components. For implementation reasons, non-ideal proportional resonant (PR) controllers $G_{PR,ni}(s)$ are used instead of ideal PR $G_{PR,i}(s)$

$$G_{PR,i}(s) = \frac{k_i s}{s^2 + \omega^2} \rightarrow G_{PR,ni}(s) = \frac{2k_i\omega_c s}{s^2 + 2\omega_c s + \omega^2} \tag{23}$$

where ω is the resonant frequency and $\omega_c = \omega/Q$. The integral gain k_i is chosen considering dynamic error settling time.

5.2 External state variables control

Under identical line side impedance condition (the impedances towards the grid are identical for both classical MMC and GIMC), i.e.

$$L_{MMC} = \frac{L_{arm}}{2} + L_\sigma + L'_g \leftrightarrow L_{GIMC} = \frac{L_\sigma}{2} + L'_g \tag{24}$$

the grid current control is identical to classical MMC and GIMCs. The control implementation relies on PR controllers in stationary reference frame ($\alpha\beta$) [Fig. 7*b* (bottom right)]. In that sense, it is not different from a classical grid tied inverter control algorithms. The frequency information, ω, is retrieved by a phase-locked loop (PLL). As grid unbalance handling is out of the scope of this paper, a *dq*-PLL is implemented.

5.3 Modulation and arm balancing

Depending on the modulation technique, the arm balancing can either be based on a sorting algorithm or on a proportional controller that is deployed in a decentralised manner on each SM. In this paper, phase disposition pulse-width modulation

$$\boldsymbol{M} = \begin{bmatrix} \cos(\theta_L) & -\sin(\theta_L)/\sqrt{3} & \sin(\theta_L)/\sqrt{3} \\ \sin(\theta_L - 2\pi/3)/\sqrt{3} & \cos(\theta_L - 2\pi/3) & -\sin(\theta_L - 2\pi/3)/\sqrt{3} \\ -\sin(\theta_L + 2\pi/3)/\sqrt{3} & \sin(\theta_L + 2\pi/3)/\sqrt{3} & \cos(\theta_L + 2\pi/3) \end{bmatrix} \tag{22}$$

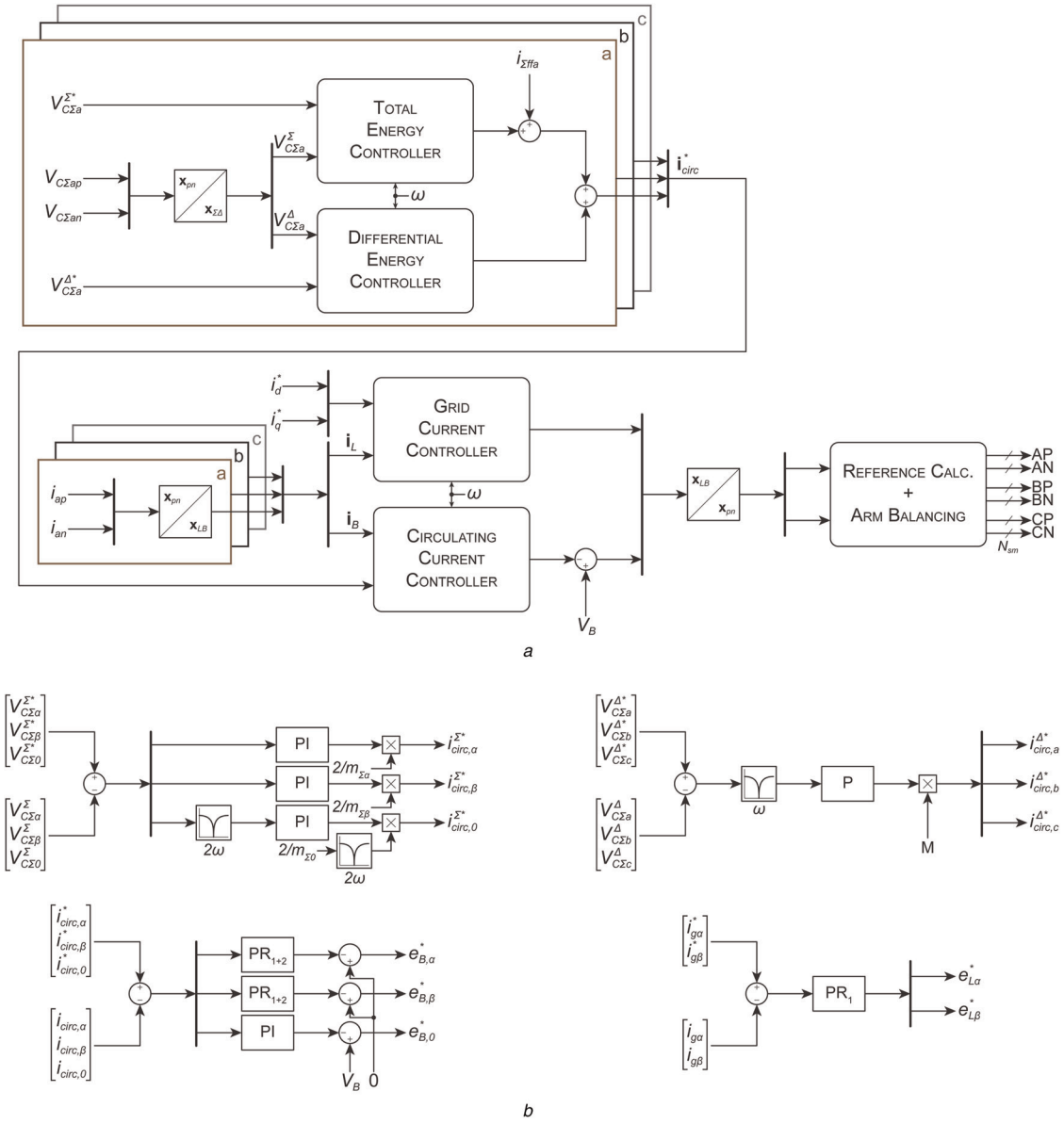

Fig. 7 *Control structure*

a Complete control scheme, as well as arm balancing

b Detailed control blocks: total energy control (top left), differential energy control (top right), circulating current control (bottom left) and grid current control (bottom right)

(PD-PWM) in combination with the restricted sorting algorithm was selected [20]. PD-PWM offers lower total harmonic distortion (THD) compared to phase-shifted pulse-width modulation. The implementation requires only one carrier and a quantiser per arm. For each transition in the arm voltage waveform, the best candidate SM is inserted/bypassed, leading to an optimised modulation. Compared to a classical sorting algorithm, this method avoids big shifts between the sets of inserted and bypassed SMs. Regarding its implementation, no sorting algorithm is required, but only min/max searches, in contrast to the original implementation using two sorting loops.

5.4 Second harmonic circulating current injection

A second harmonic circulating current component might be added to the capacitive arm power expressions. Its magnitude and phase are free to choose. As it can be seen in (25a), the double underlined term could be used to compensate for the single underlined term in $2\omega t$, leading to the definition of $\hat{i}_{\text{circ},2}$ and θ_2. This principle was initially proposed in [21] (see (25a))

$$\hat{i}_{\text{circ},2} = \frac{m\hat{i}_{\text{g}}}{4}, \quad \theta_2 = \phi \tag{25b}$$

$$\begin{aligned} p_{C,p} = e_p i_p &= \frac{V_{\text{B}}}{2}\left(1 - m\cos(\omega t)\right)\left(I_{\text{circ},0} + \frac{1}{2}\hat{i}_{\text{g}}\cos(\omega t + \phi) + \hat{i}_{\text{circ},2}\cos(2\omega t + \theta_2)\right) \\ &= \frac{1}{2}V_{\text{B}}I_{\text{circ},0} + \frac{1}{4}V_{\text{B}}\hat{i}_{\text{g}}\cos(\omega t + \phi) + \underline{\underline{\frac{1}{2}V_{\text{B}}\hat{i}_{\text{circ},2}\cos(2\omega t + \theta_2)}} - \frac{1}{2}mV_{\text{B}}I_{\text{circ},0}\cos(\omega t) \\ &\quad \underline{-\frac{1}{8}mV_{\text{B}}\hat{i}_{\text{g}}}\left(\cos(\phi) + \underline{\cos(2\omega t + \phi)}\right) - \frac{1}{4}V_{\text{B}}m\hat{i}_{\text{circ},2}\left(\cos(\omega t + \theta_2) + \cos(3\omega t + \theta_2)\right) \end{aligned} \tag{25a}$$

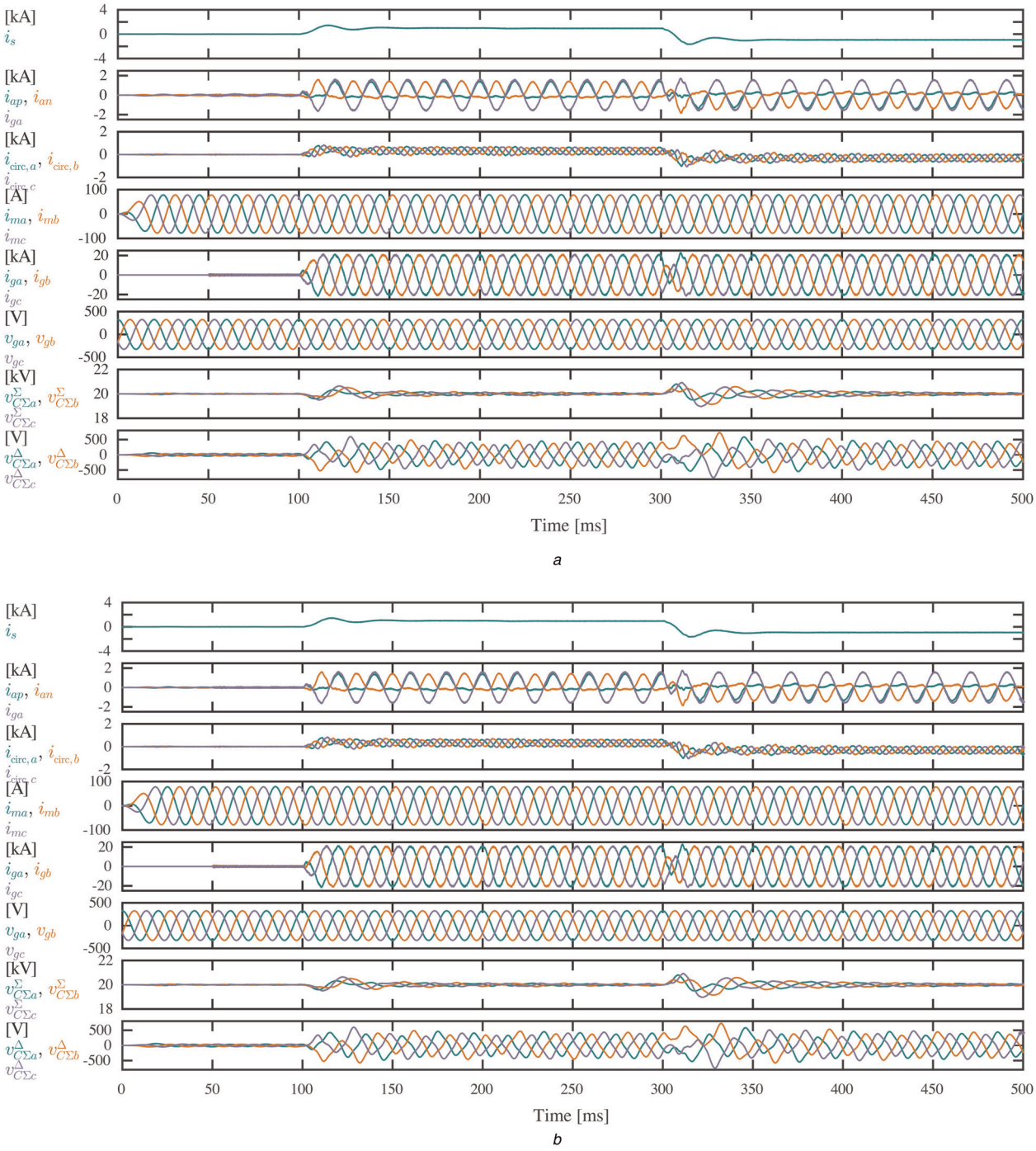

Fig. 8 *Simulation results*

a Classical MMC with second harmonic circulating current injection
b Stacked GIMC with second harmonic circulating current injection
c Interleaved GIMC with second harmonic circulating current injection
d Stacked GIMC without second harmonic circulating current injection

6 Simulation results

All three topologies are implemented in Matlab/Simulink with PLECS blockset as fully switched models. Extensive simulation results show the DC bias cancellation in the magnetising flux component (the magnetising current i_{mag}, image of the magnetising flux, has been selected here instead, as $\Lambda_{\mathrm{m}} = L_{\mathrm{m}} i_{\mathrm{m}}$), demonstrating the effectiveness of the use of a multi-windings LFT. Dynamic performances of the control structure are assessed, considering reference and load changes.

For all simulations, the scenario is the same regarding the current profile: during the first 50 ms, the transformer is magnetised. At $t = 5$ ms, the grid connection is established. At first, converters operates at nominal power (only active) and feeds the AC grid, followed by a reactive current increase to one-third of the nominal current (and as a consequence a reduction of $i_{gd,\mathrm{ref}}$ to maintain $I_{\max} = 2SV_{\mathrm{B}}/(3\hat{v}_{\mathrm{g}}) = \sqrt{i^2_{gd,\mathrm{ref}} + i^2_{gq,\mathrm{ref}}}$ constant). At $t = 300$ ms, an active power reversal is applied. Please note that each current reference change is applied with a ramp over 10 ms. Two sets of simulations are carried: (i) with second harmonic circulating current injection and (ii) without second harmonic circulating current. In any case, a DC circulating current corresponding to the power transfer, namely $\hat{v}_{\mathrm{g}} i_{gd,\mathrm{ref}}/(2V_{\mathrm{B}})$, is feed-forwarded in the circulating current control.

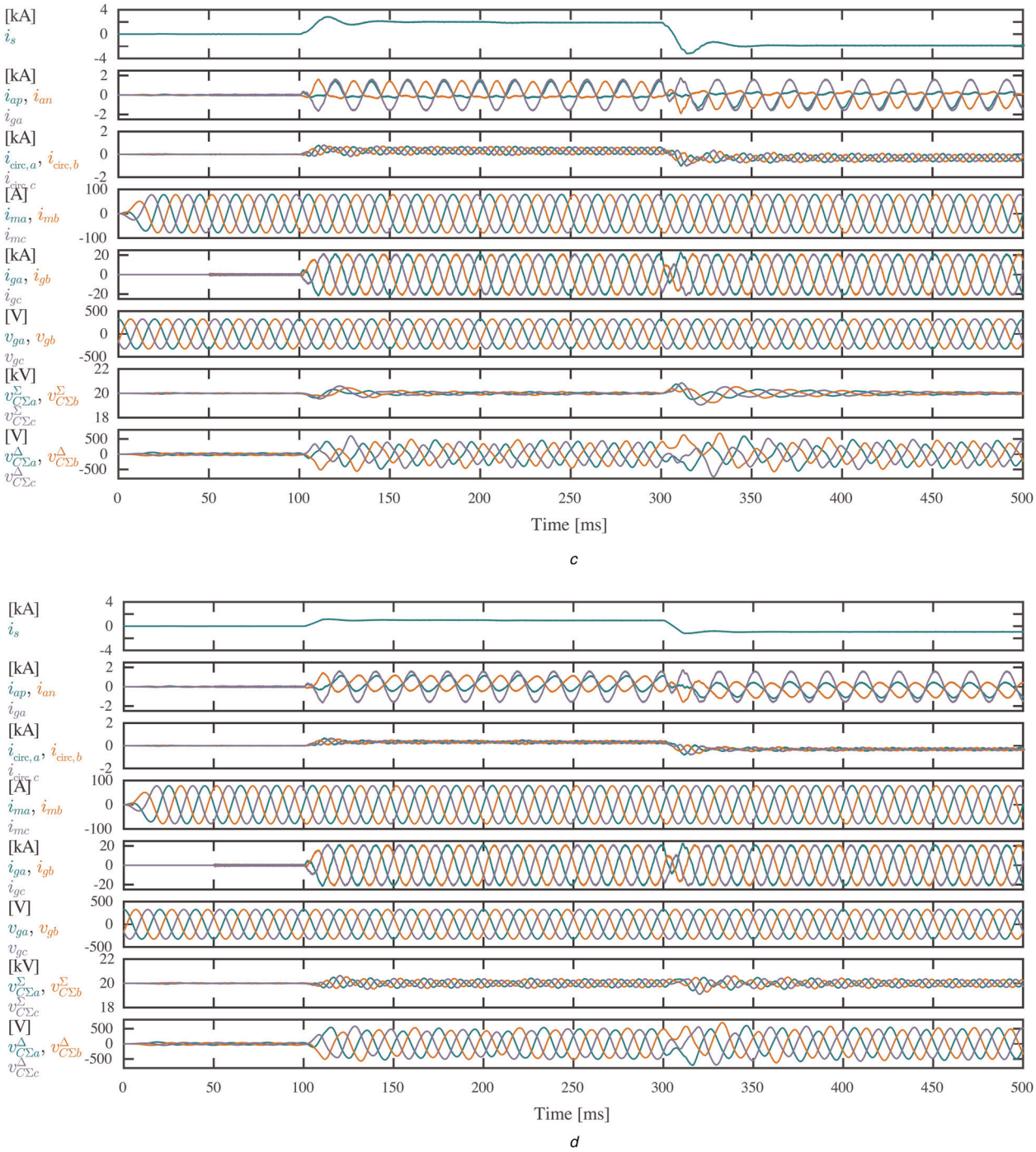

Fig. 8 *Continued*

6.1 Case 1 – circulating current injection

The simulation results for case 1 are presented in Figs. 8*a*–*c*. In these figures, the presence of a second harmonic circulating current is clearly visible in the third plot from the top. As a consequence, the sums of the summed capacitor voltages have reduced oscillations. For the stacked GIMC and the interleaved GIMC, similar dynamics and magnitudes compared to the classical MMC case are obtained. During the whole simulation, the transformer does not experience any DC bias (fourth plot). Note that for the interleaved GIMC, the DC bus current i_{bus} (first plot) is twice compared to the two other topologies, as the power transfer is maintained with a DC-link voltage halved.

Based on results from these simulations, the absence of difference between GIMC and the classical MMC is confirmed from a control point of view, matching the observations on the obtained state-space models in Section 3. For that reason, only the stacked GIMC topology has been considered for the second case. Despite being applied to only one topology, the simulation results can be easily extended to the two complementary ones without restriction.

6.2 Case 2 – no circulating current injection

In case that no second harmonic circulating current is injected, the circulating current only contains a DC term and a fundamental frequency term used for vertical balancing (Fig. 8*d*). This mode of operation leads to reduced arm current RMS value, but at the same time increased capacitor voltage ripples can be observed. Nevertheless, the circulating current controller performs the same function as with the classical MMC.

7 Conclusion

The integration of the LFT into the MMC has been analysed in this paper for the high power MVDC/3-LVAC conversion. Two basic converter structures, interleaved GIMC and stacked GIMC, have been proposed and analysed. Both of them enable the cancellation of the DC flux inside the LFT, making the proposal feasible. The modelling has shown great similarities with the classical MMC with external LFT, allowing for the same control method to be deployed. Detailed simulations have been carried with switched PLECS models for all three topologies, with and without second harmonic circulating current injection. It has been shown that for the proposed topologies similar arm dynamics can be achieved under equivalent arm impedances. This implies that care should be taken during arm inductance value selection and design, realised as leakage inductance of the integrated LFT. The proposed GIMC topologies are suited for high power applications with large voltage step ratio, offering prospects of highly efficient single-stage conversion in contrast to various competing SST proposals.

8 Acknowledgments

This work was part of the Swiss Competence Centers for Energy Research (SCCER) initiative which is supported by the Swiss Commission for Technology and Innovation (CTI) with focus on Future Swiss Electrical Infrastructure (FURIES).

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