

# Fast Simulation of Electromagnetic Transients in Power Systems: Numerical Solvers and their Coupling with the Electromagnetic Time Reversal Process

THÈSE N° 6903 (2016)

PRÉSENTÉE LE 21 MARS 2016

À LA FACULTÉ DES SCIENCES ET TECHNIQUES DE L'INGÉNIEUR  
LABORATOIRE DES SYSTÈMES ÉLECTRIQUES DISTRIBUÉS - CHAIRE EOS HOLDING  
ET  
LABORATOIRE DE COMPATIBILITÉ ÉLECTROMAGNÉTIQUE  
PROGRAMME DOCTORAL EN GÉNIE ÉLECTRIQUE

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

PAR

Reza RAZZAGHI

acceptée sur proposition du jury:

Dr S.-R. Cherkaoui, président du jury  
Prof. M. Paolone, Prof. F. Rachidi-Haeri, directeurs de thèse  
Prof. J. Mahseredjian, rapporteur  
Prof. X. Guillaud, rapporteur  
Prof. A. Skrivervik, rapporteuse



ÉCOLE POLYTECHNIQUE  
FÉDÉRALE DE LAUSANNE

Suisse  
2016



To my parents & my sister with all my love...



# Acknowledgements

This work would not have been completed without the help and support of many kind people around me, to only some of whom it is possible to give particular mention here.

First and foremost, I would like to express my deepest gratitude to my thesis directors, Prof. Mario Paolone and Prof. Farhad Rachidi for giving me the opportunity to pursue my PhD thesis under their supervision. Their deep knowledge, kindness, invaluable guidance, scientific enthusiasm, excellent support, and endless encouragement made the PhD period a wonderful experience. It has been truly an honor to work with them during the past few years. Thanks Mario, thanks Farhad!

My sincere thanks go to the members of my jury, Prof. Jean Mahseredjian, Prof. Xavier Guillaud, Prof. Anja Skrivervik, and Dr. Rachid Cherkaoui for their encouraging and insightful comments. I am in particular grateful to Prof. Jean Mahseredjian for offering me the unique opportunity to do an internship in his lab at École Polytechnique de Montréal.

I would like also to acknowledge the Swiss National Science Foundation (Grant 200021\_146414) for funding this dissertation.

I would like to address my heartfelt thanks to Prof. Majid Sanaye-Pasand and Dr. Mahdi Davarpanah my supervisors during my Master's project at UT for their constant help, support and encouragement.

I am deeply grateful to Mrs. Andrée Moinat and Mrs. Sophie Flynn secretaries of the Laboratory, for all their constant availability, sympathy, and kindness. Merci Andrée et Sophie!

My time at EPFL was made enjoyable by an amicable environment in the laboratory. Tremendous thanks to all the members of ELL building for the friendly atmosphere and the priceless moments (listed without order): Jean-Michel Buemi, Dr. Keyhan Sheshyekani, Dr. Lazar Bizumic, Dr. Carlos Alberto Romero, Dr. Alexander Smorgonskiy, Dr. Felix Vega, Nicolas Mora, Gaspar Lugrin, Dr. Ali Ahmadi-Khatir, Dr. Paolo Romano, Dr. Stela Sarri, Dr. Omid Alizadeh Mousavi, Dr. Mokhtar Bozorg, Mostafa Nick, Maryam Bahramipanah, Mohammad Azadifar, Dr. Konstantina Christakou, Dr. Dimitri Torregrossa, Marco Pignati, Lorenzo Reyes, Lorenzo Zanni, Georgios Sarantakos, Dr. Fabrizio Sossan, Asja Derviskadic, Emil Namor, Dr. Daniele Colangelo, David Becerra, Zhaoyang Wang, Asia Codino, Enrica Scolari, Andrea Polini, and Sylvain Robert. Special thanks go to my dear colleague, Andreas Kettner, for helping me to translate the thesis abstract in German.

During my stay in Lausanne, I was fortunate to meet wonderful people with whom I have shared incredible moments. Here, I would like to thank my special friends in Lausanne for their friendship, supports, and kind helps; Elahe, Sina, Majid, Arizu, Ali, Mahdi, Ali, Razieh, Farhang, Leili.

Last but not least, my deepest and forever thanks to my beloved parents for their dedication and many years of support, for their endless love and infinite patience and compassion. I wish to express my heartfelt thanks to my sister, Mahsa for being an important part of my life. This thesis is dedicated to them.

*Lausanne, January 29, 2016*

Reza Razzaghi

# Abstract

The development of modern and future power systems is associated with the definition of new approaches for their simulation, control, and protection. To give an example, the increasing connection of massive renewable energy conversion systems is justifying the integration of DC infrastructures (eventually, multi-terminal HVDC) in the current AC power grids. Furthermore, the existing passive distribution networks are evolving by integration of decentralized and intermittent generation units which results in Active Distribution Networks (ADNs). As a consequence, complex power system topologies are emerging requiring adequate simulation tools capable to reproduce, possibly in real-time, their dynamic behavior. In this context, future operation/protection practices of power networks might rely on the availability of chip-scale real-time simulators (RTS) that will enable the implementation of efficient protection/fault location processes that, in principle, should be capable to comply with the restrictive constraints associated with these complex systems.

Within this context, the work presented in the thesis contributes to the integration of new concepts of the fault location in AC/DC systems that can be deployed in chip-scale real-time simulation hardware represented by Field Programmable Gate Arrays (FPGAs). The development of the proposed fault location platform is done in two steps.

First, an original fault location method based on the Electromagnetic Time Reversal (EMTR) theory is proposed. The proposed method is validated for the case of various power networks topologies and its performance is assessed. Compared to the existing fault location methods, the proposed approach is suitably applicable to different topologies including MTDCs and ADNs.

Next, a new automated FPGA-based solver for RTS is proposed. The developed FPGA-RTS uses a specific automated procedure to couple the simulation platform with an offline simulation environment (EMTR-RV) without the need for Hardware Description Language (HDL). It is able to simulate both power electronics converters and power system grids and thanks to the use of particular parallel computational algorithms, it can accurately simulate, in real-time, Electromagnetic Transient (EMT) phenomena taking place in power converters and travelling wave propagation along multi-conductor transmission lines within very small simulation time steps (in the order of some hundreds of nanoseconds). To overcome the limitations associated with the Fixed Admittance Matrix Nodal Method (FAMNM), a method to assess the optimal value of the parameter of the Associated Discrete Circuit (ADC) switch model used by FAMNM is proposed.

Finally, a specific application of the developed FPGA-RTS is explored for the development of a fault location platform by leveraging the EMTR theory. To this end, the proposed EMTR-based fault location method is integrated with the FPGA-RTS to develop an efficient fault location platform. Thanks to the fast EMT simulation capability of the FPGA-RTS, the developed fault location platform is able to estimate the accurate fault location within very short time scales. Moreover, the developed platform is compatible with the constraints characterizing complex topologies such as MTDC networks (e.g., the ultra-fast operation of the protection systems). The developed fault location platform is validated by making reference to an MTDC grid and an ADN, and it is shown to exhibit remarkable fault location accuracy as well as robustness against uncertainties such as fault type, the presence of noise, measurement systems delay, and fault impedance.

**Keywords-** Power systems protection, Fault location, Electromagnetic time reversal, Electromagnetic transients simulation, Real-time simulation, Field Programmable Gate Array, Fixed Admittance Matrix Nodal Method, Associated Discrete Circuit, Hardware-in-the-loop, Multi-terminal HVDC, Power electronics.



# Résumé

Le développement des systèmes électriques modernes est associé à la définition de nouvelles approches pour leur simulation, leur contrôle et leur protection. L'utilisation croissante des systèmes de conversion d'énergie renouvelable justifie, par exemple, l'intégration des infrastructures en courant continu (et même HVDC multi-terminaux) dans les réseaux électriques AC actuels. En outre, les réseaux de distribution passifs existants sont en train d'évoluer grâce à l'intégration d'unités de production décentralisées et intermittentes et deviennent ainsi des réseaux de distribution actifs (ADNs). Par conséquent, des structures complexes de systèmes électriques émergent, nécessitant des outils de simulation adéquats capables de reproduire leurs comportements dynamiques, de préférence en temps réel. Dans ce contexte, les pratiques futures dans l'exploitation ou la protection des réseaux électriques devraient compter sur la disponibilité de simulateurs en circuit intégré fonctionnant en temps réel (RTS) qui permettront la mise en œuvre de processus efficaces de localisation des défauts et de protection qui, en principe, devraient être capables de respecter les contraintes restrictives associées à ces systèmes complexes.

Dans ce cadre, le travail présenté dans cette thèse contribue à l'intégration de nouveaux concepts de localisation des défauts dans les systèmes AC/DC qui puissent être déployés en temps réel sur du matériel à échelle réduite en utilisant un FPGA (Field Programmable Gate Arrays). Le développement de la plate-forme proposée pour la localisation des défauts se fait en deux étapes.

Tout d'abord, on propose une méthode innovante de localisation des défauts basée sur la théorie du retournement temporel (Electromagnetic Time Reversal - EMTR). La méthode proposée est validée en considérant différentes topologies de réseaux électriques pour lesquelles les performances de cette méthode sont évaluées.

Comparée aux méthodes de localisation de défaut existantes, la méthode proposée est parfaitement applicable aux réseaux en courant continu MTDC et les réseaux de distribution actifs (ADN).

On propose par la suite un nouveau solveur automatisé pour un simulateur en temps réel (RTS) basé sur FPGA. Le simulateur FPGA-RTS développé utilise une procédure automatisée spécifique pour coupler la plate-forme de simulation avec un environnement de simulation hors ligne (EMTR-RV) sans avoir besoin de recourir à un langage de programmation bas-niveau (Hardware Description Language - HDL). Le solveur proposé est capable de simuler aussi bien des convertisseurs de puissance que des réseaux électriques, et grâce à l'utilisation d'algorithmes de calcul parallèles spécifiques il peut simuler avec précision et en temps réel les phénomènes transitoires qui se produisent dans les convertisseurs de puissance, ainsi que les phénomènes de propagation d'ondes dans les lignes de transmission multi-conductrices, le tout en employant des temps de simulation de l'ordre de quelques centaines de nanosecondes.

Pour faire face aux limites associées à la méthode dite de Fixed Admittance Matrix Nodal (FAMNM), on propose une méthode capable d'évaluer la valeur optimale du paramètre du modèle ADC (Associated Discrete Circuit) d'interrupteur utilisé par FAMNM.

Enfin, la méthode basée sur le retournement temporel proposée dans ce travail est intégrée dans le solveur FPGA-RTS afin de développer une plateforme efficace de localisation des défauts. Grâce à la capacité de simulation rapide des transitoires électromagnétiques du FPGA-RTS, la plate-forme de localisation des défauts développée est en mesure d'établir avec précision et dans de très brefs délais le lieu du défaut. En outre, la plateforme développée est compatible avec les contraintes spécifiques liées aux topologies complexes comme celles des réseaux MTDC (par exemple, la contrainte liée au déclenchement rapide des systèmes de protection). La plateforme de localisation des défauts développée est validée en faisant référence à un réseau MTDC et à un réseau de distribution actif. Il a été démontré que la plateforme développée est caractérisée par une remarquable précision dans la localisation des défauts et une robustesse face aux incertitudes liées au type de panne, à la présence du bruit, au retard des systèmes de mesure, et à l'impédance du défaut.

**Mots-clés:** Protection des réseaux haute tension, Localisation des défauts, Retournement temporel, Simulation de transitoires électromagnétiques, Simulation en temps réel, Field Programmable Gate Array, Fixed Admittance Matrix Nodal Method, Associated Discrete Circuit, Hardware-in-the-loop, Multi-terminal HVDC, Électronique de puissance.

# Zusammenfassung

Für die Entwicklung des elektrischen Energiesystems der Zukunft werden neue Ansätze für Simulation, Regelung und Netzschutz benötigt. Das hat verschiedene Gründe. Zum einen ist es durch die Eingliederung erneuerbarer Energiesysteme im grossen Stil sinnvoll, das bestehende Wechselstromnetz mit neuen, auf Gleichstrom basierten Technologien zu ergänzen (zum Beispiel Multi-Terminal HVDC, MTDCs). Zum anderen findet durch das Aufkommen dezentraler Energieerzeugungseinrichtungen ein Wandel von passiven zu aktiven Verteilnetzen (Active Distribution Networks, ADNs) statt. Die sich daraus ergebenden Systemtopologien sind äusserst kompliziert und erfordern geeignete Simulationsmethoden, damit sich das dynamische Verhalten überhaupt in Echtzeit simulieren lässt. In diesem Zusammenhang stellen sogenannte Chip-Scale Echtzeitsimulatoren (Real-Time Simulators, RTS) eine attraktive Lösung dar. Diese ermöglichen nämlich die Verwirklichung effizienter Fehlerlokalisierungsmethoden, welche auch solch anspruchsvollen Anforderungen, wie sie die obig genannten Systeme mit sich bringen, Rechnung tragen können.

Die vorliegende Arbeit einen Beitrag zur Umsetzung neuer Fehlerlokalisierungskonzepte für Wechsel- und Gleichstromsysteme, die sich in Chip-scale Echtzeitsimulationshardware, oder genauer gesagt Field-Programmable Gate Arrays (FPGAs), implementieren lassen. Die Entwicklung der hier vorgestellten Plattform für Fehler-lokalisierung gliedert sich in zwei Schritte.

Zunächst wird eine neue Lokalisierungsmethode, die auf der Electromagnetic Time Reversal Theory (EMTR) basiert, vorgestellt. Deren Wirksamkeit wird anhand verschiedener Arten von Netzwerken untersucht. Im Gegensatz zu existierenden Ansätzen ist dieser neue Ansatz auch für MTDCs und ADNs bestens geeignet.

Des Weiteren wird ein neuer, FPGA basierter Solver für RTS vorgestellt. Der in dieser Arbeit entwickelte FPGA-RTS nutzt ein automatisches Verfahren, um die Simulatorplattform mit einem Offline Simulation Environment (EMTR-RV) zu koppeln, ohne dass dafür eine Hardware Description Language (HDL) notwendig wäre. Dadurch können sowohl leistungselektronische Konverter als auch elektrische Energiesysteme simuliert werden. Die Nutzung bestimmter parallelisierter Algorithmen können sogar elektromagnetische Transiente (EMT), die sich an Konvertern ereignen, sowie Wellenausbreitung entlang Mehrleiterkabeln mit hoher zeitlicher Auflösung (in der Größenordnung von einigen hundert Nanosekunden) in Echtzeit simuliert werden. Um die Einschränkungen, die sich aus der Fixed Admittance Matrix Nodal Method (FAMNM) ergeben, zu überwinden, wurde eine Methode entwickelt, mit der sich die Parameter des Associated Discrete Circuit (ADC) Switch Models der FAMNM optimal berechnen lassen.

Schliesslich wird eine besondere Anwendung des entwickelten FPGA-RTS aufgezeigt, nämlich die Entwicklung einer effizienten Plattform für Fehlerlokalisierung, welche sich die EMTR Theorie zunutze macht. Zu diesem Zweck wird die hier vorgestellte EMTR-basierte Methode in den FPGA-RTS integriert. Dank der hohen Leistungsfähigkeit des FPGA-RTS bezüglich EMT Simulationen, ist es möglich, einen Fehler binnen sehr kurzer Zeit genau zu lokalisieren. Insbesondere eignet sich die Plattform dafür, komplexe Topologien wie MTDC Netzwerke (mit ultra-schnellem Betrieb der Schutzsysteme) abzubilden. Die Validierung orientiert sich an einem an einem MTDC Netz wie auch an einem ADN Netz. Wie dargelegt wird, kann ein Fehler mit hoher Genauigkeit lokalisiert werden, wobei die Methode eine hohe Robustheit gegenüber Unsicherheitsfaktoren wie Fehlertypus, Rauschen, Measurement System Delay und Fault Impedance aufweist.

**Stichworte:** Netzschutz, Fehlerlokalisierung, Electromagnetic time reversal, Simulation elektromagnetischer Transiente, Echtzeitsimulation, Field Programmable Gate Array, Fixed Admittance Matrix Nodal Method, Associated Discrete Circuit, Hardware-in-the-loop, Multi-Terminal Hochspannungsgleichstrom, Leistungselektronik.

# Contents

Acknowledgements.....	v
Abstract (English, /Français/ Deutsch).....	vii
Contents.....	xiii
List of Figures.....	xvii
List of Tables.....	xxiii
List of Acronyms.....	xxv
<b>1 Introduction.....</b>	<b>1</b>
1.1 Motivation of the Thesis .....	1
1.1.1 The Issue of Fault Location.....	2
1.1.2 Need for FPGA-Based RTS for Power Electronics and Power Systems Applications	3
1.2 Objectives and Contributions of the Thesis .....	4
1.2.1 Fault location in Power Networks Based on Electromagnetic Time Reversal (EMTR) Theory .....	4
1.2.2 Automated FPGA-RTS for the EMT Simulations of Power Electronic Devices and Power System Grids.....	5
1.3 Thesis Outline .....	6
<b>2 Fault Location in Power Networks Based on Electromagnetic Time-Reversal..</b>	<b>9</b>
2.1 Introduction.....	10
2.2 Review of the Existing Fault Location Methods for Power Networks .....	12
2.2.1 Phasor-Based Methods.....	12

2.2.2	Travelling Wave-Based Methods .....	13
2.2.3	Knowledge-Based Methods.....	15
2.3	Time Reversal Theory .....	15
2.3.1	Time Reversal Cavity, Time Reversal Mirror .....	15
2.3.2	Electromagnetic Time Reversal (EMTR).....	18
2.4	EMTR Application to the Fault Location Problem .....	20
2.5	Proposed EMTR-Based Fault Location Method .....	22
2.5.1	Frequency-Domain Derivation.....	23
2.5.2	Time-Domain Algorithm.....	28
2.6	The Issue of Losses .....	30
2.6.1	Inverted-Loss Back-Propagation Model.....	31
2.6.2	Lossless Back-Propagation Model .....	31
2.6.3	Lossy Back-Propagation Model .....	32
2.6.4	Comparison of the Back-Propagation Models.....	32
2.7	Experimental Validation.....	36
2.8	Application Examples and Performance Evaluation .....	40
2.8.1	Inhomogeneous Network Composed of Mixed Overhead- Coaxial Cable Lines ...	40
2.8.2	Radial Distribution Network: IEEE 34-Bus Test Distribution Feeder .....	43
2.8.3	Series-Compensated Transmission Line .....	46
2.9	Conclusion.....	50
<b>3</b>	<b>Improved EMT Simulations Based on Fixed Admittance Matrix Nodal Method</b>	
	<b>53</b>	
3.1	Introduction .....	54
3.2	State-of-the-Art of the RTSs for Power Electronics and Power Systems .....	56
3.3	Review of the EMT Simulation Principles.....	61
3.3.1	State-Space Method.....	62
3.3.2	Nodal Analysis .....	62
3.3.3	Numerical Integration Methods.....	63
3.3.4	EMT simulation Models for Network Elements .....	66
3.4	Optimal Assessment of the ADC Switch Model Used by FAMNM.....	74
3.4.1	FAMNM.....	74

3.4.2	Problem Definition.....	74
3.4.3	The Proposed Methodology.....	76
3.4.4	Method Verification towards Error and Losses Functions.....	80
3.4.5	Validation Examples.....	82
3.5	Conclusion.....	92
<b>4</b>	<b>FPGA-RTS for Power Electronics and Power Systems EMT Simulations .....</b>	<b>93</b>
4.1	Introduction.....	94
4.2	Proposed Architecture for the FPGA-RTS.....	95
4.3	Pre-Processing Unit.....	97
4.3.1	Data_ext.....	97
4.3.2	Values_sim.....	98
4.3.3	ANAM.....	99
4.3.4	Opt_Gs.....	101
4.3.5	TL_coeff.....	101
4.4	FPGA-Based Real-Time Solver.....	102
4.4.1	Numerical Representation.....	103
4.4.2	Efficient Matrix-to-Vector Multiplier.....	104
4.4.3	RHS Vector Update.....	108
4.5	Validation Examples.....	112
4.5.1	HIL Validation of a Two-Level Three-Phase Converter.....	112
4.5.2	Fault Originated Transients in Multi-Terminal HVDC Network.....	119
4.5.3	Fault Originated Transients in a Three-Phase AC Network.....	123
4.6	Conclusion.....	125
<b>5</b>	<b>Integration of the EMTR in the Proposed FPGA-RTS for the Development of a Fast and Efficient Fault Location System .....</b>	<b>127</b>
5.1	Introduction.....	128
5.1.1	Fault Location Challenges in HVDC-MTDC Networks.....	128
5.1.2	Fault Location Challenges in ADNs.....	130
5.1.3	The Proposed Approach.....	130
5.2	EMTR-Based Fault Location with Limited Time Reversal Window.....	131
5.2.1	Example of the Application of EMTR-Based Fault Location Method for MTDC Networks with Limited Time Reversal Window and Single Observation Point.....	132

5.3	Integration of the EMTR with the Developed FPGA-RTS .....	135
5.4	Application of the Developed Fault Location Platform for a Meshed MTDC Network 138	
5.4.1	Performance Assessment With Respect to the Fault Location and Fault Type.....	140
5.4.2	Performance Assessment with Respect to Noise.....	142
5.4.3	Performance Assessment of Time-Shifted Time Reversed Windows.....	143
5.4.4	Performance Assessment with Respect to Fault Impedance .....	145
5.5	Application of the Developed Fault Location Platform for a Radial ADN.....	146
5.5.1	Performance Assessment with Respect to the Fault Location and Fault Type.....	148
5.5.2	Performance Assessment with Respect to Noise.....	150
5.5.3	Performance Assessment of Time-Shifted Time Reversed Windows.....	151
5.5.4	Performance Assessment with Respect to Fault Impedance .....	152
5.6	Conclusion.....	153
<b>6</b>	<b>Conclusions.....</b>	<b>155</b>
6.1	Summary and Conclusions.....	155
6.1.1	Fault Location in Power Networks Based on EMTR Theory.....	155
6.1.2	Efficient EMT Simulations Based on FAMNM.....	157
6.1.3	Automated FPGA-RTS for Power Electronics and Power Systems EMTs Simulations.....	157
6.1.4	FPGA-Based Fault Location Platform Based on the EMTR.....	158
6.2	Contributions .....	159
6.3	Future Works.....	159
	<b>Bibliography .....</b>	<b>161</b>
	<b>Curriculum Vitae.....</b>	<b>177</b>



# List of Figures

Figure 2.1. Time reversal cavity illustration (adapted from [46]). (a) Divergent propagation from the source. (b) Convergent back-propagation to the source.....	17
Figure 2.2. The TRM focusing procedure (adapted from [46]). (a) Divergent incident wave from the source. (b) Convergent back-injected waves into the source. ....	18
Figure 2.3. Paths covered by travelling waves caused by a fault at Bus 02. ....	22
Figure 2.4. Simplified representation of the post-fault line configuration for the EMTR analytical validation. ....	23
Figure 2.5. Representation of the EMTR applied to the single-line model. ....	25
Figure 2.6. Normalized FCSE as a function of the GFL $x'_f$ with multiple observation points. The real fault location is at $x'_f=8$ km.....	27
Figure 2.7. Representation of the EMTR applied to the single-line model of Figure 2.4 where a single observation point is placed at the beginning of the line.	27
Figure 2.8. Normalized FCSE as a function of the GFL $x'_f$ with single observation point. The real fault location is at $x'_f=8$ km. ....	28
Figure 2.9. Flow-chart of the proposed EMTR-based fault location method.....	29
Figure 2.10. Equivalent circuit of a single-wire line above a ground plane. ....	31
Figure 2.11. Magnitude of the per-unit-length longitudinal impedance as a function of frequency. The ground conductivity is $\sigma_g = 0.001$ S/m. ....	33
Figure 2.12. Magnitude of the per-unit-length transverse admittance as a function of frequency. Ground conductivity is $\sigma_g = 0.001$ S/m.....	34
Figure 2.13. Phase and group velocities as a function of the frequency. Ground conductivity is $\sigma_g = 0.001$ S/m.....	34
Figure 2.14. Fault current energy normalized to its maximum, for the three back-propagation models. Ground conductivity $\sigma_g = 0.01$ S/m. ....	35

Figure 2.15. Fault current energy normalized to its maximum, for the three back-propagation models. Ground conductivity $\sigma_g = 0.001$ S/m. ....	35
Figure 2.16. Topologies adopted for the reduced-scale experimental setup: (a) a single transmission line configuration (RG-58 coaxial cable), (b) a T-shape network made of both RG-58 and RG-59 coaxial cables.....	36
Figure 2.17. MOSFET-emulated fault adopted in the reduced-scale experimental setup: (a) schematic representation, (b) built PCB board.....	38
Figure 2.18. The experimental setup used for the EMTR-based fault location method validation. ....	38
Figure 2.19. Experimentally measured waveforms for a fault location $x_f = 26$ m for the topology of Figure 2.16-(a); (a) direct-time voltage measured at the observation point located at the beginning of the line. Measured fault currents as a result of the injection of time-reversed signal at guessed fault locations (b) $x_f' = 23$ m, (c) $x_f' = 26$ m (real fault location) and (d) $x_f' = 28$ m.....	39
Figure 2.20. Normalized FCSE as a function of the position of the GFL for the configuration shown in Figure 2.16 (a). The real fault location is at $x_f = 26$ m.....	39
Figure 2.21. Normalized FCSE as a function of the position of the GFL for the topology presented in Figure 2.16-b. The real fault is at $x_f = 34.1$ m in RG-58. ....	40
Figure 2.22. Schematic representation of the inhomogeneous network under study implemented in the EMTP-RV simulation environment.....	41
Figure 2.23. Normalized FCSE as a function of the GFL and for different guessed fault resistance values. The real fault location is at $x_f = 7$ km and real fault impedance is $0 \Omega$ .....	42
Figure 2.24. Normalized FCSE as a function of the GFL and for different guessed fault resistance values. The real fault location is at $x_f = 5$ km and real fault impedance is $100 \Omega$ .....	43
Figure 2.25. IEEE 34-bus distribution system implemented in EMTP-RV. ....	44
Figure 2.26. Normalized FCSE as a function of the GFL and for different guessed fault resistance values: a) three-phase-to-ground solid fault ( $0 \Omega$ ) at Bus 808, b) three-phase-to-ground high-impedance fault ( $100 \Omega$ ) at Bus 812. ....	45
Figure 2.27. Normalized FCSE as a function of the GFL and for different guessed fault resistance values: a) single-phase-to-ground solid fault ( $0 \Omega$ ) at Bus 810, b) single-phase-to-ground high-impedance fault ( $0 \Omega$ ) at Bus 806. ....	46
Figure 2.28. Schematic representation of the series-compensated three-conductor transmission line system implemented in the EMTP-RV. ....	47

Figure 2.29. Normalized energy of the fault current as a function of GFLs and for different guessed fault resistance values (i.e., 1 and 10 Ohms); (a) three-phase-to-ground fault at $x_f = 75$ km, (b) double-phase-to-ground fault at $x_f = 35$ km, (c) single-phase-to-ground fault at $x_f = 25$ km. ....	49
Figure 3.1. Time frame of various transient phenomena (adapted from [74])......	55
Figure 3.2. Schematic representation of HIL test by means of RTDS. ....	56
Figure 3.3. Evolution of Real-Time Simulation Technologies. ....	59
Figure 3.4. Stability region of BE method (adapted from [121]). ....	65
Figure 3.5. Stability region of trapezoidal method (adapted from [121]). ....	66
Figure 3.6. Lumped elements (R, L, C) and relevant companion model. ....	68
Figure 3.7. Single line representation of a single conductor transmission line connecting nodes $k$ and $m$ (adapted from [74]). ....	70
Figure 3.8. Bergeron transmission line model (adapted from [74])......	70
Figure 3.9. ADC switch model (adapted from [130])......	73
Figure 3.10. Schematic representation of the test case composed of a single-conductor transmission line and a switch.....	76
Figure 3.11. Line current at the beginning of the line for four switch representation models (i) ideal switch, (ii) FAMNM for $G_s = 0.1$ , and (iii) FAMNM for $G_s = 1$ , and (iv) FAMNM for $G_s = 10$ . ....	76
Figure 3.12. Definition of Euclidian distance between eigenvalues of the network admittance matrix based on FAMNM and those associated with the admittance matrices of two reference networks. ....	79
Figure 3.13. Schematic of the RLC case study including one switch. ....	83
Figure 3.14. Objective, error, and switch-losses functions for the case of the RLC test case of Figure 3.13.....	83
Figure 3.15. Objective, error, and switch-losses functions for the case of transmission line test case (Figure 3.10) with variable $G_s$ . ....	84
Figure 3.16. Time-domain simulated waveforms for voltage at the end of the transmission line (second test case of Figure 3.10 for different values of $G_s$ . ....	84
Figure 3.17. Schematic of the RLC case study including two switches.....	85
Figure 3.18. Objective function used to assess the optimal $G_s$ values for the case of RLC circuit with two switches shown in Figure 3.17.....	85

Figure 3.19. Time-domain simulated waveforms for switch #2 voltage for the optimal values of $G_{S1}$ , $G_{S2}$ for the circuit composed of RLC elements and two switches.....	86
Figure 3.20. Time-domain waveforms for switch #2 current for the optimal values of $G_{S1}$ , $G_{S2}$ for the circuit composed of RLC elements and two switches.....	86
Figure 3.21. Schematic representation of the test case composed of a single-conductor transmission line and two switches.....	87
Figure 3.22. Objective used to assess the optimal $G_s$ values for the case of a single-conductor transmission line with two switches shown in Figure 3.21. ....	87
Figure 3.23. Error functions used to assess the optimal $G_s$ values for the case of a single-conductor transmission line with two switches shown in Figure 3.21. ....	87
Figure 3.24. Time-domain waveforms for switch #1 voltage for the optimal values of $G_{S1}$ , $G_{S2}$ for the case of a single-conductor transmission line with two switches.....	88
Figure 3.25. Schematic representation of single phase DC/AC converter.....	88
Figure 3.26. Objective function used to assess the optimal $G_s$ values for the case of single phase power converter with four switches shown in Figure 3.25. ....	89
Figure 3.27. Time-domain simulated waveforms for switch #4 voltage for two sets of switches parameters values including the optimal ones optimal. ....	89
Figure 3.28. Time-domain simulated waveforms for switch #4 current for two sets of switches parameters values including the optimal ones optimal. ....	89
Figure 3.29. Schematic representation of the two-level three-phase inverter. ....	90
Figure 3.30. The calculated objective function for the optimal assessment of the switch conductance values of the two-level three-phase inverter. ....	91
Figure 3.31. Time-domain simulated waveforms of the load current for ideal switch representation and FAMNM based optimal $G_s$ and non-optimal one.....	91
Figure 3.32. Time-domain simulated waveforms of the switch#1 voltage for ideal switch representation and FAMNM based optimal $G_s$ and non-optimal one. ....	91
Figure 4.1. Schematic representation of NI CompactRIO platform. ....	95
Figure 4.2. Hardware architecture of developed FPGA RTS based on NI 9033. ....	96
Figure 4.3. The flowchart of the algorithm in Data_ext to read <i>netlist</i> files.....	98
Figure 4.4. Values_sim module input/outputs. ....	99
Figure 4.5. ANAM module inputs/outputs. ....	101

Figure 4.6. Opt_Gs module inputs/outputs. ....	101
Figure 4.7. FP numerical representation. ....	104
Figure 4.8. FXP numerical representation. ....	104
Figure 4.9. RHS computation module for lumped elements. ....	109
Figure 4.10. Structure of the transmission lines circular buffers using FIFOs. ....	111
Figure 4.11. RHS computation for the transmission lines. ....	112
Figure 4.12. Schematic representation of the HIL setup. ....	113
Figure 4.13. Schematic of the considered inverter and MANA variables. ....	113
Figure 4.14. HIL test setup. ....	114
Figure 4.15. Comparison of the FPGA-RTS results with the EMTP-RV ones .....	116
Figure 4.16. Error of the load currents (reference values of Figure 4.15). ....	117
Figure 4.17. The schematic of the HIL validation setup. ....	118
Figure 4.18. Comparison of the FPGA-HIL test results with the measured ones. ....	118
Figure 4.19. Error of the load currents in pu. (reference values of Figure 4.18). ..	118
Figure 4.20. Schematic representation of the MTDC network under study. ....	119
Figure 4.21. Comparison between the simulation results obtained using Thevenin equivalent and VSC models for the positive pole voltage at Station 1. ....	120
Figure 4.22. Error between the simulation results obtained using Thevenin equivalent and VSC models for the positive pole of Station 1. ....	120
Figure 4.23. Comparison between the simulation results obtained using Thevenin and VSC models for the positive pole voltage at Station 1. A first-order high-pass filter is applied for the results obtained by Thevenin equivalent model. ....	121
Figure 4.24. Comparison between the FPGA-based simulations with respect to the EMTP-RV ones: phase-to-ground voltage observed in the positive pole of the station 1 subsequent to a solid p2p fault in the middle of the first transmission line. ....	122
Figure 4.25. Comparison between the FPGA-based simulations with the EMTP-RV ones: phase-to-ground voltage observed in the negative pole of the station 5 subsequent to a solid p2p fault in the middle of the first transmission line. ....	122
Figure 4.26. Norm of the error of the node voltages computed with the FPGA-simulator vs the EMTP-RV ones. ....	122
Figure 4.27. Schematic representation of the considered AC network. ....	123

Figure 4.28. Comparison between the FPGA-based simulations with respect to the EMTP-RV ones: phase-to-ground voltage observed in phase c of substation 1, for a solid three-phase fault in the 30 km of the 4 transmission line. ....	124
Figure 4.29. Norm of the errors of the voltages observed at station 1 .....	124
Figure 5.1. Schematic representation of the MTDC network under study. ....	134
Figure 5.2. Impact of time reversal window length on the accuracy of the proposed EMTR-based fault location method (the real fault location is in line 2 at 20 km). 134	
Figure 5.3. A faulty line in a network in which EMTR-fault location is applied. .	136
Figure 5.4. Structure of the developed fault location platform. ....	138
Figure 5.5. Transient signals in station 5 for positive pole. The green waveform corresponds to time window from the fault occurrence to the breakers openings. 139	
Figure 5.6. Time-reversed voltage signal recorded at station 5 for positive pole..	139
Figure 5.7. Example of FCSE as a function of guessed fault location along the line 3 for different observation point back-injections. The fault is p2p at 20 km. ....	141
Figure 5.8. (a) The time-reversed voltage signal recorded at station 5 for positive pole; (b) the same signal by adding 20 dB noise. ....	142
Figure 5.9. FCSE as a function of GFL for a p2p fault at 60km of line 3. The fault impedance is 100 $\Omega$ . ....	145
Figure 5.10. FCSE as a function of GFL for a p2g fault at 18 km of line 2. The fault impedance is 50 $\Omega$ . ....	145
Figure 5.11. FCSE as a function of GFL for a p2p fault at 9km of line 1. The fault impedance is 50 $\Omega$ . ....	146
Figure 5.12. Radial distribution network composed of 5 transmission lines. ....	146
Figure 5.13. (a) Observed post-fault voltage waveform for phase c for a a-b-g fault at 5km of Line1, (b) 50 Hz component, (c) extracted high frequency transients. .	147
Figure 5.14. FCSE as a function of GFLs along all the lines. The real fault is at 5km of the Line1 and the fault type is a-b-g. ....	148
Figure 5.15. FCSE as a function of GFLs along all the lines. The real fault is at 15km of the Line4 and the fault type is a-g. ....	148
Figure 5.16. FCSE as a function of GFL for a 3ph fault at 25km of line 2. The fault impedance is 100 $\Omega$ . ....	152
Figure 5.17. FCSE as a function of GFL for a ph-ph fault at 10km of line 1. The fault impedance is 100 $\Omega$ . ....	153

# List of Tables

Table 2.1. Parameters of the Line. ....	33
Table 2.2. Location error according to the three Models of Back-Propagation. ....	35
Table 3.1. Companion models parameters associated with RLC elements. ....	68
Table 4.1. CompactRIO-9033 specifications. ....	96
Table 4.2. Decomposed ANAM <sup>-1</sup> . ....	105
Table 4.3. Decomposed RHS. ....	105
Table 4.4. ANAM <sup>-1</sup> mapping based on RHS elements. ....	105
Table 4.5. ANAM <sup>-1</sup> and RHS elements mapping by removing redundant information. ....	106
Table 4.6. ANAM <sup>-1</sup> and RHS elements mapping with respect to the number of iterations in each row. ....	107
Table 4.7. ANAM <sup>-1</sup> and RHS elements mapping for the fixed size iterations by adding zeros. ....	107
Table 4.8. Performance and hardware usage comparison of the sparse and non-sparse matrix to vector multipliers ....	108
Table 4.9. FPGA hardware usage for the HIL test case. ....	116
Table 4.10. FPGA hardware usage for the MTDC network case study. ....	121
Table 4.11. FPGA hardware usage for the three-phase power network case study. ....	123
Table 5.1. Performance assessment of the developed fault location platform by considering different fault types at different locations along the lines. ....	141

Table 5.2. Performance assessment of the developed fault location platform by considering different fault types at different locations along the lines. The time-reversed signals are contaminated with 40 dB SNR noise. ....	143
Table 5.3. Performance assessment of the developed fault location platform by considering different fault types at different locations along the lines. The time-reversed signals are contaminated with 20 dB SNR noise. ....	143
Table 5.4. Performance assessment of the developed fault location platform by considering different fault types at different locations along the lines. The measurement systems time delay to start recording the signals is 1 ms. ....	144
Table 5.5. Performance assessment of the developed fault location platform by considering different fault types at different locations along the lines. The measurement systems time delay to start recording the signals is 2 ms. ....	144
Table 5.6. Performance assessment of the developed fault location platform for the case of ADN by considering different fault types at different locations along the lines. ....	149
Table 5.7. Performance assessment of the developed fault location platform for the case of ADN by considering different fault types at different locations along the lines. The recorded transient signals are contaminated with 40 dB noise. ....	150
Table 5.8. Performance assessment of the developed fault location platform for the case of ADN by considering different fault types at different locations along the lines. The recorded transient signals are contaminated with 20 dB noise. ....	150
Table 5.9. Performance assessment of the developed fault location platform for the case of ADN by considering different fault types at different locations along the lines. The measurement systems time delay to start recording the signals is 1 ms. ....	151
Table 5.10. Performance assessment of the developed fault location platform for the case of ADN by considering different fault types at different locations along the lines. The measurement systems time delay to start recording the signals is 2 ms. ....	152



# List of Acronyms

<b>ADN</b>	<b>Active Distribution Network</b>
<b>ALE</b>	<b>Average Location Error</b>
<b>ANAM</b>	<b>Augmented Nodal Admittance Matrix</b>
<b>ANN</b>	<b>Artificial Neural Network</b>
<b>BAF</b>	<b>Bode's Asymptotic Fitting</b>
<b>BE</b>	<b>Backward Euler</b>
<b>CP</b>	<b>Constant Parameter</b>
<b>CHIL</b>	<b>Controller Hardware-In-the-Loop</b>
<b>CWT</b>	<b>Continuous Wavelet Transform</b>
<b>DFR</b>	<b>Digital Fault Recorder</b>
<b>DG</b>	<b>Distributed Generation</b>
<b>DMA</b>	<b>Direct Access Memory</b>
<b>DSP</b>	<b>Digital Signal Processor</b>
<b>DWT</b>	<b>Discrete Wavelet Transform</b>
<b>EMTP</b>	<b>Electromagnetic Transient Program</b>
<b>EMTR</b>	<b>Electromagnetic Time Reversal</b>
<b>FCSE</b>	<b>Fault Current Signal Energy</b>

<b>FD</b>	<b>F</b> requency <b>D</b> ependent
<b>FE</b>	<b>F</b> orward <b>E</b> uler
<b>FIFO</b>	<b>F</b> irst- <b>I</b> n <b>F</b> irst- <b>O</b> ut
<b>FP</b>	<b>F</b> loating <b>P</b> oint
<b>FXP</b>	<b>F</b> ixed <b>P</b> oint
<b>GFL</b>	<b>G</b> uessed <b>F</b> ault <b>L</b> ocation
<b>GPS</b>	<b>G</b> lobal <b>P</b> ositioning <b>S</b> ystem
<b>GUI</b>	<b>G</b> raphical <b>U</b> ser <b>I</b> nterface
<b>IED</b>	<b>I</b> ntelligent <b>E</b> lectronic <b>D</b> evice
<b>LCC</b>	<b>L</b> ine <b>C</b> ommutated <b>C</b> onverters
<b>LTE</b>	<b>L</b> ocal <b>T</b> runcation <b>E</b> rror
<b>MANA</b>	<b>M</b> odified <b>A</b> ugmented <b>N</b> odal <b>A</b> nalysis
<b>NEMP</b>	<b>N</b> uclear <b>E</b> lectromagnetic <b>P</b> ulse
<b>PCM</b>	<b>P</b> hase- <b>C</b> onjugate <b>M</b> irror
<b>RHS</b>	<b>R</b> ight <b>H</b> and <b>S</b> ide
<b>RTS</b>	<b>R</b> eal- <b>T</b> ime <b>S</b> imulator
<b>SNR</b>	<b>S</b> ignal to <b>N</b> oise <b>R</b> atio
<b>TNA</b>	<b>T</b> ransient <b>N</b> etwork <b>A</b> nalyzer
<b>TR</b>	<b>T</b> ime <b>R</b> eversal
<b>TRM</b>	<b>T</b> ime <b>R</b> eversal <b>M</b> irror
<b>ULM</b>	<b>U</b> niversal <b>L</b> ine <b>M</b> odel
<b>VSC</b>	<b>V</b> oltage <b>S</b> ource <b>C</b> onverter
<b>WT</b>	<b>W</b> avelet <b>T</b> ransform

# 1

## Introduction

### 1.1 Motivation of the Thesis

Fundamental changes are taking place in the monitoring, control and protection of modern power grids where an increasing amount of renewable energy sources are progressively and massively hosted. It is generally acknowledged that such integration of renewables into existing grids depends on the successful combination of specific control processes and availability of new technologies. This last element is motivating the emergence of complex power systems and power electronics architectures in order to interface sources at various voltage levels of DC and AC grids.

In this context, high-performing electromagnetic transient (EMT) simulation tools capable to study, possibly in real-time, the dynamic behavior of these complex systems are needed to study, and develop, new solutions for the monitoring, control and protection of modern power grids.

Real-time simulators (RTSs) are specific simulation platforms able to replicate, in real-time, the exact behavior of the system under study. This peculiarity enables their coupling with real (hardware) controllers and protection systems making possible the fast prototyping of new solutions via hardware-in-the-loop (HIL) analysis.

At the same time, the growing complexity of power converters topologies (e.g., multi-modular converters - MMC) and the need for the definition of their controls, calls for more accurate and faster RTS capable to accurately simulate the switching transients and perform realistic HIL simulations. In this respect, conventional RTSs are characterized by major limitations which bound their application for

particular cases. Therefore, there is the need to develop faster RTS platforms which are able to accurately simulate complex topologies within much lower simulation time steps (i.e., in the range of hundreds of nanoseconds).

At the same time, there is an unexplored field related to the coupling of RTSs with the real-time operation of power grids. One of the typical application examples refers to fault management and, more specifically, to the possibility of merging fault location and relaying functionalities in complex systems (especially multi-terminal DC – MTDC – grids and active distribution networks (ADN)).

### 1.1.1 The Issue of Fault Location

The fault location problem has been extensively studied in the literature for many years and numerous methods have been proposed for both transmission and distribution networks. Nevertheless, despite the vast amount of literature, the problem of fault location still represents a challenge for both transmission and distribution networks. In general, the accuracy of the existing fault location methods are affected by several factors including: pre-fault system condition, load flow, power swing, communication link accuracy (for the case of multi-end methods), fault impedance, and presence of noise. In particular, for the case of MTDC grids and ADNs, the problem is more critical and requires more in-depth studies.

Indeed, the massive integration of new types of generation units (i.e., renewable energy resources) available in remote locations (e.g., offshore wind farms) requires new grid topologies mainly based on the MTDC topology. The protection and fault location in such networks is a challenging task and represents the major obstacle to pervasive deployment of such networks. The transmission lines in MTDC networks are generally long and spread over seas which limits the accessibility of the maintenance team. Furthermore, since the lines in such networks are considered to transfer bulk power over long distances, the loss of a line might cause overloading and congestion in other lines.

Existing methods for point-to-point HVDC links cannot be applied to MTDC networks due to more complex topology and characteristics of these networks. Therefore, more sophisticated fault location techniques are necessary for the case of MTDC network. In this respect, few fault location methods have been proposed in the literature. However, the investigations are in their early stages and more studies are necessary to be carried out.

On the other hand, typical fault location methods based on the estimation of the post-fault impedance, are not applicable in the case of ADNs. With the hypothesis of having a fully passive power system, such estimation could provide useful

information to locate the fault when compared with the line impedance. However, the presence of other sources (e.g. associated with the increasing penetration of dispersed generation (DG)s) can largely affect the accuracy of these procedures. Therefore, travelling wave-based methods (which are not affected by the presence of DGs) might be preferred to locate faults in these networks. Nevertheless, one of the main limitations associated with these methods is that, in general, they require multi-end measurements in order to provide a reasonable accuracy. Therefore, there is an associated need for installing several measurement stations and fast communication links that add a non-negligible amount of complexity and might impair the reliability of the system. On the other hand, the use of a single measurement station might not allow to obtain the required level of accuracy.

### 1.1.2 Need for FPGA-Based RTS for Power Electronics and Power Systems Applications

Existing RTSs are mainly based on digital signal processors (DSP) or general purpose CPU-based platforms where the real-time simulation is achieved by partitioning large networks into smaller sub-systems and processing them in parallel. For these type of RTSs, the minimum achievable real-time simulation time step is in the range of few tens of microseconds. The main reason for this relatively large simulation time step is the partial sequential operations that the CPU architectures need to deploy. The growing complexity of the power systems and power electronic devices and the need for accurate EMT simulations of fast transients, require a higher frequency bandwidth of the real-time simulators. The relatively large simulation time steps required by these simulators do not allow to represent in real-time high frequency phenomena such as EMTs in power converters or travelling wave transients taking place in transmission lines (e.g., fault and switching transients).

FPGA is a suitable alternative to be used as a real-time simulator computational core. The main advantage of FPGA over CPU or DSP is its hardwired parallel processing that enables the implementation of specific methodologies that dramatically reduce the sequencing of the operations taking place in CPUs or DSPs. Furthermore, In FPGAs the latency associated with the import/export of the I/Os are lower compared to the CPUs. Finally, FPGAs are fully configurable chips, which allow to be configured for specific applications.

The existing FPGA-based RTSs are mainly dedicated to the power electronics applications and their HIL tests where the switches are represented by means of associated discrete circuit (ADC) model in which the switch is represented by a constant conductance in parallel with a controlled current source. This specific switch model enables adapting the so-called fixed admittance matrix nodal method (FAMNM), which is widely used in the proposed FPGA-RTSs in the literature. This

method, irrespective of the number of the switches and their states, allows obtaining a fixed nodal admittance matrix during switching transitions. Therefore, it results in accelerating the EMT simulation of switching devices and performing the real-time simulation of these circuits within very small simulation time steps in the order of hundreds of nanoseconds. However, this simple model introduces artificial oscillations and non-negligible errors in the simulation results. In particular, the considered value for the conductance can dramatically impact the simulation results accuracy and it is essential to calculate the optimal conductance value to minimize the relevant simulation errors. Nevertheless, the existing FPGA-RTSs adopting this switch model do not consider this impact and, in general, the quantitative error assessments are not provided.

Another important drawback of FPGA-RTSs is their difficult programming associated with the use of hardware description languages (HDL). This low level programming, limits the scalability of the solvers and, as a consequence, the representation of complex circuits. Additionally, any modification in the implemented algorithm/model requires, in general, a time-consuming recompilation of the HDL code. A few automated FPGA-based RTSs have been proposed to avoid the difficulties of the FPGAs programming. However, the applications of these simulators are mainly dedicated to power electronics HIL simulations. Therefore, these studies have not accounted for the possibility to simulate power networks including propagative transmission lines.

## 1.2 Objectives and Contributions of the Thesis

The aim of this thesis is to address the above-mentioned challenges regarding the problems of fault location in power networks and FPGA-based real-time simulators for power electronic and power grids. In this thesis, a new automated general purpose FPGA-based RTS is developed that solves the problem of switch models and variable grid topologies. Furthermore, a specific application of this FPGA-based RTS is explored in order to merge relaying and fault location functionalities by leveraging the electromagnetic time reversal (EMTR) theory. In what follows, the main contributions of the thesis are summarized by making reference to the two steps accomplished to develop the fault location platform.

### 1.2.1 Fault location in Power Networks Based on Electromagnetic Time Reversal (EMTR) Theory

An original fault location technique based on the EMTR theory is presented. The proposed method takes advantage of the time reversal invariance of the telegraphers' equations describing the wave propagation in transmission lines. The approach is successfully applied to different types of transmission and distribution

networks and is able to overcome several limitations associated to existing fault location methods. More specifically, the proposed method can be used in the case of inhomogeneous networks composed of different transmission lines with different characteristic impedances and propagation constants (for example, networks comprising overhead lines and underground cables). A further advantage of the developed EMTR-based fault location method is that it minimizes the number of observation points required to perform the measurement of the transient signals. In particular, it is shown that a single observation point located at the secondary winding of a substation transformer is enough to correctly identify the fault location, even for complex topologies. In addition, the performance of the method is very robust to the topology of the system, fault type and impedance, presence of series compensation, presence of noise, and delay of the measurement systems.

### **1.2.2 Automated FPGA-RTS for the EMT Simulations of Power Electronic Devices and Power System Grids**

In order to develop an automated FPGA-RTS dedicated to high-performance EMT simulations, the thesis proposes an efficient method for an accurate simulation of switching devices. In particular, by considering the drawback of the classical ADC switch model, a novel method for the optimal assessment of the parameters of the ADC model is presented. The proposed method is based on the minimization of the Euclidian distance between the eigenvalues of the network admittance matrix based on FAMNM, and those associated with the admittance matrices of reference networks corresponding to all possible switching permutations. To prove the correctness of the proposed method, a comparison between the proposed metric and specifically defined error functions is presented and discussed. Several validation examples are considered to prove the performance of the proposed method.

Then, an automated FPGA-based real-time EMT simulator is proposed which integrates the developed model for switching devices. An automated procedure is used to overcome the limitations of current FPGA-RTSs.

The proposed RTS is implemented into an industrial real-time embedded system (the National Instruments CompactRio real-time platform) and has the following features: (i) it makes use of the modified augmented nodal analysis (MANA) method, (ii) it integrates the FAMNM together with the optimal selection of the switch conductance parameter, (iii) it enables the possibility of accurately reproducing electromagnetic switching transients taking place in power electronic switching devices together with electromagnetic wave propagation in transmission lines, and (iv) it enables to reach extremely low integration time steps and provides an automated procedure to directly translate the schematic representation of the electrical circuits designed in the EMTP-RV simulation environment to the relevant FPGA solver by avoiding the need of HDL programming languages. Such

peculiarity enables a straightforward applicability of the proposed FPGA-based RTS to various power electronics and power systems applications.

The performance of the developed FPGA-RTS is assessed by considering three validation examples. They refer to (i) a two-level three-phase inverter, (ii) a multi-terminal HVDC network, and (iii) a three-phase AC network. The comparison of the obtained results with offline benchmark simulations and HIL results showed an excellent agreement together with a high computation efficiency.

## 1.3 Thesis Outline

The structure of the thesis dissertation is as follows.

**Chapter 2** presents first an overview of the existing fault location methods by classifying them into three general categories and by highlighting their advantages and disadvantages. Then, a novel and efficient fault location method based on the EMTR theory is presented. The proposed EMTR-based fault location method is validated using an experimental setup and several validation examples by making reference to different types of power networks.

**Chapter 3** presents a brief history of the development of RTSs for EMT applications. In particular, the need for a new type of RTS based on FPGA is highlighted and a summary of existing FPGA-RTS is presented. Also in this chapter, the effect of the ADC switch model parameter, used in the FAMNM, on the accuracy of the simulation results is discussed. Then, a novel method for the optimal assessment of this parameter is presented. To prove the correctness of the proposed method, a comparison between the proposed metric and specific defined error functions is presented and discussed. Several validation examples are considered to prove the performance of the proposed method.

**Chapter 4** presents a new automated FPGA-RTS dedicated to EMT simulations of power electronic devices and power systems. The proposed method for the optimal assessment of the ADC switch model, presented in Chapter 3, is coupled with the developed FPGA-RTS to provide very accurate simulation results. The FPGA solver is implemented using parallel algorithms applied to efficiently handle sparse matrix multiplications. Three validation examples are provided to test the performance of the proposed FPGA-RTS including a two-level three-phase converter, and two power networks composed of propagative transmission lines.

**Chapter 5** presents an original fault location platform applied to MTDC grids and ADNs. The proposed platform is developed by merging the proposed EMTR-based fault location method, presented in Chapter 2, and the developed FPGA-RTS, presented in Chapter 4. The fast EMT simulation capability of the developed



FPGA-RTS is exploited to perform the fault location process within short time periods. The possibility of applying the EMTR-fault location process using a limited time reversal window is also explored. Then, by taking advantage of this peculiarity, the chapter illustrates the architecture of the developed fault location platform. Its performance is validated by making reference to an MTDC grid and an ADN and, by considering numerous simulated fault cases. In particular, its robustness is assessed considering different fault locations and types, presence of noise in the transient signals, measurement systems time delay, and fault impedance.

**Chapter 6** summarizes the main contributions of this research and provides an outlook on the potential future works.



# Fault Location in Power Networks Based on Electromagnetic Time-Reversal

## Summary

In this chapter, a review of existing fault location methods is presented by classifying them into three general categories and by highlighting the advantages and disadvantages associated with the methods of each category.

Time reversal (TR) process is presented as a focusing procedure by demonstrating the time reversal cavity and time reversal mirror (TRM) concepts. Then, the theory of electromagnetic time reversal (EMTR), the extension of the TR process to the electromagnetic waves, is explained.

The proposed fault location method based on the EMTR theory is explained. The analytical derivation as well as the proposed time domain algorithm are presented. The impact of the losses is carefully studied by discussing different back-propagation models.

The proposed EMTR-based fault location method is validated first using an experimental setup in which the fault location is assessed in a real network formed by coaxial cables. Then, several validation examples are performed by making reference to different types of power networks including (i) inhomogeneous network composed of mixed overhead- coaxial cable lines, (ii) radial distribution network, (iii) series-compensated transmission lines. The resulting fault location accuracy and robustness against uncertainties (e.g., fault impedance, fault type, network topology) are tested and, in this respect, the proposed method appears to be very promising for real applications.

### 2.1 Introduction

Existing power systems are evolving and becoming more complex by enormous increase of the generation units, which require new transmission and distribution lines and which should satisfy customers' need in terms of power quality and reliability. However, transmission and distribution networks are always prone to short-circuit faults due to natural events such as falling trees, wind, lightning, ice storm or mechanical failure of insulators or other equipment [1].

In transmission networks, fault location functionality is needed for the identification of the faulty line and the adequate reconfiguration of the network to prevent severe cascading consequences. In distribution networks, fault location is more associated with the quality of service in terms of duration of interruptions when permanent faults occur. Still with reference to distribution networks, the increasing use of distributed generators (DG) calls for accurate and fast fault location procedures aimed at minimizing the network service restoration time, and, consequently, minimizing the unsupplied power.

To comply with the restrictive requirements of modern power systems and to ensure the reliability of the power supply, power systems are equipped with accurate and fast protection and control systems exploiting several fundamental functionalities, including fault location. As in most cases the failure of the power transfer is due to mechanical damages, the first step to repair the damage and recover the network is to identify the fault location. Fast and accurate fault location procedures result in faster repair and recovery of the power supply. Therefore, the fault location function can be implemented into [1]: (i) protection relays, (ii) digital fault recorders (DFR), (iii) stand-alone fault locator, or (iv) offline post-fault analysis program.

It is worth observing that, in general, the time constraint for fault location systems is longer than the one for protection systems as precise fault location requires, in general, complex processing which might take more time compared to the protection. Greater precision allows, in fact, shortening the time of intervention of the maintenance teams. As an example, in the Dutch networks, approximately 70% of all interruptions are originated on medium voltage networks and the recovery time, allowing the location of the fault and action on the devices of maneuver, is on average 90 minutes [2].

The fault location problem has been extensively studied in the literature for many years and numerous methods have been proposed. First, the subject was studied for transmission networks due to the impact of this function on power systems operation and difficulty of locating faults in meshed networks. Then, studies were extended to distribution networks as the power quality started to attract more

attention. Despite the vast amount of literature on fault location methods, the problem of fault location still presents essential challenges for both transmission and distribution networks:

**Transmission networks:** the rapid growth in size and complexity of the transmission systems, the emergence of the new measurement systems, and recent advances in telecommunication technologies, have made possible the definition of new types of fault location methods. Typical examples refer to: wide area monitoring and synchronized measurements, advanced measurement systems dedicated to the acquisition of high-frequency travelling wave signals, and fast and powerful processing hardware available in intelligent electronic devices (IED).

**Distribution systems:** the precise fault location problem is even more challenging due to following reasons (e.g., [1], [3]):

- Distribution lines are often characterized by the presence of DGs which can largely affect the accuracy of fault location procedures developed for the passive distribution networks;
- Lines are often characterized by a significant dissymmetry between the phases;
- The effect of the fault impedance on the fault location accuracy can be significant;
- The load conditions of the phases can be unbalanced and the load current, which is superimposed to the fault current, changes during the fault;
- The measurement errors associated with the measurement transformers can be important in the case of very small values of the voltage during the fault (i.e., high levels of short-circuit currents are experienced).

Therefore, the fault location problem is still an important ongoing topic of research.

This chapter is organized as follows. In Section 2.2, a review of the existing fault location methods for the transmission and distribution networks are presented. Section 2.3 presents the theory of time-reversal with special attention to the EMTR theory. The application of EMTR to fault location is presented in Section 2.5. The issue of losses is discussed in Section 2.6, followed by the experimental validation of the proposed fault location method described in Section 2.7. Section 2.8 presents several application examples to distribution and transmission networks. Finally, conclusions are presented in Section 2.9.

## 2.2 Review of the Existing Fault Location Methods for Power Networks

The fault location problem in transmission lines has been a topic of investigation since 1950s [4] and numerous fault location methods have been proposed in the literature. The various proposed fault location procedures can be classified into three main categories [1], [3]:

1. Methods that analyze pre-fault and post-fault voltage/current phasors (phasor-based methods);
2. Methods that analyze fault-originated electromagnetic transients of currents and/or voltages, (travelling wave-based methods);
3. Knowledge-based approaches (artificial intelligence methods).

### 2.2.1 Phasor-Based Methods

Using the voltage/current phasors at the line terminals is the most straightforward approach to calculate fault location. These methods rely on the calculated impedance of the faulty line to identify the fault location. According to the availability of utilized measurements, the methods belonging to these category can be further classified into the following sub-categories: (i) single-end (one-terminal) measurement methods (e.g., [5], [6], [7], [8]), (ii) double-end (two-terminal) measurement methods (e.g., [9], [10], [11], [12], [13]), and (iii) multi-end algorithms (e.g., [14], [15], [16], [17], [18]) that employ measurements from multiple ends of multi-terminal transmission lines. Double-end and multi-end measurement-based fault location methods can be based on either unsynchronized (e.g., [11], [19], [20]) or synchronized (e.g., [9], [17]) voltage/current measurements.

Single-end measurement based fault location methods estimate the fault distance by using voltage and current measurements at a particular end of the line. These approaches are simpler compared to the two-terminal or multi-terminal measurement-based ones since they do not require communication means. Therefore, they are more attractive for practical applications. However, the solution of the fault location problem requires several assumptions and simplifications ([5], [6]) which impact the fault location accuracy [7]. The accuracy of these methods depends on the fault resistance, load, configuration of the line, and load flow unbalance.

On the other hand, the methods based on double/multiple-end measurements provide more accurate and robust fault location results compared to the single-end methods. These methods rely on communication links to exchange the data

between multiple ends. The availability of multiple data enables to eliminate the effect of the fault resistance and other affecting parameters, and therefore to minimize the fault location estimation error. However, the performance of these methods is mainly dependent on efficient communication links which add non-negligible complexity to the system. Multi-end fault location methods require global positioning system (GPS) to provide a common time reference. Their performance can be affected by the accuracy and the loss of the GPS signal [13].

Despite the straightforward solutions provided by the impedance-based fault location methods, their accuracy might be affected by the fault resistance, configuration of the line, load flow unbalance, and the presence of DGs [3]. The latter becomes more important for the case of active distribution networks (ADNs) where DGs are connected to the distribution system feeders that can largely affect the accuracy of these procedures. Moreover, these methods are not applicable to HVDC transmission systems, which are one of the essential elements of modern power systems.

### 2.2.2 Travelling Wave-Based Methods

Travelling wave-based methods consider the voltage (and/or current) waves which are travelling at the line propagation speed from the fault location towards the line terminals. Compared to phasor-based fault location methods, travelling wave-based methods are considered to be more precise and offer some advantages. On the other hand, in general, they require complex signal processing techniques [1]. To overcome the limitations associated with the phasor-based fault location methods, travelling wave-based methods have been increasingly investigated in the literature (e.g., [21], [22], [23], [24], [25], [26]). These methods rely on the analysis of the high-frequency components of the fault-originated transient signals which are rather uninfluenced by the fault impedance [27]. In particular, these methods are considered as the best way to identify fault location in DC transmission systems (e.g., [28]).

Travelling wave-based fault location methods analyze different a feature of the travelling waves and utilize various techniques to identify the fault location. One of the first adopted techniques is based on the cross-correlation between the forward and backward travelling waves [22]. The main drawback of such method is the discrimination of the travelling waves originated from the fault point from those reflected at remote ends of the line [29]. Moreover, the accuracy of this method is mainly dependent on the sampling window [29]. The improved correlation-based method is proposed in [29] which uses combined short and long window lengths. The arrival time-based methods identify the fault location by assessing the arrival time of the travelling waves at one (single-end) or different terminals of the line (multi-end) [30].

In single-end methods, the arrival times of the initial and reflected travelling waves at one single terminal of the line are used. The fault location is identified by assessing the time delay between successive reflections of the measured travelling wave signals at one terminal (e.g., [30], [31]). These methods avoid the cost and complexities associated with multi-end measurement synchronization and communication links. However, these methods are known to be more complex and less accurate compared to multi-end ones. Indeed, the main difficulty related to single-end methods is the detection and discrimination of the fault-originated waves from the reflections associated with other terminals [30]. Moreover, these methods commonly have problems of locating close-by faults [32].

Multi-end methods, which rely on multiple measurement locations, are more straightforward and precise compared to single-end methods. For the case of a single line, if the two-terminal measurements are synchronized, the difference between the arrival times of the travelling waves at the two terminals can be used to identify the fault location. To this end, precise GPS signal is required to synchronize the measurements at two terminals and the wave velocity should be known [3], [33]. Nevertheless, despite several advantages provided by two-end synchronized fault location methods (e.g., insusceptibility to the variations of source impedances, fault distances, and fault impedances), practically speaking, their application are limited due to the synchronization problems and lack of common time reference in all substations [34]. To cope with this issue, unsynchronized measurements methods for the fault location problem have been proposed (e.g., [32], [34]).

Wavelet analysis is a powerful signal processing tool which is able to analyze the signal in both time and frequency domain. A particular feature of the wavelet transformation (WT) is the automatic altering of the data window according to the frequency. This peculiarity is suitable for rapid alternations in the analyzed transient signal. WT has been successfully applied to overcome the shortcomings associated with the travelling-wave based methods (e.g., [25], [27], [35]). First, discrete-wavelet transform (DWT) was used to identify the fault location due to its straightforward implementation and the reduced computation time [36]. However, compared to DWT, the continuous-wavelet transform (CWT) provides more detailed and continuous analysis of the signal. This is the result of smooth shifting of the analyzed wavelet over the full domain of the signal compared to the dyadic shift in DWT [37]. Therefore, CWT-based fault location methods provide more precise results (e.g., [27], [35], [36]). The limitation associated with these methods is related to the use of traditional mother wavelets, which does not allow identifying all the characteristic frequencies of the travelling waves. In [27], a method has been proposed to overcome this problem by building specific mother wavelets inferred from the fault-originated transient waveforms. Nevertheless, the



application of WT-based fault location methods requires considerable amount of computational efforts.

Despite the more precise fault location accuracy of the travelling wave-based methods compared to phasor-based methods, their accuracy might still be affected by the following factors [3]:

- Requirement of a detailed network model and lines characteristics.
- Assessment of the number of observation points versus the number of possible multiple fault location solutions.
- Requirement of a precise time stamping for methods requiring multiple synchronized metering stations.
- Loss of GPS signal impacting the fault location accuracy.
- Requirement of large bandwidth measurement systems.

### 2.2.3 Knowledge-Based Methods

In addition to the previous approaches, several research efforts have been performed on the use of knowledge-based fault location methods. Expert systems identify the most probable fault location by means of available information regarding the network status (e.g., the state of switches, unpowered user complaints, etc.) (e.g., [38], [39]). artificial neural networks (ANN) and fuzzy logic have been widely studied for the fault location problem. (e.g., [40], [41]). Nevertheless, the extensive training of such methods limits their application to real systems.

## 2.3 Time Reversal Theory

### 2.3.1 Time Reversal Cavity, Time Reversal Mirror

The term of time reversal (TR) was first introduced in the literature by B. Bogert of Bell Labs in 1957 who introduced the TR as a technique to compensate the delay distortion of slow pictures and television signals in wired lines [42]. In his experiments, he observed that the picture quality is enhanced by applying the TR procedure, in particular when the transmission characteristic of the system is uniform. A similar approach was used in [43] as an automatic distortion correction for efficient pulse transmission in telephone networks. Later, in [44], the same idea was used to develop zero-phase digital filters. Although these studies had shown several interesting features of the TR technique, they mainly used the TR as a signal processing algorithm.

Later, Mathias Fink et al. presented the TR concept as a new approach for focusing ultrasonic waves [45], [46], [47], [48]. The basic principles of the TR applied to ultrasonic fields were presented in [45], [46], as a technique to focus a wave on a target through an inhomogeneous medium. In [45], the concept of optical phase-conjugate mirrors (PCM) was extended for ultrasonic waves. In optics, PCM, which is used for monochromatic fields, is an efficient technique to compensate the phase distortion which is the consequence of the aberrations of an optical system or inhomogeneities of the refractive index in the transmitting medium. PCM reverses the phase of an incident monochromatic distorted wave. The generated wave will back-propagate in the medium without distortion [45]. The limitation associated with PCM is that it works with monochromatic fields. Therefore, it cannot be applied for ultrasonic waves which are broadband. TR process is a generalization of the PCM which is also able to be applied to broadband signals. In contrast to PCM that works in a continuous mode, TR allows the choice of any temporal time window to be time reversed [45], [46].

For the TR process to be applicable, the main criterion is that the wave equation has to be time reversal invariant. As an example, consider the propagation equation of an acoustic pressure in a lossless fluid medium [46]:

$$\vec{\nabla} \cdot \left( \frac{\vec{\nabla} p}{\rho} \right) - \frac{1}{\rho c^2} \frac{\partial^2 p}{\partial t^2} = 0 \quad (2.1)$$

One can note that since there is only a second order time derivative, the pressure propagation equation is symmetrical over the time operator and as a consequence, if  $p(r, t)$  is a pressure field solution of this equation, then  $p(r, -t)$  is also a solution. Therefore, the propagation equation is time reversal invariant [46]. Since  $p(r, -t)$  is not an experimentally valid solution, in order to ensure the causality requirements, the time-reversed signal is shifted in time as  $p(r, T-t)$  where  $T$  is the period in which  $p(r, t)$  is recorded. It is worth noting that, the TR operator  $t \rightarrow -t$  is equivalent to the phase conjugation in the frequency domain. In general, TR operation can also be applied in the frequency domain using the following equivalence [45]:

$$p(r, -t) \leftrightarrow F^*(r, \omega) \quad (2.2)$$

where  $F(\vec{r}, \omega)$  is the Fourier transform of  $p(r, t)$  and the subscript  $*$  denotes the complex conjugate. In principle, in order to effectively focus the back-injected waves to the source, the process should be performed in the whole space (3D). However, this is an unrealistic solution. Considering the fact that wave at any point of a medium can be calculated by the knowledge of the field and its normal derivative on a closed surrounding surface, this problem can be reduced to a 2D

surface [46]. Therefore, the TR process can be simplified by considering the time reversal cavity where the source is surrounded by a closed surface and the pressure field and its normal derivative is measured at any point of the closed surface [46]. The focusing procedure in a time reversal cavity is shown in Figure 2.1. The procedure consists of two stages: (a) the distorted pressure field is recorded by the transducers which cover completely the cavity surface; (b) the recorded signals are time-reversed and re-injected back into the medium from the cavity transducers. The back-injected field refocuses again in the initial source point.

Despite the refocusing capability of the time-reversal cavity, its realization is difficult since, in practice, it is not feasible to surround the medium by the transducers. In fact, the process can be physically done by using a limited number of transducers, which do not necessarily enclose the source point. Nonetheless, using a proper spatial distribution of the transducers allows to capture enough samples along the wavefront and enables to focus through an inhomogeneous medium [46], [48]. This is the idea of the time reversal mirror (TRM).

A TRM consists of a 1D or 2D reversible transducer arrays, which are able to record the incident fields originated by a distant source. The transducer's response to the local field is linear. The recorded fields of the transducers are reversed in time and then reemitted by the same transducers. Such procedure allows to convert divergent incident waves originated from a distant source, which are distorted in an inhomogeneous medium, into a convergent reflected wave, focusing again on the source [45], [46]. Figure 2.2 shows the TRM focusing procedure. The interesting peculiarity of the TRM is that it works even if there is an inhomogeneous medium between the target and the mirror.

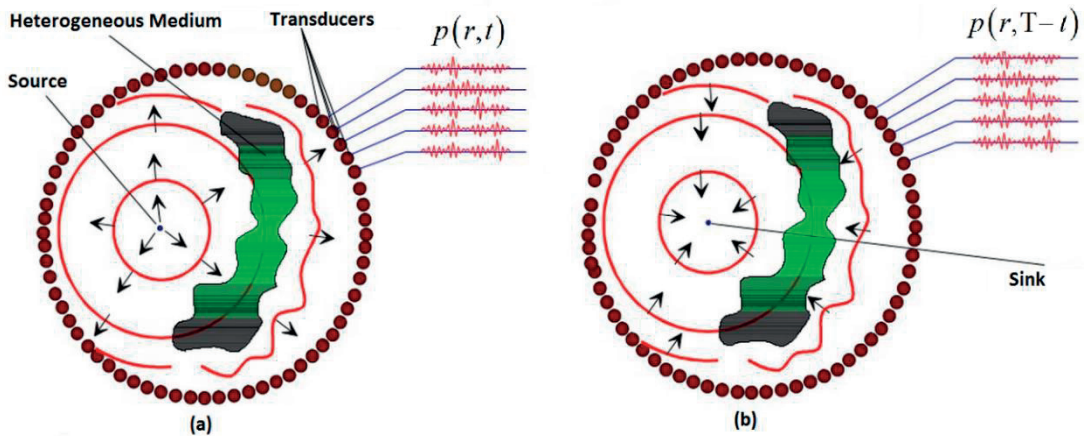
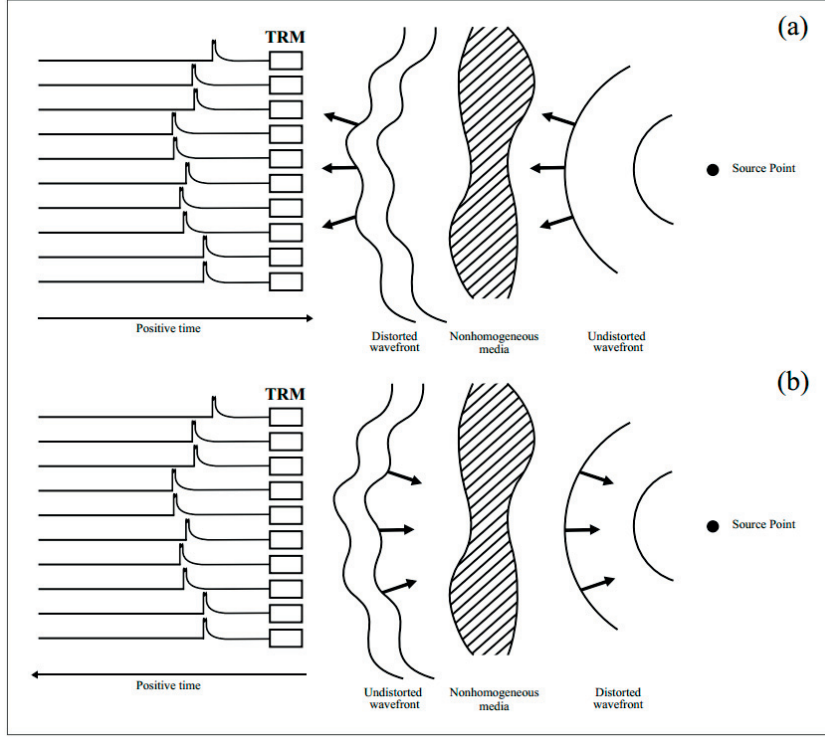


Figure 2.1. Time reversal cavity illustration (adapted from [46]). (a) Divergent propagation from the source. (b) Convergent back-propagation to the source.



**Figure 2.2.** The TRM focusing procedure (adapted from [46]). (a) Divergent incident wave from the source. (b) Convergent back-injected waves into the source.

As it is illustrated in Figure 2.2, the TRM procedure consists of two main steps [46]: (a) a diverging waves originated by a source and distorted in the inhomogeneous medium are captured by the transducer array elements. (b) The captured signals are time-reversed and back-propagated through the same medium. The back-propagated waves are refocused at the source point.

### 2.3.2 Electromagnetic Time Reversal (EMTR)

Twelve years after the development of the concept of TRM, its application was successfully extended to electromagnetic waves [49], [50], [51]. In [49], G. Lerosey et al. presented the first single-channel TR experiment for electromagnetic waves in GHz domain for the temporal and spatial focusing.

Similar to the acoustic waves, in order to apply EMTR, the electromagnetic wave has to be time reversal invariant. Let us consider Maxwell's equations in vacuum [52]:

$$\nabla \cdot (\varepsilon(\vec{r}) \vec{E}(\vec{r}, t)) = \rho(\vec{r}, t) \quad (2.3)$$

$$\nabla \cdot (\mu(\vec{r}) \vec{H}(\vec{r}, t)) = 0 \quad (2.4)$$

$$\nabla \times \vec{E}(\vec{r}, t) = -\mu(\vec{r}) \frac{\partial \vec{H}(\vec{r}, t)}{\partial t} \quad (2.5)$$

$$\nabla \times \vec{H}(\vec{r}, t) = \varepsilon(\vec{r}) \frac{\partial \vec{E}(\vec{r}, t)}{\partial t} + \vec{J}(\vec{r}, t) \quad (2.6)$$

where  $\vec{E}(\vec{r}, t)$  and  $\vec{H}(\vec{r}, t)$  are, respectively, the electric and the magnetic field,  $\rho(\vec{r}, t)$  is the charge density,  $\vec{J}(\vec{r}, t)$  is the electric current density.  $\varepsilon(\vec{r})$  and  $\mu(\vec{r})$  are, respectively, the electric permittivity and the magnetic permeability. Mathematically, TR implies making the substitution  $t \rightarrow -t$ .

In order to study the TR invariance of the Maxwell's equations, the electric and magnetic fields as well as the charge and current densities has to be analyzed under the TR operation. As known, electric charge density does not change under TR operation. However, the TR operator changes the sign of charges velocity. As a result, the associated current density should change sign as well [53]. Therefore, the sign of the electric field  $\vec{E}(\vec{r}, t)$  remains unchanged under TR operator, while the magnetic field  $\vec{H}(\vec{r}, t)$  sees a change of sign as a result of the change of sign of the current density [53], [54]. Summing up, we have:

$$\rho(\vec{r}, t) \xrightarrow{TR} \rho(\vec{r}, -t), \quad \vec{E}(\vec{r}, t) \xrightarrow{TR} \vec{E}(\vec{r}, -t) \quad (2.7)$$

$$\vec{J}(\vec{r}, t) \xrightarrow{TR} -\vec{J}(\vec{r}, -t), \quad \vec{H}(\vec{r}, t) \xrightarrow{TR} -\vec{H}(\vec{r}, -t) \quad (2.8).$$

Considering equations (2.7) and (2.8), the Maxwell's equation under TR operator results in:

$$\nabla \cdot (\varepsilon(\vec{r}) \vec{E}(\vec{r}, -t)) = \rho(\vec{r}, -t) \quad (2.9)$$

$$\nabla \cdot (\mu(\vec{r}) (-\vec{H}(\vec{r}, -t))) = 0 \quad (2.10)$$

$$\nabla \times \vec{E}(\vec{r}, -t) = -\mu(\vec{r}) \frac{\partial (-\vec{H}(\vec{r}, -t))}{\partial (-t)} \quad (2.11)$$

$$\nabla \times (-\vec{H}(\vec{r}, -t)) = \varepsilon(\vec{r}) \frac{\partial \vec{E}(\vec{r}, -t)}{\partial (-t)} + (-\vec{J}(\vec{r}, -t)) \quad (2.12).$$

The situation here is different from the acoustic wave equation where there is a second-order time derivative. The equations (2.9)-(2.12) are identical to one of (2.3)-(2.6). Therefore, one can conclude that Maxwell's equations are TR invariant [53], [54]. It is worth observing that, the electromagnetic propagation in a dissipative

medium is not TR invariant unless an inverted-loss medium is considered for the reversed time [54]. To see this, consider Ohm's law:

$$\vec{J}(\vec{r}, t) = \sigma(\vec{r})\vec{E}(\vec{r}, t) \quad (2.13)$$

where  $\sigma(\vec{r})$  is the conductivity of the medium. Applying the TR operator results in [55]:

$$-\vec{J}(\vec{r}, -t) \neq \sigma(\vec{r})\vec{E}(\vec{r}, -t) \quad (2.14).$$

In order to hold TR invariance for the Ohm's law, the sign of the conductivity would need to be changed (i.e.,  $\sigma(\vec{r}) \xrightarrow{TR} -\sigma(\vec{r})$ ).

EMTR has received large attention for several interesting applications including: focusing of electromagnetic waves and applications in biomedical engineering (e.g., [56]), target imaging in a cluttered environment (e.g., [50]), landmine detection (e.g., [57]), communications and radar (e.g., [51]), and more recently, lightning location (e.g., [55], [58]). The latter applies EMTR-based procedure to identify the lightning strike location by using a simulation program which time reverses the recorded waveforms (originated by the strike) and re-injects them back by simulation into the location network domain.

The aim of this research is to study the possibility of applying EMTR to the problem of fault location in power networks in which the wave propagation is formulated using the telegraphers' equations for multi-conductor transmission lines. Compared to other applications of the EMTR, its application for the fault location in transmission lines is more straightforward since the electromagnetic waves are confined in a 1D medium.

## 2.4 EMTR Application to the Fault Location Problem

The limitations associated with the existing travelling wave-based fault location methods (e.g., requirement of time-synchronized, multi-end measurement stations and complexity due to the sophisticated signal processing techniques) is the motivation to study more efficient fault location techniques. As the TR has been shown to be effective in focusing electromagnetic waves, it might also be an efficient method for locating faults in power networks.

First, we need to examine the properties of the transmission line wave equations under the TR operator. The voltage wave equation for a multiconductor, lossless transmission line reads [59], [60]:

$$\frac{\partial^2}{\partial x^2} \mathbf{U}(x,t) - \mathbf{L}'\mathbf{C}' \frac{\partial^2}{\partial t^2} \mathbf{U}(x,t) = 0 \quad (2.15)$$

where  $\mathbf{U}(x,t)$  is a vector containing the phase voltages at position  $x$  and time  $t$ ,  $\mathbf{L}'$  and  $\mathbf{C}'$  are the per-unit-length matrices of inductance and capacitance of the line, respectively. Time reversing (2.15) yields:

$$\frac{\partial^2}{\partial x^2} \mathbf{U}(x,-t) - \mathbf{L}'\mathbf{C}' \frac{\partial^2}{\partial t^2} \mathbf{U}(x,-t) = 0 \quad (2.16).$$

Therefore, if  $\mathbf{U}(x,t)$  is a solution of the wave equation, then  $\mathbf{U}(x,-t)$  is a solution too. In other words, the wave equation is invariant under a time-reversal transformation if there is no absorption during propagation in the medium. In our specific application, this hypothesis is satisfied if the transmission line is lossless. However, since power network transmission lines are generally characterized by small values for the longitudinal resistance, the applicability of EMTR to lossy lines could also be considered. This point will be further discussed later in section 2.6.

In practical implementations, a signal  $s(x,t)$  is necessarily measured only during a finite period of time from an initial time selected here as the origin  $t = 0$  to a final time  $t = T$ , where  $T$  is the duration of the signal. To make the argument of the time-reversed variables be positive for the duration of the signal, we will consider, in addition to time reversal, an additional time delay  $T$ .

$$s(x,t) \mapsto s(x, T - t) \quad (2.17).$$

In order to illustrate the EMTR application to the fault location problem, a brief explanation of the electromagnetic transients associated with faults in power systems is presented.

A fault event in a power system can be associated with an injection into the power system itself of a step-like wave initiated by the fault occurrence. The fault-generated waves travel along the lines of the network and get reflected at the line extremities which are characterized by reflection coefficients whose values depend on the line surge impedance (characteristic impedance) and the input impedances of the connected power components. In particular, the line extremities can be grouped into three categories, namely: line terminals with power transformers, junctions to other lines, and the fault location. As discussed in [35], [61], for each of these boundary conditions the following assumptions can be reasonably made:

- Extremities, where a power transformer is connected, can be assumed, for the travelling waves, as open circuits, and therefore, the relevant voltage

## 2.5 Proposed EMTR-Based Fault Location Method

reflection coefficient is close to +1; indeed, fault-originated travelling waves are characterized by a spectrum with high-frequency components for which the input impedance of power transformers is generally dominated by a capacitive behavior with capacitances values in the order of few hundreds of pF (e.g. [61]);

- Extremities that correspond to a junction between more than two lines are characterized by a negative reflection coefficient;
- The reflection coefficient of the extremity where the fault is occurring is close to -1, as the fault impedance can be assumed to be significantly smaller than the line surge impedance.

With the above assumptions and for a given network topology, it is possible to determine a certain number  $p$  of paths, each one delimited between two extremities. Figure 2.3 illustrates these paths for a simplified network topology composed of a main feeder and a lateral. A given observation point in the system where voltage or current waveforms are measured will observe a superposition of travelling waves associated with the various paths.

Therefore, one can conclude that the domain of application of any fault location method belonging to the travelling waves-based methods described in Section 2.2.2 is formed by a one-dimensional space (associated to the line longitudinal coordinate  $x$ ) with given boundary conditions. In what follows, the proposed fault location method based on EMTR is presented.

## 2.5 Proposed EMTR-Based Fault Location Method

The application of the EMTR to locate faults in a power network will be based on three following steps.

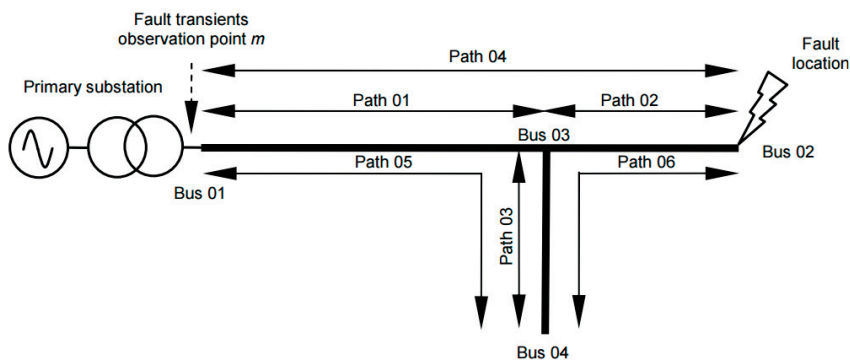


Figure 2.3. Paths covered by travelling waves caused by a fault at Bus 02. Adapted from [62].



(i) measurement of the fault-originated electromagnetic transient in a single observation point, (ii) simulation of the back-injection of the time-reversed measured fault signal for different guessed fault locations (GFLs) and using the network model, (iii) assessment of the fault location by determining, in the network model, the point characterized by the largest energy concentration associated with the back-injected time-reversed fault transients. In what follows, we illustrate the analytical aspects related to the proposed EMTR-based fault location method.

As described in [45], [46], one of the main hypotheses of the TR method is that the topology of the system needs to remain unchanged during the transient phenomenon of interest. Fault transients in power networks do not satisfy such a condition as the presence of the fault itself involves a change in the network topology when the fault occurs (i.e. at  $t = t_f$ ). However, for reversed times  $t$  such that  $t < T - t_f$ , EMTR is still applicable if the guessed fault is considered at the correct location. On the other hand, for a guessed location that does not coincide with the real one, time-reversal invariance does not hold. As a result of this property, time-reversed back-propagated signals will combine constructively to reach a maximum at the correct fault location. This property will be validated in the next sections to analytically prove the method and is used in both experimental measurements and simulation test cases.

### 2.5.1 Frequency-Domain Derivation

The aim of this sub-section is to analytically describe the behavior of the line response after a fault. In order to express analytically the line response, the problem is formulated in the frequency-domain. In particular, to provide a more straightforward use of the EMTR technique, we will make reference to a single-conductor overhead lossless transmission line (Figure 2.4) of length  $L$ . The line parameters may refer to a typical overhead transmission line. In particular, the surge impedance (characteristic impedance) is in the order of a few hundred Ohms. We assume that at both line extremities power transformers are connected.

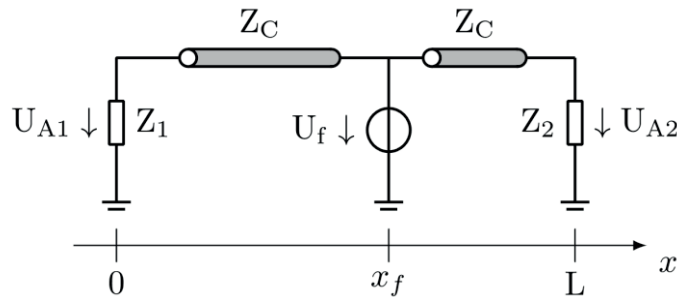


Figure 2.4. Simplified representation of the post-fault line configuration for the EMTR analytical validation.

Therefore, as discussed before, they are represented by means of high input impedances ( $Z_1$  and  $Z_2$  in Figure 2.4). The fault coordinate is  $x_f$  and fault transient waveforms are assumed to be recorded either at one end or at the two ends of the line. As the line model is lossless, the damping of the transients is provided only by the fault impedance, if any, and the high terminal impedances  $Z_1$  and  $Z_2$ .

As the analyzed fault transients last for only a few milliseconds, we assume that the pre-fault condition of the line is characterized by a constant value of voltage all along the line length ( $0 \leq x \leq L$ ).

To specify the boundary conditions of the two line sections of Figure 2.4, namely for  $0 \leq x \leq x_f$  and  $x_f \leq x \leq L$ , we can define reflection coefficients at  $x=0$  ( $i = 1$  of Figure 2.4) and  $x=L$  ( $i = 2$  of Figure 2.4) as:

$$\rho_i = \frac{Z_i - Z_C}{Z_i + Z_C}; \quad i=1,2 \quad (2.18).$$

Without losing generality, coefficients  $\rho_i$  in (2.18) could be assumed as frequency-independent within the considered short observation time. Concerning the boundary condition at the fault location, we assume to represent it by means of a voltage source  $U_f(\omega)$  located at  $x=x_f$ . Here, for the sake of abstraction, we represent the fault by means of an ideal voltage source with zero internal impedance that, as a consequence, represents a solid fault. Therefore, the voltage reflection coefficient in this point of the line is  $\rho_f=-1$ . Additionally, in view of the lossless line assumption, the line propagation constant,  $\gamma$ , is purely imaginary, namely:  $\gamma=j\beta$ , with  $\beta=\omega/c$ . The analytical expressions of voltages observed at the line terminals  $x=0$  and  $x=L$  in the frequency domain read:

$$U_{A1}(\omega) = U(0, \omega) = \frac{(1 + \rho_1)e^{-\gamma x_f}}{1 + \rho_1 e^{-2\gamma x_f}} U_f(\omega) \quad (2.19)$$

$$U_{A2}(\omega) = U(L, \omega) = \frac{(1 + \rho_2)e^{-\gamma(L-x_f)}}{1 + \rho_2 e^{-2\gamma(L-x_f)}} U_f(\omega) \quad (2.20).$$

Note that the effect of the ground losses can be represented as an additional frequency-dependent longitudinal impedance [63]. However, except for the case of distributed exciting sources (such as those produced by a nearby lightning discharge), ground losses can be disregarded for typical overhead power lines [64].

Now, the EMTR process can be carried out by using either (i) two observation points located at both extremities of the line, or (ii) one observation point.

### 2.5.1.1 Frequency-Domain Application of EMTR by Considering Two Observation Points at Each Line Terminal

According to TRM, a number of observation points at which transient signals initiated by the source (here: the fault) are measured could be used to apply the TR process. In a first step, it is assumed that two observation points at both ends of the line are used.

Equations (2.19) and (2.20) provide the frequency-domain expressions of fault-originated voltages at two observation points located at the line terminals. In agreement with the EMTR method, we can replace these observation points with two sources each one imposing the time-reversed voltage fault transients. As shown in (2.2), the TR operator in frequency domain is represented by the complex conjugate of the Fourier transform of the signal. Therefore, the time reversed recorded voltage transients are  $U_{A1}^*(\omega)$  and  $U_{A2}^*(\omega)$  where \* denotes the complex conjugate. Here we consider the Norton equivalents as:

$$I_{A1}^* = \frac{U_{A1}^*(\omega)}{Z_1} \quad (2.21)$$

$$I_{A2}^* = \frac{U_{A2}^*(\omega)}{Z_2} \quad (2.22)$$

where  $I_{A1}^*$  and  $I_{A2}^*$  are the injected currents as shown in Figure 2.5. As the location of the fault is the unknown of the problem, we will place it at a generic location  $x'_f$ . The contributions in terms of currents at the unknown fault location  $x'_f$  coming from the first and the second time-reversed sources  $I_{A1}^*$  and  $I_{A2}^*$ , are given respectively by:

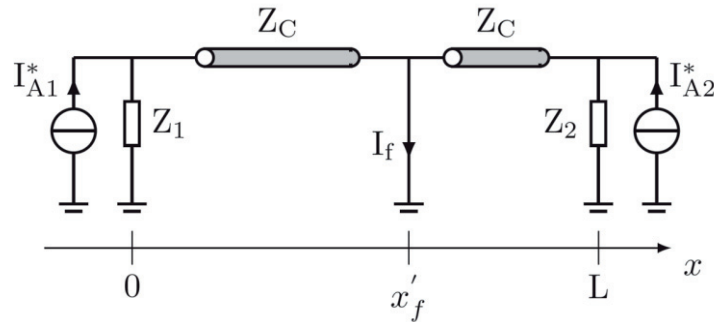


Figure 2.5. Representation of the EMTR applied to the single-line model of Figure 2.4.

$$I_{\Pi}(x'_f, \omega) = \frac{(1 + \rho_1) e^{-\gamma x'_f}}{1 + \rho_1 e^{-2\gamma x'_f}} I_{A1}^*(\omega) \quad (2.23)$$

$$I_{\Pi_2}(x'_f, \omega) = \frac{(1 + \rho_2) e^{-\gamma(L-x'_f)}}{1 + \rho_2 e^{-2\gamma(L-x'_f)}} I_{A2}^*(\omega) \quad (2.24).$$

Introducing (2.19)- (2.22) into (2.23) and (2.24), we obtain:

$$I_{\Pi}(x'_f, \omega) = \frac{(1 + \rho_1)^2 e^{-\gamma(x'_f-x_f)}}{Z_1(1 + \rho_1 e^{-2\gamma x'_f})(1 + \rho_1 e^{+2\gamma x_f})} U_f^*(\omega) \quad (2.25)$$

$$I_{\Pi_2}(x'_f, \omega) = \frac{(1 + \rho_2)^2 e^{-\gamma(x'_f-x_f)}}{Z_2(1 + \rho_2 e^{-2\gamma(L-x'_f)})(1 + \rho_2 e^{+2\gamma(L-x_f)})} U_f^*(\omega) \quad (2.26).$$

Therefore, we can derive a closed-form expression for the total current flowing through the GFL  $x'_f$ :

$$I_f(x'_f, \omega) = I_{\Pi}(x'_f, \omega) + I_{\Pi_2}(x'_f, \omega) \quad (2.27).$$

In what follows, we will make use of (2.27) to show the capability of the EMTR to converge the time-reversed injected transients to the fault location.

Let us make reference to a line characterized by a total length  $L=10$  km and let us assume a fault occurring at  $x_f=8$  km. The line is characterized by terminal impedances  $Z_1=Z_2=100$  k $\Omega$  and, for the fault, we assume  $U_f=1/j\omega$  v/(rad/s). The line is lossless and the per-unit-length capacitance and inductance are  $C=7.10E-12$  F/m and  $L=1.56E-6$  H/m, respectively.

By moving  $x'_f$  from 0 to  $L$ , it is possible to compute the current at the GFLs using (2.27). Figure 2.6 shows the normalized fault current signal energy (FCSE) (where the normalization has been implemented with respect to the maximum signal energy value of  $I_f$  for all the guessed fault locations) within a frequency-spectrum ranging from DC to 1 MHz. From Figure 2.6, it is clear that the energy of  $I_f(x'_f, \omega)$  reaches its maximum when the GFL coincides with the real one.

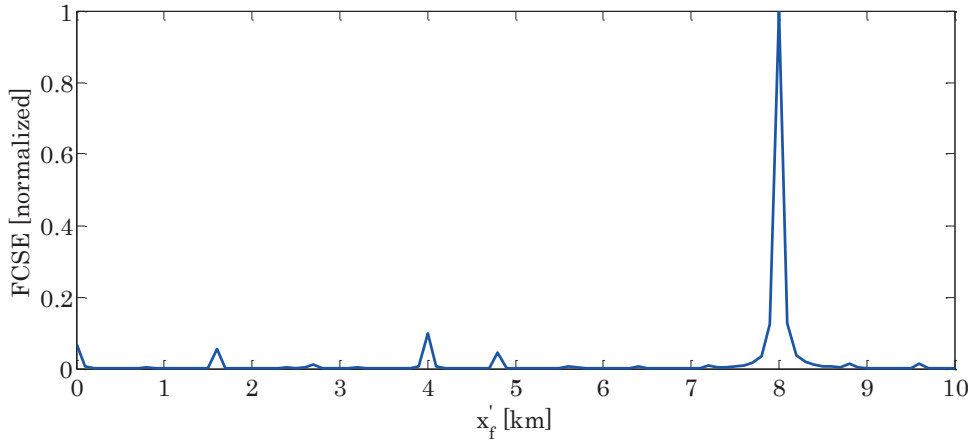


Figure 2.6. Normalized FCSE as a function of the GFL  $x'_f$  with multiple observation points. The real fault location is at  $x'_f=8$  km.

### 2.5.1.2 Frequency-Domain Application of EMTR by Considering One Observation Point

As it was mentioned before, one of the main problems in power systems protection is the limited number of observation points where measurement equipment can be placed. Therefore, the demonstration that the EMTR-based fault location method could be applied also for the case of a single observation point is of importance. To this end, let us assume that the fault-originated electromagnetic transients are observed only at one location, namely at the line left terminal. The network schematic in the time reversal state will be the one in Figure 2.7.

By making reference to the configuration of the previous case, we can extend the procedure to the case where only one injecting current source ( $I_{A1}$ ) is considered. In particular, we can derive from (2.21) the fault current at the guessed fault location  $x'_f$  as follows:

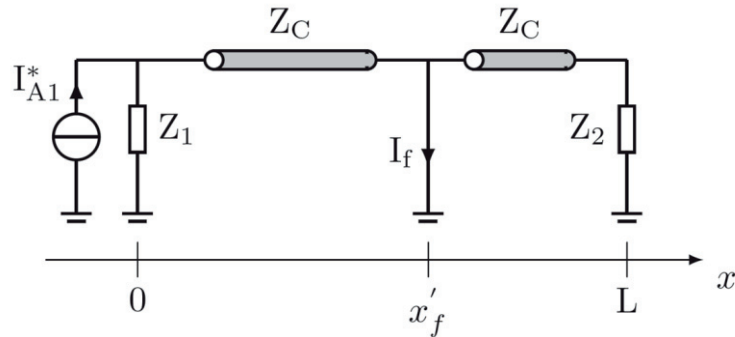


Figure 2.7. Representation of the EMTR applied to the single-line model of Figure 2.4 where a single observation point is placed at the beginning of the line ( $x = 0$ ).

$$I_f(x'_f, \omega) = I_{\Pi}(x'_f, \omega) = \frac{(1 + \rho_1)^2 e^{-\gamma(x'_f - x_f)}}{Z_1(1 + \rho_1 e^{-2\gamma x'_f})(1 + \rho_1 e^{+2\gamma x_f})} U_f^*(\omega) \quad (2.28).$$

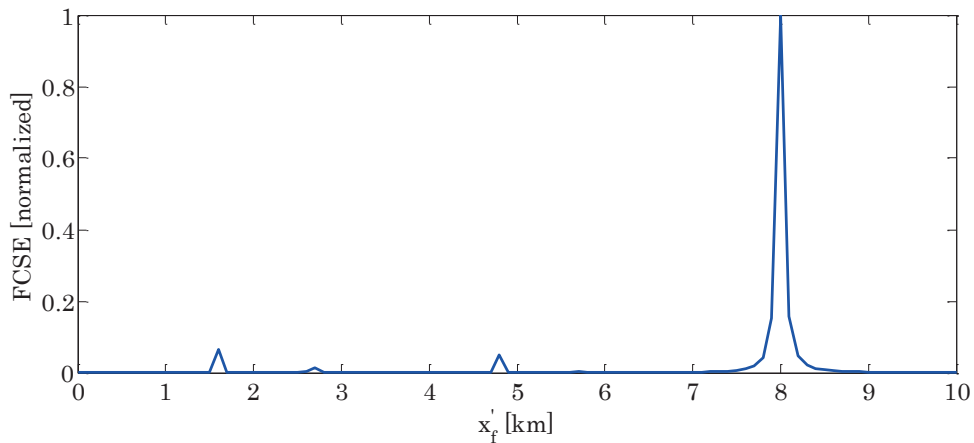
Figure 2.8 shows the normalized FCSE of  $I_f$  (where the normalization has been implemented with respect to the maximum signal energy value of  $I_f$  for all the GFLs) within a frequency-spectrum ranging from DC to 1 MHz.

It can be noted that the energy of  $I_f(x'_f, \omega)$  is maximum when the GFL is equal to the real one even for the case of a single observation point. From Figure 2.6 and Figure 2.8, it can further be observed that the two curves, corresponding respectively to one and to two observation points, provide accurately the correct fault location and the method can be effectively applied using a single observation point.

### 2.5.2 Time-Domain Algorithm

In the previous section, we have derived closed-form expressions for the fault current as a function of the guessed fault location. The purpose of this section is to extend the proposed method to realistic time-domain cases. The flow-chart shown in Figure 2.9 illustrates the step-by-step fault location procedure proposed in this study.

As it can be seen, the proposed procedure, similarly to other methods proposed in the literature (e.g., [25]), requires the knowledge of the network topology as well as its parameters. Such knowledge is used to build a corresponding network model.



**Figure 2.8. Normalized FCSE as a function of the GFL  $x'_f$  with single observation point. The real fault location is at  $x'_f=8$  km.**

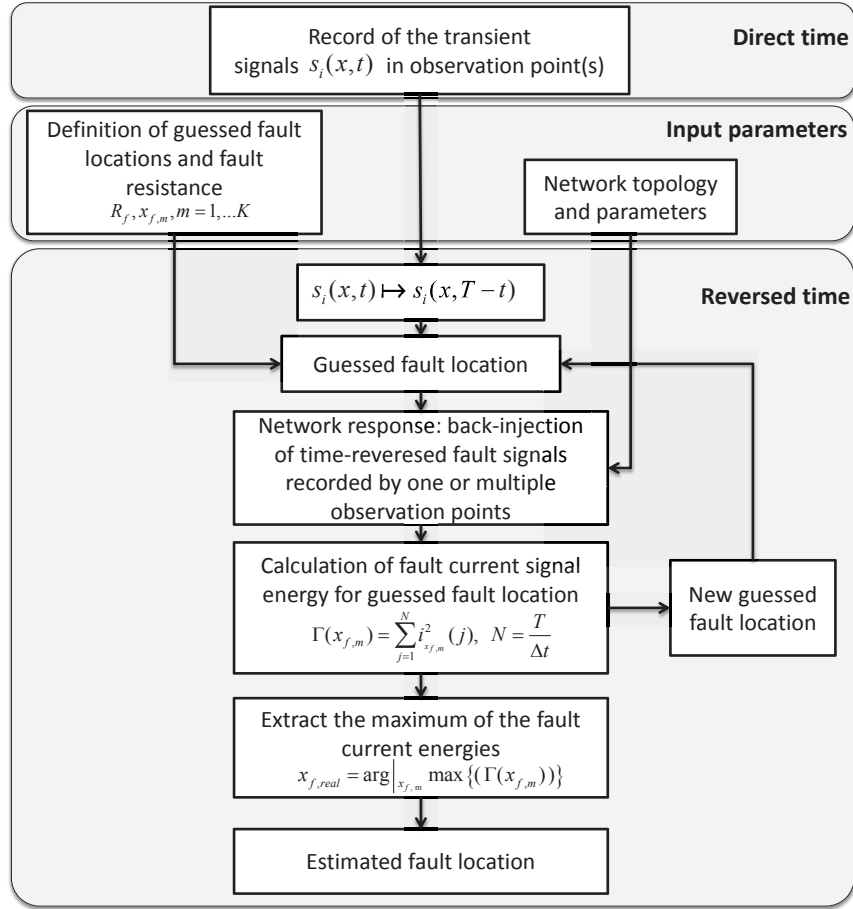


Figure 2.9. Flow-chart of the proposed EMTR-based fault location method.

Then, we assume to record fault transients,  $s_i(x, t)$  (with  $i=1,2,3$  for a three-phase system) at a generic observation point located inside the part of the network with the same voltage level comprised between transformers. The transient signals initiated by the fault is assumed to be recorded within a specific time window:

$$s_i(t), t \in [t_f, t_f + T] \quad (2.29)$$

where  $t_f$  is the fault triggering time, and  $T$  is the recording time window large enough to damp-out  $s_i(t)$ .

The unknowns of the problem are the fault type, location and impedance. Concerning the fault type, we assume that the fault location procedure will operate after the relay maneuver. Therefore, the single or multi-phase nature of the fault is assumed to be known. Concerning the fault location, we assume a set of a-priori locations  $x_{f,m}, m=1, \dots, K$  for which the EMTR procedure is applied. Concerning the fault impedance, for all the GFLs, an a-priori value of the fault resistance,  $R_{fj}$ , is assumed. As it will be shown in the application examples and performance

evaluation section, different guessed values of  $R_{xf}$  do not affect the fault location accuracy.

The recorded signals are reversed in time and back-injected from an observation points into the system for each  $x_{f,m}$ . In order to make the argument of the time-reversed variables be positive for the duration of the signal, we add, in addition to time reversal, a time delay equal to the duration of the recording time  $T$ :

$$\hat{t} = (T + t_f) - t \quad (2.30)$$

$$\bar{s}(\hat{t}), \hat{t} \in [0, T] \quad (2.31).$$

As shown in Figure 2.9, for each of the GFL, we can compute the FCSE that corresponds to the energy of the currents flowing through the GFL as:

$$\Gamma(x_{f,m}) = \sum_{p=1}^M \sum_{j=1}^N \left[ i_{x_{f,m}}^p(j) \right]^2, \quad T = N\Delta t \quad (2.32)$$

where  $N$  is the number of samples and  $\Delta t$  the sampling time, and  $p$  indicates the number of conductors in the line which are involved in the fault. According to the EMTR method presented in the previous section, the energy given by (2.32) is maximized at the real fault location. Thus, the maximum of the calculated FCSEs will indicate the real fault point:

$$x_{f,real} = \arg \left|_{x_{f,m}} \max \{ (\Gamma(x_{f,m})) \} \right. \quad (2.33).$$

## 2.6 The Issue of Losses

As discussed by equation (2.16), the telegrapher's equations are invariant under a TR transformation for lossless lines. Electromagnetic propagation involving a dissipative medium is not rigorously time reversal invariant unless an inverted-loss medium is considered for the reverse times. In this section, the effect of the line losses on the accuracy of the fault location method is analyzed by considering three different back-propagation models: lossless, lossy, and inverted-loss [65]. The presented analysis will be based on the transmission line theory. For the sake of simplicity, we make reference to Figure 2.10 that represents the equivalent circuit of a differential length of a single-wire line above a ground plane [66].

In Figure 2.10,  $L'$ ,  $C'$  and  $G'$  are the per-unit-length longitudinal inductance, transverse capacitance and transverse conductance, respectively,  $Z_w$  is the per-unit-length internal impedance of the wire,  $Z'_g$  and  $Y'_g$  are the per-unit-length



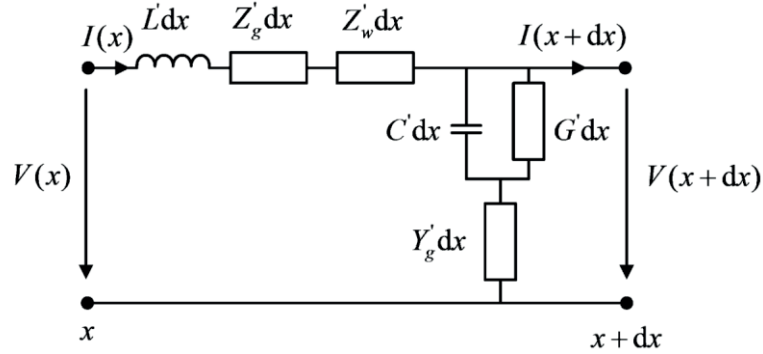


Figure 2.10. Equivalent circuit of a single-wire line above a ground plane.

ground impedance and admittance which account respectively for the losses associated with the penetration of magnetic and electric fields in the ground [66].

The effect of losses (in the conductor and in the ground) results essentially in an attenuation of propagated transients and a modification of the propagation speed, both effects being generally frequency dependent. In the application of the EMTR to fault location in which the timing is crucial, the modification of the propagation speed is expected to be more critical than the attenuation of the amplitude [65]. In what follows, three different back-propagation models will be investigated [65].

### 2.6.1 Inverted-Loss Back-Propagation Model

This model is equivalent to invert the real part of the propagation constant:

$$\tilde{\gamma} = -\alpha + j\beta \quad (2.34)$$

Note that this is not a physical model since the line itself becomes active and gives energy to the signal that is propagating along it. However, this model can be numerically implemented (even though some software does not allow negative parameters). In this case, it can readily be shown that the telegrapher's equations are time-reversal invariant. An exact location is hence expected as a result of the application of this model, under the assumption that the line parameters are perfectly known.

### 2.6.2 Lossless Back-Propagation Model

In this model, the losses in the back propagation are disregarded. In other words, the back-propagation line per-unit-length parameters associated with losses become:

$$\tilde{Z}'_w = 0, \tilde{Z}'_g = 0, \tilde{G}' = 0, \tilde{Y}'_g \rightarrow \infty \quad (2.35)$$

Hence, the propagation and phase velocity will in general not be the same as during the direct propagation, leading possibly to inaccuracies in the determination of fault location. The resulting propagation constant for the back propagation is therefore:

$$\tilde{\gamma} = j\beta \quad (2.36).$$

### 2.6.3 Lossy Back-Propagation Model

In this model, a lossy model for the line is used for the back propagation. The back-propagation line per-unit-length parameters become in this case:

$$\tilde{Z}'_w = Z'_w, \tilde{Z}'_g = Z'_g, \tilde{G}' = G', \tilde{Y}'_g = Y'_g \quad (2.37)$$

And the resulting propagation constant for the back propagation is:

$$\tilde{\gamma} = \gamma = \alpha + j\beta \quad (2.38).$$

Even though a lossy medium is not time-reversal invariant, the propagation speed, which is a key parameter, remains unchanged. Therefore, it can be shown that all contributions from discontinuities that would occur in a real network will add up in phase at the fault location. For this reason, we can expect more accurate results with this model than those associated with a lossless back-propagation model.

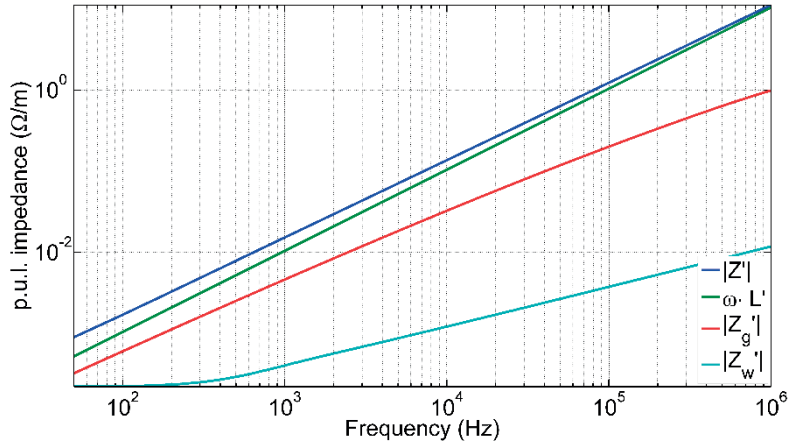
### 2.6.4 Comparison of the Back-Propagation Models

To compare the performance of the three models described in the previous section, we will consider a simple configuration of a 10 km long single-wire overhead line above a finitely-conducting ground. The assumed fault is located at 8 km from the left terminal where the voltage transient generated by the fault is recorded. The EMTR location procedure described in section 2.5 is used. The propagation in direct time takes the losses into account, and the back-propagation is simulated making use of each of the three models presented previously. The computation is made in the frequency domain, in the range 1 kHz – 1 MHz and is implemented in Matlab®. The parameters of the line are given in Table 2.1.

The per-unit-length parameters of the line were computed using expressions that can be found in [64], [66]. The magnitude of the total per-unit-length longitudinal impedance  $Z'$  is plotted in Figure 2.11 as a function of the frequency. In the same plot, we have also shown the contributions of the inductive term, ground and wire impedances. It can be seen that the ground losses are dominant compared to the losses in the conductor [63].

**Table 2.1. Parameters of the Line.**

Parameter	Value
Height above the ground	10 m
Diameter of the wire	1 cm
Conductivity of the wire (copper)	$5.8 \cdot 10^7$ S/m
Relative permittivity of the ground	10
Conductivity of the ground	$10^{-2}$ - $10^{-3}$ S/m
Terminal resistances	50 k $\Omega$


**Figure 2.11. Magnitude of the per-unit-length longitudinal impedance as a function of frequency. The ground conductivity is  $\sigma_g = 0.001$  S/m.**

The magnitude of the total per-unit-length admittance  $Y'$  is plotted in Figure 2.12. It can be seen that the capacitive term is dominant and the losses due to the transverse air and ground admittances are negligible [64]. Figure 2.13 shows the plot of the phase and group velocities as a function of the frequency, when considering losses in the line. Since the considered line is overhead, the velocity when disregarding losses is almost equal to the speed of light in vacuum. Now, considering the proposed EMTR-based fault location method for this network, the energy of the current flowing from the conductor to the ground in the back-propagated time at different GFLs along the line are calculated. The simulations are carried out using the three back-propagation models described before, and considering two different values for the ground conductivity,  $\sigma_g = 0.01$  S/m and  $\sigma_g = 0.001$  S/m.

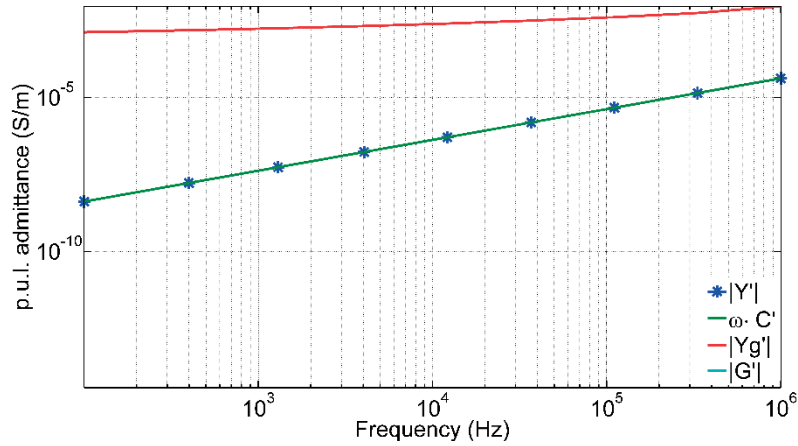


Figure 2.12. Magnitude of the per-unit-length transverse admittance as a function of frequency. Ground conductivity is  $\sigma_g = 0.001$  S/m.

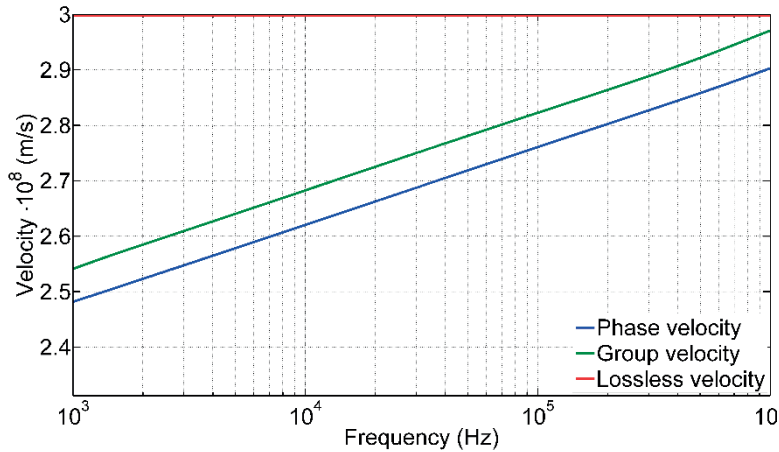


Figure 2.13. Phase and group velocities as a function of the frequency. Ground conductivity is  $\sigma_g = 0.001$  S/m.

Figure 2.14 and Figure 2.15 show the FCSE normalized to its maximum, for the three back-propagation models. The ground conductivities are considered  $\sigma_g = 0.01$  and  $\sigma_g = 0.001$  S/m, respectively.

It can be seen that the lossy and inverted-loss models were able to locate the fault at the correct position (8 km). On the other hand, the lossless back-propagation model was not able to accurately locate the fault. The location errors for the two considered values for the ground conductivity (0.01 S/m and 0.001 S/m) were respectively 800 m and 1.3 km (Table 2.2). The obtained results are consistent with those related to the use of EMTR to locate lightning discharges. By considering this example, we can conclude that as expected, an inverted-loss model for the back-propagation results in a perfect estimation of the fault location.

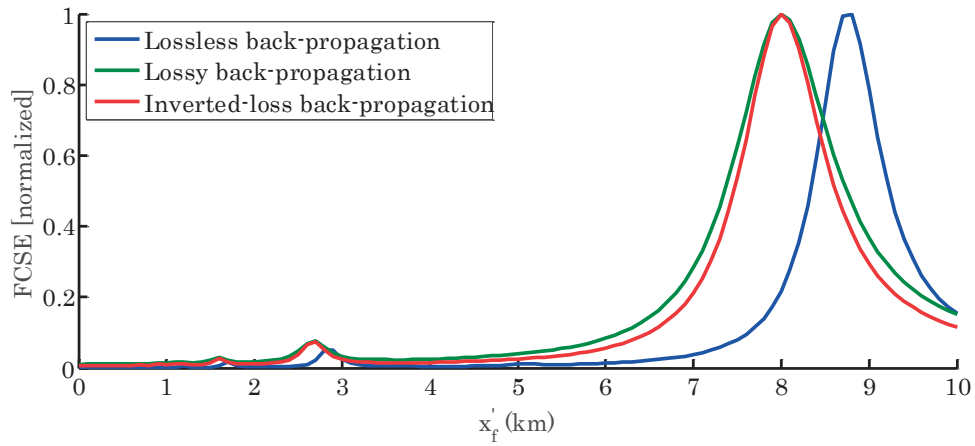


Figure 2.14. Fault current energy normalized to its maximum, for the three back-propagation models. Ground conductivity  $\sigma_g = 0.01$  S/m.

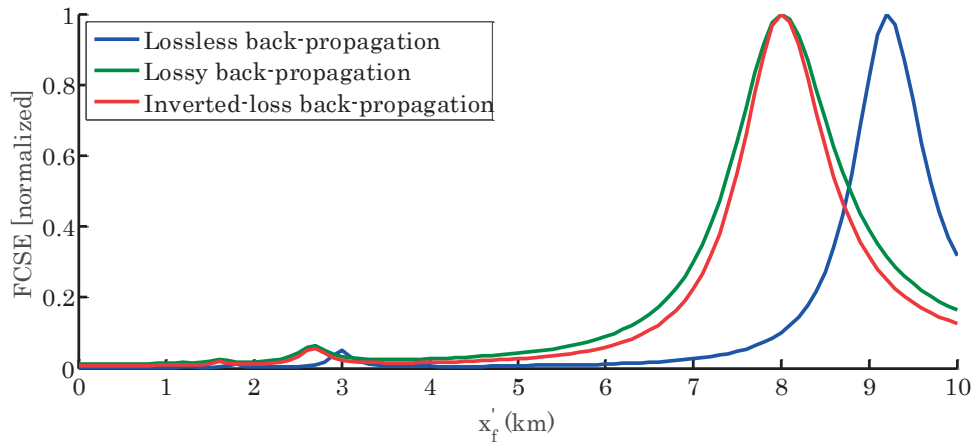


Figure 2.15. Fault current energy normalized to its maximum, for the three back-propagation models. Ground conductivity  $\sigma_g = 0.001$  S/m.

Table 2.2. Location error according to the three Models of Back-Propagation.

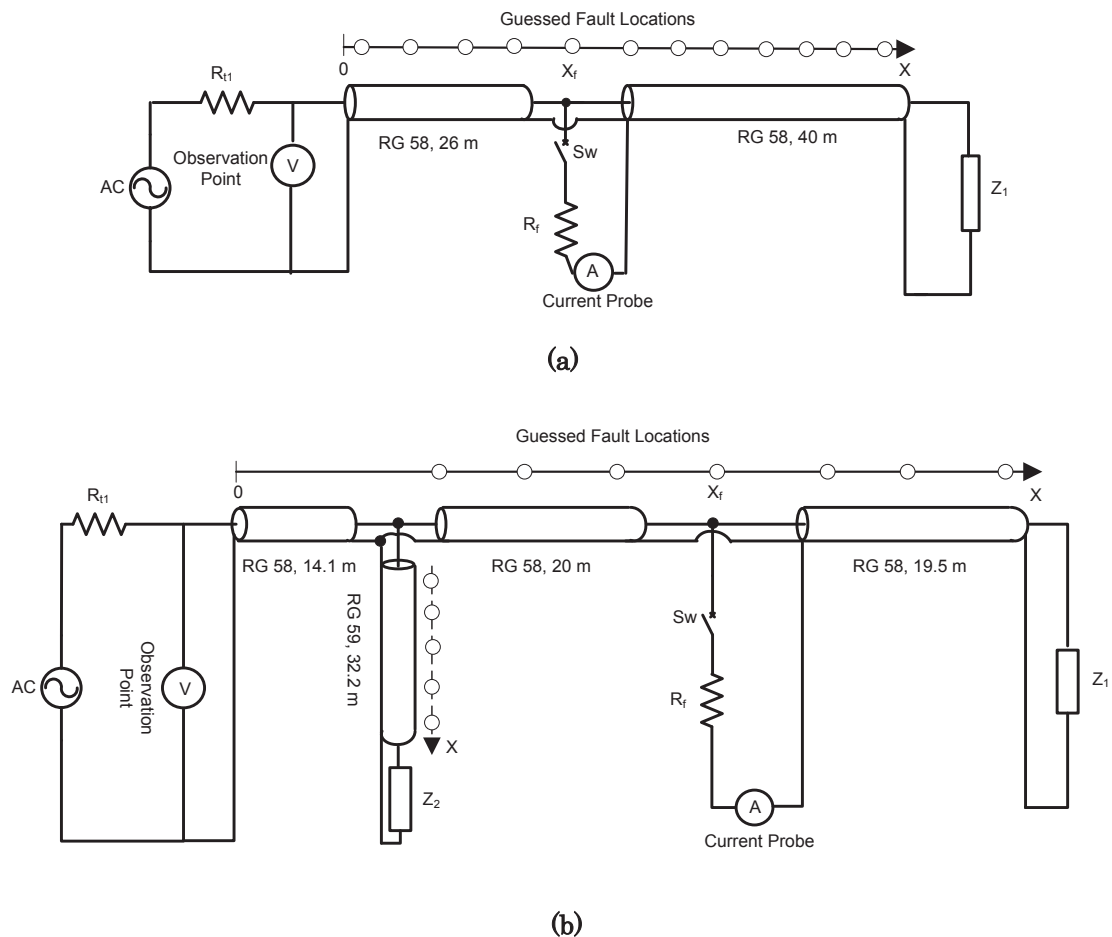
Back-propagation model	Error (km)	
	$\sigma_g = 0.01$ S/m	$\sigma_g = 0.001$ S/m
Lossless back-propagation	0.8	1.3
Lossy back-propagation	0	0
Inverted-loss back-propagation	0	0

## 2.7 Experimental Validation

It is also observed that, a back-propagation model in which the losses are included results also in a perfect estimation of the fault location, even though in this case the telegrapher's equations are not strictly time-reversal invariant. This is a very significant result since it allows the use of commercial codes to simulate the back-propagation phase during which the time-reversed fault-generated transients are injected into the network [65].

## 2.7 Experimental Validation

To provide a ground truth validation of the EMTR-based fault location method, a real experimental test is carried out by making reference to a reduced-scale coaxial cable system. Such a system has been realized by using standard RG-58 and RG-59 coaxial cables where real faults were hardware-initiated. The topologies adopted to carry out the experimental validation are shown in Figure 2.16.



**Figure 2.16.** Topologies adopted for the reduced-scale experimental setup: (a) a single transmission line configuration (RG-58 coaxial cable), (b) a T-shape network made of both RG-58 and RG-59 coaxial cables.

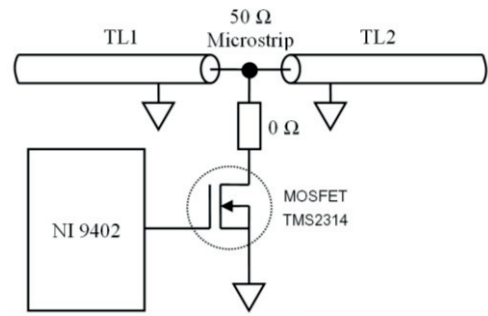
As seen on the figure, the first topology corresponds to a single transmission line whilst the second one corresponds to a T-shape network where the various branches are composed of both RG-58 and RG-59 cables (i.e. each branch has a different surge impedance but the same propagation speed). Figure 2.16 shows also the GFLs at which the current flowing through the fault was measured. For each considered topology, transients generated by the fault are recorded at one observation point, shown also on Figure 2.16.

The fault-originated transients were measured by means of a 12-bit oscilloscope (LeCroy Waverunner HRO 64Z) operating at a sampling frequency of 1 GSa/s (Giga Samples per second). For the direct time, the oscilloscope directly records voltages at the shown observation points marked in Figure 2.16 (a) and (b). For the reversed-time, the current at each GFL was measured by using a 2877 Pearson current probe characterized by a transfer impedance of  $1 \Omega$  and an overall bandwidth of 300 Hz - 200 MHz. It is worth observing that the switching frequencies for the adopted reduced-scale systems are in the order of few MHz.

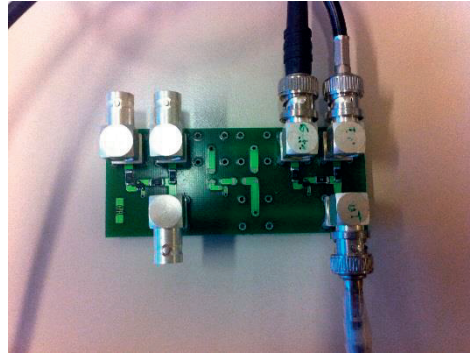
The time-reversed transient waveforms were generated by using a 16-bit arbitrary waveform generator (LeCroy ArbStudio 1104) operating at a sampling frequency of 1 GSa/s (the same adopted to record the fault-originated waveforms). The lines were terminated by high impedances ( $Z_1$  and  $Z_2$  equal to  $1 \text{ M}\Omega$ ) and the voltage source injecting the time-reversed signal was connected to the line through a lumped resistance of  $R = 4.7 \text{ k}\Omega$  in order to emulate, in a first approximation, the high-input impedance of power transformers with respect to fault transients.

The faults were generated at an arbitrary point of the cable network. They were realized by a short circuit between the coaxial cable shield and the inner conductor. It is important to underline that such type of faults excites the shield-to-inner conductor propagation mode that is characterized, for the adopted coaxial cables, by propagation speeds of 65.9% (RG-58) and 82% (RG-59) of the speed of light  $c$ . It is worth noting that the limited lengths of the reduced-scale cables (i.e. tens of meters) involve propagation times in the order of tens to hundreds of nanoseconds. Such a peculiarity requires that the fault emulator needs to be able to change its status in a few nanoseconds in order to correctly emulate the fault. The chosen switch was a high-speed MOSFET (TMS2314) with a turn-on time of 3 ns. The MOSFET was driven by a National Instruments digital I/O card C/series 9402 able to provide a gate signal to the MOSFET with a sub-nanosecond rise time and a maximum voltage of 3.4 V. The schematic representation of the circuit of the hardware fault emulator and the built PCB board are illustrated in Figure 2.17 (a) and (b), respectively. Note that the experiment reproduces solid faults since no resistors were placed between the MOSFET drain and the transmission line conductors. The experimental setup is depicted in Figure 2.18.

## 2.7 Experimental Validation

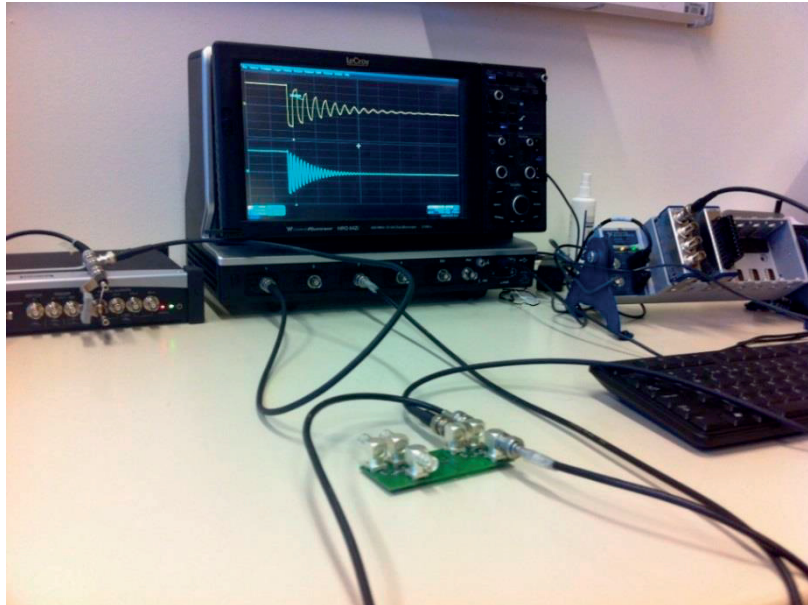


(a)



(b)

**Figure 2.17. MOSFET-emulated fault adopted in the reduced-scale experimental setup: (a) schematic representation, (b) built PCB board.**



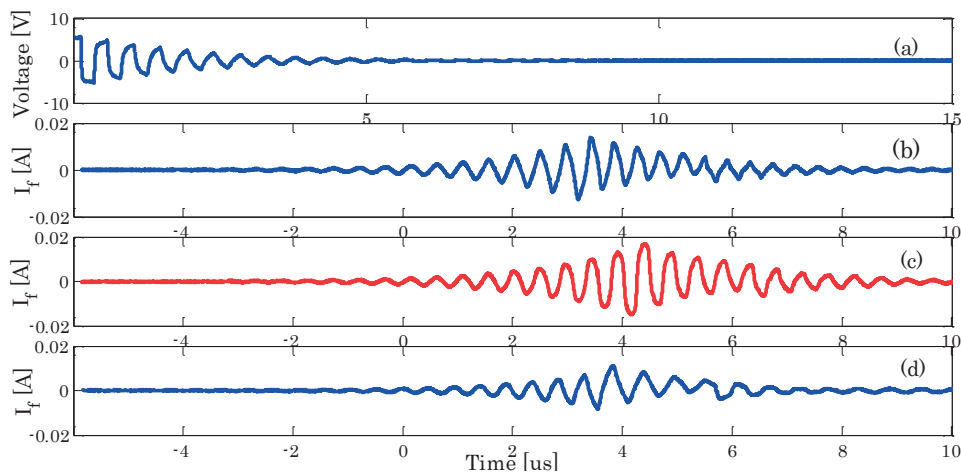
**Figure 2.18. The experimental setup used for the EMTR-based fault location method validation.**

By making reference to the topology of Figure 2.16 (a), Figure 2.19 (a) shows the measured direct-time voltage at the considered observation point for a fault location  $x_f = 26$  m. The measured voltage was then time-reversed and injected back into the line using the arbitrary waveform generator for each of the 12 different guessed fault locations that are indicated in Figure 2.16 (a). For each case, the fault current resulting from the injection of the time-reversed signal of Figure 2.19 (a) was measured using the Pearson current probe. Figure 2.19 (b)-(d) show the waveforms of the fault current at the guessed fault locations  $x'_f = 23$  m,  $x'_f = 26$  m and  $x'_f = 28$  m respectively, resulting from the injection of the time-reversed signal.

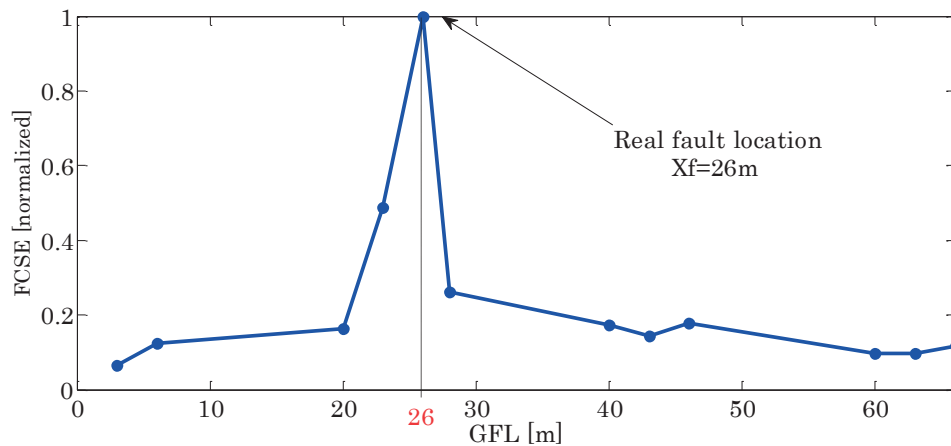


The normalized FCSE is shown in Figure 2.20 as function of the GFL (also in this case, the normalization has been implemented with respect to the maximum signal energy of the fault current in the guessed fault location). As it can be observed, the correct fault location is uniquely and clearly identified.

Figure 2.21 shows the same signal energy profiles for the case of the topology of Figure 2.16 (b). In this case, the real fault location is at a distance of 34.1 m from the source and in the RG-58 section of the network. As it can be observed, also in the case of a multi-branched network with lines characterized by different electrical parameters (i.e. inhomogeneous lines with different surge impedances), the proposed methodology correctly identifies the fault location.



**Figure 2.19.** Experimentally measured waveforms for a fault location  $x_f = 26$  m for the topology of Figure 2.16-(a); (a) direct-time voltage measured at the observation point located at the beginning of the line. Measured fault currents as a result of the injection of time-reversed signal at guessed fault locations (b)  $x'_f = 23$  m, (c)  $x'_f = 26$  m (real fault location) and (d)  $x'_f = 28$  m.



**Figure 2.20.** Normalized FCSE as a function of the position of the GFL for the configuration shown in Figure 2.16 (a). The real fault location is at  $x_f = 26$  m.

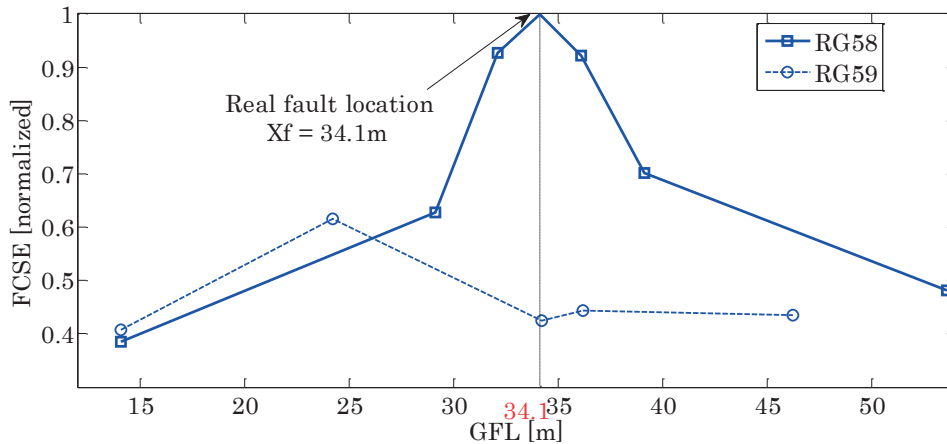


Figure 2.21. Normalized FCSE as a function of the position of the GFL for the case of the topology presented in Figure 2.16-b. The real fault location is at  $x_f = 34.1$ m in RG-58.

## 2.8 Application Examples and Performance Evaluation

In order to evaluate the performance of the EMTR-based fault location method, several application examples are considered by making reference to different types of power networks including (i) inhomogeneous network composed of mixed overhead-coaxial cable lines, (ii) radial distribution network, (iii) series-compensated transmission line.

### 2.8.1 Inhomogeneous Network Composed of Mixed Overhead-Coaxial Cable Lines

For the first application examples, reference is made to the case of a network composed of a three-conductor transmission line and an underground coaxial cable shown in Figure 2.22.

The overhead line length is 9 km and the cable length is 2 km. They are modeled by means of a constant-parameter model implemented within the EMTP-RV simulation environment [67], [68], [69]. Both the overhead line and the cable parameters have been inferred from typical geometries of 230 kV lines and cables. The series impedance and shunt admittance matrices for the line and cable are given by (2.39)-(2.42) and have been calculated in correspondence of the line and cable switching frequency.

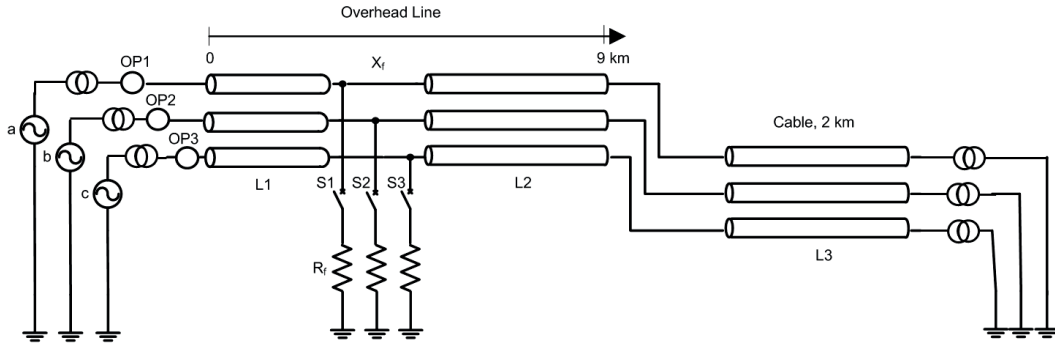


Figure 2.22. Schematic representation of the inhomogeneous network under study implemented in the EMTP-RV simulation environment.

$$Z_{Line} = \begin{bmatrix} 1.10 + j15.32 & 1.00 + j5.80 & 1.00 + j4.64 \\ 1.00 + j5.80 & 1.09 + j15.33 & 1.00 + j5.80 \\ 1.00 + j4.64 & 1.00 + j5.80 & 1.10 + j15.32 \end{bmatrix} \frac{\Omega}{km} \quad (2.39)$$

$$Y_{Line} = \begin{bmatrix} 2 \cdot 10^{-4} + j67.53 & -j16.04 & -j7.91 \\ -j16.04 & 2 \cdot 10^{-4} + j70.12 & -j16.04 \\ -j7.91 & -j16.04 & 2 \cdot 10^{-4} + j67.53 \end{bmatrix} \times 10^{-6} \frac{S}{km} \quad (2.40).$$

$$Z_{Cable} = \begin{bmatrix} 0.07 + j0.70 & 0.05 + j0.45 & 0.05 + j0.41 & 0.05 + j0.62 & 0.05 + j0.45 & 0.05 + j0.41 \\ 0.05 + j0.45 & 0.07 + j0.70 & 0.05 + j0.45 & 0.05 + j0.45 & 0.05 + j0.62 & 0.05 + j0.45 \\ 0.05 + j0.41 & 0.05 + j0.45 & 0.07 + j0.70 & 0.05 + j0.41 & 0.05 + j0.45 & 0.05 + j.62 \\ 0.05 + j0.62 & 0.05 + j0.45 & 0.05 + j0.41 & 0.03 + j0.62 & 0.05 + j0.45 & 0.05 + j0.41 \\ 0.05 + j0.45 & 0.05 + j0.62 & 0.05 + j0.45 & 0.05 + j0.45 & 0.03 + j0.62 & 0.05 + j0.45 \\ 0.05 + j0.41 & 0.05 + j0.45 & 0.05 + j0.62 & 0.05 + j0.41 & 0.05 + j0.45 & 0.03 + j0.62 \end{bmatrix} \frac{\Omega}{km} \quad (2.41)$$

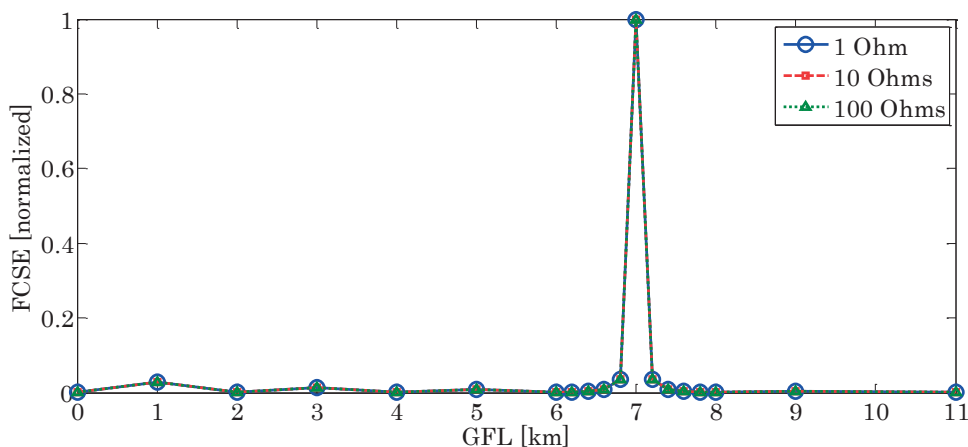
$$Y_{Cable} = \begin{bmatrix} 0.12 + j41.46 & 0 & 0 & -0.12 - j41.46 & 0 & 0 \\ 0 & 0.12 + j41.46 & 0 & 0 & -0.12 - j41.46 & 0 \\ 0 & 0 & 0.12 + j41.46 & 0 & 0 & -0.12 - j41.46 \\ -0.12 - j41.46 & 0 & 0 & 2.35 + j94.61 & 0 & 0 \\ 0 & -0.12 - j41.46 & 0 & 0 & 2.35 + j94.61 & 0 \\ 0 & 0 & -0.12 - j41.46 & 0 & 0 & 2.35 + j94.61 \end{bmatrix} \times 10^{-6} \frac{S}{km} \quad (2.42)$$

As it can be observed, the simulated lines take into account the losses. Concerning the line start and cable end, they are assumed to be terminated with power transformers represented, as discussed before, by high impedances, assumed, in a first approximation, equal to 100 k $\Omega$ . The supply of the line is provided by a three-phase AC voltage source placed at  $x = 0$ . All the fault transients were observed at the overhead line start in three observation points, shown as OP1, OP2, OP3 in Figure 2.22, corresponding to the three conductors of the line (left terminal).

Two fault cases are considered to examine the performance of the proposed method for the case of inhomogeneous networks (i) a three-phase-to-ground fault at 7 km away from the source with a 0  $\Omega$  fault impedance (solid) and, (ii) a three-phase-to-ground fault at 5 km away from the source with a 100  $\Omega$  fault impedance (high-impedance fault). In agreement with the proposed procedure, the position of the GFL is moved along the overhead and cable lines assuming, for the fault impedance, a priori fixed values of 1, 10, and 100  $\Omega$ .

Figure 2.23 and Figure 2.24 show the energy of the current flowing through the GFL for solid and high impedance faults, respectively. These figures illustrate the calculated normalized FCSEs for three a-priori guessed values of the fault resistance, namely 1, 10 and 100  $\Omega$ , as a result of the injection of the time-reversed voltage at the observation points (overhead line left terminal). In order to evaluate the accuracy of the proposed method, the position of the GFL is varied with a step of 200 m near to the real fault location.

As it can be seen, the proposed method is effective in identifying the fault location in inhomogeneous networks even when losses are present. The proposed method shows very good performances for high-impedance faults and, also, appears robust against the a priori assumed fault impedance. The accuracy of the method appears to be less than 200 m (assumed value for the separation between GFL).



**Figure 2.23.** Normalized FCSE as a function of the GFL and for different guessed fault resistance values. The real fault location is at  $x_f = 7$  km and real fault impedance is 0  $\Omega$ .

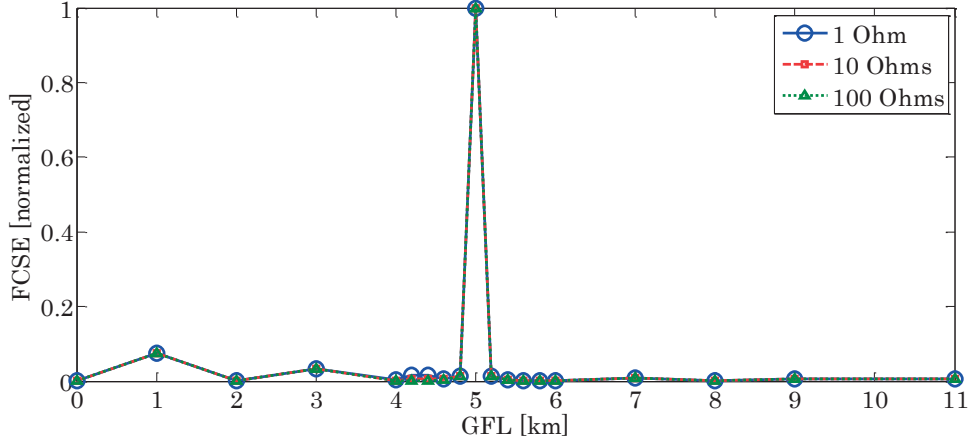


Figure 2.24. Normalized FCSE as a function of the GFL and for different guessed fault resistance values. The real fault location is at  $x_f = 5$  km and real fault impedance is  $100 \Omega$ .

### 2.8.2 Radial Distribution Network: IEEE 34-Bus Test Distribution Feeder

In order to test the performance of the proposed fault location method in multi-branch, multi-terminal distribution networks, the IEEE 34-bus test feeder is considered. The model of this network is the same adopted in [27] where, for the sake of simplicity, the following assumptions have been done:

1. All transmission lines are considered to be characterized by configuration “ID #500” as reported in [70];
2. The loads are considered to be connected via interconnection transformers and are located at lines terminations.

Figure 2.25 shows the IEEE 34-bus test distribution network implemented in the EMTP-RV simulation environment. According to the blocking behavior of the transformers for travelling waves, such a configuration could be divided into three zones where these zones are characterized by the buses between two transformers. For this case study, only the first zone is considered as it shown in Figure 2.25. The observation point for this network is located at the secondary winding of the transformer and is shown in Figure 2.25.

Four different case studies are considered to examine the performance of the proposed method: (i) a three-phase-to-ground fault at Bus 808 with a  $0 \Omega$  fault impedance, (ii) a three-phase-to-ground fault at Bus 812 with a  $100 \Omega$  fault impedance, (iii) a single-phase-to-ground fault at Bus 810 with a  $0 \Omega$  fault impedance, and (iv) a single-phase-to-ground fault at Bus 806 with a  $100 \Omega$  fault impedance.

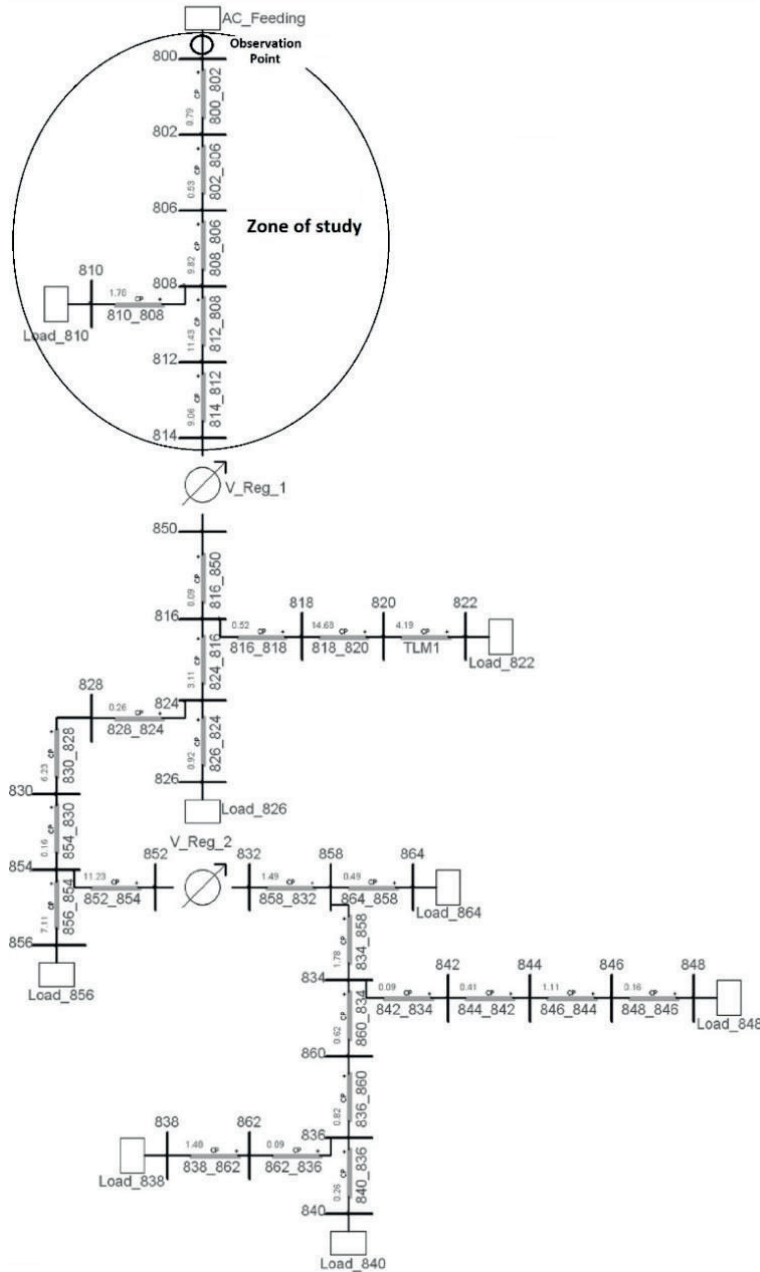
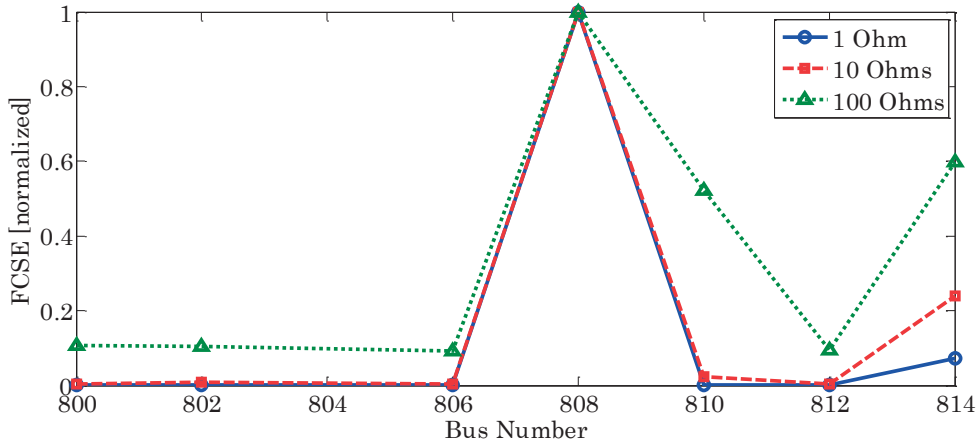
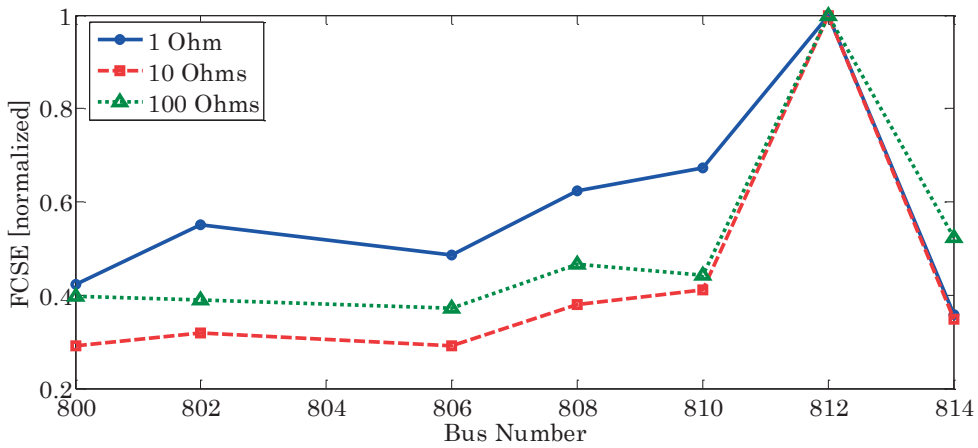


Figure 2.25. IEEE 34-bus distribution system implemented in EMTP-RV.

The recorded transient signals are time-reversed and, for each GFL, the current flowing through the fault resistance is calculated by simulating the network with back-injected time-reversed signals from the observation points. As for the previous cases, the normalized signal energy of this current is calculated for all GFLs with different guessed fault impedances (i.e., 1, 10, 100  $\Omega$ ). Figure 2.26 shows the calculated FCSEs for (a) a three-phase-to-ground solid (0  $\Omega$ ) fault at Bus 808, and (b) a three-phase-to-ground high-impedance fault (100  $\Omega$ ) at Bus 812.



(a)

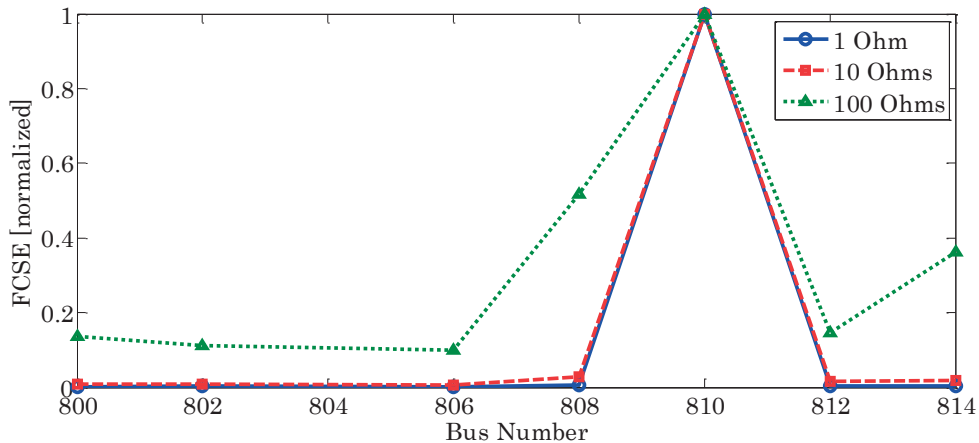


(b)

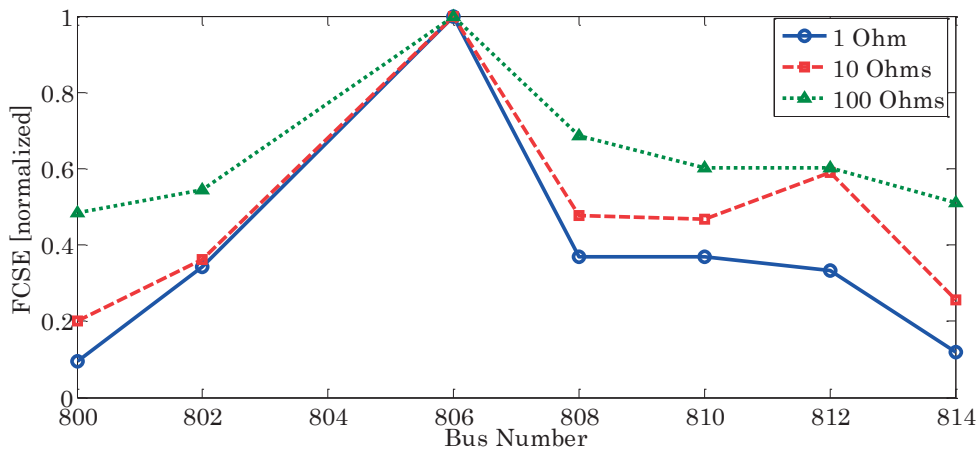
**Figure 2.26. Normalized FCSE as a function of the GFL and for different guessed fault resistance values: a) three-phase-to-ground solid fault ( $0 \Omega$ ) at Bus 808, b) three-phase-to-ground high-impedance fault ( $100 \Omega$ ) at Bus 812.**

Figure 2.27 shows the calculated FCSE for (a) a single-phase-to-ground solid ( $0 \Omega$ ) fault at Bus 810, and (b) a single-phase-to-ground high-impedance fault ( $100 \Omega$ ) at Bus 806.

From Figure 2.26 and Figure 2.27, it is possible to infer the remarkable performances of the proposed fault location method for the case of realistic multi-branch multi-terminal lines. Additionally, the proposed method appears, also in this case, to be robust against solid and high-impedance faults as well as against different fault types (phase-to-ground or three-phase ones).



(a)



(b)

**Figure 2.27.** Normalized FCSE as a function of the GFL and for different guessed fault resistance values: a) single-phase-to-ground solid fault ( $0 \Omega$ ) at Bus 810, b) single-phase-to-ground high-impedance fault ( $0 \Omega$ ) at Bus 806.

### 2.8.3 Series-Compensated Transmission Line

In the last two decades, the advances in power electronics have enabled sophisticated applications in power systems. In particular, applying series-compensation in power systems can increase power transfer capability, improve transient stability and damp power oscillations. However, it also introduces several technical challenges, specifically for the protection and fault location algorithms. For a series-compensated system, distance and fault-location estimation algorithms are significantly affected, leading to the malfunction of relays at different situations [71], [72].

Fault location in series-compensated transmission lines has a more crucial role since these type of lines are designed to link distant nodes among which high



amount of power is usually transferred. As summarized in [73], fault location methods for series-compensated transmission lines use either one or multiple-end measurements and, in general, are based on post-fault impedance assessment. Similar to the existing phasor-based or travelling wave-based fault location methods, the multiple-end fault location methods for the series-compensated transmission lines provide more robust and precise location accuracy.

In this section, the application of the proposed EMTR-based fault location method for the series-compensated lines using single-end measurement is presented. To this end, an application example is considered by making reference to a three-conductor series-compensated transmission line. The line length is 200 km and the network is implemented within the EMTP-RV simulation environment. The series-compensation is done in the center of the transmission line to achieve a compensation degree of 50%. The relevant line parameters are the following:

- Positive sequence impedance:  $0.03293 + j0.3184 \Omega/\text{km}$
- Positive sequence capacitance:  $0.01136 \mu\text{F}/\text{km}$
- Zero sequence impedance:  $0.2587 + j1.1740 \Omega/\text{km}$
- Zero sequence capacitance:  $0.00768 \mu\text{F}/\text{km}$ .

The line is assumed to be terminated at both ends on power transformers which, for signals characterized by high-frequency spectrum content, can be replaced by high impedances ( $100 \text{ k}\Omega$  in this study).

The supply of the line is provided by a three-phase AC voltage source placed at  $x = 0$ . A schematic representation of the system is shown in Figure 2.28. In this figure, OP1, OP2, and OP3 are observation points corresponding to each conductor of the transmission line where voltage transients are recorded.

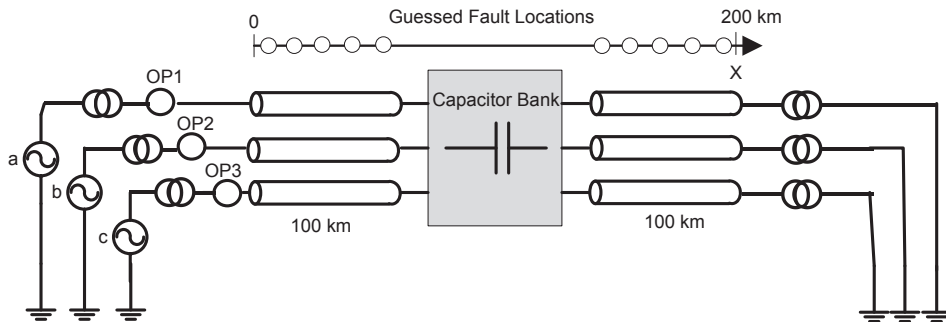
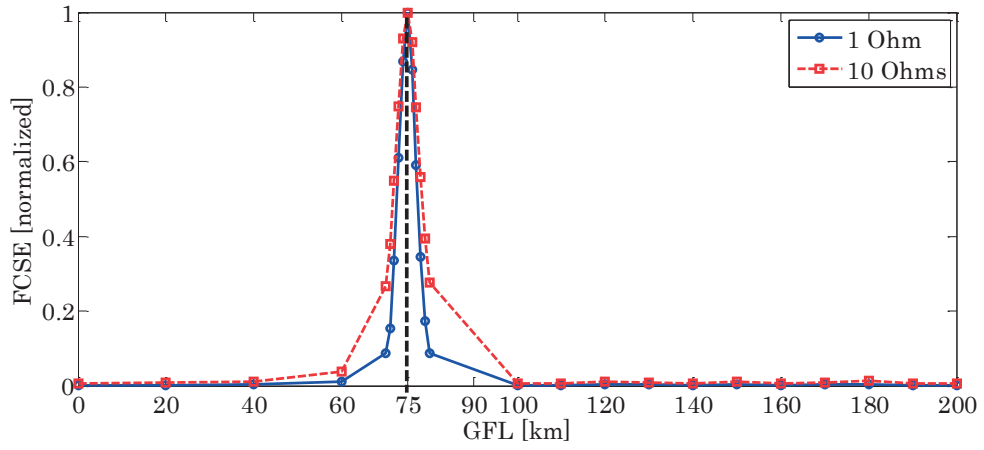


Figure 2.28. Schematic representation of the series-compensated three-conductor transmission line system implemented in the EMTP-RV.

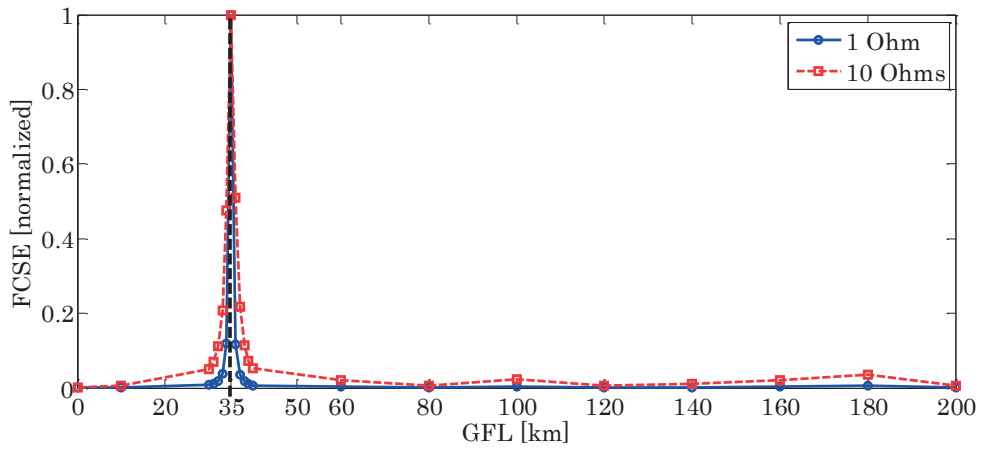
To examine the performance of the proposed method, three fault cases are considered: (i) a three-phase-to-ground fault at  $x_f = 75$  km, (ii) a double phase-to-ground fault at  $x_f = 35$  km and (iii) a single-phase-to-ground fault at  $x_f = 25$  km. All these three fault cases are assumed to be solid faults.

By applying the similar procedure used in the previous application examples, the FCSE is calculated for each fault case. Figure 2.29 (a), (b), and (c) show the energy of the current flowing through the guessed fault points for the three-phase-to-ground fault, double-phase-to-ground fault, and single-phase-to-ground fault, respectively. For each case, the energy values are normalized to the corresponding peak value. These figures illustrate the calculated normalized FCSEs for two a priori guessed values of the fault resistance, namely  $1 \Omega$  and  $10 \Omega$ . In order to evaluate the accuracy of the proposed method, the position of the GFL is varied every 1 km near to the real fault location.

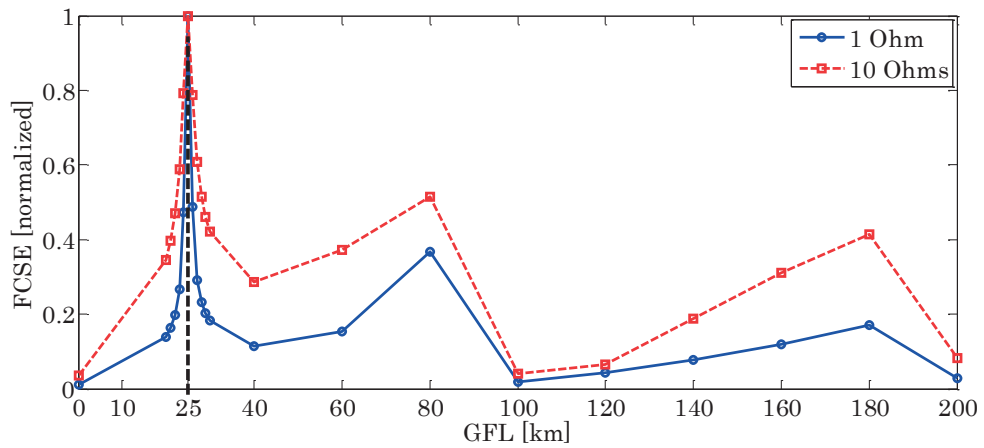
As it can be seen, the proposed method is remarkably effective in identifying the fault location for all the three fault cases even by the presence of the compensator (the maximum peak of the fault current energy is obtained at the real fault location). Additionally, it appears robust against the a priori assumed fault impedance.



(a)



(b)



(c)

Figure 2.29. Normalized energy of the fault current as a function of GFLs and for different guessed fault resistance values (i.e., 1 and 10 Ohms); (a) three-phase-to-ground fault at  $x_f = 75$  km, (b) double-phase-to-ground fault at  $x_f = 35$  km, (c) single-phase-to-ground fault at  $x_f = 25$  km.

## 2.9 Conclusion

In this chapter, first, an overview of the existing fault location methods based on the three general categories is presented. Although numerous fault location methods have already been presented in the literature, the limitations associated with the existing methods (e.g., requirement of the multi-end measurements and complexity due to sophisticated signal processing techniques) is the motivation to study more efficient fault location techniques.

Time reversal theory and in particular, EMTR is explained as a focusing technique to refocus waveforms back to a source. The basic idea of the EMTR is to take advantage of the reversibility in time of the wave equation. The transients observed in specific observation points of the system are time-reversed and transmitted back into the system. The time-reversed signals are shown to converge to the source (fault) location. The EMTR presents several advantages, namely: (i) applicability to inhomogeneous media, (ii) efficiency for systems bounded in space and characterized by a complex topology (in our case, networks with multiple terminations).

Then, the EMTR-based fault location method is proposed by taking advantage of the time reversal invariance of the telegraphers' equations in transmission lines. The applicability of the EMTR technique to locate faults is first presented; then, using transmission line equations in the frequency domain, analytical expressions are derived permitting to infer the location of the fault. A time-domain implementation of the EMTR-based fault location technique is also proposed. The application of the EMTR to locate faults in a power network is carried out in three steps: (1) measurement of the fault-originated electromagnetic transients in a single observation point, (2) simulation of the back-injection of the time-reversed measured fault signal for different guessed fault locations and using the network model, and (3) determination of the fault location by computing, in the network model, the point characterized by the largest energy concentration associated with the back-injected time-reversed fault transients.

As the telegraphers' equations are invariant under a time-reversal transformation only for lossless lines, the impact of the losses on the performance of the proposed fault location method is also discussed. Three different models of back-propagation to address the issue of losses are considered: (i) inverted-loss, (ii) lossless, and (iii) lossy models. It is shown through a numerical example related to a single-wire line above a conducting ground that, as expected, an inverted-loss model for the back-propagation results in a perfect estimation of the fault location. It is also observed that a back-propagation model in which the losses are included results also in a perfect estimation of the fault location, even though in this case the telegrapher's equations are not strictly time-reversal invariant. This can be considered as a very

significant result since it allows the use of traditional approaches to simulate the back-propagation phase during which the time-reversed fault-generated transients are injected into the network.

The proposed method is validated by means of reduced scale experiments considering two topologies, namely one single transmission line and a T-shape network. In both cases, the proposed EMTR-based approach was able to correctly identify the location of the fault. It is worth observing that, these experiments are performed in the presence of the cables losses and measurement noises.

Several validation examples were performed by making reference to different types of power networks including (i) inhomogeneous network composed of mixed overhead-coaxial cable lines, (ii) radial distribution network, (iii) series-compensated transmission line. The resulting fault location accuracy and robustness against uncertainties (e.g., fault impedance, fault type, network topology) have been tested and, in this respect, the proposed method appears to be very promising for real applications.

Compared to other transient-based fault location techniques, the proposed method is straightforwardly applicable to inhomogeneous media that, in our case, are represented by mixed overhead and coaxial power cable lines. A further advantage of the developed EMTR-based fault location method is that it minimizes the number of observation points. In particular, it is shown that a single observation point located at the secondary winding of a substation transformer is enough to correctly identify the fault location. Another important advantage of the proposed method is that its performances are not influenced by the topology of the system, fault type and impedance, and presence of series compensation.



## Improved EMT Simulations Based on Fixed Admittance Matrix Nodal Method

### Summary

This chapter discusses about efficient real-time simulation of EMTs taking place in generic power systems composed of either passive lumped elements, switches, or propagative transmission lines. First, an introduction of EMT simulations with a review of EMT simulation programs in both offline and real-time modes is given.

A brief history of the development of the real-time simulators for EMT applications both in academics and in industry is presented and the need for the development of a new category of simulators (FPGA-based) is highlighted. A summary of existing FPGA-based real-time simulators by making reference to their application targets is presented.

A review of EMT simulation principles is presented. Furthermore, a specific switch model, associated discrete circuit (ADC), used often in the context of FPGA-based real-time simulators is described. By making reference to the ADC switch model, an adapted solver based on the FAMNM is presented. It is shown that, despite the simulations acceleration resulted by using this model, the adopted value for switch conductance in ADC model impacts dramatically the accuracy of the simulation results.

A novel method for the optimal assessment of the ADC model parameter is presented. To prove the correctness of the proposed method, a comparison between the proposed metric and specific defined error functions is presented and discussed. Several validation examples are considered to prove the performance of the proposed method.

### 3.1 Introduction

EMTs are temporary phenomena taking place in power electronics devices or power systems due to switching operations, faults, lightning strikes, lines or other elements energization/ de-energization, and other disturbances. In contrast to electromechanical transient, where the phenomena takes place due to the interaction between the stored mechanical energy in the rotating machines and the electrical energy stored in system, EMT transients are due to the interaction between magnetic fields of inductances and the electric field of the capacitances of the system, or to electromagnetic wave propagation along electrically-long lines. These phenomena cover a wide frequency range, from DC to several MHz and, in general, take place in a short time window (i.e., few hundreds of milliseconds as a function of the system damping) [74]. Figure 3.1 shows the time frame of various transient phenomena taking place in power systems. The fastest natural source of electromagnetic disturbance is lightning [64] with over-voltages characterized by rise-times down to 100 ns or so and with durations of up to millisecond. It is worth noting that faster transients with nanosecond and sub-nanosecond rise-times can be induced by either high-altitude nuclear electromagnetic pulse (NEMP) [75] or using high-power microwave sources (the so-called intentional electromagnetic interferences) [76].

EMTs can damage the insulations or trigger unwanted operation of the protection and control systems. Therefore, these simulations are essential to evaluate the protection and control systems performance when the system is not in the steady state condition [77], [78].

From modeling details point of view, EMT simulations are more sophisticated and detailed compared to other types of simulations in power systems (e.g., power flow, stability analysis, etc.).

Since power networks or power electronic devices are characterized by complex topologies, it is not straightforward to derive closed-form analytical solutions describing their transient behavior. In the past, transient network analyzer (TNAs) were used to conduct EMT studies [74]. Although TNAs were allowing interesting EMT studies, their usage was complex and expensive limiting their scalability and applicability for complex topologies. Therefore, digital simulation tools have been introduced to conduct EMT studies by using discretized models of the system. In contrast to the TNA, digital EMT simulators are not able to provide continues behavior of the simulation variables and they only provide a sequence of snapshots at discrete time steps  $\Delta t$ .



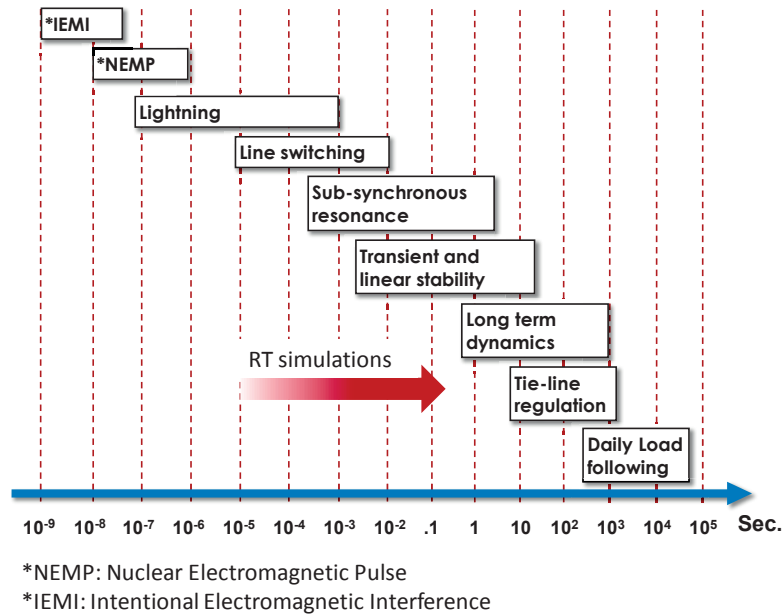


Figure 3.1. Time frame of various transient phenomena (adapted from [74]).

Simulation time step ( $\Delta t$ ) defines the discretization of the continuous network elements and is determined based on the highest EMT frequency in the simulated network. In general, lower  $\Delta t$  results in higher simulation results accuracy and the possibility to simulate faster transients.

Digital EMT simulations can be conducted in offline or in real-time mode. The main purpose of real-time simulations is their ability to be coupled with physical protection and control devices due to the real-time response of the simulated systems. Such hardware-in-the-loop (HIL) tests are not possible to be performed by offline simulators.

Electromagnetic transients program (EMTP) is the most widely used offline EMT simulation platform [67], [79]. Based on the method proposed in [67], [80], the continuous models of the lumped elements are discretized by a numerical integration method (e.g., backward-Euler, trapezoidal). Then, by using nodal analysis (modified nodal analysis, or augmented-modified nodal analysis) methods, the time-domain nodal equations of the network are derived and solved. Therefore, the differential equations describing the time-domain behavior of the elements are simply represented by algebraic equations. The other approach is to use state-space method to represent the differential equations governing the system. However, EMTP-based programs are mostly used one due to simplicity of the solver and its robustness and stability. There are several EMTP-based simulation environments with different features e.g.: ATP<sup>®</sup>, EMTP-RV<sup>®</sup>, PSCAD/EMTDC<sup>®</sup>, MICROTRAN<sup>®</sup>, etc. The historical perspective of the EMT-based offline simulation platforms is presented in [74].

It is worth observing that, due to the non-real-time feature of the offline simulators, the computation time is not the major constraint. Therefore, the simulated networks can be represented by very detailed and accurate models with higher level of complexity. Thus, in order to simulate a very short time window of a system variable, much higher computation time might be required.

Real-time simulators are specific simulation platforms which are able to replicate, in real-time, the exact behavior of the system under study. More specifically, it is a simulation that all the involved tasks (namely, reading inputs, model computations, and sending outputs) have to be performed within each specific simulation time-step. This peculiarity enables coupling physical control and protection systems with the simulated network in order to test and verify their functionality by means of HIL tests. Moreover, these simulators are used to perform repetitive and time-consuming simulations, such as statistical studies, to reduce the overall simulation time. The schematic representation of the digital real-time simulator and HIL is shown Figure 3.2. In what follows, a survey of the digital real-time simulators is presented.

### 3.2 State-of-the-Art of the RTSs for Power Electronics and Power Systems

The first digital real-time simulator was proposed in 1980s by Mathur and Wang in [81] for the real-time simulation of power networks by adapting the so-called Bergeron's constant parameters (CP) transmission line model. The developed digital real-time simulator was based on the single-chip NEC's PD77230 digital signal processor (DSP) and was interfaced with a TNA replacing the bulk network. Then, this work was extended by using frequency dependent lines [82]. A digital real-time simulator for protective relays testing was proposed in [83]. The proposed simulator was based on the IBM RISC 6000 processor to simulate power networks transients. Dual-DSP architecture was proposed in [84], [85] for the real-time simulation of transmission lines using Marti's frequency dependent line model [86].

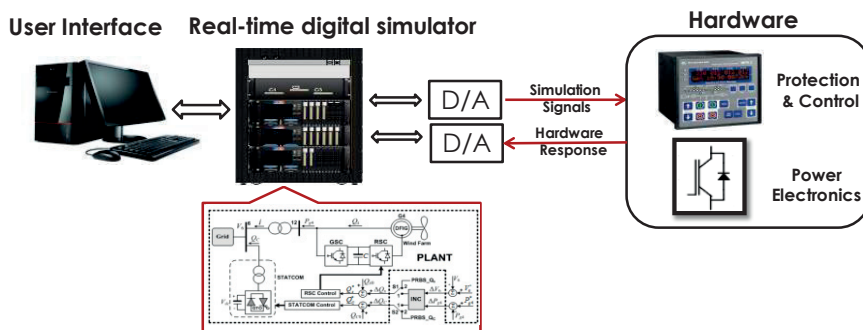


Figure 3.2. Schematic representation of HIL test by means of RTDS.

In the proposed architecture, each DSP simulates one end of the transmission lines and the data of the both ends are exchanged via a shared memory.

The idea of using standard workstations to develop a digital real-time simulator was presented in [87]. The proposed digital real-time simulator was based on the IBM RISC System/6000 Model 560 workstation using superscalar computer architecture. Timing ranging from 38 to 107  $\mu$ s were obtained for systems from 18 to 30 nodes. This performance was achieved by partitioning a large network to smaller sub-systems using the transmission lines decoupling feature. Later on, PC clusters were shown as a cost effective and extensible architecture for real-time simulation of power systems [88], [89], [90]. In this architecture, the power network is clustered and distributed over PC clusters that are interconnected by low latency interface cards.

Besides the extensive research on the development of more accurate and faster digital real-time simulators, high-speed analog emulators dedicated for computing the dynamic and transient power system phenomena have been also proposed in the literature (e.g., [91], [92]). Such emulators are mainly dedicated for the small signal and transient stability analysis.

Furthermore, commercial digital real-time simulators products are also developed and utilized by researchers and utilities. Some of the commercial digital real-time simulators are listed below.

**RTDS®**: The first commercial digital real-time simulator, aimed at control and protection systems test, was developed in RTDS Technologies Inc. in 1991 [93], [94]. The latest RTDS is composed of several racks, each one consisting of several Giga processor cards (GPC) powered by IBM RISC processors [95].

**HYPERSIM®**: developed by Hydro-Quebec and is based on multi-core super computers [96], [97]. It is able to simulate very large-scale power systems with more than 2000 three-phase buses.

**eMEGAsim®**: developed by OPAL-RT Technologies Inc. [98], [99] and is based on commercial-off-the-shelf (COTS) multi-core processor (Intel or AMD) module along with fast on-chip inter-processor shared-memory communication. The possibility of using MATLAB®, Simulink SimPowerSystems model libraries simplifies the model development and is able to simulate large distributed systems with up to 600 nodes.

**ARENE®**: developed by Électricité de France and is able to simulate high-frequency phenomena in a standard, multipurpose parallel computer [100].

The above-mentioned simulators are mainly based on DSP or general purpose CPU-based platforms where the real-time simulation is achieved by partitioning

the large networks into smaller sub-systems and process them in parallel. The partitioning is generally done by using travelling time delays of the transmission lines and each decoupled sub-system is simulated in the dedicated processing unit. After each simulation time step, transmission line data are exchanged between processing units [87]. Therefore, the minimum simulation time step is a function of partitioning method, number and speed of the processors, and the latency of communication links. For the conventional digital real-time simulators, the minimum achievable real-time simulation time step is in the range of few tens of microseconds. The main reason for this relatively large simulation time step is due to the partial sequential operations that the CPU architectures need to deploy. The growing complexity of the power systems and power electronic devices and the need for an accurate EMT simulations of high-frequency phenomena requires higher frequency bandwidth of the real-time simulators. The relatively large simulation time steps required by these simulators do not allow to represent in real-time high-frequency phenomena such as EMTs in power converters or travelling wave transients taking place in transmission lines (e.g., fault and switching transients). As an example, simulation of power converters with high switching frequencies is a serious challenge due to the “within simulation time step switching” which is the consequence of the asynchronism between the external controller and the simulated converter [101]. Therefore, very small simulation time steps are required to avoid sophisticated corrective measures to reduce the error associated with the “within simulation time step switching”. As a consequence, there is a need to utilize different hardware architecture to comply with the constraints associated with the real-time simulation of complex systems [101], [102], [103].

Field programmable gate array (FPGA) is a suitable alternative to be used as a real-time simulator computational core. The main advantage of FPGA over CPU or DSP is its hardwired parallel processing that enables the implementation of specific methodologies that dramatically reduce the sequencing of the operations taking place in CPUs or DSPs. Furthermore, in FPGAs the latency associated with the import/export of the I/Os are lower compared to the CPUs. Finally, FPGAs are fully configurable chips, which allow to be configured for specific applications. These peculiarities make FPGA a suitable alternative to CPUs or DSPs [102], [103].

During the past years, the size and computational power of FPGAs have been increased dramatically. As a consequence, FPGA-based real-time simulation has emerged as a leading trend for EMT real-time simulations, in particular, for the power electronics applications (e.g., [104], [105], [106], [107]). Figure 3.3 shows the evolution of real-time simulation technologies.

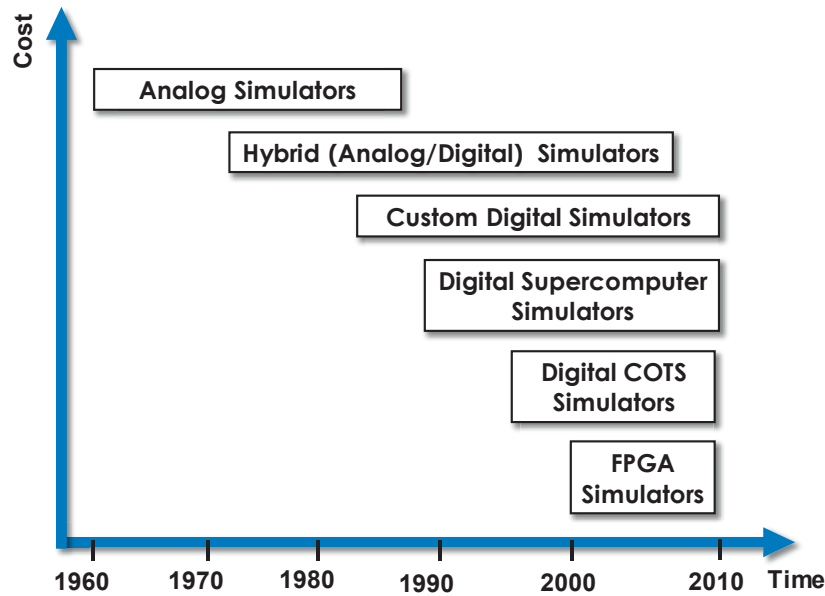


Figure 3.3. Evolution of Real-Time Simulation Technologies (adapted from [108]).

The first application of FPGAs for modeling a complete AC drive system was presented in [109] in which the digital hardware realization of a real-time simulator for an induction machine drive was proposed.

Hardware description language (VHDL) was used and by adapting a particular device-characteristic model suitable for FPGA implementation, a 2-level 6-pulse IGBT-based voltage-source converter (VSC) was implemented in Altera Stratix EP1S80 FPGA.

An FPGA-based real-time EMTP simulator was proposed in [102] which takes into account a distributed-parameter transmission line model and by using Altera Stratix S80 FPGA, the proposed simulator is able to simulate a power network composed of 15 transmission lines and 16 nodes in 960 FPGA clock cycles.

In [101], Matar and Iravani proposed an FPGA-based real-time simulation platform for power electronics applications. They use the ADC model to represent the switches and the considered application examples referred to a two-level three-phase voltage source converter and a diode-clamped three-level voltage source converter. In [104], the same authors extended the application of their proposed method to the case of three-phase AC machines. Very similar method presented in [101] was presented again in [110] for controller hardware-in-the-loop (CHIL) tests. The implemented system was a two-level voltage source converter and the simulation time step was 500 ns. The validation was done by comparing the FPGA-based CHIL results with offline simulations performed in MATLAB/Simpowersystems.

An FPGA-based real-time simulator for power electronic devices based on a realistic device-level behavioral model was presented in [111], in which the nonlinear IGBT characteristic was considered allowing a more realistic simulation of switching devices. To this end, the switching characteristics of an IGBT module were extracted from an experimental setup. Then, the measured per-unit characteristics were implemented in the ALTERA Stratix EP1S80F FPGA. Three-level VSC together with an induction machine was considered as a validation case study.

A state-space modeling approach for an FPGA-based real-time simulation of the power converters was presented in [112]. A new switch model, in state-space domain, was proposed and implemented in the FPGA-based real-time simulator for power electronic devices with high switching frequencies. Two case studies were considered: a boost converter, and a two-level three-phase converter. For the latter case, the simulator needs 16 FPGA clock cycles to perform one simulation loop. The FPGA real-time simulation results were validated using as reference SPICE simulations.

A high performance FPGA-based floating-point calculation engine aimed for the real-time simulation of power electronic circuits was presented in [107]. The performance of the proposed method was evaluated by three different topologies: a boost converter, a two-level three-phase bridge, and a two-level-three-phase bridge driven by a boost converter. The proposed simulator was able to reach time steps below  $1 \mu\text{s}$  together with very good simulation accuracy.

In [105], Matar and Iravani extended their proposed methodology to the EMT simulations of power systems. Based on the concept of hardware reconfigurability, a reconfigurable-hardware real-time power system simulator (RH-RTS) was proposed and verified by a test system composed of 14 buses and 17 transmission lines. However, the grid was partitioned into an external zone and a study zone. The external zone included 12 buses and 14 transmission lines and was represented by the so-called M-TLINE equivalent which mimics its frequency response. Therefore, only 3 transmission lines were represented by a detailed model.

Besides the extensive research on the development of the FPGA-based EMT real-time simulators, recently, a few industrial FPGA-based real-time simulator, mainly dedicated for the power electronics HIL tests were made available:

**eFPGAsim®**: developed by OPAL-RT Technologies Inc. [106], [113]. By adapting a specific solver (eHS), it is able to simulate power electronic devices and HIL tests within less than  $1 \mu\text{s}$  of simulation time step. It uses ADC switch model and adapts fixed admittance matrix nodal method (FAMNM) to keep the nodal admittance matrix unchanged during switching transitions.

**Typhoon HIL®**: provides high fidelity real-time emulators for HIL testing using a specific solver [114], [115].

Although FPGA-based real-time simulators provide several advantages compared to the CPU-based ones, their applications are characterized by some limitations. One of the main drawbacks of the FPGA-based simulators is their difficult programming associated with the use of HDL. This low-level programming limits the scalability of solvers and, as a consequence, the representation of complex models. Additionally, any modification in the implemented algorithm/model requires, in general, a time-consuming recompilation of the HDL code.

Another challenging issue regarding this type of simulators is the limitation in the matrix manipulation and, as a consequence, the inherent difficulty to represent switching maneuvers. In this respect, the most straightforward method to represent topology-variable circuits in FPGA real-time simulators is the so-called FAMNM [106]. This method, irrespective of the number of the switches and their states, allows for obtaining a fixed nodal admittance matrix during switching transitions. However, it introduces artificial oscillations and errors in the simulation results (e.g., [116]).

It is worth mentioning that a few automated FPGA-based real-time simulators have been proposed to avoid the difficulties of the FPGAs programming (e.g., [113], [115]). However, the application of these simulators is mainly dedicated to power electronics HIL simulations. Therefore, these studies do not allow the simulation of power networks including propagative transmission lines. Furthermore, the adapted switch model in FAMNM-based solvers might introduce artificial resonances and simulation errors, which are not taken into account.

In this chapter, a methodological approach is presented to improve the FAMNM-based solvers. Then, the developed approach is used in the proposed FPGA-based real-time simulation platform to develop an efficient and accurate real-time solvers. The implementation of the proposed simulator will be presented in Chapter 4. In the following section, a review of EMT simulation principles is presented.

### 3.3 Review of the EMT Simulation Principles

As described earlier, the digital computation enabled accurate and fast EMT simulation of the power systems and power electronic devices. Due to the discrete computation characteristic of computers, the main task in digital simulation is the development of suitable methods for the solution of the differential and algebraic equations, describing system behavior, at discrete time steps [74]. In general, there are two main types of methods used in power systems and power electronic

applications: (i) state-space method, and, (ii) nodal analysis [74], [77], [78]. This section synthesizes known aspects related to the numerical simulation of electrical circuits. Although it does not contain original material, it serves to introduce modeling approaches and the nomenclatures used in the next sections.

#### 3.3.1 State-Space Method

In the state-space method, the mathematical model of the system is represented by a set of variables indicating inputs/outputs and state variables. The method describes first order differential equations of the state variables as a function of input/outputs and the state variables. State-space equations, in general form, are given by [74]:

$$\begin{aligned}\dot{x} &= Ax + Bu \\ y &= Cx + Du\end{aligned}\tag{3.1}$$

where  $x$  is the vector of states and  $u$  is the vector of inputs.  $C$  and  $D$  matrices are used to obtain the vector of outputs  $y$ . This method is the most popular for the numerical integration of differential equations, due to its simplicity and lack of overhead for variable time-step solvers [74]. It is used in MATLAB/Simulink which is a general purpose simulation environment. SimPowerSystems toolbox provides a programming environment for the EMT simulations and it can be interfaced with the standard MATLAB programming environment for flexible design and testing of the control systems.

However, the construction of equation (3.1) is not straightforward and requires considerable effort. Furthermore, the representation of non-linear elements is not simple [78].

#### 3.3.2 Nodal Analysis

As described in the introduction, EMTP was the first and the most common tool for the EMT simulations. EMTP-based simulators use nodal analysis approach. The nodal analysis method is based on the equilibrium of the injected currents at each node. These equations are described by [67], [80]:

$$Y_n v = i\tag{3.2}$$

where  $Y_n$  is the nodal admittance matrix (NAM),  $v$  is the unknown node voltages, and  $i$  is the vector of injected currents. This representation assumes that all network components can be given an admittance matrix model. One of the main drawback of this representation is its inability to consider ungrounded voltage sources [69]. This problem was solved by using modified nodal analysis (MNA) by



considering an extra row for the voltage source equations and an extra column for the voltage source current. Although MNA provides a more general description of a given circuit, there are still limitations due the assumption of admittance model for every component. As an example, the ideal switch does not have an admittance model representation since the open or closed states change the nodal admittance matrix rank [69]. To overcome this limitation, a new formulation is proposed by considering more general representation of elements [69]. The new formulation is called Modified Augmented Nodal Analysis (MANA) and described as [69]:

$$\underbrace{\begin{bmatrix} Y_n & V_c & D_c & S_c \\ V_r & V_d & D_{VD} & S_{VS} \\ D_r & D_{DV} & D_d & S_{DS} \\ S_r & S_{SV} & S_{SD} & S_d \end{bmatrix}}_{ANAM} \begin{bmatrix} v_n \\ i_V \\ i_D \\ i_S \end{bmatrix} = \begin{bmatrix} i_n \\ v_b \\ d_b \\ s_b \end{bmatrix} \quad (3.3).$$

The augmented nodal admittance matrix (ANAM) includes the NAM ( $Y_n$ ) and other sub-matrices describing additional equations associated with different elements. The method is used in EMTP-RV simulation environment.

The main advantage of MNA (MANA) is the straightforward procedure to extract the NAM (ANAM). However, compared to the state-space method, the implementation of variable time step solvers is more sophisticated [78].

It is worth observing that, in view of the FPGA-based real-time simulation context, fixed time-step solvers are preferred (this hypothesis is required by the fact that FPGA systems work with a fixed clock and, usually, elaborate signals sampled at a fixed frequency). Therefore, the majority of the proposed solvers adapt MANA (e.g., [102], [101], [104], [106], [117]). In this research, we use MANA as the network solution method.

In order to form (3.3) and solve it, network elements have to be represented by their discrete-time model (i.e., the continuous functions are discretized by numerical integration methods).

### 3.3.3 Numerical Integration Methods

Various numerical integration methods can be used to discretize and solve differential equations where the accuracy of the solution depends on the step size and the selected integration method. A numerical integration method provides an approximate solution of a continuous system and the selection of a proper method has to be done by taking into account its accuracy, stability, and computational efficiency. Concerning EMT simulations, the most common approaches are [118],

[119]: (i) forward-Euler (FE) method, (ii) backward-Euler (BE) method, (iii) trapezoidal method, and (iv) Gear's second-order method.

FE and BE are first-order approximation methods. FE is based on the linear approximation of the function being integrated. Let us consider the following differential equation:

$$\frac{dx}{dt} = f(x, t) \quad (3.4).$$

As known, the associated Taylor series of the function  $x(t)$  is given by:

$$x_{n+1} = x_n + \frac{\Delta t}{1!} f(x_n, t_n) + \frac{(\Delta t)^2}{2!} f'(x_n, t_n) + \frac{(\Delta t)^3}{3!} f^{(2)}(x_n, t_n) + \dots + \frac{(\Delta t)^n}{n!} f^{(n)}(x_n, t_n) + O((\Delta t)^n) \quad (3.5)$$

FE is the expansion of the first two terms of the Taylor series, namely:

$$x_{n+1} \cong x_n + \Delta t f(x_n, t_n) \quad (3.6)$$

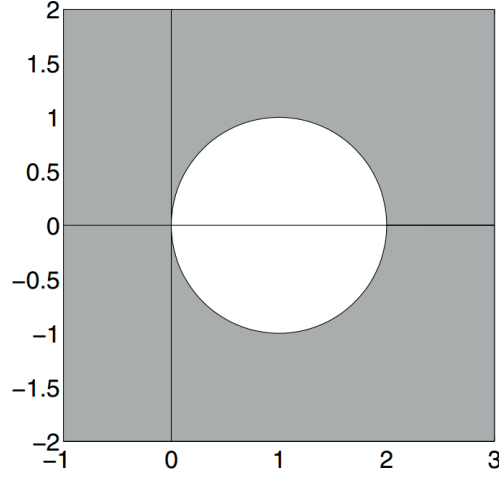
where  $\Delta t$  is the discretization time step. Since the FE is derived based on the truncation of the Taylor series, at each time step, there is an error referred to as the local truncation error (LTE). LTE is the difference between the numerical solution and the exact solution at a given time. To analyze the LTE of FE, one can compare (3.6) with the Taylor expansion of (3.5). Therefore, the LTE is given by:

$$\text{LTE} = \frac{(\Delta t)^2}{2} f^{(2)}(x_n) + O((\Delta t)^3) \quad (3.7).$$

From (3.7) it can be observed that, for a small time step, the LTE is approximately proportional to  $(\Delta t)^2$ . Furthermore, higher order methods provide lower LTE. FE is an explicit numerical integration method which calculates the state of a system at a later from the state of the system at the current time without the need to solve algebraic equations. However, the explicit methods are known to be less stable than implicit solvers due to their cumulative integration errors [120]. Therefore, FE is modified in order to have an implicit form and called BE method, which is given by:

$$x_{n+1} \cong x_n + \Delta t f(x_{n+1}, t_{n+1}) \quad (3.8).$$

Similar to the FE, the BE local truncation error is approximately proportional to  $(\Delta t)^2$ . The region of the absolute stability of the BE method is the complement in the complex plane of the disk with radius 1 centered at 1 [121], shown in Figure 3.4.



**Figure 3.4. Stability region of BE method (adapted from [121]).**

Compared to the first-order numerical integration methods, second-order methods provide less LTE. Among them, the trapezoidal method is the most common adopted for the EMT simulations [67], [118]. In principle, trapezoidal method is the average of the FE and BE methods and it involves the summation of a successive number of trapezoidal regions which approximate the integral of a function [119].

Therefore, the solution of (3.4) is given by:

$$x_{n+1} = x_n + \frac{\Delta t}{2} [f(x_n, t_n) + f(x_{n+1}, t_{n+1})] \quad (3.9).$$

As expected, the trapezoidal method is characterized by a lower LTE compared to FE and BE methods:

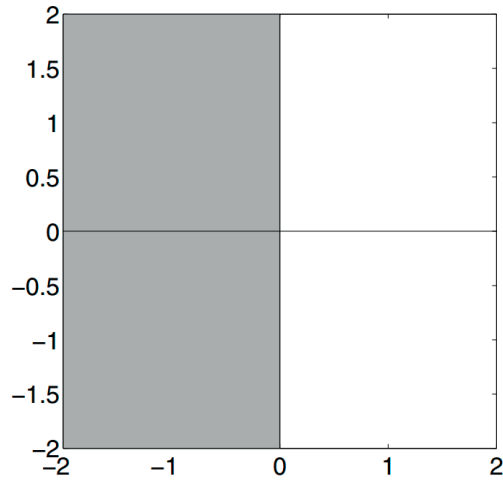
$$\text{LTE} \leq \frac{(\Delta t)^3}{12} \max |f^{(3)}(\zeta)| \quad (3.10)$$

The region of absolute stability of the trapezoidal method is the left half of the complex plane as shown in Figure 3.5.

The Gear's second order method is expressed as:

$$x_{n+1} \cong \frac{4}{3}x_n - \frac{1}{3}x_{n-1} + \Delta t \left[ \frac{2}{3}f(x_{n+1}, t_{n+1}) \right] \quad (3.11).$$

Concerning real-time simulation applications, three multiplications and two additions are required by the Gear's second order method. Moreover, it is necessary to store two past values from the previous two time-steps. These complexities limit its applications for the real-time EMT simulations.



**Figure 3.5. Stability region of trapezoidal method (adapted from [121]).**

Compared to the BE method, the trapezoidal method has a lower LTE and provides better approximation of the integrated function. Nevertheless, it requires more algebraic operations compared to BE. Furthermore, for the EMT simulations, specifically, for the case of switching devices, solutions based on the trapezoidal method might suffer from sustained oscillations [79], [118]. To overcome the instability problem of the trapezoidal method, in EMTP-RV simulation software, there is a possibility to select the trapezoidal and BE integration option in which, the solver is based on the trapezoidal method and it switches to BE at discontinuities.

It is worth noting that, it is possible to obtain the same simulation accuracy of the trapezoidal method using the BE method, by considering one order of magnitude smaller simulation time steps [118]. This is completely feasible by using FPGA-based real-time simulators, since the simulation time steps are very low compared to the CPU-based simulators. Therefore, considering its better stability and damping characteristic, we will adopt the BE method in the proposed solver.

### 3.3.4 EMT simulation Models for Network Elements

Using MANA as the network solution method and BE as the numerical integration technique, the network elements consisting of lumped elements, switches, and transmission lines are represented by their discrete-time models.

#### 3.3.4.1 Lumped Elements

In view of the use of the MANA as network modeling method, lumped elements ( $R$ ,  $L$ ,  $C$ ) are discretized and represented by their companion models [74], [67].

The discrete-time model of a resistance  $R$  is the same as its continuous-time model. The voltage and current relationship, for a resistance connected between nodes  $k$  and  $m$ , in continuous and discrete time modes are given by (3.12) and (3.13), respectively.

$$v_{km} = Ri_{km}(t) \quad (3.12)$$

$$v_{km}^{n+1} = Ri_{km}^{n+1} \quad (3.13)$$

where  $n+1$  denotes current simulation time step.

The differential equation for an inductance  $L$ , connected between nodes  $k$  and  $m$ , is

$$v_{km}(t) = L \frac{di_{km}(t)}{dt} \quad (3.14).$$

The inductor current is described by

$$i_{km}(t) = i_{km}(t - \Delta t) + \frac{1}{L} \int_{t-\Delta t}^t v_{km} dt \quad (3.15).$$

Applying the BE method yields

$$\begin{aligned} i_{km}(t) &= i_{km}(t - \Delta t) + \frac{\Delta t}{L} v_{km}(t) \\ &= I_h(t - \Delta t) + \frac{1}{R_{eq}} v_{km}(t) \end{aligned} \quad (3.16).$$

Therefore, an inductor can be represented by a companion model which is composed of an equivalent resistance in parallel with a current source [74].

Similar to an inductor, the companion model for a capacitor can be derived. The differential equation for a capacitor  $C$ , connected between nodes  $k$  and  $m$ , is

$$i_{km}(t) = C \frac{dv_{km}(t)}{dt} \quad (3.17)$$

The capacitor voltage is described by

$$v_{km}(t) = v_{km}(t - \Delta t) + \frac{1}{C} \int_{t-\Delta t}^t i_{km} dt \quad (3.18).$$

Applying the BE method yields

$$\begin{aligned}
 v_{km}(t) &= v_{km}(t - \Delta t) + \frac{\Delta t}{C} i_{km}(t) \\
 i_{km}(t) &= -\frac{C}{\Delta t} v_{km}(t - \Delta t) + \frac{C}{\Delta t} v_{km}(t) \\
 &= I_h(t - \Delta t) + \frac{1}{R_{eq}} v_{km}(t)
 \end{aligned} \tag{3.19}$$

Therefore, a capacitor can be also represented by a companion model which is composed of an equivalent resistance in parallel with a current source. The summary of the companion models of the lumped elements and the corresponding values are depicted in Figure 3.6 and Table 3.1. For the case of  $RL$ ,  $RC$ ,  $LC$ , and  $RLC$  branches, the model elements can be combined allowing components reduction (see [74] for more details).

### 3.3.4.2 Transmission Lines

For the EMT simulations of transmission lines, distributed-parameter line models are required to accurately simulate travelling wave propagation along the lines. Among the time-domain transmission line models, the Bergeron model (constant-parameter model), frequency-dependent (FD) line model [86], and universal line model (ULM) [122] are the most common ones.

The FD line model is presented by using the rational function approximations of the characteristic admittance and propagation wave functions [123], [86]. These rational function approximations are computed based on the Bode's asymptotic fitting (BAF) of the magnitude of the line functions using only real negative poles and zeros. For the case of multi-conductor transmission lines, a single real transformation matrix is used to convert modal and phase quantities. This model has been widely used in EMTP programs (e.g., EMTP-RV, PSCAD/EMTDC).

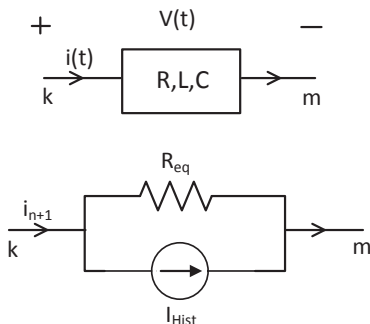


Figure 3.6. Lumped elements (R, L, C) and relevant companion model.

Table 3.1. Companion models parameters associated with RLC elements.

Element	$R_{eq}$	$I_{Hist}$
Resistor	$R$	-
Inductor	$\frac{L}{\Delta t}$	$i_n$
Capacitor	$\frac{\Delta t}{C}$	$-\frac{C}{\Delta t} v_n$

ULM was proposed to improve the accuracy of the FD line model [122]. This model takes into account the complex poles and zeros in the rational-function approximations and uses frequency-dependent transformation matrices by fitting them over the frequency range of the model using rational function approximations of the idempotent coefficients. As a consequence, both the real and imaginary parts of the propagation and characteristic admittance functions are fitted. Although, ULM uses more detailed line model, it requires considerable computational effort, which adds non-negligible complexity for the simulation algorithm. Furthermore, the numerical stability of this model might not be guaranteed and special considerations need to be taken into account to guarantee passivity [124]. Therefore, the application of ULM is limited for real-time simulations applications.

The most straightforward transmission line model for real-time applications is the so-called Bergeron model [125]. This model was first introduced as a graphical method for calculating transients in penstocks. Then, Dommel applied the method to EMT simulations in transmission lines [67]. This model allows a simple representation of constant parameters (CP) transmission line models and it is based on a circuit representation of the telegraphers' equations where each line termination is replaced by means of a lumped impedance in parallel with a controlled current source. In view of FPGA-based real-time simulation, CP line model allows straightforward and accurate simulation of travelling wave propagations in transmission lines.

In order to describe this model, let us assume a transmission line connecting node  $k$  to node  $m$  and propagation of a wave from nodes  $k$  to  $m$ , as shown in Figure 3.7. The wave propagation equations by neglecting the losses are [74]:

$$-\frac{\partial v(x,t)}{\partial x} = L' \frac{\partial i(x,t)}{\partial t} \quad (3.20)$$

$$-\frac{\partial i(x,t)}{\partial x} = C' \frac{\partial v(x,t)}{\partial t} \quad (3.21)$$

where  $v(x,t)$  and  $i(x,t)$  are voltage and current in position  $x$  of the line and  $L'$  and  $C'$  are the per-unit length inductance and capacitance of the line. The solution of these equations, after some manipulations [74], for line terminals voltages and currents can be written as:

$$i_{km}(t) = \frac{1}{Z_C} v_k(t) - I_k(t - \tau) \quad (3.22)$$

$$i_{mk}(t) = \frac{1}{Z_C} v_m(t) - I_m(t - \tau) \quad (3.23)$$

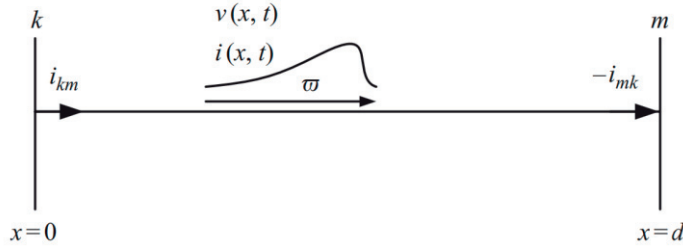


Figure 3.7. Single line representation of a single conductor transmission line connecting nodes  $k$  and  $m$  (adapted from [74]).

where  $Z_c$  is the characteristic impedance of the line and  $\tau$  is the wave propagation time along the line.

$$Z_c = \sqrt{\frac{L'}{C'}} \quad (3.24)$$

$$\omega = \frac{1}{\sqrt{L'C'}}, \quad \tau = d/\omega \quad (3.25).$$

The current history terms are described by:

$$I_k(t-\tau) = \frac{1}{Z_c} v_m(t-\tau) + i_{mk}(t-\tau) \quad (3.26)$$

$$I_m(t-\tau) = \frac{1}{Z_c} v_k(t-\tau) + i_{km}(t-\tau) \quad (3.27).$$

The above-mentioned formulations refer to the case of a lossless line. Losses can be included by adding a lumped resistance. This resistance is divided into three sections, two of them at the ends and one in the middle of the line. The equivalent Bergeron model for a lossy line is shown in Figure 3.8. In this model, voltages at the beginning and at end of the line are functions of the respective current and a current source which are described by (3.28) and (3.29) where  $R$  is total loss of the line [74], [67].

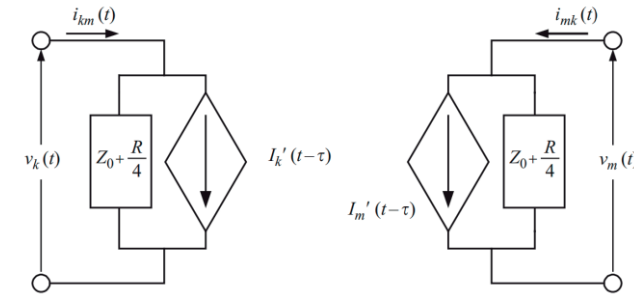


Figure 3.8. Bergeron transmission line model (adapted from [74]).



$$I_k(t-\tau) = \frac{Z_C}{(Z_C + R/4)^2} [v_m(t-\tau) + (Z_C - R/4)i_{mk}(t-\tau)] + \frac{R/4}{(Z_C + R/4)^2} [v_k(t-\tau) + (Z_C - R/4)i_{km}(t-\tau)] \quad (3.28)$$

$$I_m(t-\tau) = \frac{Z_C}{(Z_C + R/4)^2} [v_k(t-\tau) + (Z_C - R/4)i_{km}(t-\tau)] + \frac{R/4}{(Z_C + R/4)^2} [v_m(t-\tau) + (Z_C - R/4)i_{mk}(t-\tau)] \quad (3.29).$$

For multiconductor transmission lines, the same approach can be applied by replacing the scalar voltages and currents by vectors and also replacing the scalar capacitance and inductance with matrices in equations (3.30) and (3.31):

$$-\left[ \frac{dv_p}{dx} \right] = [Z'_p][i_p] \quad (3.30)$$

$$-\left[ \frac{di_p}{dx} \right] = [Y'_p][v_p] \quad (3.31)$$

where,  $[v_p]$  and  $[i_p]$  are the phase voltage and current vectors, while  $[Z'_p]$  and  $[Y'_p]$  are respectively the longitudinal impedance and the transverse admittance matrices of the multiconductor line. Making reference to eigenvalue (modal) theory, it is possible to transform the two equations from phase domain to the modal domain. This allows decoupling the equations so that they could be solved independently. To this end, transformation matrices are needed to transform the phase quantities to modal ones:

$$[v_p] = [T_v][v_m] \quad (3.32)$$

$$[i_p] = [T_i][i_m] \quad (3.33)$$

where,  $[v_m]$  and  $[i_m]$  are modal voltages and currents, and  $[T_v]$  is the transformation matrix for phase voltages and  $[T_i]$  is the one for the phase currents.

For an  $n$ -conductor transmission line, there are  $n$  natural modes and for each mode, Bergeron equations (3.26), (3.27) can be solved separately where any given mode has its own characteristic impedance and travelling speed. It is worth noting that for a CP model, the transformation matrix is real, and is calculated at a given model frequency [67].

### 3.3.4.3 Switches

Accurate and efficient switch modeling is a challenging task for EMT simulators, especially when real-time constraints need to be achieved. Detailed switch models reproducing their physical properties are used when studying phenomena such as switching losses, arcing times and electromagnetic transients associated with switching arc extinction. However, in many power systems applications, these sophisticated models cannot be used because of their required computational efforts and complexity of implementation. Therefore, behavioral switch models have been proposed for EMT real-time applications [126].

One of the most popular methods consists in representing switches as lumped electrical components. The simplest approach is the so-called two-valued resistor model where two resistors, characterized by large differences of their resistance values, are associated with each state of the switch. The typical representation consists in replacing the switch by a resistor characterized by a “small” value of resistance for the “closed-state” and a “large” value for the “open-state”. However, in this case, the system’s admittance matrix needs to be updated and re-factorized after each switching state change, generating major issues to satisfy the FPGA computational time constraints [127].

Within the context of real-time simulations, updating the admittance matrix imposes additional computational burden to solution algorithms that need to be executed within a determined time window. As a consequence, the admittance matrix re-factorization represents a major obstacle to satisfy the computational constraints.

A possible approach to circumvent this problem is the use of modeling techniques that keep the system admittance matrix constant. To this end, discrete circuit models, or associated discrete circuit (ADC), for switching devices were proposed in [128], [129], [130]. The basic idea is that the switch could be represented by a relatively small inductance when its state is ‘closed’ and by a relatively small capacitance when its state is ‘open’. As a consequence, the ADC switch model is represented by an equivalent conductance ( $G_s$ ) in parallel with a controlled current source (e.g., [130]).

The schematic of the ADC switch model is shown in Figure 3.9. In order to set the value of the conductance for both switch states, in case the BE numerical integration method is used, the following constraint should be satisfied:

$$G_s = \frac{C_s}{\Delta t} = \frac{\Delta t}{L_s} \quad (3.34)$$

where  $C_s$  and  $L_s$  are the discrete-time switch capacitance and inductance respectively, and  $\Delta t$  is the simulation time-step. For other numerical integration

methods, a similar approach could be applied to relate  $G_s$  to the switch capacitance and inductance. It is worth observing that equation (3.34), with different analytical forms, holds also in case other numerical integration techniques are used [130].

As a consequence of this representation, the relevant model is composed of a constant conductance in parallel with a current source (see Figure 3.9). As a function of the switch on/off state, the value of the current source ( $j_s^{n+1}$  in Figure 3.9) is updated at each time-step based on the switch current/voltage.

The advantage of this method is that the value for the switch conductance  $G_s$  is fixed irrespective of the switch on/off state. As a result, the nodal admittance matrix will remain unchanged during switching operations as the switch state only affects the value of the shunt current source. The current source associated with the switch at the simulation step  $n+1$  is defined as [130]:

$$J_s^{n+1} = \begin{cases} -i_s^n & s^{n+1} = 1 \\ G_s v_s^n & s^{n+1} = 0 \end{cases} \quad (3.35)$$

where  $s^{n+1}$  is the switch state at the current time step. The way a switch status is updated depends on the device type. For the ideal switch, the current state is the command given to the switch and for IGBT-diode pair, the current state of the switch is given by the Boolean expression [130]:

$$s^{n+1} = c^{n+1} + s^n (i^n \leq 0) + s^n (v^n < 0) \quad (3.36).$$

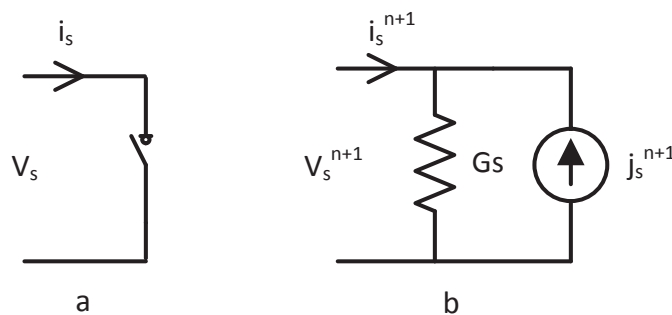


Figure 3.9. ADC switch model (adapted from [130]).

## 3.4 Optimal Assessment of the ADC Switch Model Used by FAMNM

### 3.4.1 FAMNM

In view of using MANA and BE and by using the discrete-time elements models described before, one can obtain a general MANA formulation as follows:

$$\begin{aligned}
 [A][x] &= [b] \Rightarrow \\
 \begin{bmatrix} a_{11} & a_{12} & \dots & a_{1n} \\ a_{21} & a_{22} & \dots & a_{2n} \\ \dots & \dots & \dots & \dots \\ a_{n1} & a_{n2} & \dots & a_{nn} \end{bmatrix} \begin{bmatrix} x_1(t) \\ x_2(t) \\ \dots \\ x_n(t) \end{bmatrix} &= \begin{bmatrix} b_1(t-l\Delta t) \\ b_2(t-l\Delta t) \\ \dots \\ b_n(t-l\Delta t) \end{bmatrix} \quad (3.37)
 \end{aligned}$$

where  $[x]$  is the vector of unknown nodal voltages (both phase and modal domains) and branch currents (both phase and modal domains), and  $[b]$  is the vector of injected currents including the current sources for history terms in discrete circuit components models. For the case of injected currents  $l = 0$ , for lumped elements ( $L$ ,  $C$ )  $l = 1$ , and for transmission lines  $l = p_m \Delta t$  (where  $p_m \Delta t$ , with  $\underline{p_m} \in \mathbb{N}$ , represents the propagation time of the mode  $m$  of a given transmission line of the system). In addition, line transformation matrices ( $[T_v]$  and  $[T_i]$ ) are included in matrix  $[A]$ . Details on the composition of  $[A]$  are given in the next chapter.

It is worth mentioning that for the case of transmission lines, the solution at one terminal requires the knowledge of the variables at the other terminal with specific time delays corresponding to the travelling times. In most cases, the delays are not multiples of the simulation time step (i.e.,  $p_m \notin \mathbb{N}$ ). Therefore, interpolation techniques are required to calculate the intermediate values. Among different interpolation techniques [131], the most common for EMTP applications is the linear interpolation [79]. In this research, we have adopted linear interpolation for the EMT simulations of transmission lines.

### 3.4.2 Problem Definition

ADC switch representation and as a consequence, FAMNM solution method provides the advantage of keeping ANAM constant during switching transitions. This peculiarity is an important aspect for the case of FPGA-based real-time simulators, where, due to the very low time steps and complexity of FPGA programming, matrix manipulation is a challenging issue. Therefore, several

proposed FPGA-based real-time simulators adopt ADC switch model (e.g., [101], [104], [106], [107], [113], [117]). The ANAM is built once, inverted and used by the FPGA solver. However, this approximate switch model introduces artificial transients and errors in the simulation results [101], [116], [130], [132].

According to [130], one approach for determining the value of  $G_s$  is to select  $C_s$  and  $L_s$  in (3.34) equal to the corresponding real switch parameters. Then, the values of  $G_s$  and  $\Delta t$  could be determined using (3.34). However, the main drawback of this approach is that the required simulation time step might become extremely small resulting in prohibitive computational times.

One solution to solve the artificial oscillations result by ADC model have been proposed in [133], in which a damping resistance was added in series to the ADC switch model. The purpose of the damping resistance was to mitigate artificial oscillations due to the interaction between the capacitor of the switch model in the open state and external inductive elements. Power losses in power electronic switches mainly consist of the loss during the ON state, diode reverse-recovery current loss, turnoff transition, and turn-on transition. The considered resistance in the ADC switch model is too simplistic to include all these losses. Although, this resistance might slightly improve the damping of the artificial oscillations, it also introduces artificial losses to the system. Moreover, the proper determination of the resistance value increases the complexity of the model.

A different approach to solve this problem is the optimal selection of the conductance parameter  $G_s$ . One possibility is to consider an *a priori* value for  $G_s$  and, then, find the corresponding optimal value by comparing the simulation results with benchmark ones in order to minimize the relevant errors [134] (i.e., obtained by off-line simulations where the switches are represented by ideal devices). However, such a trial-and-error approach provides solutions that require specific and time-consuming assessments in which the uniqueness of the solution is not guaranteed.

Therefore, there is a need to assess the optimal value of  $G_s$  to minimize the simulation errors. In order to illustrate the impact of the adopted value for  $G_s$  on the simulation results accuracy, a time-domain simulation of the inrush of a single-conductor transmission line is considered. As it is shown in Figure 3.10, the network is composed of a source, representing an infinite power bus, supplying an HV/MV transformer that feeds a 1 MW/0.3 MVar load and a transmission line.

The transmission line parameters are those of a typical 20 kV lossy overhead line, namely a surge impedance of 400 Ohms and a propagation time equal to 117  $\mu$ s. In order to simplify the interpretation of the results, a single-phase model has been considered.

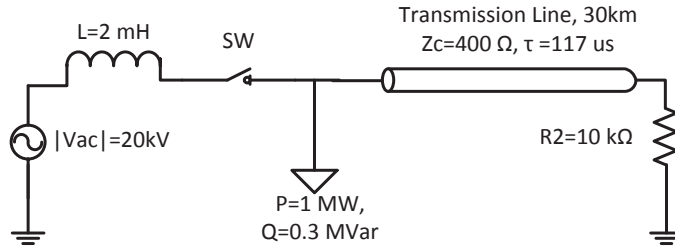


Figure 3.10. Schematic representation of the test case composed of a single-conductor transmission line and a switch.

This network has been simulated in EMTP-RV simulation environment where the switch was modeled using either an ideal switch (reference case), or a ADC model with different values for the conductance. Figure 3.11 shows the effect of the switch conductance value on the accuracy of the simulated current at the feeding terminal of the transmission line. It can clearly be observed that the adopted value for  $G_s$  affects dramatically the simulation accuracy of the FAMNM vs the reference one in which an ideal switch has been considered. Therefore, it is crucial to find the proper value of  $G_s$  in order to have accurate simulation results. In what follows, the proposed method to calculate the optimal value of the switch conductance is presented.

### 3.4.3 The Proposed Methodology

The proposed method is based on the minimization of the Euclidian distance between the eigenvalues of the network admittance matrix  $[A_n]$  based on FAMNM, and those associated with the admittance matrices of reference networks corresponding to the all possible switching permutations.

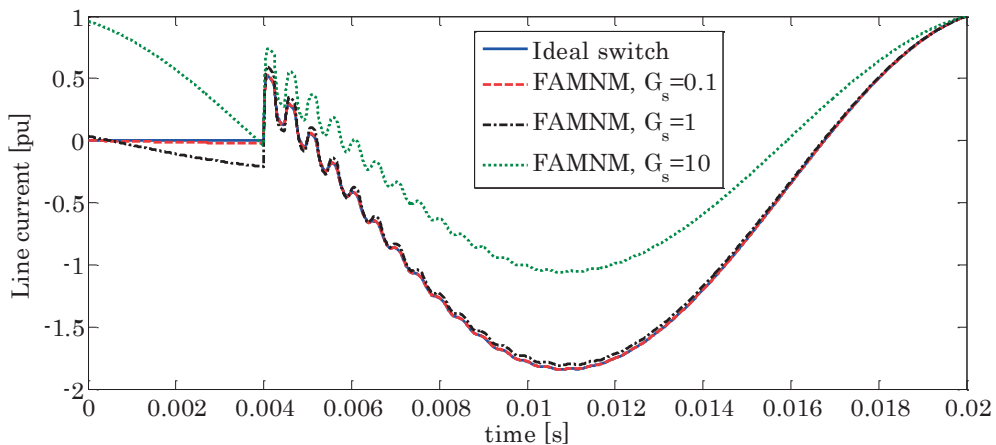


Figure 3.11. Line current at the beginning of the line for four switch representation models (i) ideal switch, (ii) FAMNM representation for  $G_s= 0.1$ , and (iii) FAMNM representation for  $G_s= 1$ , and (iv) FAMNM representation for  $G_s= 10$ .

In order to clearly describe the proposed method, it will be first explained for the case of a network with a single switch. Then, it is generalized for the case of networks with multiple switches.

### 3.4.3.1 Proposed Method for Networks Composed of a Single Switch

The proposed method allows for the evaluation of the optimal value of the switch conductance  $G_s$  as the solution of an optimization problem where the objective function is associated with the distances between the eigenvalues of  $[A_n]$  obtained using the FAMNM (of course, this set of eigenvalues is inherently function of  $G_s$ ) and two other sets of eigenvalues of matrices  $[A_n]$  related to the ‘ON’ and ‘OFF’ states of the considered switch. In this respect, it is worth observing that the proposed approach is a formal process aiming at identifying the characteristics of the discrete-time switch conductance that minimizes a suitably defined objective function that exhibits minimum coinciding with those of objective functions related to artificial losses introduced by the FAMNM or to the errors in the reference simulated waveforms, see Section 4.3 for further details).

Let  $[A_n^p]$ ,  $[A_n^c]$ , and  $[A_n^o]$  be the nodal admittance matrices when the switch is represented by FAMNM, ideal switch in ‘ON’ state, and ideal switch in ‘OFF’ state, respectively. The three matrices are all supposed to be of rank  $n$ . As stated in a fundamental theorem of linear algebra, if  $\mathbf{B}$  is a base of the vector space  $\mathbf{V}$  (of dimension  $n$ ) and  $\mathbf{W}$  another vector space of dimension  $n$ , for each transformation  $\varphi: \mathbf{B} \rightarrow \mathbf{W}$ , there is one and only one linear map  $\mathbf{T}: \mathbf{V} \rightarrow \mathbf{W}$  such that  $\mathbf{T}|_{\mathbf{B}} = \varphi$ . Now, since  $[A_n^p]$ ,  $[A_n^c]$ , and  $[A_n^o]$  are real matrices of rank  $n$ , we can define three bases  $\mathbf{B}_p$ ,  $\mathbf{B}_c$  and  $\mathbf{B}_o$  of  $\mathbf{R}^n$  associated with the respective eigenvalues:

$$\mathbf{B}_p \leftrightarrow \lambda_i^p(G_s) = \text{eig}\left\{[A_n^p]\right\}, i = 1, 2, \dots, n \quad (3.38)$$

$$\mathbf{B}_c \leftrightarrow \lambda_i^c = \text{eig}\left\{[A_n^c]\right\}, i = 1, 2, \dots, n \quad (3.39)$$

$$\mathbf{B}_o \leftrightarrow \lambda_i^o = \text{eig}\left\{[A_n^o]\right\}, i = 1, 2, \dots, n \quad (3.40).$$

Note that  $\lambda_i^p(G_s)$ ,  $\lambda_i^c$ ,  $\lambda_i^o$  denote respectively the corresponding eigenvalues for each nodal admittance matrix. As already clarified,  $\lambda_i^p(G_s)$  is a function of  $G_s$  whereas,  $\lambda_i^c$  and  $\lambda_i^o$  are fixed.

Since for each matrix  $[A_n^p]$ ,  $[A_n^c]$ , and  $[A_n^o]$  we can associate a unique base ( $\mathbf{B}_p$ ,  $\mathbf{B}_c$  and  $\mathbf{B}_o$ , respectively), in view of the fundamental theorem of linear algebra, these transformations are unique. Therefore, the objective is to determine  $\mathbf{B}_p$  such that  $\mathbf{T}|_{\mathbf{B}_p}$  provides results that are as close as possible to both  $\mathbf{T}|_{\mathbf{B}_c}$  and  $\mathbf{T}|_{\mathbf{B}_o}$ . A possible metric to achieve such an objective is to minimize the squared Euclidian distances for each eigenvalue calculated as:

$$\gamma_i^c(G_s) = \left\{ \operatorname{Re}[\lambda_i^p(G_s)] - \operatorname{Re}[\lambda_i^c] \right\}^2 + \left\{ \operatorname{Im}[\lambda_i^p(G_s)] - \operatorname{Im}[\lambda_i^c] \right\}^2 \quad (3.41)$$

$$\gamma_i^o(G_s) = \left\{ \operatorname{Re}[\lambda_i^p(G_s)] - \operatorname{Re}[\lambda_i^o] \right\}^2 + \left\{ \operatorname{Im}[\lambda_i^p(G_s)] - \operatorname{Im}[\lambda_i^o] \right\}^2 \quad (3.42)$$

In these equations,  $\gamma_i^c(G_s)$  and  $\gamma_i^o(G_s)$  denote, as a function of  $G_s$ , the squared Euclidian distances between the  $i^{\text{th}}$  eigenvalue of  $[A_n^p]$  and the corresponding one of  $[A_n^c]$  and  $[A_n^o]$  respectively. These distances, for a generic  $i^{\text{th}}$  eigenvalue are illustrated in Figure 3.12.

Then, the following total distance (for a given eigenvalue) can be defined:

$$\eta_i(G_s) = \gamma_i^o(G_s) + \gamma_i^c(G_s) \quad (3.43).$$

It is possible to define an objective function as the sum of all normalized distances:

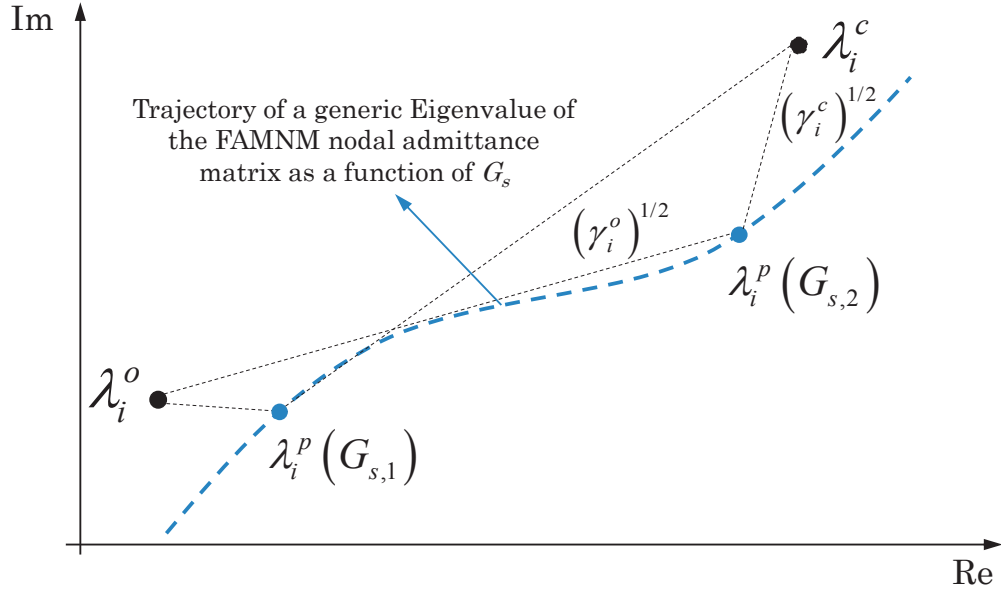
$$\Gamma(G_s) = \sum_{i=1}^n \left( \frac{\eta_i(G_s)}{\max\{\eta_i(G_s)\}} \right) \quad (3.44).$$

Note that the normalization is done in order to give equal weight to all eigenvalues distances.

The optimum value for  $G_s$  is defined as the one that minimizes the objective function (3.44). In other words:

$$G_s^* = \arg|_{G_s} \min\{\Gamma(G_s)\} \quad (3.45).$$





**Figure 3.12. Definition of Euclidian distance between eigenvalues of the network admittance matrix based on FAMNM and those associated with the admittance matrices of two reference networks.**

### 3.4.3.2 Extension to Networks with Multiple Switches

For the case of a network with  $N$  switches, the number of possible switching permutations is  $2^N$ . Therefore, there are  $2^N$  set of eigenvalues of the nodal admittance matrix associated with ideal switch representations, namely:

$$\lambda_i^x = \text{eig} \left\{ \left[ A_n^x \right] \right\}, \begin{cases} i = 1, 2, \dots, n \\ x \in 2^N \end{cases} \quad (3.46)$$

where  $x$  is one of the possible switches permutations. Additionally, the eigenvalues of nodal admittance matrix associated with the FAMNM switch representation are function of switches conductance, namely:

$$\lambda_i^p(G_{s1}, G_{s2}, \dots) = \text{eig} \left\{ \left[ A_n^p \right] \right\}, i = 1, 2, \dots, n \quad (3.47)$$

where, for each switch, a different conductance value has been considered.

The squared Euclidian distances associated with the  $i^{\text{th}}$  eigenvalue have to be calculated for all possible permutations:

$$\eta_i(G_{s1}, G_{s2}, \dots) = \sum_x \left( \left\{ \text{Re} \left[ \lambda_i^p(G_{s1}, G_{s2}, \dots) \right] - \text{Re} \left[ \lambda_i^x \right] \right\}^2 + \left\{ \text{Im} \left[ \lambda_i^p(G_{s1}, G_{s2}, \dots) \right] - \text{Im} \left[ \lambda_i^x \right] \right\}^2 \right) \quad (3.48).$$

The objective function extended to the general case reads:

$$\Gamma(G_{s1}, G_{s2}, \dots) = \sum_{i=1}^n \left( \frac{\eta_i(G_{s1}, G_{s2}, \dots)}{\max\{\eta_i(G_{s1}, G_{s2}, \dots)\}} \right) \quad (3.49)$$

The optimum values for the switches conductance come from the solution of the following optimal problem:

$$G_{s1}^*, G_{s2}^*, \dots = \arg \left|_{G_{s1}, G_{s2}, \dots} \min \{ \Gamma(G_{s1}, G_{s2}, \dots) \} \right. \quad (3.50).$$

It is worth observing that for networks with multiple switches, there might be preferred switching sequences. Thus, all the permutations are not used equally. Therefore, the number of the possible permutations and number of the switch conductance values can be significantly reduced. As an example, for the case of a two-level three-phase inverter, by considering the switching modes where each switch conducts for 180 degrees of a cycle, there are eight possible switching permutations. Moreover, network portioning can reduce the possible combinations and accelerate the process.

### 3.4.4 Method Verification towards Error and Losses Functions

#### 3.4.4.1 Error Function Associated with Switches Voltage and Current Errors

In order to verify the correctness of the solution provided by (3.50), we have first compared the objective function defined by (3.49) with an error function inferred from the differences between the voltage/current waveforms obtained for various values of  $G_s$  and reference values obtained using the ideal switch model. Such an error function includes time-domain switch voltage and current waveforms subsequent to switch state transitions (in particular, subsequent to pairs of ‘ON’-‘OFF’ transitions). Indeed, as it is stated in [130], switch current error in ‘OFF’ state is proportional to  $G_s$  whereas, switch voltage error in ‘on’ state is inversely proportional to  $G_s$ . This specific property has been exploited to define the error function. Specifically, the following procedure has been adopted: the switch current error is calculated, for each of the  $N_1$  switches in ‘OFF’ state, as the difference between the instantaneous values of the switch current given by the FAMNM solver and the current provided by a reference simulation where the switch is considered as an ideal device. The same procedure is considered to calculate the switch voltage error for each of the  $N_2$  switches, which are in ‘on’ state. For the  $i^{th}$  switch, the current and voltage errors,  $E_{sw_i}^I(G_{s1}, G_{s2}, \dots)$  and  $E_{sw_i}^V(G_{s1}, G_{s2}, \dots)$ , are then given by:

$$E_{\omega_1}^I(G_{s1}, G_{s2}, \dots) = \sum_{k=0}^m [i_{\omega_1}(G_{s1}, G_{s2}, \dots)_k - i_{k, \omega_1}^*]^2, m = \frac{T}{\Delta t}, \omega_1 = 1, 2, \dots, N_1 \quad (3.51)$$

$$E_{\omega_2}^V(G_{s1}, G_{s2}, \dots) = \sum_{k=0}^m [v_{\omega_2}(G_{s1}, G_{s2}, \dots)_k - v_{k, \omega_2}^*]^2, m = \frac{T}{\Delta t}, \omega_2 = 1, 2, \dots, N_2 \quad (3.52)$$

Note that in (3.51) and (3.52),  $T$  is a given time window where one possible switching permutation occurs. Discrete variables  $i_{\omega_1}(G_{s1}, G_{s2}, \dots)_k$  and  $v_{\omega_2}(G_{s1}, G_{s2}, \dots)_k$  correspond to the discretized instantaneous values of switch current and voltage when the switch is represented by its approximate model and, thus, they are function of all switch conductances. Discrete variables  $i_{k, \omega_1}^*$  and  $v_{k, \omega_2}^*$  are the corresponding discretized instantaneous switch current and voltage, obtained from reference simulations where the switch are represented as ideal devices.

To define the error function, the effect of all  $N$  switches should be taken into account. Namely, for each possible permutation, the sum of the current errors for all switches in ‘OFF’ state and the sum of the voltage errors for all the switches in ‘ON’ state are considered as:

$$E^x(G_{s1}, G_{s2}, \dots) = \sum_{\omega_1} \left( \frac{E_{\omega_1}^I(G_{s1}, G_{s2}, \dots)}{\max(E_{\omega_1}^I(G_{s1}, G_{s2}, \dots))} \right) + \sum_{\omega_2} \left( \frac{E_{\omega_2}^V(G_{s1}, G_{s2}, \dots)}{\max(E_{\omega_2}^V(G_{s1}, G_{s2}, \dots))} \right) \quad (3.53).$$

For all possible switching cases, the same procedure is applied by considering the same time window  $T$  for the calculation and by changing the switches state.

Finally, in order to take into account all possible permutations, the overall error function is defined as the sum of normalized errors calculated for each possible permutation in (3.53), as follows:

$$E(G_{s1}, G_{s2}, \dots) = \sum_x \left( \frac{E^x(G_{s1}, G_{s2}, \dots)}{\max(E^x(G_{s1}, G_{s2}, \dots))} \right) \quad (3.54).$$

### 3.4.4.2 Losses Function Associated with Switches Losses

A further way to verify the correctness of the solution provided by (3.50) is to compare it with another function that represents the switch losses when these devices are represented by using the FAMNM approach. For the case of an ideal switch, the switch losses are zero during the ‘off’ and ‘on’ states since switch current/voltage are null. To this end, the switch losses in ‘off’ and ‘on’ states,  $P_{\omega_1}^O(G_{s1}, G_{s2}, \dots)$  and  $P_{\omega_2}^C(G_{s1}, G_{s2}, \dots)$  respectively, can be straightforwardly calculated as follows:

$$P_{\omega_1}^O(G_{s_1}, G_{s_2}, \dots) = \frac{1}{m} \sum_{k=0}^m (v_{\omega_1}^o(G_{s_1}, G_{s_2}, \dots)_k \cdot i_{\omega_1}^o(G_{s_1}, G_{s_2}, \dots)_k), m = \frac{T}{\Delta t}, \omega_1 = 1, 2, \dots, N_1 \quad (3.55)$$

$$P_{\omega_2}^C(G_{s_1}, G_{s_2}, \dots) = \frac{1}{m} \sum_{k=0}^m (v_{\omega_2}^c(G_{s_1}, G_{s_2}, \dots)_k \cdot i_{\omega_2}^c(G_{s_1}, G_{s_2}, \dots)_k), m = \frac{T}{\Delta t}, \omega_2 = 1, 2, \dots, N_2 \quad (3.56)$$

where discrete variables  $i_{\omega_1}^o(G_{s_1}, G_{s_2}, \dots)_k$ ,  $v_{\omega_1}^o(G_{s_1}, G_{s_2}, \dots)_k$  and  $i_{\omega_2}^c(G_{s_1}, G_{s_2}, \dots)_k$ ,  $v_{\omega_2}^c(G_{s_1}, G_{s_2}, \dots)_k$  correspond to the discretized instantaneous values of switch current and voltage in ‘off’ and ‘on’ states respectively, when the switch is represented by the FAMNM.

The impact of all switches in a possible switching permutation is taken into account by considering the sum of all switches losses as:

$$P^x(G_{s_1}, G_{s_2}, \dots) = \sum_{\omega_1} \left( \frac{P_{\omega_1}^O(G_{s_1}, G_{s_2}, \dots)}{\max(P_{\omega_1}^O(G_{s_1}, G_{s_2}, \dots))} \right) + \sum_{\omega_2} \left( \frac{P_{\omega_2}^C(G_{s_1}, G_{s_2}, \dots)}{\max(P_{\omega_2}^C(G_{s_1}, G_{s_2}, \dots))} \right) \quad (3.57)$$

where  $P^x(G_{s_1}, G_{s_2}, \dots)$  is the overall loss for one of the possible switching permutation.

Then, the total losses function takes into account all possible switching permutations by summing the normalized overall losses calculated in (3.57):

$$P(G_{s_1}, G_{s_2}, \dots) = \sum_x \left( \frac{P^x(G_{s_1}, G_{s_2}, \dots)}{\max(P^x(G_{s_1}, G_{s_2}, \dots))} \right) \quad (3.58).$$

In the next section, we will show that the optimal value for  $G_s$  provided by (3.50) corresponds also to the minimum of the error function (3.54) and losses function (3.58), proving that the proposed approach satisfies these two criteria at the same time.

### 3.4.5 Validation Examples

In order to validate our proposed method, two simulation cases are considered. The first simulations refer to electrical circuits composed of one switch. The second cases study refer to electrical circuits composed of multiple switches. These case studies are carried out by making reference to two different types of electrical circuits: (i) circuits composed of RLC elements, and (ii) circuits including transmission lines.

### 3.4.5.1 Circuits with One Switch

The first simulation case study refers to an electrical circuit composed of RLC elements and one switch. The schematic diagram of the considered circuit is shown in Figure 3.13. This circuit is simulated within the EMTP-RV simulation environment considering both an ideal model and a discrete-time model for the switch. As previously mentioned, the backward Euler method was used for the numerical integration with a time step  $\Delta T = 4 \mu\text{s}$ .

For the circuit shown in Figure 3.13, the ANAMs are formed for the cases where the switch is represented by (i) FAMNM, (ii) ideal switch in ‘ON’ case, and (iii) ideal switch in ‘OFF’ case. Then, according to the proposed method, the objective function (3.49) is determined. In order to calculate the error and losses functions, the following switching transition is considered: the switch is in open position and it is closed at  $t = 10 \text{ ms}$ . Then, it is opened again at  $t = 20 \text{ ms}$ . For all values of  $G_s$  (i.e.,  $0 \leq G_s \leq 1$ ), equations (3.49), (3.54), and (3.58) are calculated. The objective function together with the corresponding error and losses functions are shown in Figure 3.14. As it can be clearly observed, all the three functions have their minimum when  $G_s$  is equal to 0.11.

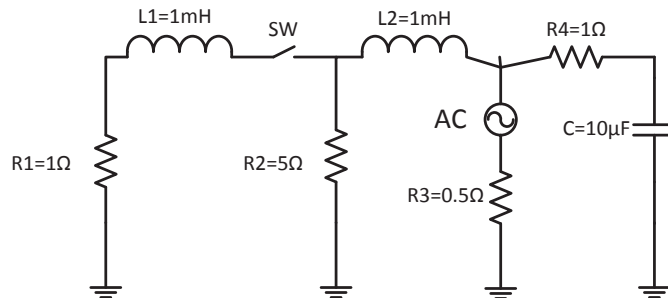


Figure 3.13. Schematic representation of the RLC case study including one switch.

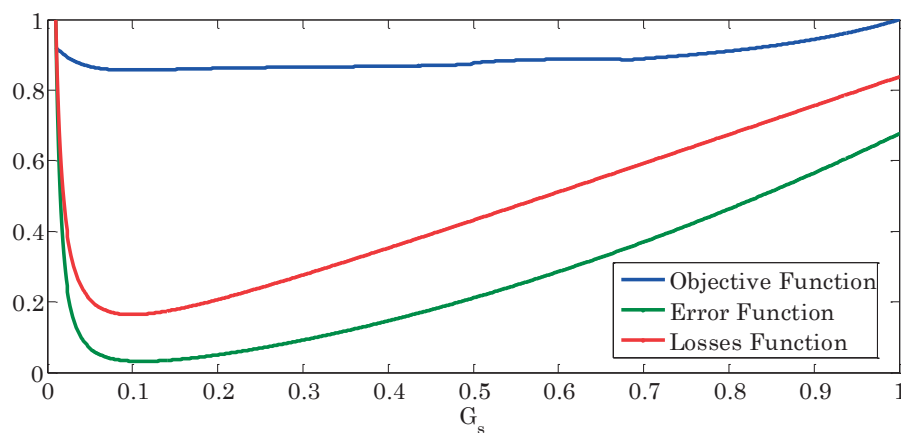


Figure 3.14. Objective, error, and switch-losses functions for the case of the RLC test case of Figure 3.13.

The second simulation example refers to a network shown previously in Figure 3.10, which includes a single-conductor transmission line. By applying the same procedure for  $0 \leq G_s \leq 0.5$ , the objective, error, and losses functions are calculated (see Figure 3.15). As it is shown on Figure 3.15, these three functions exhibit the same behavior as for the previous case, with a common minimum occurring for a value of  $G_s$  equal to 0.01.

With reference to the second test case, Figure 3.16 illustrates the time-domain simulations of the voltage at the end of the line for different values of  $G_s$  including the optimal value previously identified ( $G_s^*=0.01$ ). It can be seen that the simulations obtained using the optimum value for the conductance are in agreement with those obtained using EMTP-RV. Figure 3.14 and Figure 3.15 show that the proposed objective function could be utilized as an efficient tool to find the optimum value for  $G_s$  without performing any off-line benchmark simulations.

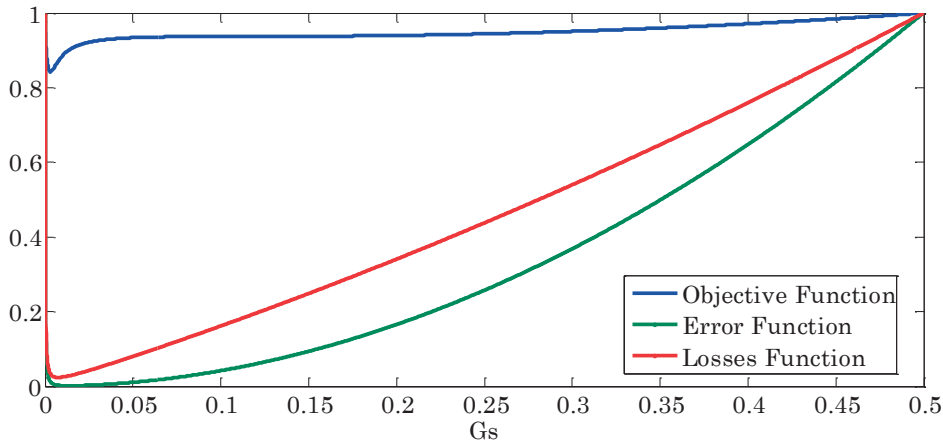


Figure 3.15. Objective, error, and switch-losses functions for the case of transmission line test case (Figure 3.10) with variable  $G_s$ .

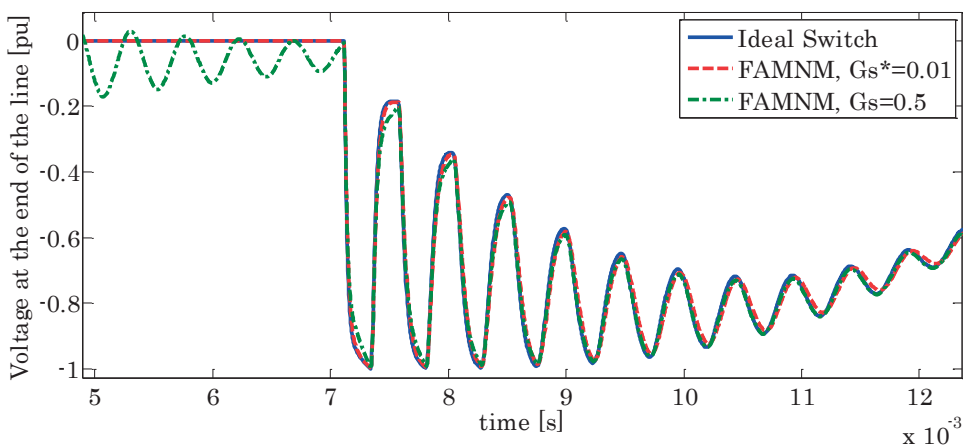


Figure 3.16. Time-domain simulated waveforms for voltage at the end of the transmission line (second test case of Figure 3.10 for different values of  $G_s$ ).

### 3.4.5.2 Circuits with Multiple Switches

In order to validate the performance of the proposed method, additional investigations have been done for the case of networks with two switches. To this end, the simulation example refers to an RLC circuit including two switches. The schematic diagram of the considered circuit is shown in Figure 3.17.

According to the proposed method, for each switch, a dedicated  $G_s$  value is considered and equations (3.49), (3.54), and (3.58) are formed to find the objective, error and losses functions. Figure 3.18 shows the objective function. As it is shown on this figure, the minimum values correspond to  $G_{s1}^*=0.4$  and  $G_{s2}^*=0.18$ , and the ideal representation.

In Figure 3.19 and Figure 3.20, the time-domain simulations of the voltage and current of switch #2 of Figure 3.17 show that a very good match is achieved between the results of the FAMNM representation with optimal conductance value.

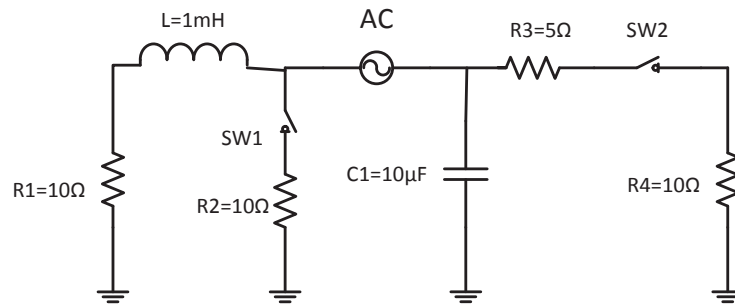


Figure 3.17. Schematic representation of the RLC case study including two switches.

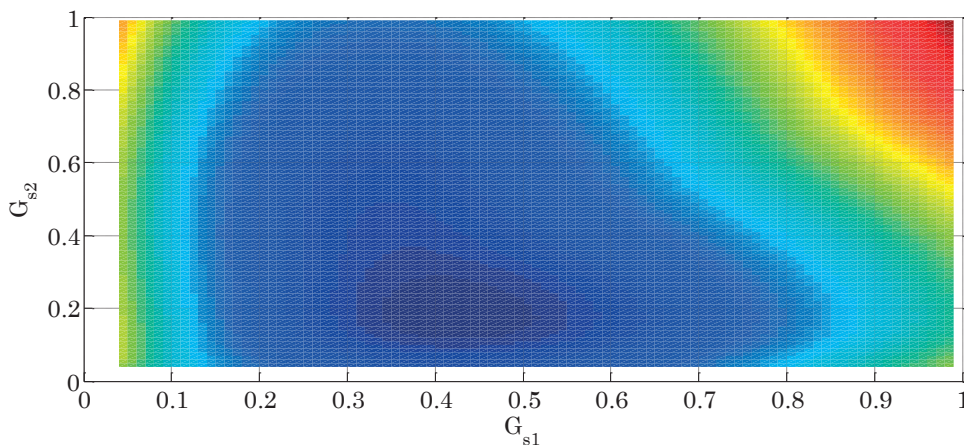


Figure 3.18. Objective function used to assess the optimal  $G_s$  values for the case of RLC circuit with two switches shown in Figure 3.17.

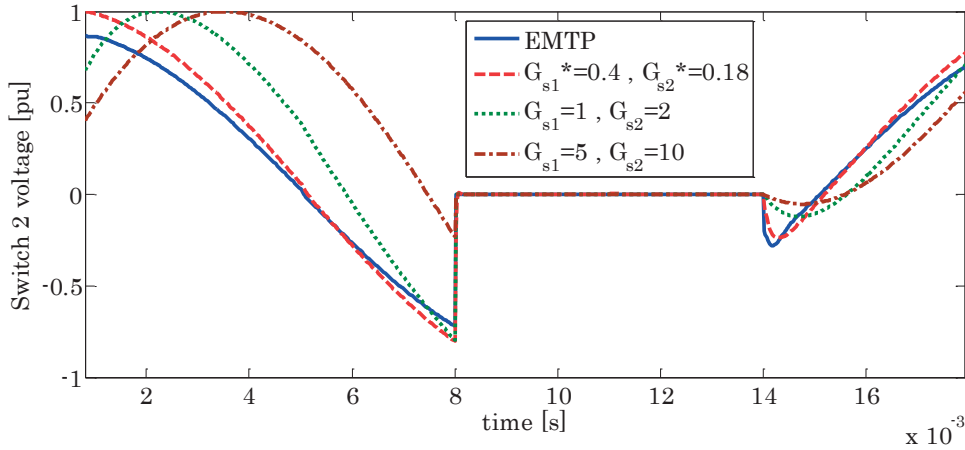


Figure 3.19. Time-domain simulated waveforms for switch #2 voltage for the optimal values of  $G_{s1}$ ,  $G_{s2}$  for the circuit composed of RLC elements and two switches.

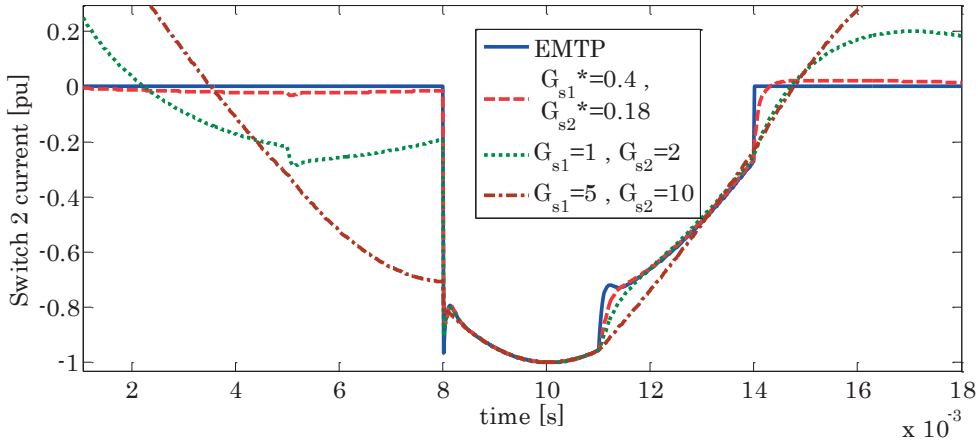


Figure 3.20. Time-domain simulated waveforms for switch #2 current for the optimal values of  $G_{s1}$ ,  $G_{s2}$  for the circuit composed of RLC elements and two switches.

The next example refers to a network with a single-conductor transmission line and two switches. The schematic diagram of the considered network is shown in Figure 3.21.

The objective and error functions are shown in Figure 3.22 and Figure 3.23, respectively. Both functions exhibit the minimum at  $G_{s1}^*=0.001$  and  $G_{s2}^*=0.005$ . In Figure 3.24, the time-domain simulations of the voltage of switch #1 of Figure 3.21 shows that a very good match is achieved between the results of the FAMNM representation with optimal conductance value.



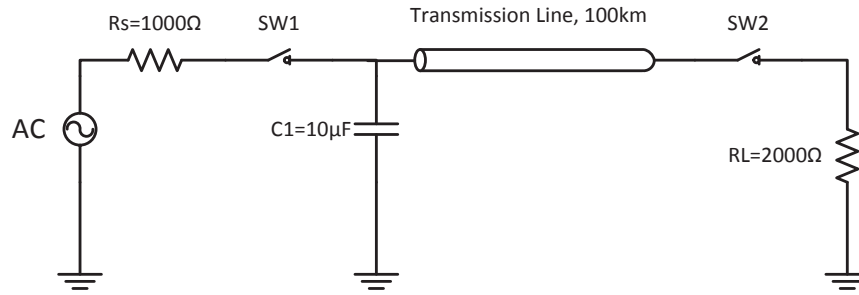


Figure 3.21. Schematic representation of the test case composed of a single-conductor transmission line and two switches.

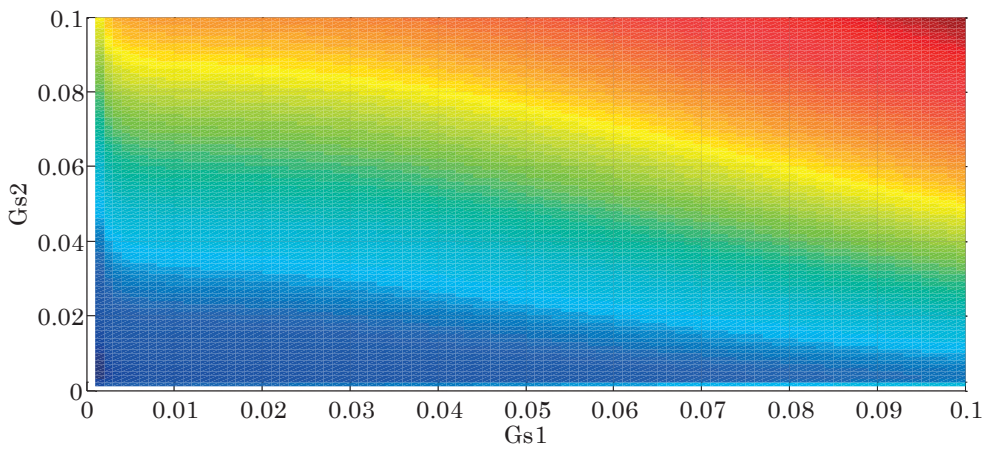


Figure 3.22. Objective used to assess the optimal  $G_s$  values for the case of a single-conductor transmission line with two switches shown in Figure 3.21.

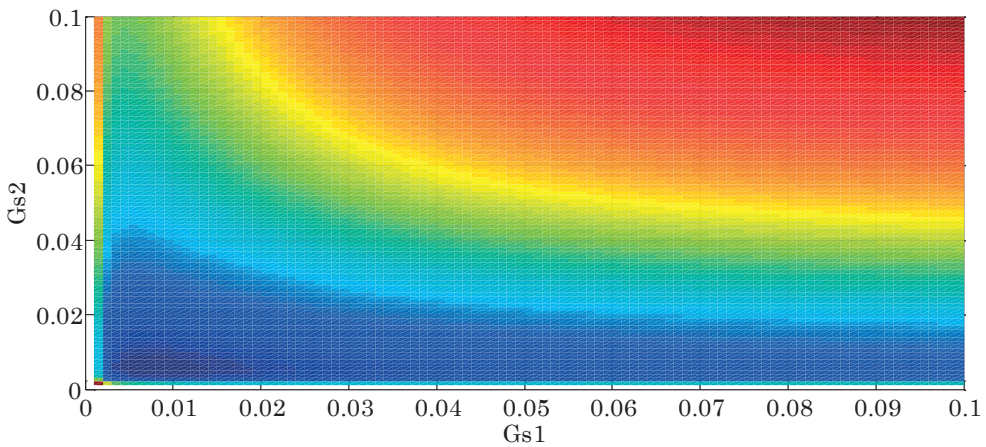
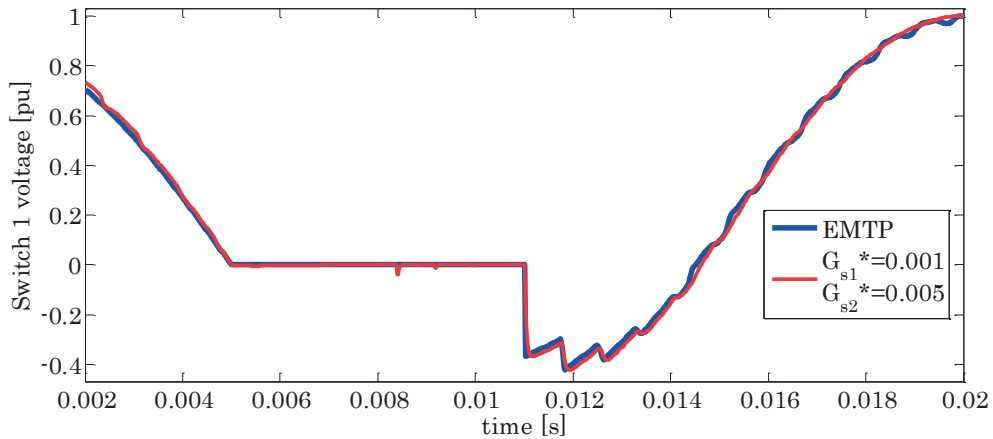


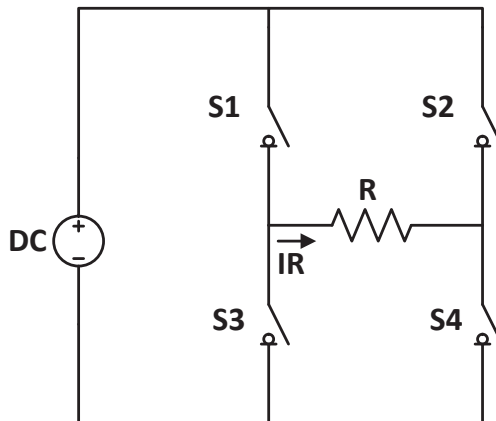
Figure 3.23. Error functions used to assess the optimal  $G_s$  values for the case of a single-conductor transmission line with two switches shown in Figure 3.21.



**Figure 3.24. Time-domain simulated waveforms for switch #1 voltage for the optimal values of  $G_{s1}$ ,  $G_{s2}$  for the case of a single-conductor transmission line with two switches shown in Figure 3.21.**

The fifth test case makes reference to a single-phase power converter where four switches are considered. In view of the symmetricity of the circuit, the  $G_s$  of the four switches have been grouped by two. Namely, switches S1 and S4 and switches S2 and S3 have common  $G_{s14}$  and  $G_{s23}$  values, respectively. The schematic representation of this system is shown in Figure 3.25.

The relevant objective function is shown in Figure 3.26. It can be observed that the minimum of this function corresponds to  $G_{s14}= 1$  and  $G_{s23}= 0.8$ . The time domain simulation results for switch S4 voltage and current for different switches parameters values are shown in Figure 3.27 and Figure 3.28 which support the correctness of the proposed objective function.



**Figure 3.25. Schematic representation of single phase DC/AC converter.**

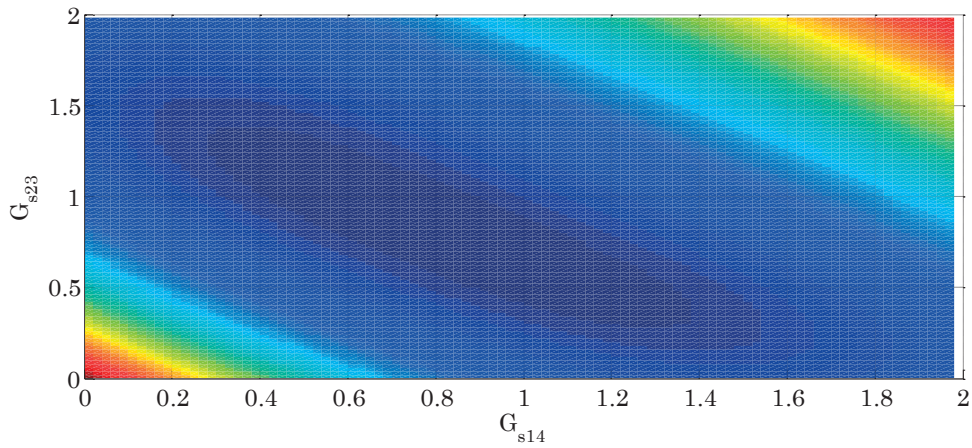


Figure 3.26. Objective function used to assess the optimal  $G_s$  values for the case of single phase power converter with four switches shown in Figure 3.25.

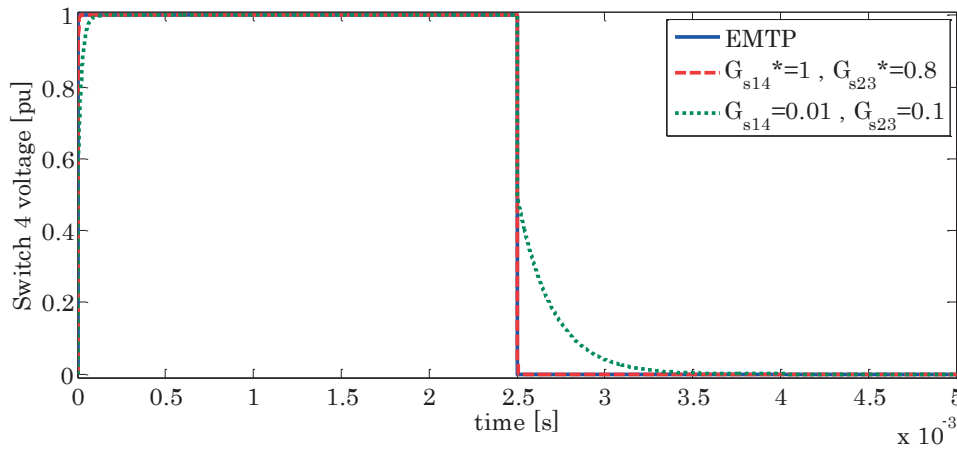


Figure 3.27. Time-domain simulated waveforms for switch #4 voltage for two sets of switches parameters values including the optimal ones optimal.

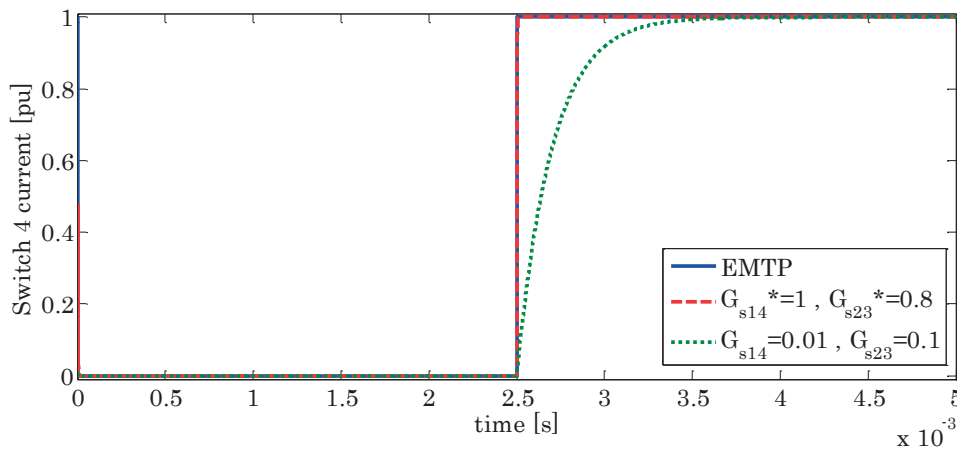


Figure 3.28. Time-domain simulated waveforms for switch #4 current for two sets of switches parameters values including the optimal ones optimal.

The last validation example refers to a two-level three-phase inverter that is connected to an inductive filter (10 mH) and a resistive load (20  $\Omega$ ). The schematic of the circuit is shown in Figure 3.29.

By considering the switching modes where each switch conducts for 180 degrees of a cycle, there are eight possible switching permutations as: (S1,S2,S6), (S1,S2,S3), (S2,S3,S4), (S3,S4,S5), (S4,S5,S6), (S1,S5,S6), (S1,S3,S5), and (S2,S4,S6). Therefore, we obtain eight ANAM corresponding to each status of the ideal switches. Among them, six switching patterns generate non-zero voltage across the load and two of them (the upper or lower switches are conducting) generate zero voltage across the load.

According to the proposed method, the first step to calculate the optimal value for the switch conductance is to find the sets of eigenvalues corresponding to the possible switching permutations and also, the ones of the FAMNM. It is worth noting that, since the load and filter parameters are identical for all the phases, the eigenvalues for the two sets of patterns are equal for each set. Therefore, in view of the symmetrical nature of the circuit, one identical conductance value can be assigned to the six switches. By applying the optimization method, Figure 3.30 shows the objective function that allows to infer the optimal value of  $G_s=0.51$ . Figure 3.31 and Figure 3.32 show the time domain simulations of the load current and switch#1 voltage for the ideal switch model and FAMNM, respectively. The FAMNM-based simulations are done by using two different values for  $G_s$ , the calculated optimal one ( $G_s =0.51$ ) and non-optimal random value ( $G_s =0.1$ ). These figures illustrate that the optimal conductance value provide more accurate results and better agreement with the benchmark one.

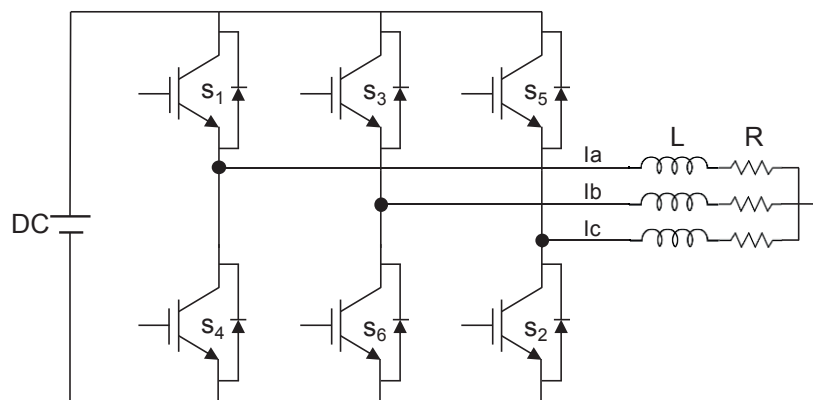


Figure 3.29. Schematic representation of the two-level three-phase inverter.

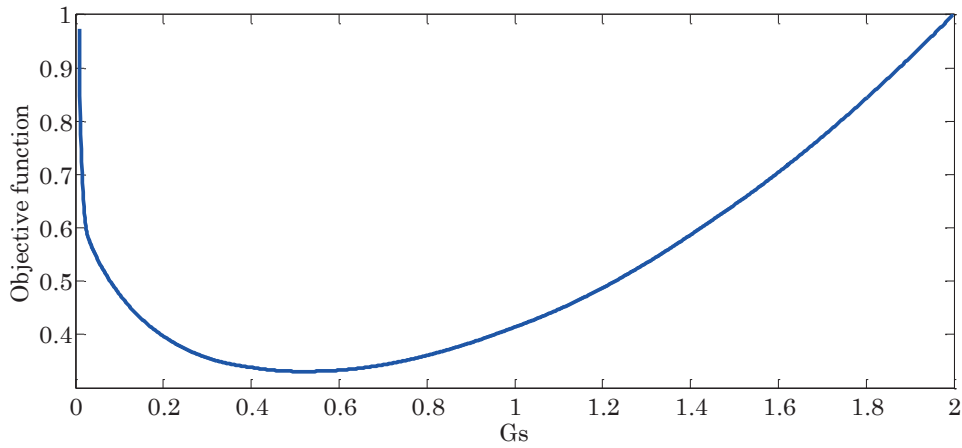


Figure 3.30. The calculated objective function for the optimal assessment of the switch conductance values of the two-level three-phase inverter shown in Figure 3.29.

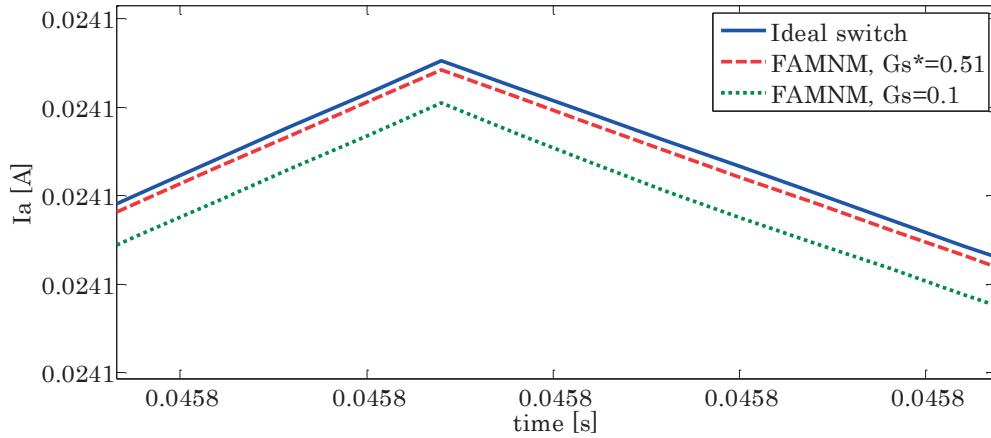


Figure 3.31. Time-domain simulated waveforms of the load current for ideal switch representation and FAMNM based optimal  $G_s$  and non-optimal one.

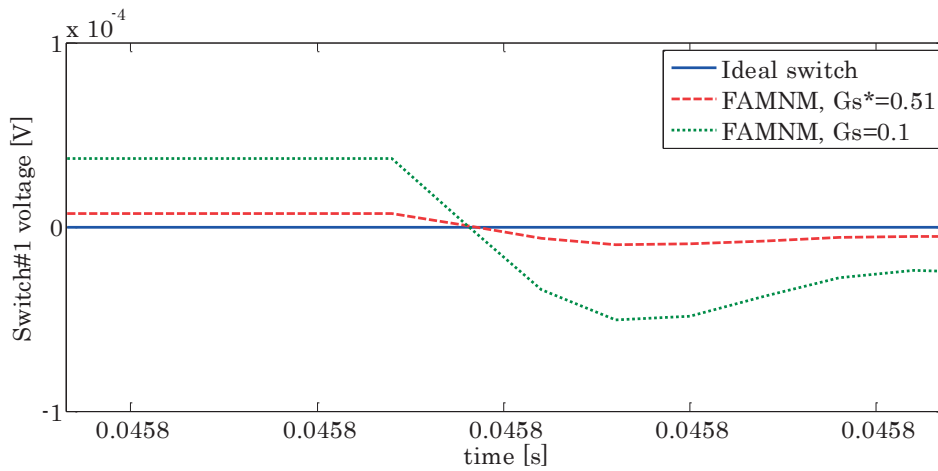


Figure 3.32. Time-domain simulated waveforms of the switch#1 voltage for ideal switch representation and FAMNM based optimal  $G_s$  and non-optimal one.

## 3.5 Conclusion

This chapter discusses about efficient real-time simulation of EMT taking place in generic power systems composed of either passive lumped elements, switches, or propagative transmission lines.

A review of the state of the art of real-time simulators was presented by making presenting a brief history of the development of the real-time simulators for EMT applications, their characteristics and drawbacks, the need for the FPGA-based real-time simulators, and review of the proposed FPGA-based real-time simulators.

A review of EMT simulation principles was presented to explain the different network formulation methods, numerical integration methods, and associated network elements models. Furthermore, a specific switch model, ADC, used often in the context of FPGA-based real-time simulators was described.

By making reference to the ADC switch model, an adapted solver based on the FAMNM was presented. The advantages and disadvantages of FAMNM method were highlighted. In particular, the impact of inaccurate parameter associated with the ADC switch model on the simulation results accuracy was discussed.

A novel method for the optimal assessment of the ADC model parameter was presented. The proposed method is based on the minimization of the Euclidian distance between the eigenvalues of the network admittance matrix based on FAMNM, and those associated with the admittance matrices of reference networks corresponding to the all possible switching permutations. To prove the correctness of the proposed method, a comparison between the proposed metric and specific defined error functions was presented and discussed.

The proposed method was validated by making reference to several validation examples including RLC circuit composed of single or two switches, networks including transmission lines, single phase inverter, and two-level three-phase inverter. The proposed method is proven to be correct in identifying the optimal conductance value of the discrete-time switch model. The results of the proposed method minimize: (i) the differences with reference-model current/voltage waveforms, and (ii) losses in the discrete-time switch conductance.

Without the need of performing off-line benchmark simulations, the proposed method represents a powerful solution for the representation of switches within real-time simulation platforms that rely on the use of the FAMNM (i.e., FPGAs).

# FPGA-RTS for Power Electronics and Power Systems EMT Simulations

## Summary

This chapter presents a new automated FPGA-RTS dedicated to EMT simulations of power electronic devices and power system networks. The proposed FPGA-RTS is based on MANA and in particular, it adapts FAMNM method for the modeling of circuits including switches, as described in Chapter 3. The proposed method for the optimal assessment of the ADC switch model, presented in Chapter 3, is coupled with the developed FPGA-RTS to provide very accurate simulation results.

The proposed FPGA-RTS is composed of two parts: (i) pre-processing unit, (ii) FPGA real-time solver. The pre-processing unit reads the *netlist* file generated by EMTP-RV and translates the information to the relevant data required by the simulator.

The FPGA solver is implemented using parallel algorithms applied for with the matrix to vector multiplication and Right-Hand-Side (RHS) vector updates. A specific method is used for the matrix to vector multiplication by taking advantage of the sparsity of the ANAM. The RHS vector update is performed in parallel and independently for different types of elements including lumped elements, switches, and transmission lines.

Three validation examples are provided to test the performance of the proposed FPGA-RTS. The first case refers to a HIL test by making reference to a two-level three-phase inverter. Furthermore, two case studies are analyzed by using the proposed FPGA-RTS to simulate fault originated transient signals taking place in (i) a multi-terminal HVDC network, and (ii) a three-phase AC network.

## 4.1 Introduction

As described in Chapter 3, compared to CPUs or DSPs, FPGAs are suitable alternatives to be used as the computational engine in RTSs computational engine. More specifically, the main advantage of the FPGA over CPU or DSP is associated with the hardwired parallel processing of FPGAs that enables the implementation of specific methodologies that dramatically reduce the sequencing of the operations taking place in CPUs or DSPs. Furthermore, in FPGAs the latency associated with the import/export of the I/Os is lower compared to CPUs. Finally, FPGAs are fully configurable chips which allow to be configured for specific applications. Therefore, FPGA-based real-time EMT simulation is a leading trend for HIL applications, in particular, for power electronics applications which enables to simulate, in real-time, high-frequency phenomena, such as electromagnetic transients, in power converters or travelling wave transients taking place in transmission lines.

Despite their significant benefits, FPGA-based RTSs suffer from some limitations. One of the main drawbacks is their difficult programming associated with the use of HDL. This low level programming, limits the scalability of the solvers and, as a consequence, the representation of complex circuits. Additionally, any modification in the implemented algorithm/model requires, in general, a time-consuming recompilation of the HDL code. A few automated FPGA-based RTSs have been proposed to avoid the difficulties of the FPGAs programming (e.g., [113], [115]). However, the applications of these simulators are mainly dedicated to power electronics HIL simulations. Therefore, these studies have not accounted for the possibility to simulate power networks including propagative transmission lines.

Another challenging issue regarding FPGA simulators is the limitation in the matrix manipulation and, as a consequence, the inherent difficulty to represent switching maneuvers. As explained earlier, the common approach to circumnavigate this problem is the use of ADC switch model and FAMNM-based solution method. Although this modeling method enables ultra-fast simulation of switching devices, its parameter impacts dramatically the simulation results accuracy (see Chapter 3). The existing literature in the context of FPGA-based real-time simulation for power electronics does not take into account the impact of the switch conductance value in the simulated model. Generally, FMANM-based approaches are adopted without quantitative error assessments to verify the developed FPGA-RTS (e.g., [101], [135], [117]).

By making reference to the above-mentioned challenges, in this Chapter, an automated FPGA-based real-time EMT simulator is proposed. The proposed RTS is implemented in an industrial real-time embedded system (the National Instruments CompactRio real-time platform) and has the following features: (i) it makes use of the MANA method, (ii) it integrates the FAMNM together with the



optimal selection of the switch conductance parameter, (iii) it enables the possibility of accurately reproducing electromagnetic switching transients taking place in power electronic switching devices together with electromagnetic wave propagation in transmission lines, and (iv) it enables to reach extremely low integration time steps and provides an automated procedure to directly translate the schematic representation of the electrical circuits designed in EMTP-RV to the relevant FPGA solver. Such peculiarity enables a straightforward applicability of the proposed FPGA-based RTS to various power electronics and power systems applications. In what follows, the structure of the proposed FPGA-based RTS is described.

## 4.2 Proposed Architecture for the FPGA-RTS

The proposed FPGA-based RTS is developed by using National Instruments CompactRIO platform. CompactRIO platform consists of an embedded controller for communication and processing, a reconfigurable chassis housing the user-programmable FPGA, I/O modules, and graphical LabVIEW software for rapid real-time programming. The processor is used for network communication, data logging, control, and processing with the deterministic and reliable NI Linux Real-Time OS. The user-programmable FPGA allows to implement custom hardware for high-speed control, and processing operations. The schematic representation of the CompactRIO platform is shown in Figure 4.1.

Different models of this platform with different features have been introduced and widely used for industrial applications. For the developed FPGA-RTS, the adopted hardware setup is NI CompactRIO-9033 which consists of an Intel Atom dual-core processor, a Xilinx Kintex-7 FPGA (7K160T), and reconfigurable I/O modules. This embedded system is based on NI Linux Real-Time OS and is programmed by using the NI LabVIEW environment. The advantages of using this platform are its high performance, reconfigurability, control and acquisition capabilities in a compact, rugged package, easy programming by using graphical LabVIEW programming environment, and ability to be used in harsh industrial environments. The specifications of the adopted NI CompactRIO-9033 are summarized in Table 4.1.

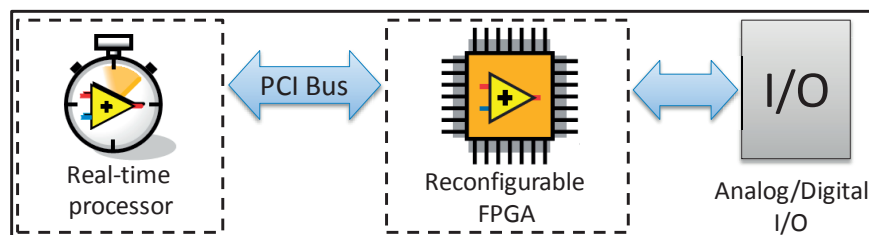
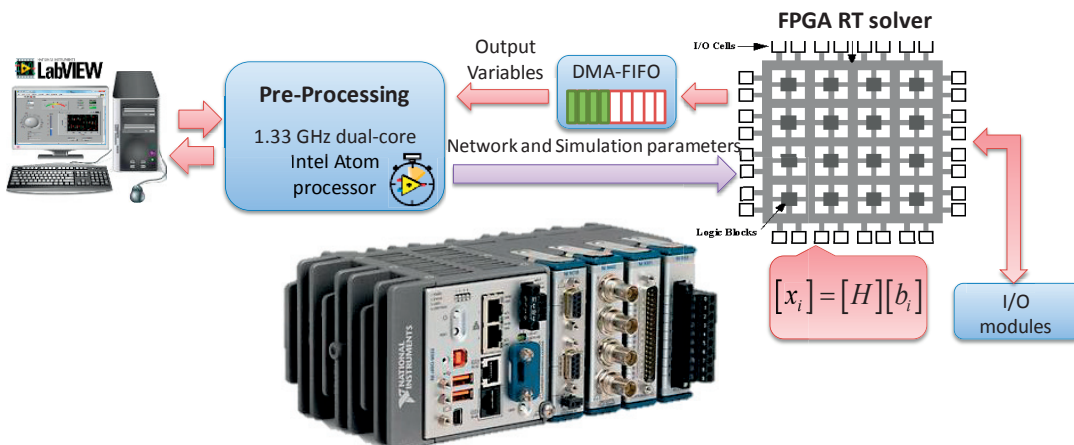


Figure 4.1. Schematic representation of NI CompactRIO platform.

**Table 4.1. CompactRIO-9033 specifications.**

<b>CPU</b>	Type	Intel Atom E3825
	Number of cores	2
	CPU frequency	1.33 GHz
	On-die L2 cache	1 MB (shared)
<b>FPGA</b>	Type	Xilinx Kintex-7 7K160T
	Number of flip-flops	202,800
	Number of 6-input LUTs	101,400
	Number of DSP slices	600
	Available block RAM	11,700 kbits
	Number of DMA channels	16

The architecture of the proposed FPGA-based RTS is composed of 2 main sections: (i) the pre-processing unit, (ii) the FPGA real-time solver. The pre-processing unit is implemented in the CPU of the embedded system and dedicated to the processing and calculation of the information required by the FPGA real-time solver. This unit communicates with the development PC by an Ethernet cable to exchange data and provides the Graphical User Interface (GUI) for the developed simulator. The real-time network solver is implemented in the configurable FPGA and communicates with the processor by direct access memory (DMA). The FPGA is also coupled with I/Os to provide the external access for the input/outputs. The schematic of the developed FPGA-RTS is shown in Figure 4.2. In what follows, different units of the developed FPGA-RTS are explained.



**Figure 4.2. Hardware architecture of the developed FPGA RTS based on NI 9033.**

### 4.3 Pre-Processing Unit

The proposed real-time simulator uses EMTP-RV simulation environment as a GUI to define the network under study and its parameters. The fact that the EMTP-RV is used as a GUI to generate the *netlist* file passed to the FPGA solver, allows a straightforward validation of this latter.

Then, the designed circuit is analyzed by this software to generate the so-called *netlist* file containing all the information about the circuit components, their values, and interconnections. The *netlist* file is then used to extract the relevant information to be passed to the FPGA solver.

Since this is an offline process, it is done by the CPU of the hardware platform. The pre-processing unit is composed of different modules which are dedicated to extract the information required by the FPGA solver.

#### 4.3.1 Data\_ext

The **Data\_ext** module is implemented to read the network *netlist* file and arrange all the needed data in a two-dimensional array, so that all this information can be easily accessed by other modules. It is important to mention that certain specifications have to be met, as the algorithm reads one line at a time and compares the characters with some predefined ones. To this aim, the following terminology is adopted:

1. The nodes have to be named with the letter  $v$ , followed by the number of the node  $i$ ,  $\forall i = 1 \dots N$ , where  $N$  is the number of nodes to be considered.
2. The resistors, inductors and capacitors have to be named with the letter which indicates the type of the element (R, L, C, SW, DC or AC) followed by its corresponding number  $i$ , defined in the same way as in the previous point.
3. Transmission lines are named by  $TLMi$  where  $i$  denotes the number of the line.
4. The numbers for each element must have a consecutive order inside their element type (e.g. R1, R2, L1, C1, C2, C3, TLM1, TLM2,...).

The RLC elements are identified by the keyword “*\_RLC*” at the beginning of their corresponding line in *netlist* file. The implemented algorithm obtains the name of the elements and the names of the connected nodes and stores them in a 1D array. Then, the algorithm scans the next line and, in case of existence of an RLC element, it appends the previously generated array. The switches and the DC and

AC sources are differentiated by the keywords “\_SW”, “\_Vp” and “\_Vsine”, respectively. The procedure to obtain the data is the same as for the RLC elements.

Concerning the transmission lines, additional information such as propagation time, length, modal characteristic impedance, and losses are also extracted and augmented to the Data array. The output vector of this module (Data) is used by another modules. The flowchart of the algorithm implemented in the **Data\_ext** module to read *netlist* files is shown in Figure 4.3.

### 4.3.2 Values\_sim

This module reads the Data array generated by **Data\_ext** module and extracts the relevant simulation data. In particular, it builds the initial ANAM and determines the number of each types of elements, number of unknown node voltages, unknown branch currents (associates with inductors, switches, voltage sources, and transmission lines) and their position in the unknown vector. This information are transferred to FPGA to determine the RHS vector of MANA equation. The **Values\_sim** module inputs/outputs are shown in Figure 4.4.

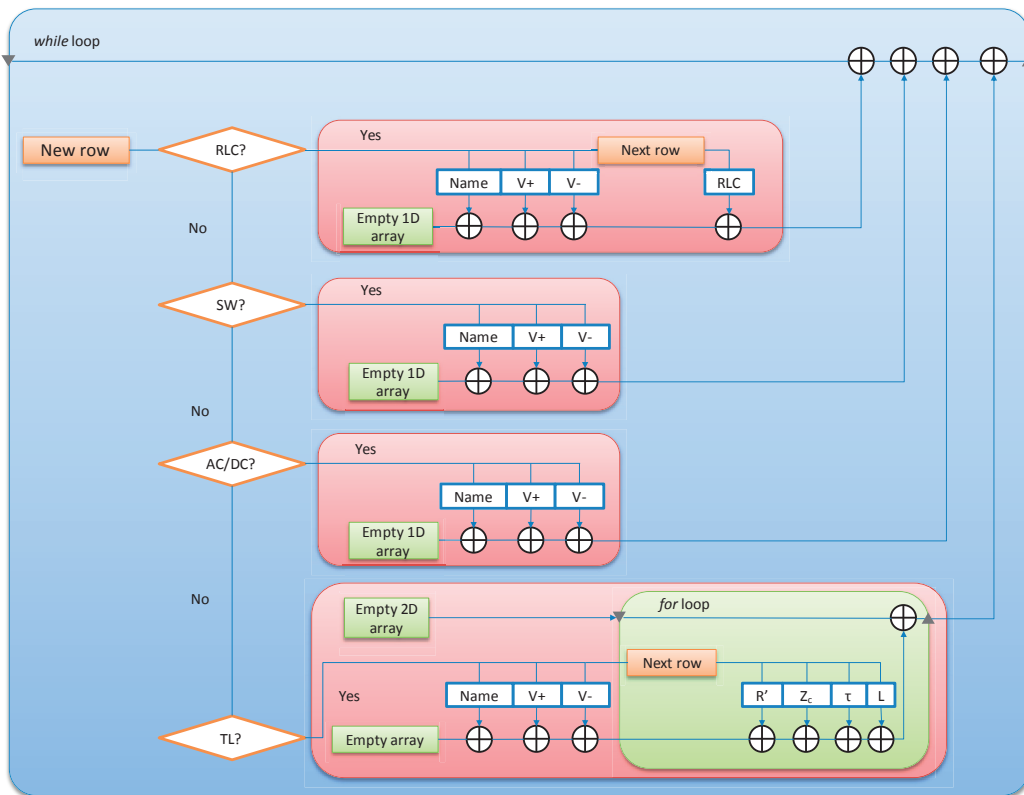


Figure 4.3. The flowchart of the algorithm implemented in the **Data\_ext** module to read *netlist* files.

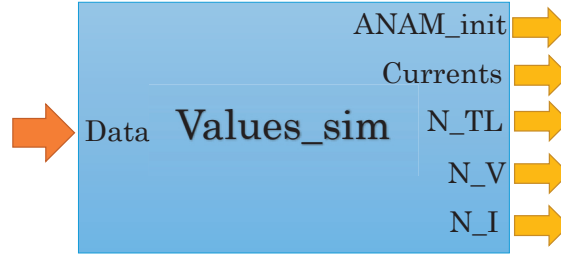


Figure 4.4. Values\_sim module input/outputs.

### 4.3.3 ANAM

The ANAM is built, inverted and transferred to the FPGA solver. This matrix is built such that the vector of unknown variables is based on the following order:

$$\left[ \left\{ V_i^N \right\}, \left\{ V_{k_1}^d, V_{m_1}^d, \dots, V_{k_{N_1}}^d, V_{m_{N_1}}^d \right\}, \left\{ V_{k_1}^c, V_{m_1}^c, \dots, V_{k_{N_2}}^c, V_{m_{N_2}}^c \right\}, \left\{ I_j^L \right\}, \left\{ I_k^{sw} \right\}, \left\{ I_n^{source} \right\}, \left\{ I_{p_1}, \dots, I_{p_{N_1+N_2}} \right\}, \dots, \left\{ I_{k_1}^d, I_{m_1}^d, \dots, I_{k_{N_1}}^d, I_{m_{N_1}}^d \right\}, \left\{ I_{k_1}^c, I_{m_1}^c, \dots, I_{k_{N_2}}^c, I_{m_{N_2}}^c \right\} \right] \quad (4.1)$$

where:

- $\left\{ V_i^N \right\}$  is the sub-array of node voltages
- $\left\{ V_{k_1}^d, V_{m_1}^d, \dots, V_{k_{N_1}}^d, V_{m_{N_1}}^d \right\}$  is the sub-array of node voltages for single-conductor transmission lines and  $N_1$  is the number of single-conductor transmission lines,
- $\left\{ V_{k_1}^c, V_{m_1}^c, \dots, V_{k_{N_2}}^c, V_{m_{N_2}}^c \right\}$  is the sub-array of modal voltages corresponding to multi-transmission lines and  $N_2$  is the number of multi-conductor transmission lines times the number of conductor in each line,
- $\left\{ I_j^L \right\}$  is the sub-array of inductors branch currents and  $j$  is the index for the inductor branch currents,
- $\left\{ I_k^{sw} \right\}$  is the sub-array of switches branch currents and  $k$  is the index for the switch branch currents,
- $\left\{ I_n^{source} \right\}$  is the sub-array of voltage sources currents being  $n$  is the index for the voltage sources,

- $\{I_{p_1}, \dots, I_{p_{N1+N2}}\}$  is the sub-array of transmission lines branch currents,
- $\{I_{k_1}^d, I_{m_1}^d, \dots, I_{k_{N1}}^d, I_{m_{N1}}^d\}$  is the sub-array of single-conductor transmission lines currents,
- $\{I_{k_1}^c, I_{m_1}^c, \dots, I_{k_{N2}}^c, I_{m_{N2}}^c\}$  is the sub-array of transmission lines modal currents.

Thus, this matrix consists of different blocks, considering the rows and columns corresponding to the sub-arrays of variables described in the above paragraph. The ANAM is built based on the network admittances and, also, additional information concerning the transmission lines (i.e., modal-to-phase transformation matrices). With  $m$  transmission lines with  $c$  conductors per line, there will be  $h=4mc$  transformation equations. The transformation matrices are imported by a specific sub-module which reads the *TLMi\_rv.out* generated files by EMTP-RV where  $i$  indicates  $i^{\text{th}}$  transmission line.

Based on the information provided by the **Data\_ext** and **Values\_sim** modules, and considering the defined variables order, the ANAM is formed as:

$$\begin{bmatrix} [a_{ii}]_{k \times n} \\ [T_{v,i}]_{h \times n} \end{bmatrix}_{n \times n} \begin{bmatrix} [x_i]_{k \times 1} \\ [x_j]_{h \times 1} \end{bmatrix}_{n \times 1} = \begin{bmatrix} [b_i]_{k \times 1} \\ [0]_{h \times 1} \end{bmatrix}_{n \times 1} \quad (4.2).$$

In (4.2),  $[a_{ii}]$  is the sub-matrix including admittances and extra rows for additional variables, and  $[T_{v,i}]$  is the sub-matrix including modal-to-phase (and vice versa) transformation matrices. Basically, the solution of the network variables corresponds to the solution of the linear equation (4.2) given by:

$$\begin{bmatrix} [x_i]_{k \times 1} \\ [x_j]_{h \times 1} \end{bmatrix}_{n \times 1} = \begin{bmatrix} [a_{ii}]_{k \times n} \\ [T_{v,i}]_{h \times n} \end{bmatrix}_{n \times n}^{-1} \times \begin{bmatrix} [b_i]_{k \times 1} \\ [0]_{h \times 1} \end{bmatrix}_{n \times 1} \quad (4.3).$$

The inputs/outputs of ANAM module is shown in Figure 4.5. It is worth noting that, this module calculates also the ANAM matrices corresponding to the open ( $[A^o]$ ) and closed states of the ( $[A^c]$ ) switches. These matrices are used by **Opt\_Gs** module to calculate the optimal conductance values of the switches.

A further operations are performed to take advantage of ANAM sparsity and to process the matrix to be used by the efficient matrix to vector multiplier implemented in FPGA. The details of these extra processes will be given in subsection 4.4.2.

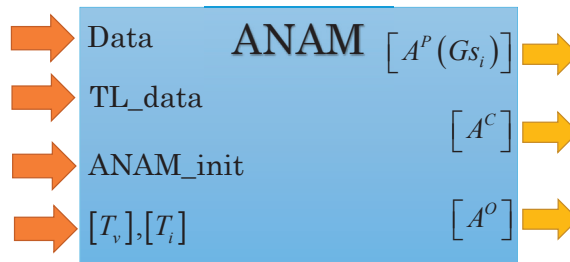


Figure 4.5. ANAM module inputs/outputs.

#### 4.3.4 Opt\_Gs

This module is dedicated to calculate the optimal value of the ADC switch parameters. In particular, the method proposed in Chapter 3 for the assessment of the optimal ADC switch parameter is implemented. Therefore, the Data array provided by the **Data\_ext** module is used together with the  $[A^p(G_s)]$ ,  $[A^o]$ ,  $[A^c]$  matrices calculated by **ANAM**. Then, all the calculated optimal values  $G_{s_i}$  for all switches are stored in an array to be transferred to the FPGA solver. Furthermore, these values are used to update the initial ANAM to generate the final one. The inputs and outputs of this sub-module is shown in Figure 4.6.

#### 4.3.5 TL\_coeff

The transmission lines RHS elements are calculated based on a weighted sum of both the modal voltages and the modal currents of each one of them with respect to the impedance coefficients described in (4.4)-(4.7). Furthermore, additional variables are necessary for the interpolation equations associated with the transmission line (equation (4.8)). Since these coefficients are constant during simulation, they can be computed in the offline stage of the simulator and transferred to the FPGA solver.

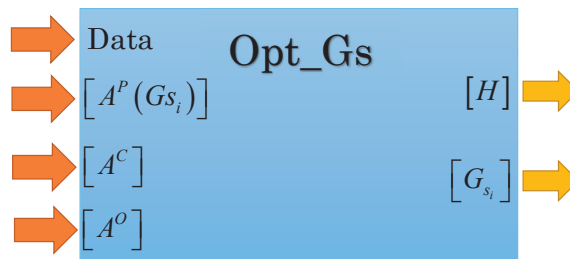


Figure 4.6. Opt\_Gs module inputs/outputs.

The calculated coefficients are as follows:

$$K_1^{\rho,i} = \frac{Z_C^{\rho,i}}{(Z_C^{\rho,i} + R^{\rho,i}/4)^2} \quad (4.4)$$

$$K_2^{\rho,i} = \frac{Z_C^{\rho,i}}{(Z_C^{\rho,i} + R^{\rho,i}/4)^2} \times (Z_C^{\rho,i} - R^{\rho,i}/4) \quad (4.5)$$

$$K_3^{\rho,i} = \frac{R^{\rho,i}/4}{(Z_C^{\rho,i} + R^{\rho,i}/4)^2} \quad (4.6)$$

$$K_4^{\rho,i} = \frac{R^{\rho,i}/4}{(Z_C^{\rho,i} + R^{\rho,i}/4)^2} \times (Z_C^{\rho,i} - R^{\rho,i}/4) \quad (4.7).$$

In these equations,  $Z_C^{\rho,i}$  is the characteristic impedance and  $R^{\rho,i}$  is the resistance representing the lumped losses in the CP line model. Superscripts  $\rho$  and  $i$  denote the corresponding mode and the number of the transmission line, respectively.

Furthermore, the linear interpolation coefficients as well as the length of the circular buffers dedicated for the travelling time delays associated with each transmission line mode are calculated (see Section 4.4 for the relevant transmission lines model) using:

$$\begin{aligned} \tau^{\rho,i} &= p^{\rho,i} \Delta t + \varepsilon_1^{\rho,i} \\ \varepsilon_2^{\rho,i} &= \Delta t - \varepsilon_1^{\rho,i} \\ \alpha_0^{\rho,i} &= \varepsilon_2^{\rho,i} / \Delta t \\ \alpha_1^{\rho,i} &= \varepsilon_1^{\rho,i} / \Delta t \end{aligned} \quad (4.8).$$

These values are stored in the dedicated memories to be transferred to the FPGA solver.

Once all these data are properly computed by the specific sub-modules, they are forwarded to the FPGA solver. While some small portion of data is directly sent as individual elements, arrays or clusters, the other larger arrays (such as line coefficients) are sent using a DMA-FIFO memory. This allows saving resources and increasing the computation efficiency of the FPGA solver.

## 4.4 FPGA-Based Real-Time Solver

As already discussed, the main reason to move towards FPGA-based real-time simulators is the inherent massive parallel computational power. Therefore, the FPGA solver has to have a parallel structure. However, the solution of (4.3)



requires two inherent sequential steps: (i) solving the linear algebraic equations to find the unknown voltages and currents and, (ii) updating the RHS vector based on the calculated values in step (i). These two tasks are dependent and cannot be solved in parallel. Nevertheless, within each step, the following parallel sub-tasks can be identified: (a) RHS computation for lumped elements and switches, (b) RHS computation for transmission lines, (c) nodal matrix to RHS vector multiplication. The FPGA-based calculations can be performed based on fixed-point (FXP) or Floating-Point (FP) numerical representations. First, a brief introduction to the FXP or FP numerical representations is presented.

#### 4.4.1 Numerical Representation

The adopted numerical representation of variables impacts dramatically the performance, hardware utilization, and accuracy of the FPGA design. FP-based calculation has the advantages of dynamic range and higher accuracy. However, FP-based computations take longer execution time and require more hardware resources to implement. As known, an FP number has three parts (Figure 4.7): a mantissa, exponent, and sign bit. The mantissa contains the decimal number in scientific notation scaled to the power specified by the exponent.

An FXP number has two parts (Figure 4.8): an integer (which may contain a sign bit) and a fraction. The integer and fractional parts represent the portion of the number before and after the decimal point, respectively. In this representation, this point between the integer and fraction is called the radix point.

In LabVIEW FPGA, when configuring an FXP data type, one specifies the word length (total number of bits for the fixed-point representation) and the integer length (number of bits in the integer portion of the FXP representation). The leftover bits are for the fraction, such that the integer plus the fraction equals the word length. The maximum allowed word length is 64 bits.

Although FP numerical representation provides higher dynamic range of the variables and more precise results, FP-based FPGA architectures require higher hardware utilization and represent slower performances [105]. However, it is possible to achieve the desired computational accuracy by carefully selecting the FXP numerical representation. The developed FPGA solver is mainly based on FXP numerical representation. Thanks to the normalized simulation variables, and by careful configuration of the word length and radix point, FXP is able to provide sufficient simulation results accuracy. Nevertheless, there is a possibility to use FP calculations by scarifying the computation time.

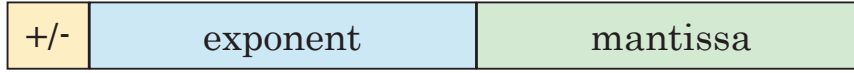


Figure 4.7. FP numerical representation.

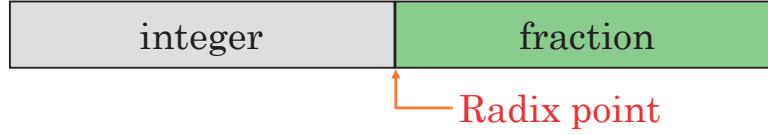


Figure 4.8. FXP numerical representation.

#### 4.4.2 Efficient Matrix-to-Vector Multiplier

Matrix-to-vector multiplication is the core of the real-time simulator which consumes significant amount of resources and simulation time. Thanks to FAMNM switch representation, the ANAM is constant during the simulation. Thus, it is computed once in the pre-processing unit, inversed and transferred to the FPGA solver.

The main characteristic of the ANAMs associated with power system networks is their sparsity [74]. Therefore, in order to save both computation time and hardware resources, it is essential to consider this important peculiarity of the ANAM. To this end, an efficient matrix-to-vector multiplier is developed. The developed algorithm takes advantage of the ANAM sparsity to accelerate the multiplication and reduce the hardware usage. The created ANAM based on (4.3) is analyzed to extract the useful information and re-process the ANAM and RHS vector. It is worth mentioning that, the proposed matrix to vector multiplier is exact in the sense that, the method does not involve approximation in the multiplication process.

To explain the developed sparse matrix to vector multiplier, let us consider a simple example:

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} = \underbrace{\begin{bmatrix} 2 & 0 & 5 & 0 \\ 0 & 0 & 4 & 1 \\ 0 & 3 & 0 & 4 \\ 7 & 0 & 0 & 0 \end{bmatrix}}_{ANAM^{-1}} * \underbrace{\begin{bmatrix} 1 \\ 2 \\ 4 \\ 0 \end{bmatrix}}_{RHS} \quad (4.9).$$

The first step of the proposed algorithm is to look at the row index of the zero elements of the RHS vector and replace the corresponding columns in the  $ANAM^{-1}$  matrix. In our example, the fourth row of the RHS is zero, thus the fourth column of the  $ANAM^{-1}$  will be replaced by zeros. Our new equation is the following:

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} = \underbrace{\begin{bmatrix} 2 & 0 & 5 & 0 \\ 0 & 0 & 4 & 0 \\ 0 & 3 & 0 & 0 \\ 7 & 0 & 0 & 0 \end{bmatrix}}_{ANAM^{-1}} * \underbrace{\begin{bmatrix} 1 \\ 2 \\ 4 \\ 0 \end{bmatrix}}_{RHS} \quad (4.10).$$

Now we will represent each nonzero element of the  $ANAM^{-1}$  as a set of triplets with its information on the row and the column. We will also do the same for the RHS representing it as a couple with the information on the row index. The decomposed  $ANAM^{-1}$  and RHS are shown in Table 4.2 and Table 4.3.

For each row of the  $ANAM^{-1}$ , we can put next to each other the value and the column index of the  $ANAM^{-1}$  next the corresponding row index of the RHS and its value. Now, the  $ANAM^{-1}$  values that will be multiplied to the RHS values are next to each other. The  $ANAM^{-1}$  mapping is shown in Table 4.4.

**Table 4.2. Decomposed  $ANAM^{-1}$ .**

Value	Row index	Column index
2	1	1
5	1	3
4	2	3
3	3	2
7	4	1

**Table 4.3. Decomposed RHS.**

Value	Row index
1	1
2	2
4	3

**Table 4.4.  $ANAM^{-1}$  mapping based on RHS elements.**

$ANAM^{-1}$			RHS	
Row index	Value	Column index	Row index	Value
1	2	1	1	1
1	5	3	3	4
2	4	3	3	4
3	3	2	2	2
4	7	1	1	1

Since, the RHS vector is a variable one being updated at each simulation time-step, we only need to know the corresponding row indices of the RHS elements with respect to the each row of the ANAM<sup>-1</sup>. Thus, we can remove unnecessary information such as the ANAM<sup>-1</sup> column indices and the RHS values. It is worth noting that, since the elements of RHS vector are updated at each iteration, they cannot be stored in the fixed memories. Furthermore, the RHS vector needs to be reused by the Multiplication and Accumulation (MAC) operator corresponding to each row of ANAM<sup>-1</sup>. The RHS vector duplication for each row occupies significant FPGA resources. Therefore, only the necessary RHS row indices are stored in the memory and the RHS sub-vector associated with each row of ANAM<sup>-1</sup> is reconstructed based on these indices. Now, the mapping is shown in Table 4.5.

Since, in some rows there might be more than one nonzero element, for a given  $x_i$  in (4.10), more than one step MAC operations might be needed.

**Table 4.5. ANAM<sup>-1</sup> and RHS elements mapping by removing redundant information.**

ANAM <sup>-1</sup>		RHS
Row	Value	Row index
1	2	1
1	5	3
2	4	3
3	3	2
4	7	1

Therefore, it is required to use a MAC function with variable iterations ( $N_{xi}$ ) where  $N_{xi}$  is the number of nonzero elements corresponding to the  $i^{th}$  row of the modified ANAM<sup>-1</sup> described by (4.10). Using variable size loops in FPGAs results in significant hardware usage and non-optimal FPGA performance. Therefore, it is necessary to use fixed iterations for different rows of ANAM<sup>-1</sup>. One possibility to overcome this issue is to determine the maximum required number of iterations and for the rows who have fewer nonzero elements than this maximum number, zeros are added. Although, this might seem to be inefficient, overall, the hardware usage and the performance is better than the variable size iterations.

For the considered example, since the maximum number of nonzero elements in one row of (4.10) is 2, the other rows are augmented by adding zeros. Table 4.6 shows the mapping with the number of required iteration within each row of ANAM<sup>-1</sup>.

Table 4.7 shows the final mapping with fixed size iterations and added zeros.

**Table 4.6. ANAM<sup>-1</sup> and RHS elements mapping with respect to the number of iterations in each row.**

ANAM <sup>-1</sup>		RHS
Nr. Of iterations	Value	Row index
2	2	1
-	5	3
1	4	3
1	3	2
1	7	1

**Table 4.7. ANAM<sup>-1</sup> and RHS elements mapping for the fixed size iterations by adding zeros.**

ANAM <sup>-1</sup>		RHS
Nr. Of iterations	Value	Row index
2	2	1
	5	3
2	4	3
	0	0
2	3	2
	0	0
2	7	1
	0	0

The calculated ANAM<sup>-1</sup> in (4.3) is processed by following the same algorithm and by making reference to Table 4.7, two sets of data are needed to be stored and transferred to the FPGA solver: (i) the values of ANAM<sup>-1</sup>, and (ii) the corresponding row indices of RHS vector. The first set is stored in the memory by using proper FXP numerical configuration. The row indices of RHS vector are stored in the memory using unsigned integer numbers.

For every  $x_i$  in (4.10), based on the row indices of Table 4.7 the associated RHS sub-vector is built and the MAC is performed between the ANAM<sup>-1</sup> and corresponding RHS elements, using the fixed iteration size. Table 4.8 shows the performance and hardware usage of the normal (but computationally optimized) matrix-to-vector-multiplier compared to the developed sparse efficient one. It can be observed, the proposed sparse matrix to vector multiplication method improves the performance while decreasing significantly the FPGA hardware usage.

**Table 4.8. Performance and hardware usage comparison of the sparse and non-sparse matrix to vector multipliers**

	Latency	Slice Registers	Slice LUTs	DSP48s
<b>Non-sparse method</b>	184 cycles	10.1%	39.4%	48.5%
<b>Sparse method</b>	166 cycles (-10%)	4.7% (-53%)	15.5% (-60%)	6.7% (-86%)

### 4.4.3 RHS Vector Update

As stated earlier, the ANAM is built based on the order for the unknown vector described in (4.1). Based on this order, and by taking advantage of the parallel computation capability of FPGAs, dedicated sub-tasks devoted to update the RHS for the particular type of element are considered.

#### Lumped Elements

The RHS variables for the lumped ( $L, C$ ) elements are function of corresponding node voltages and branch currents in the previous time step (the RHS element for the resistor is zero). Therefore, the required values to compute RHS elements are stored in the FPGA memory to be accessed in the next iteration. Then, the stored variables are used to update the RHS elements. It is worth observing that, in the CPU-based real-time simulators, the update of the RHS elements is done sequentially for different types of elements. However, thanks to the inherent parallel processing capability of the FPGA, these tasks are done in parallel. For inductors and capacitors, a dedicated computational unit has been implemented. The RHS elements for the inductors and capacitors can be expressed by the general equation (4.11):

$$I_{His\_L_i, C_i}^{n+1} = \gamma_{L_i, C_i} x_i^n \quad (4.11)$$

where  $I_{His\_L_i, C_i}^{n+1}$  is the history element for the  $i^{th}$  inductor or capacitor in the current time step,  $\gamma_{L_i, C_i}$  is the coefficient corresponding to the  $i^{th}$  inductor (or capacitor) and  $x_i^n$  is the inductor (or capacitor) state variable in the previous time step. For the case of inductors,  $\gamma_{L_i, C_i} = 1$ ,  $x_i^n = i_{L_i}^n$ , and for the capacitors  $\gamma_{L_i, C_i} = -\frac{C_i}{\Delta t}$ ,  $x_i^n = v_{C_i}^n$ .

Equation (4.11) needs to be executed  $N_c + N_L$  times, where  $N_c$  and  $N_L$  are the number of capacitors and inductors, respectively. However, they can be decoupled into  $N_c$  and  $N_L$  independent and parallel operations. Therefore, two levels of parallelism can be applied in this sub-module in order to accelerate the

computations: (i) parallel updating of the RHS for capacitors and inductors, and (ii) parallel calculation of RHS for individual inductors and capacitors. The RHS computation unit dedicated for the inductors and capacitors is shown in Figure 4.9.

### Switches

The RHS elements of the switches are calculated using another dedicated sub-module. After calculating the optimal conductance values in the offline pre-processing, these values are transferred to the FPGA to be used in this sub-module.

Then, according to the switches states and by accessing to their voltages and currents, the RHS elements are calculated as [130]:

$$J_{sw_i}^{n+1} = \begin{cases} -i_{s_i}^n & s^{n+1} = 1 \\ G_{s_i} v_{s_i}^n & s^{n+1} = 0 \end{cases} ; i = 1, \dots, N_{sw} \quad (4.12)$$

where  $J_{sw_i}^{n+1}$  is the RHS variable for the  $i^{th}$  switch,  $i_{s_i}^n$  is the  $i^{th}$  switch current,  $v_{s_i}^n$  is the  $i^{th}$  switch voltage,  $G_{s_i}$  is the  $i^{th}$  switch optimal conductance value,  $s^{n+1}$  is the switch current state, and  $N_{sw}$  is the number of switches. A specific sub-block is considered to update the switch status, based on the switch type (e.g., diode, IGBT-diode pair). Similar to the lumped elements, the RHS ones for the switches are calculated in parallel. The only difference in the RHS computation for this element is that it accounts for the switch state.

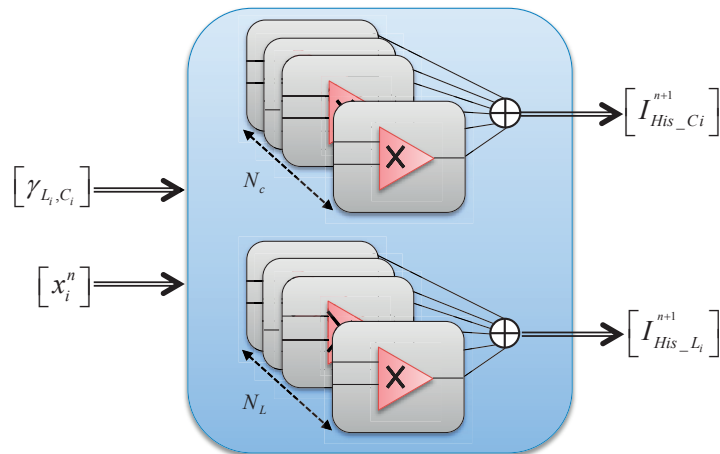


Figure 4.9. RHS computation module for lumped elements.

### Independent Sources

The RHS values for the independent sources, depending on the application, are either imported from the real analog input module, or calculated inside the solver. These values are inserted into the RHS vector in parallel and independently.

### Transmission Lines

Multi-conductor transmission lines are transformed into single conductor equivalents by using the phase-to-modal transformation matrices. These transformation matrices are imported from the EMTP-RV generated data files by the pre-processing unit and then are used to build the ANAM. The RHS element for each decoupled mode of multi-conductor transmission line is defined as [74]:

$$I_K^{\rho,i}(t-\tau) = K_1^{\rho,i} \times V_m^{\rho,i}(t-\tau^{\rho,i}) + K_2^{\rho,i} \times I_{mk}^{\rho,i}(t-\tau^{\rho,i}) + K_3^{\rho,i} \times V_k^{\rho,i}(t-\tau^{\rho,i}) + K_4^{\rho,i} \times I_{km}^{\rho,i}(t-\tau^{\rho,i}) \quad (4.13)$$

$$I_M^{\rho,i}(t-\tau) = K_1^{\rho,i} \times V_k^{\rho,i}(t-\tau^{\rho,i}) + K_2^{\rho,i} \times I_{km}^{\rho,i}(t-\tau^{\rho,i}) + K_3^{\rho,i} \times V_m^{\rho,i}(t-\tau^{\rho,i}) + K_4^{\rho,i} \times I_{mk}^{\rho,i}(t-\tau^{\rho,i}) \quad (4.14)$$

where  $K_1^{\rho,i}$ ,  $K_2^{\rho,i}$ ,  $K_3^{\rho,i}$ ,  $K_4^{\rho,i}$  are the impedance coefficients defined in (4.4)-(4.7).

In the discrete-time domain, since  $\tau^{\rho,i}/\Delta t \notin N$ , an interpolation technique is needed to calculate the intermediate values. Therefore, for the case of a linear interpolation [131], the RHS element for each mode of each transmission line is:

$$\left(I_K^{\rho,i}\right)^{n-p} = \alpha_0^{\rho,i} \times f_1(n-p^{\rho,i}) + \alpha_1^{\rho,i} \times f_1(n-p^{\rho,i}-1) \quad (4.15)$$

$$\left(I_M^{\rho,i}\right)^{n-p} = \alpha_0^{\rho,i} \times f_2(n-p^{\rho,i}) + \alpha_1^{\rho,i} \times f_2(n-p^{\rho,i}-1) \quad (4.16)$$

where:

$$f_1(n-p^{\rho,i}) = K_1^{\rho,i} \times V_m^{\rho,i}(n-p^{\rho,i}) + K_2^{\rho,i} \times I_{mk}^{\rho,i}(n-p^{\rho,i}) + K_3^{\rho,i} \times V_k^{\rho,i}(n-p^{\rho,i}) + K_4^{\rho,i} \times I_{km}^{\rho,i}(n-p^{\rho,i}) \quad (4.17)$$

$$f_2(n-p^{\rho,i}) = K_1^{\rho,i} \times V_k^{\rho,i}(n-p^{\rho,i}) + K_2^{\rho,i} \times I_{km}^{\rho,i}(n-p^{\rho,i}) + K_3^{\rho,i} \times V_m^{\rho,i}(n-p^{\rho,i}) + K_4^{\rho,i} \times I_{mk}^{\rho,i}(n-p^{\rho,i}) \quad (4.18)$$

and the interpolation coefficients are calculated as (4.8).



Note that there is an inherent feature in (4.15) and (4.16) which enables the pipelining of these equations reducing the FPGA resources usage. Namely, in (4.15) and (4.16),  $f_1(n - p^{\rho,i} - 1)$  has been already calculated in the previous time step and stored in the memory. Therefore, for each RHS element, this function needs to be calculated once.

In order to apply the travelling time delay to each propagation mode, dedicated dynamic circular buffers are considered for each mode of each transmission line. LabVIEW-FPGA built-in FIFOs are used as the circular buffers since they provide an inherent capability to impose the travelling time delay to the transmission lines voltages and currents. For a FIFO with size  $p$ , the element written at iteration  $n$  will be exported again at iteration  $p+n$ . This inherent write-and-shift capability of the FIFO enables straightforward implementation of the circular buffers to impose time delays corresponding to the travelling times associated with different modes of the transmission lines.

The initial size of the FIFOs is determined long enough such that it covers the possible longest line in the network. Then, in the simulation initialization, based on the exact line length, the corresponding FIFO is initialized with  $p^{\rho,i}$  zeros, which is defined as (4.8). In particular, the size of these circular buffers is determined by  $p^{\rho,i}$  which is pre-computed in the pre-processing. The designed dynamic circular buffers allow the dynamic changing of the buffer size without the need of modifying the FPGA code (i.e., it is possible to change the transmission lines lengths). The structure of a FIFO circular buffer is shown in Figure 4.10. This RHS computation procedure for the transmission lines is shown in Figure 4.11.

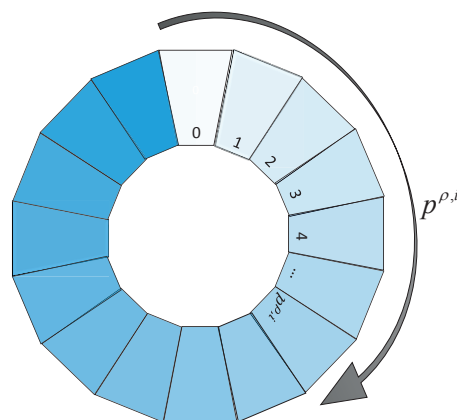


Figure 4.10. Structure of the transmission lines circular buffers using FIFOs.

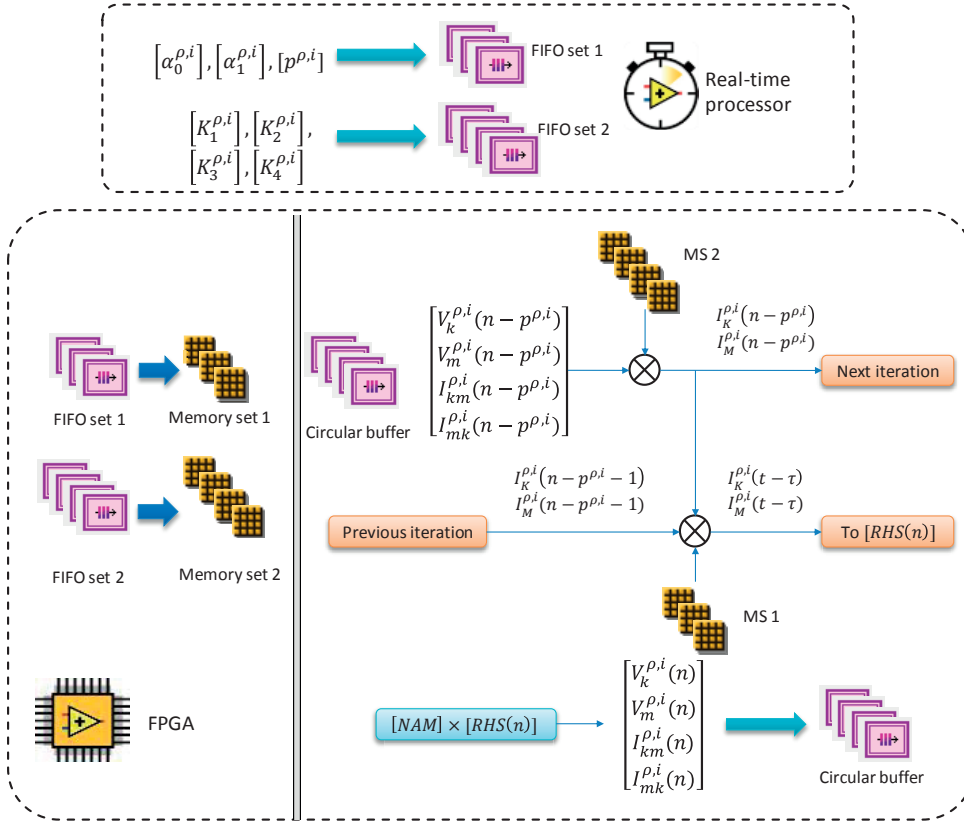


Figure 4.11. RHS computation for the transmission lines.

## 4.5 Validation Examples

In order to validate the performances of the developed FPGA-based real-time simulator, three case studies have been considered: (i) HIL analysis of the switching transients into a two-level three-phase inverter, (ii) analysis of the fault-originated electromagnetic transients in a multi-terminal HVDC network, and (iii) analysis of the fault-originated electromagnetic transients in a three-phase transmission network.

### 4.5.1 HIL Validation of a Two-Level Three-Phase Converter

To validate the performance of the developed FPGA-based real-time simulator, we have adopted the experimental test setup in which power components are composed of a two-level three-phase inverter connected to an inductive filter (10 mH) and a resistive load (20  $\Omega$ ). The global setup is depicted in Figure 4.12. It shows three main parts: the system under study (which can be an FPGA based real-time model or a real inverter), the DS 1104 controller board and the HMI (human machine interface).

A classical  $dq$  synchronous frame current controller (e.g. [136]) has been used and implemented in a DS1104 controller board with a PowerPC 603e@250 MHz, 16bit ADC and a sampling rate of  $2\mu\text{s}$  (time step of the controller has been fixed to  $50\mu\text{s}$ ). The real inverter is a three-phase two-level inverter based on SEMIKRON SKM75GB123d, and the current sensors are E3n sensors from fluke, with a bandwidth of 100kHz and a precision of  $\pm 3\%$  ( $-3\text{dB}$ ). The modeled circuit with the MANA variables and the picture of this setup and the schematic representation of are shown in Figure 4.13 and Figure 4.14, respectively.

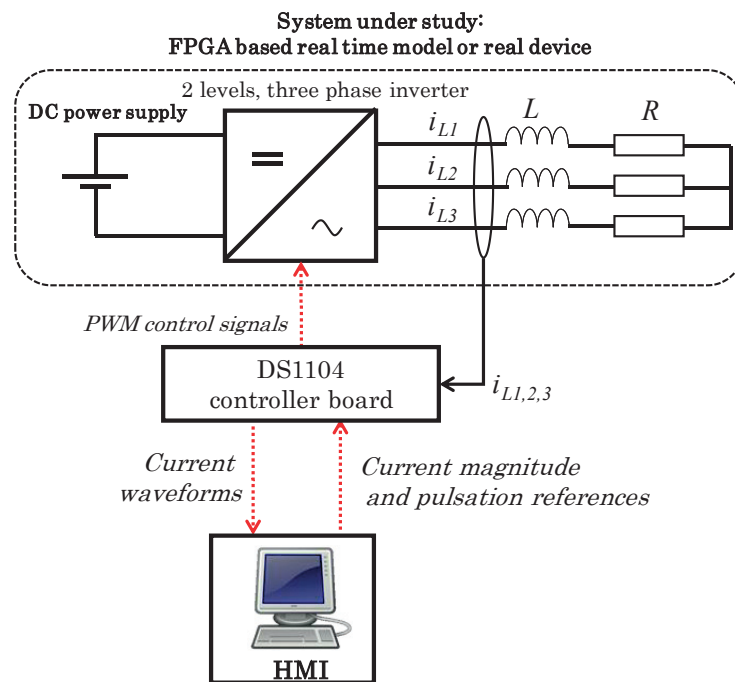


Figure 4.12. Schematic representation of the HIL setup.

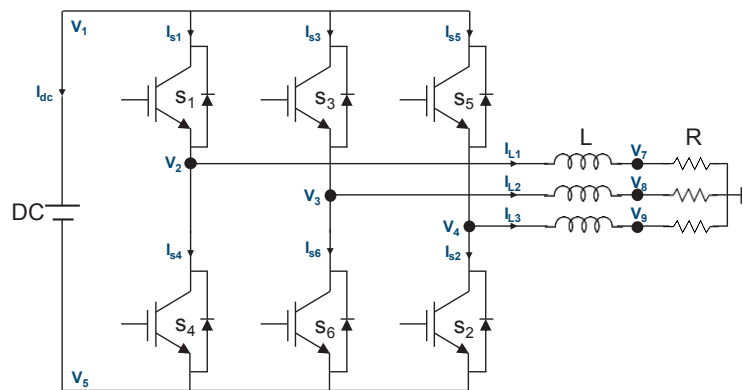


Figure 4.13. Schematic representation of the considered two-level three-phase inverter and MANA variables.

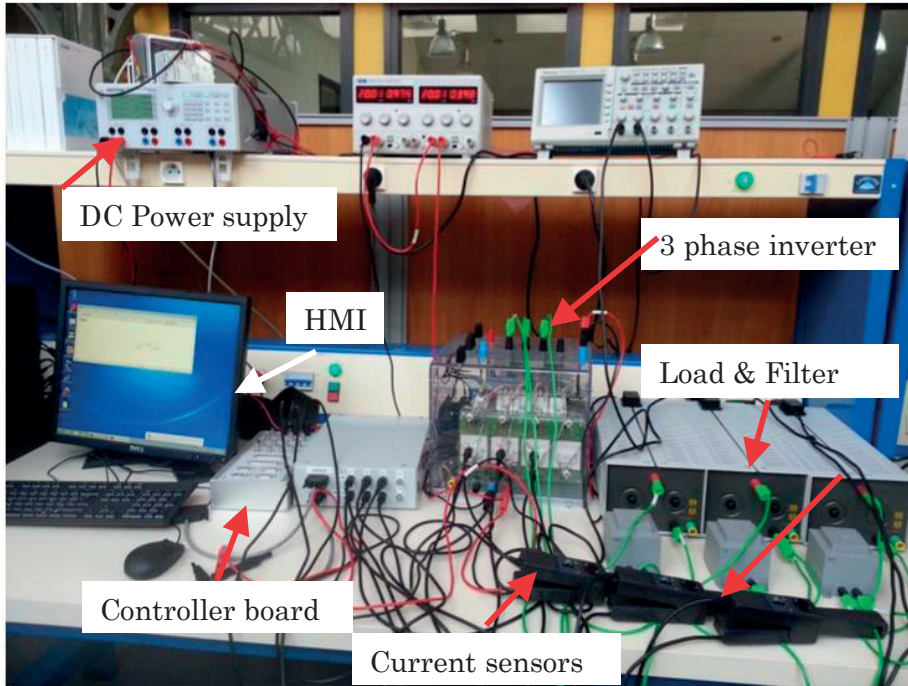


Figure 4.14. HIL test setup.

Since the FPGA solver is based on FXP numerical representation and as a consequence, it limits the amplitude of the simulation variables, the per-unit model of this circuit is derived based on the following base values:

$$\begin{aligned} V_{base} &= 60 \text{ V} \\ I_{base} &= 10 \text{ A} \end{aligned} \quad (4.19).$$

Then, the pre-processing unit analyzes the EMTP-RV generated *netlist* file and builds the corresponding ANAM as equation (4.20). This matrix is inverted and converted to the FXP representation based on 40 bits for the word length and 19 bits for the integer part.

The optimization process to find the optimal values for the switch conductances is performed in the pre-processing phase. By considering the switching modes where each switch conducts for 180 degrees of a cycle, there are eight possible switching permutations: (S1,S2,S6), (S1,S2,S3), (S2,S3,S4), (S3,S4,S5), (S4,S5,S6), (S1,S5,S6), (S1,S3,S5), and (S2,S4,S6). Therefore, we obtain eight ANAM corresponding to each status of the ideal switches. Among them, six switching patterns generate a non-zero voltage across the load and two of them (the upper or lower switches are conducting) generate zero voltage across the load.

According to the method presented in Chapter 3, the first step to calculate the optimal value for the switch conductance is to find the sets of eigenvalues corresponding to the possible switching permutations and also, the ones of the FAMNM.

$$\begin{bmatrix}
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & -1 & 0 & 0 & 1 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 & 0 & 0 & 1 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & -1 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & -1 & 0 & -1 \\
 0 & 0 & 0 & 0 & 0 & \frac{1}{R} & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{R} & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{R} & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & -G_{eqL1} & 0 & 0 & 0 & 0 & G_{eqL1} & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & -G_{eqL2} & 0 & 0 & 0 & 0 & G_{eq2} & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & -G_{eqL3} & 0 & 0 & 0 & 0 & G_{eq3} & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
 G_{s1} & -G_{s1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & G_{s2} & -G_{s2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\
 G_{s3} & 0 & -G_{s3} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 \\
 0 & G_{s4} & 0 & 0 & -G_{s4} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 \\
 G_{s5} & 0 & 0 & -G_{s5} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\
 0 & 0 & G_{s6} & 0 & -G_{s6} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\
 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
 \end{bmatrix}
 \begin{bmatrix}
 V_1^{n+1} \\
 V_2^{n+1} \\
 V_3^{n+1} \\
 V_4^{n+1} \\
 V_5^{n+1} \\
 V_6^{n+1} \\
 V_7^{n+1} \\
 V_8^{n+1} \\
 J_{L1}^{n+1} \\
 J_{L2}^{n+1} \\
 J_{L3}^{n+1} \\
 J_{S1}^{n+1} \\
 J_{S2}^{n+1} \\
 J_{S3}^{n+1} \\
 J_{S4}^{n+1} \\
 J_{S5}^{n+1} \\
 J_{S6}^{n+1} \\
 J_{dc}^{n+1}
 \end{bmatrix}
 =
 \begin{bmatrix}
 0 \\
 0 \\
 0 \\
 0 \\
 0 \\
 0 \\
 0 \\
 0 \\
 J_{His\_L1}^{n+1} \\
 J_{His\_L2}^{n+1} \\
 J_{His\_L3}^{n+1} \\
 J_{SW1}^{n+1} \\
 J_{SW2}^{n+1} \\
 J_{SW3}^{n+1} \\
 J_{SW4}^{n+1} \\
 J_{SW5}^{n+1} \\
 J_{SW6}^{n+1} \\
 V_{dc}^{n+1}
 \end{bmatrix}
 \quad (4.20).$$

It is worth noting that, since the load and filter parameters are identical for all the phases, the eigenvalues for the two sets of patterns are equal for each set.

Therefore, in view of the symmetrical nature of the circuit, one identical conductance value can be assigned to the six switches. By applying the optimization method, the objective function exhibits an optimal value of  $G_s=0.51$  (see Chapter 3). This value is used to build the ANAM and also update the switches RHS elements.

It is worth noting that, in order to achieve extremely low simulation time steps, the FPGA solver architecture is modified such that maximum parallel computations are achieved. In particular, the matrix-to-vector-multiplier is implemented using the highest level of parallel operations.

The switching PWM controller is also implemented into the FPGA (in parallel with the solver). The total utilized FPGA hardware resources including the implemented PWM controller is shown in Table 4.9.

Concerning the achieved integration time step, the simulation needs 6 FPGA ticks per time step. Consequently, by considering the 40 MHz FPGA clock, it results into an integration time step of **150 ns**.

Concerning the accuracy assessment, Figure 4.15 illustrates the three-phase load currents in a half period duration obtained by the FPGA-based real-time simulator, and by EMTP-RV off-line simulation environment, respectively. In this figure, the PWM carrier frequency is 1 kHz. Figure 4.16 shows the error between the load currents of the benchmark model and the ones of the FPGA simulator. The error is calculated based on the per-unit values of the load currents in two different simulations. It can be inferred by post-processing that the FPGA-based results are characterized by an extremely contained maximum error of only **0.0002 pu**. The reasons behind this small error are two: (i) the truncation realized by the FXP simulation calculations, and (ii) the ADC switch model which, as known, introduces approximations in the simulation results.

Table 4.9. FPGA hardware usage for the HIL test case.

Resource	Utilized percentage
Slice registers	10.1
Slice LUTs	28
Block RAMs	1.5
DSP48s	85.3

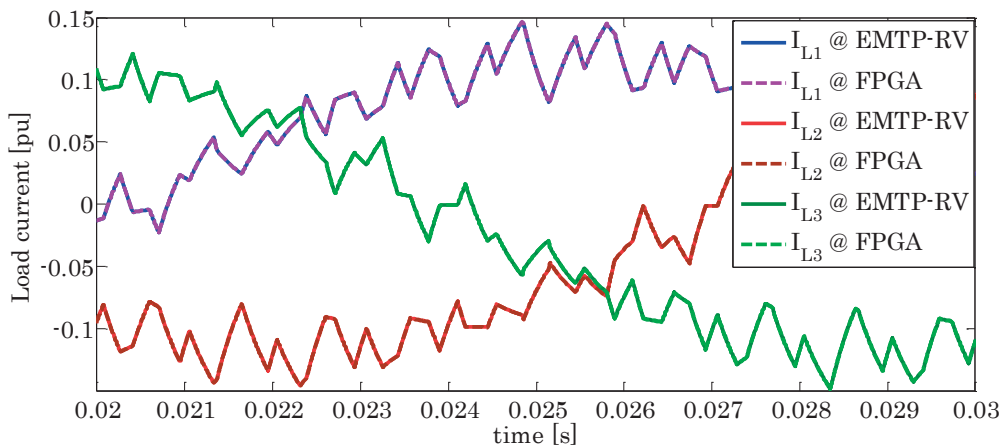
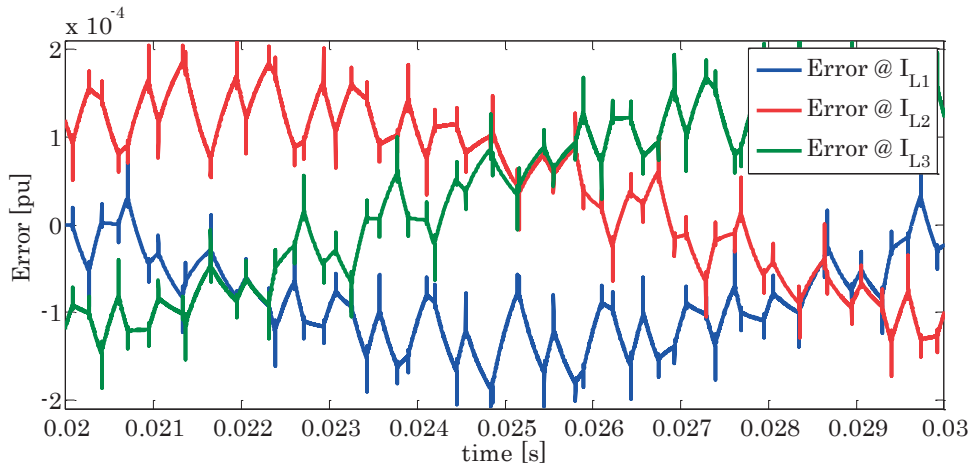


Figure 4.15. Comparison of the FPGA-based real-time solver results with the corresponding EMTP-RV ones (three-phase load currents).



**Figure 4.16. Error of the load currents (reference values of Figure 4.15).**

A further validation test is performed by making reference to an HIL simulation test using the proposed FPGA-based real-time simulator. To this end, first, the experimental setup described previously is used to perform the HIL test with the proposed real-time simulation platform. The external PWM controller (the PWM frequency is 1 kHz) is coupled with the simulator by using digital input modules. In particular, the switches gate signals are determined by NI-9401 which is a high-speed digital I/O module and the gate signals loop and the simulation one are synchronized. To export the simulation generated signals, NI-9263 is used which is an analog output module. Since, the maximum sampling rate of this module is 100 kHz, the generated load current signals are down-sampled by this frequency to be monitored in the oscilloscope.

Then, the same controller is coupled with a physical inverter which is connected to the physical inductive filter and resistive load with the same value of the HIL simulation. The controller type and parameters are identical to the ones of the HIL test. The load currents are measured by using the current sensors described earlier and are observed by the oscilloscope. The schematic of the HIL validation setup is shown in Figure 4.17.

Figure 4.18 shows the comparison of the HIL simulation results and the measured waveforms for the three phase load currents in a half a period. Figure 4.19 shows the errors between the HIL simulation results and the measured waveforms. It can be observed that the HIL simulation results are in very good agreement with the measurements with obvious higher errors compared to the offline simulations. The reasons for this error are: (i) the presence of noise in the measurements, (ii) the limited current sensors bandwidth, (iii) the error associated with adopted models used for the converter filter and load, and (iv) the non-linear behavior of the switches in the real inverter compared to the linear switch model in the HIL simulation. However, in spite of the above-listed sources of errors, the comparison

## 4.5 Validation Examples

appears very satisfactory providing an experimental validation of the proposed FPGA simulation platform.

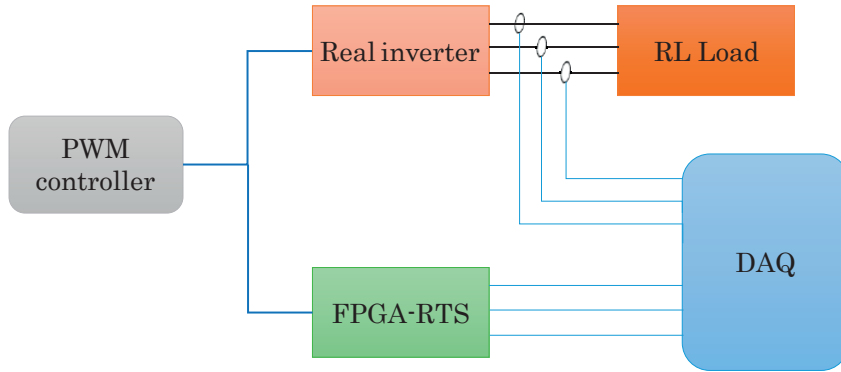


Figure 4.17. The schematic of the HIL validation setup.

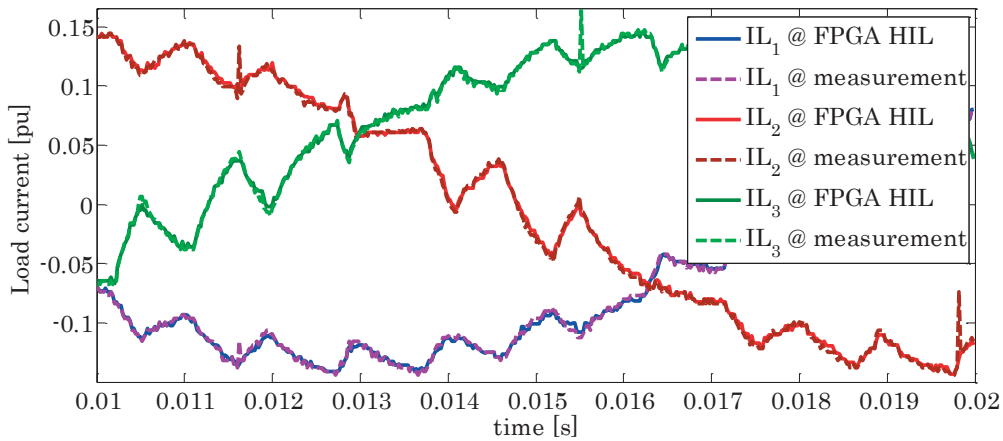


Figure 4.18. Comparison of the FPGA-based HIL test results with the measured ones (three-phase load currents).

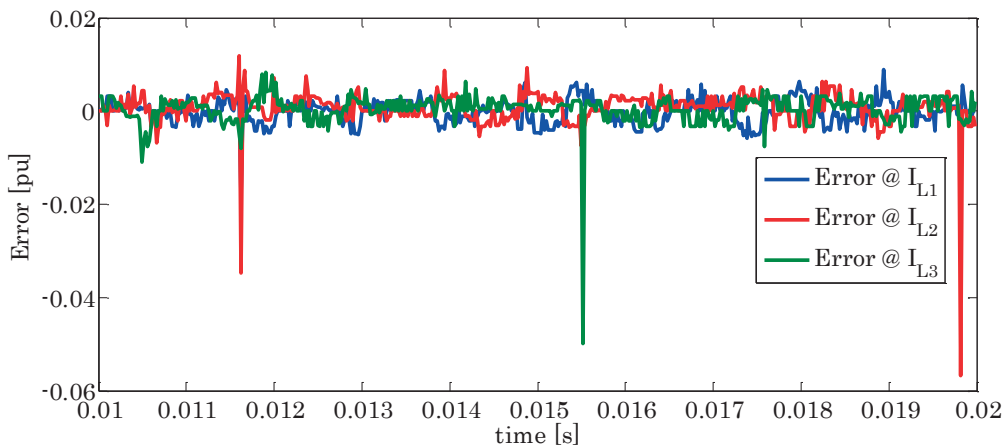


Figure 4.19. Error of the load currents in pu. (reference values of Figure 4.18).



#### 4.5.2 Fault Originated Transients in Multi-Terminal HVDC Network

The second case study refers to a multi-terminal HVDC (MTDC) network composed of five transmission lines terminated to five power converter stations as shown in Figure 4.20. The transmission lines are characterized by two conductors and each line is segmented into two sections in order to have a possibility of applying a fault at any arbitrary position along each line. Therefore, the total network is composed of ten two-conductor transmission lines and ten nodes. Transmission lines data are extracted from [137].

In this example, we are interested to evaluate the capability of the developed FPGA-RTS to simulate travelling wave propagation in transmission lines. For this reason, the power converters are represented by their Thévenin equivalent model since we are targeting to simulate post-fault travelling wave transients [138], [139]. As it will be discussed in Chapter 5, the typical time span required by the EMTR-based fault location process is about 10 ms. Therefore, the considered Thévenin equivalent model exhibits a sufficient level of accuracy to represent the traveling wave reflection behavior of the converter in this specific time window. As an example, Figure 4.21 shows the comparison between the Thévenin equivalent model and VSC model [140] for the fault-originated voltage transients observed in positive pole of the Station 1. Figure 4.22 shows the error between the simulation results using these two models and it can be observed the error contains low-frequency signal which is due to the dynamics of the converter controller in the VSC model.

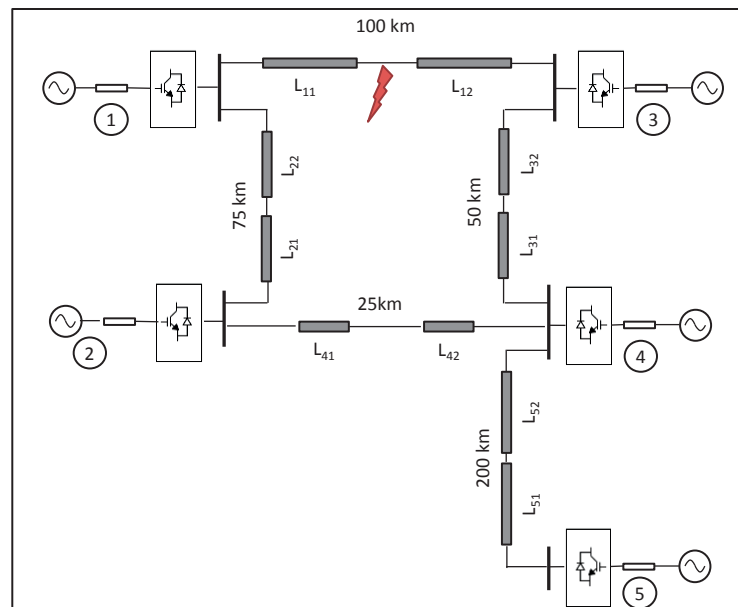


Figure 4.20. Schematic representation of the MTDC network under study.

This low-frequency content can be filtered-out using a high-pass filter. As an example, a first order high-bandwidth Butterworth filter with a cutoff-frequency of 40 Hz is applied. Figure 4.23 shows the comparison between the filtered simulation results obtained using the Thévenin equivalent model and those obtained by the VSC model. It can be observed that the results are in good agreement.

By following the same procedure and by considering EMTP-RV simulation results as benchmark, the FPGA-RTS is developed. For this case study, 213 FPGA clock cycles are required to perform one simulation iteration which, by considering the 40 MHz FPGA clock, results into 5.325  $\mu$ s. The considered FXP format is 42,9 bits and the total utilized FPGA resources are shown in Table 4.10.

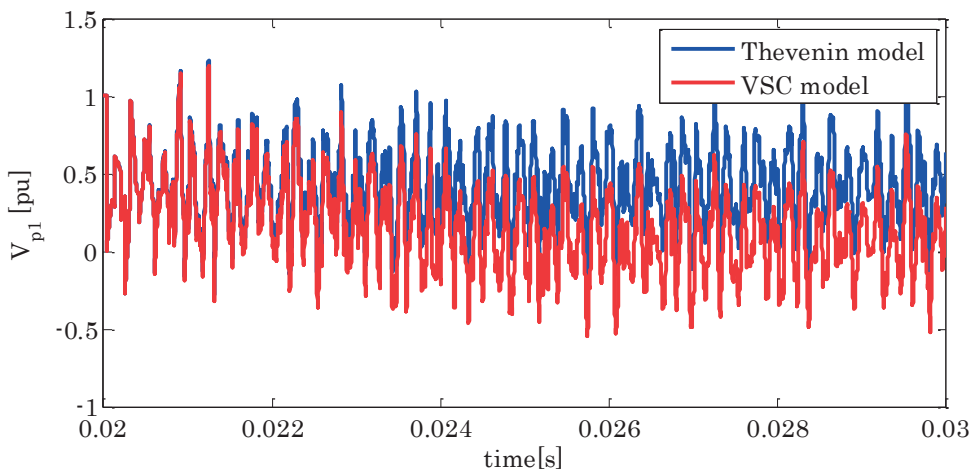


Figure 4.21. Comparison between the simulation results obtained using the Thévenin equivalent and VSC models for the positive pole voltage at Station 1.

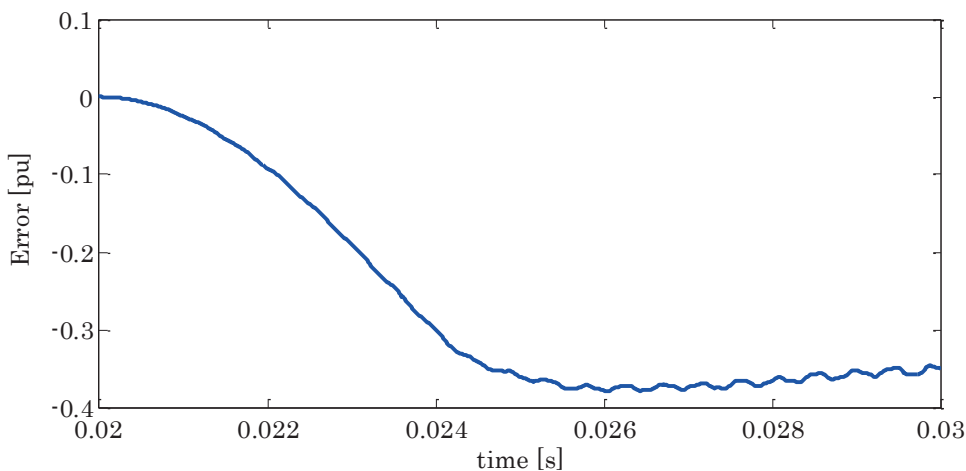


Figure 4.22. Error between the simulation results obtained using the Thévenin equivalent and VSC models for the positive pole of Station 1.

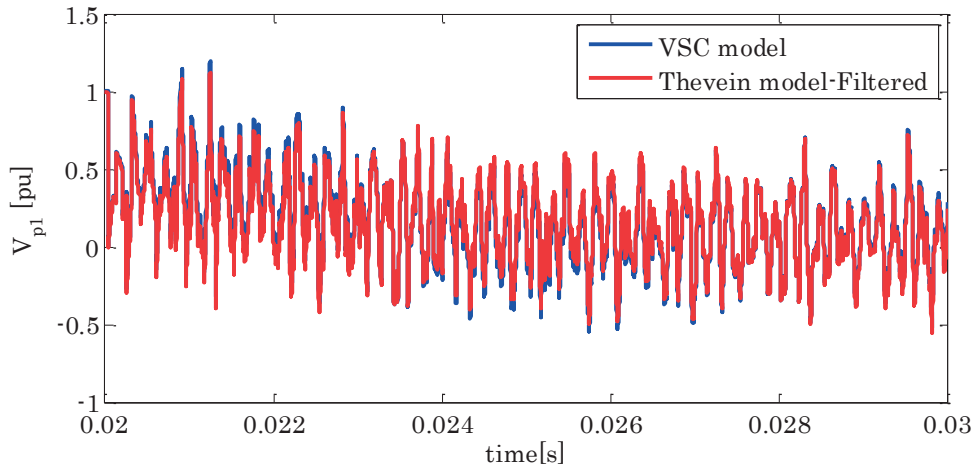


Figure 4.23. Comparison between the simulation results obtained using the Thévenin equivalent and VSC models for the positive pole voltage at Station 1. A first-order high-pass filter is applied for the results obtained by the Thévenin equivalent model.

Table 4.10. FPGA hardware usage for the MTDC network case study.

Resource	Utilized percentage
Slice registers	34.9
Slice LUTs	58.6
Block RAMs	63.4
DSP48s	55.3

The comparison between the EMTP-RV and the FPGA models refers to the case of fault-originated electromagnetic transients. In this respect, the considered network configuration allows applying any type of fault (i.e., pole-to-pole, or pole-to-ground) at an arbitrary location of the desired line. As an example, a pole-to-pole solid fault is considered in the middle of the first transmission line (i.e., 50 km). Figure 4.24 and Figure 4.25 show the comparison between the FPGA-based simulations with the benchmark ones for the phase-to-ground voltage observed at the positive pole of Station 1 and negative pole of Station 5, respectively. Figure 4.26 illustrates the norm of the error of the node voltages. The error is calculated based on the squared differences of the per-unit voltages of the five nodes obtained by the FPGA simulations and the corresponding EMTP-RV ones (positive and negative poles voltages of each node are considered). As it can be observed, the maximum value of the norm of the errors reached during this simulation is of 0.007 pu.

## 4.5 Validation Examples

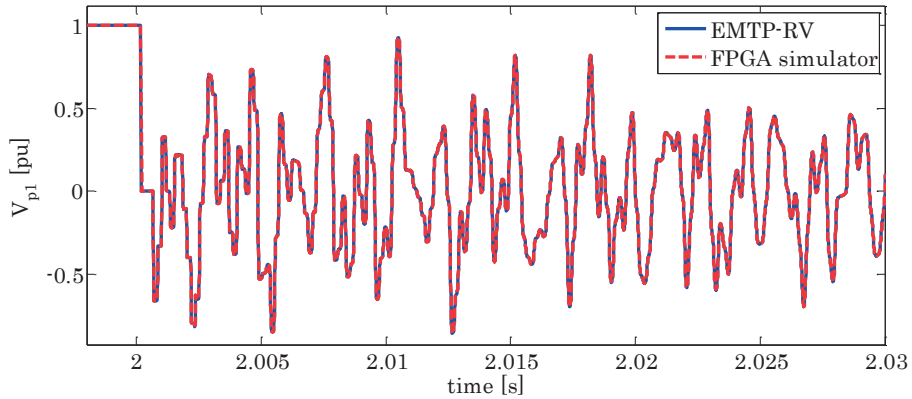


Figure 4.24. Comparison between the FPGA-based simulations with respect to the EMTP-RV ones: phase-to-ground voltage observed in the positive pole of the station 1 subsequent to a solid pole-to-pole fault in the middle of the first transmission line (Figure 4.20).

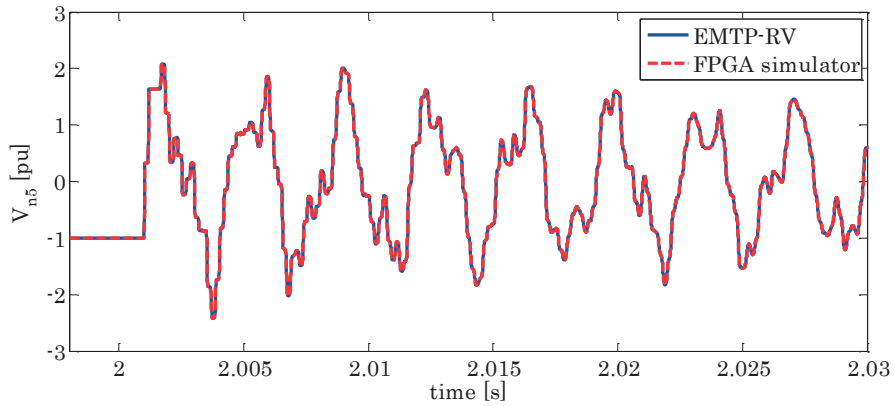


Figure 4.25. Comparison between the FPGA-based simulations with respect to the EMTP-RV ones: phase-to-ground voltage observed in the negative pole of the station 5 subsequent to a solid pole-to-pole fault in the middle of the first transmission line (see Figure 4.20).

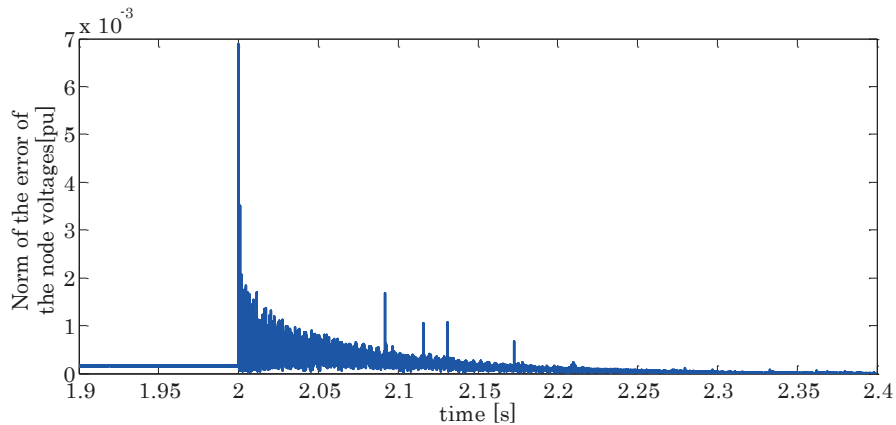


Figure 4.26. Norm of the error of the node voltages computed with the FPGA-simulator vs the EMTP-RV ones.

### 4.5.3 Fault Originated Transients in a Three-Phase AC Network

The third validation example refers to a three-phase AC system composed of five transmission lines terminated on five four substations. The lines are divided into two sections which enables applying different types of faults in correspondence of an arbitrary location along each line. Therefore, the total network is composed by ten three-conductor transmission lines and ten nodes. The simplified representation of this network is shown in Figure 4.27. By following the same procedure adapted for the previous cases and by considering the EMTP-RV simulation results as the benchmark ones, the performances of the FPGA-RTS have been assessed.

For this case study, 256 FPGA clock cycles are required to perform one simulation iteration and send out the output variables which, by considering the 40 MHz FPGA clock, results into an integration time step of 6.4  $\mu$ s. In this examples, in order to save FPGA resources and accelerate the simulation, the AC voltage sources are implemented inside FPGA solver using a pre-defined sinusoidal waveforms generate for one period. Then, the pre-defined waveforms for three-phase voltages are stored in dedicated memories and re-called in each period. The considered FXP format is 32,6 bits and the total utilized FPGA resources are shown in Table 4.11.

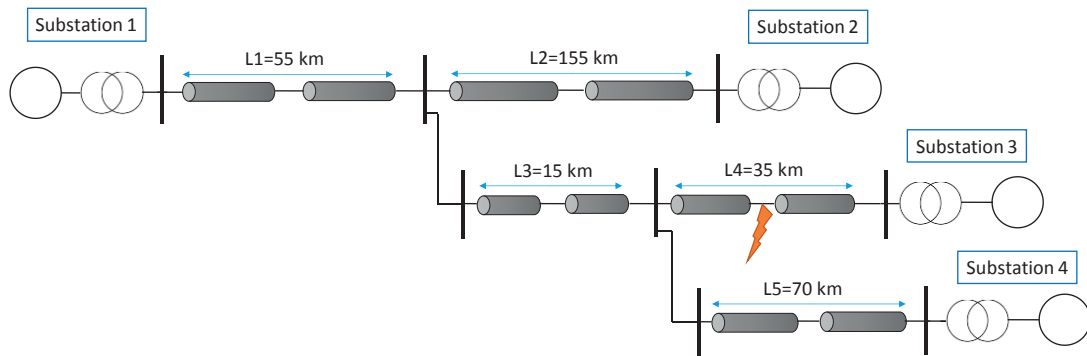
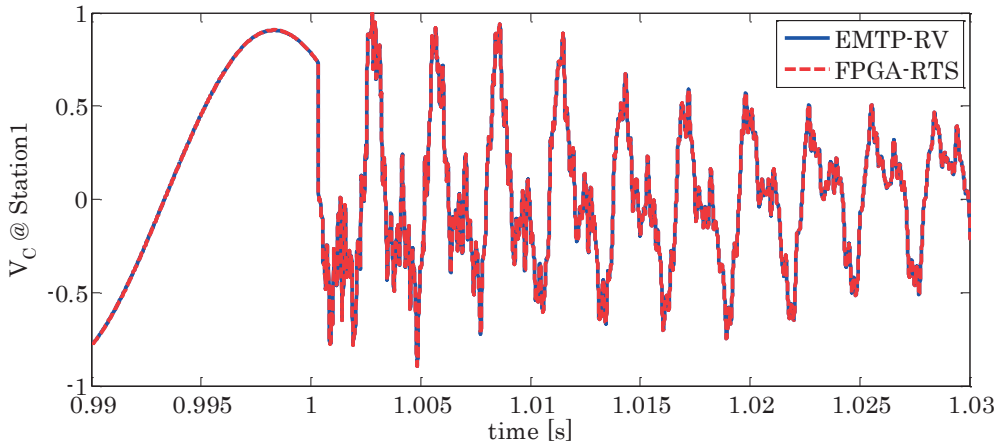


Figure 4.27. Schematic representation of the considered three-phase AC network.

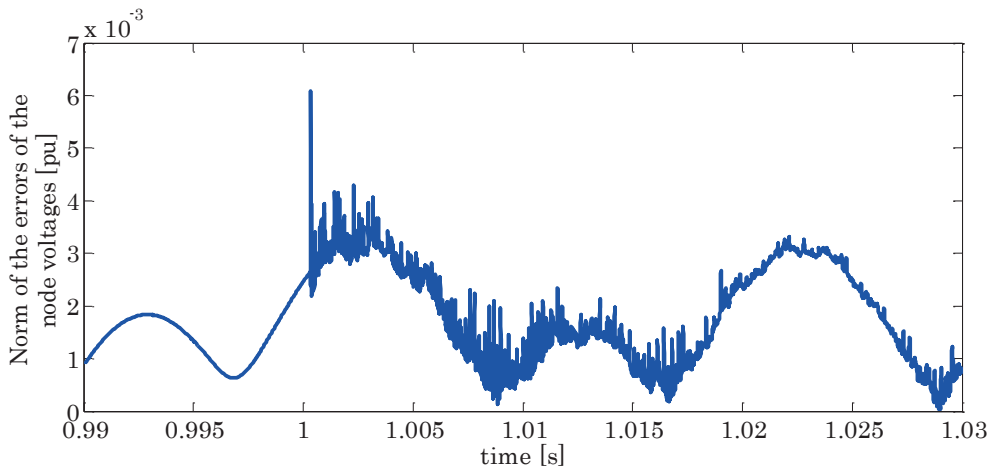
Table 4.11. FPGA hardware usage for the three-phase power network case study.

Resource	Utilized percentage
Slice registers	41.3
Slice LUTs	65.9
Block RAMs	44
DSP48s	61.5

Similar to the MTDC network case study, the comparison between the EMTP-RV and the FPGA models refers to the case of fault-originated electromagnetic transients. In this respect, as previously stated, the considered network configuration allows applying any type of fault at an arbitrary location of the desired line. As an example, a b-c-g fault is considered in the 30 km of the fourth transmission line. Figure 4.28 shows the comparison between the FPGA-based simulations with the benchmark ones for the phase-to-ground voltage observed at the phase “c” of Substation 1. Figure 4.29 illustrates the norm of the errors of the three-phase node voltages which is characterized by maximum 0.006 pu.



**Figure 4.28.** Comparison between the FPGA-based simulations with respect to the EMTP-RV ones: phase-to-ground voltage observed in correspondence of the phase c of substation 1, subsequent to a solid three-phase fault in the 30 km of the fourth transmission line (see Figure 4.27).



**Figure 4.29.** Norm of the errors of the three-phase voltages observed at station 1. (reference values of Figure 4.28).

## 4.6 Conclusion

The chapter presented an automated FPGA-based RTS for power electronics and power systems applications. The proposed real-time simulator was implemented in an industrial real-time embedded system (National Instruments CompactRio real-time platforms) and has the following features: (i) it makes use of the MNA method, (ii) it integrates the FAMNM together with the optimal selection of the switch conductance parameter, (iii) it uses an efficient sparse matrix to vector multiplier which improves which improves the efficiency while significantly decreasing the FPGA hardware usage, (iv) it enables the possibility to accurately reproduce electromagnetic switching transients taking place in power electronic switching devices together with electromagnetic waves propagation in transmission lines, and (v) it enables to reach extremely low integration time steps and provides an automated procedure to directly translate the schematic representation of the electrical circuits designed in EMTP-RV to the relevant FPGA solver. Such peculiarity enables the straightforward applicability of the proposed FPGA-based real-time simulator to various power electronics and power systems applications.

Three validation examples were considered. They refer to (i) a two-level three-phase inverter, (ii) a multi-terminal HVDC network, and (iii) three-phase AC network. The comparison of the obtained results with respect to offline benchmark ones and the HIL validation showed an excellent agreement together with high computation efficiency.

The proposed FPGA RTS exhibits remarkable performance in terms of the achieved simulation time step and the accuracy of the simulation result.





# Integration of the EMTR in the Proposed FPGA-RTS for the Development of a Fast and Efficient Fault Location System

## Summary

This chapter presents a fault location platform that merges the proposed EMTR-based fault location method, presented in Chapter 2, and the developed FPGA-RTS presented in Chapter 4. The fast EMT simulation capability of the developed FPGA-RTS is exploited to perform the fault location process within short time periods. The proposed platform is then used to locate faults in two different power networks: an MTDC grid and an ADN.

In order to deploy the proposed EMTR fault location method in an embedded system, first, the possibility of applying the process using a limited time reversal window is explored. In particular, this feature is critical for the case of MTDC networks where the fast protective relays disconnect the faulty line in a few milliseconds.

By taking advantage of the possibility of applying EMTR fault location using a single observation point and a limited time reversal window, the developed fault location platform is presented. The performances of the developed platform are validated considering several configurations, varying different parameters like fault location, fault type, the presence of noise in the transient signals, measurement systems time delay, and fault impedance.

## 5.1 Introduction

### 5.1.1 Fault Location Challenges in HVDC-MTDC Networks

In modern power systems, complex topologies are often needed to interconnect the generation units and supply fast growing loads. In particular, these complex topologies enable massive integration of new types of generation units (i.e., renewable energy resources) available in remote locations (e.g., offshore wind farms). Traditional AC transmission systems are not the most suitable option to massively transfer the generated power for these distant generation units due to various technical and economical reasons [141]. The major challenges associated with long AC transmission lines are the static and dynamic stability margins, the large demand of reactive power compensation, and high power losses [142]. From a cost analysis point of view, it is shown that the breakeven point to use DC transmission systems instead of AC counterparts is 90 km [143]. Moreover, compared to AC, DC links provide fast control of active and reactive power and avoid the resonance between DC collection link and the AC network [143]. Therefore, it is preferable to use DC transmission systems to interconnect large-scale distant wind farms.

Another challenge concerning large-scale offshore wind farms is the uncertainty, unpredictability, and variability of the generated power due to the nature of the wind. One of the solutions to overcome this challenge is the interconnection of remote wind farms and other types of energy resources (e.g., hydro and solar) by means of multi-terminal HVDC (MTDC) networks. MTDC networks provide balancing of the generated power in geographically spread generation units, taking advantage of different weather conditions over the wide geographical area of the generation units [141]. As an example, the generated wind power in Baltic Sea and North Sea can be balanced with the hydro pump-storage plants mainly located in Central Europe across the Alps (Southern Germany, Austria, Switzerland, Eastern France, and Northern Italy) and Norway [141], [143]. Furthermore, compared to point-to-point HVDC links, MTDC networks provide higher reliability of the power transfer, flexible power flow control between the stations and the AC grid [144].

The significant progress in the development of VSC will result in a more pervasive deployment of MTDC networks. Compared to line commutated converters (LCC), VSCs are the most appropriate converter topology for MTDC networks. The main reason is that they use a common DC voltage at each converter station which simplifies the implementation and control of the parallel connections [141]. Therefore, VSCs are considered as the preferred topology for the proposed MTDC networks such as European Super Grid [141] and North Sea wind farms connection [145].

Aside from the advantages provided by meshed MTDC networks, the protection and fault location problem represent the major challenge for the realization of these grids. Therefore, the fault location problem in HVDC-MTDC requires more sophisticated processes (e.g., [141], [146]). Indeed, in the protection schemes of traditional point-to-point HVDC links, current-regulating reactors limit the short circuit currents and, additionally, the same protection scheme disconnects the system without the main selectivity requirements. However, for the case of MTDC networks, the rapid rise of the short-circuit current and the limited short-circuit current tolerance of the converters' anti-parallel diodes, require the protection system to be characterized by ultra-short time of intervention in which it has to discriminate the faulted line and, then, take the necessary counteraction measures [147], [148]. The early proposed protection schemes were based on the disconnection of AC side breakers to extinguish the DC side fault (e.g., [149]). Therefore, the entire DC system was disconnected. However, this practice is not acceptable in HVDC-MTDC networks. Indeed, the protection system has to be able to identify the faulty line and trigger the correct breakers at both ends of the line in a selective manner within few milliseconds [150]. Therefore, it is important to equip the network with fast fault location systems and DC breakers. In this respect, a few selective protection methods have been proposed in the literature which are based on different techniques such as Wavelet Transform (WT) or differential protection (e.g., [147], [149], [150], [151], [152]).

As a consequence, MTDC protection systems need to be merged with fast fault location processes. This issue is particularly critical for the case of MTDC networks since the transmission lines are generally long and spread over seas which limit the accessibility of the maintenance team. Furthermore, since the lines in such networks are considered to transfer bulk power over long distances, the loss of a line might cause overloading and congestion in other lines. Few fault location methods for the MTDC networks have been proposed in the literature (e.g., [149], [150], [153], [154]). However, the investigations are in the early stages and more studies are necessary to be carried out.

As known, the majority of the proposed fault location methods for HVDC networks are based on travelling waves which provide accurate fault location estimates (e.g., [33], [155]). However, compared to point-to-point HVDC links, the application of travelling wave-based fault location methods for MTDC networks could be challenging due to the following reasons:

- Due to multiple paths for the travelling waves in the MTDC networks, the fault location problem is more complicated compared to the case of two-terminal HVDC lines and can end up in multiple fault location identifications [27];

- Methods using multiple-end measurements (i.e., measurements at multiple terminals) provide, in general, more accurate and reliable results. However, they require multiple observation stations with time-synchronization and fast communication links between them adding non-negligible complexity to the system;
- Sophisticated processing techniques employed by the conventional travelling wave-based fault location methods (e.g., WT, short-time Fourier transformation, etc.) might require considerable computational effort that does not necessarily match the limited time constraints associated with MTDC networks [28].

### 5.1.2 Fault Location Challenges in ADNs

In addition to the emergence of MTDC networks and the need for fast and reliable fault location systems, the restrictive requirements associated with the power quality and stability of the modern power systems require faster and more accurate fault location systems. In particular, typical fault location methods used nowadays, which are based on the estimation of the post-fault impedance might fail in the case of ADN. With the hypothesis of having a fully passive power system, such estimation could provide useful information to locate the fault when compared with the line impedance. However, the presence of other sources (e.g. associated with the increasing penetration of DGs) can largely affect the accuracy of these procedures [59]. Therefore, travelling wave-based methods (which are not affected by the presence of DGs) are used for such networks. As stated in Chapter 2, in real applications, single-end fault location methods are preferred to avoid the need for complex communication links.

### 5.1.3 The Proposed Approach

To overcome the above-mentioned challenges for both cases of HVDC-MTDC networks and ADNs, in this chapter a novel fault location system is presented. The developed fault location platform combines the EMTR-based fault location method, presented in Chapter 2, with the FPGA-based RTS proposed in Chapter 3. The developed platform takes advantage of the fast EMT simulation capability of the proposed FPGA-RTS to perform the fault location process within very short computation time.

First, we explore the possibility of applying the EMTR-based fault location method presented in Chapter 2 by considering the constraints associated with MTDC networks. In particular, the proposed EMTR-fault location method is applied by considering a limited time reversal window, which is determined by the protection system operation. Then, the integration of EMTR-based fault location method and

the developed FPGA-RTS is explained. The developed FPGA-EMTR fault location system is validated by considering two test networks: (i) an MTDC meshed network, and, (ii) a radial distribution system. For both networks, the performance of the developed system is assessed by considering a comprehensive set of simulation case studies.

## 5.2 EMTR-Based Fault Location with Limited Time Reversal Window

As it has been shown in Chapter 2, the EMTR-based fault location technique has been successfully applied for locating faults in inhomogeneous networks, radial distribution networks and series-compensated transmission lines. For these cases, it has been assumed that the fault location system operates after the protection relays maneuver and that the time delay of the protection system and the breakers opening time are large enough such that the recorded transient signals are relatively damped out. However, for the case of MTDC networks this assumption is not valid since, as discussed earlier, the protection system time scales are much lower than those of the AC grids [156]. The protection system has to act very fast to identify the faulty line and disconnect it. The fault identification and line disconnection time are mainly dependent on the protection system speed and the technology of the DC breakers, which are still under investigation. Considering the typical time scales for the operation of protection system and the current interruption time required by the DC breakers, the total time to disconnect the faulty line is around 10 ms [147], [156]. As a consequence, the observation points located at the converter sides are not able to record the full time window of the fault-originated travelling waves.

After the opening of faulted line breakers, the system configuration and the boundary conditions associated with the travelling waves are changed. In this respect, it is worth noting that one of the main hypotheses in time reversal theory is that *the system configuration should remain unchanged during the time-reversal process*. In addition, the breakers opening introduces additional surges that propagate in the system with additional travelling waves superimposed to the fault-originated ones. Therefore, the proposed EMTR-based fault location technique has to be suitably modified in order to overcome this problem. One straightforward approach to solve this problem is to consider a time window of the recorded transient signals prior to the opening of the breakers, so that only the fault originated travelling waves are considered. Another challenge concerning MTDC networks is the existence of the multiple paths for the travelling waves and reflections from different boundaries. Therefore, it is important to explore the possibility of applying the time-reversal process for the media with multiple

reflective boundaries using limited time reversal window. This specific aspect is further discussed in the next section.

### 5.2.1 Example of the Application of EMTR-Based Fault Location Method for MTDC Networks with Limited Time Reversal Window and Single Observation Point

It has been shown that, when time reversal process is applied to a reflective medium, the boundaries of the medium can be considered as many virtual sources. For such boundary conditions, the information is confined in the system. Such peculiarity allows performing the process by using only one real source in the back-propagation system [157], [158]. In fact, if the geometry of the medium shows *ergodic* and *mixing properties*, all information can be collected at only one observation point. In other words, if the generated wave at a given point of the medium, after multiple reflections, passes every location of the medium, all the information about the source can be redirected toward a single observation point. Therefore, for systems where there are multiple reflective boundaries, like MTDC networks where the lines are terminated on power converter stations<sup>1</sup>, the process can be effectively applied by using only one observation point to record the transient signals and back-inject in the back-propagation model.

Concerning the impact of the time reversal window on the time reversal process performance for refocusing applications, in [157] Fink et al. have shown that the duration of the back-injected signal (time reversal window length) impacts the amplitude of the reconstructed wave. More specifically, the amplitude of the reconstructed waveform increases linearly with the time reversal window duration (i.e.,  $\Delta T$ ). The amplitude of the noise is a function of the square root of the time-reversal window (i.e.,  $\sqrt{\Delta T}$ ). Thus, the peak-to-noise ratio of the reconstructed signal increases with the square root of the time-reversal window [157]. As a consequence, the time reversal window impacts the sharpness of the reconstructed injected pulse. However, it is shown that the peak-to-noise ratio saturates for large time reversal windows as multiple reflections cross over the observation point [157], [158]. For the case of acoustic cavities, the saturation time is reached after the Heisenberg time ( $\tau_{\text{Heisenberg}}$ ) which is the minimum time duration to resolve each of the eigenmodes in the cavity [159]. Practically speaking, it is the time required

---

<sup>1</sup> As discussed in chapter 4, terminals of an HVDC grid where power converters are located are characterized by high values of input impedance for relatively high frequencies characterizing fault transients (e.g., [138])

by all the rays radiated by a point source to reach the vicinity of any point in the cavity within a wavelength [159].

One of the important conclusions is that, in a closed reflecting medium, it is still possible to reconstruct the source by using a limited time reversal window [157], [158], [159]. The duration of the time reversal window is determined by the required refocusing quality. Larger time window contains multiple reflections along the medium boundaries, which improve the time reversal performance.

We take advantage of these two important peculiarities of the time reversal process to apply the proposed EMTR-based fault location method for the case of MTDC networks with multiple reflective boundaries and limited time reversal window. Therefore, the recorded fault-originated transient signals at a given observation point are truncated at a time corresponding to the faulty line disconnection time. Then, the windowed transient signals are used to perform the fault location process.

To assess the performance of the proposed EMTR-based fault location method with limited time reversal window for the specific case of the MTDC networks, a grid composed of five transmission lines is considered. This topology has been defined within the European project TWENTIES<sup>1</sup>. The lines are terminated in five converter stations and each line is divided into two segments allowing the possibility of applying a fault in an arbitrary location along the line. The schematic representation of the network is shown in Figure 5.1. A pole-to-pole (p2p) fault is considered at 20 km of the second line (the total line length is 40 km). As discussed earlier, for the case of MTDC networks, the time constraints for the protection systems is very extreme. Since the fault location procedure is performed after the fault clearance, we assume that the fault location system has the knowledge of the faulty line. Therefore, we narrow down the Guessed Fault Locations (GFL) investigation zone only to the faulty line.

By following the procedure presented in Chapter 2, and by considering only 10 ms of the fault originated transient signals recorded at the observation point located at the 5<sup>th</sup> converter station, the fault current energies are calculated for different GFLs along the faulty line. Figure 5.2 shows the fault current energies as a function of GFL for different time reversal window. Each curve is normalized to its own maximum value. It is observed that the increase in the time reversal window duration results in a narrower peak around the localized fault point, and provides better accuracy.

---

<sup>1</sup> <http://www.twenties-project.eu/node/1>

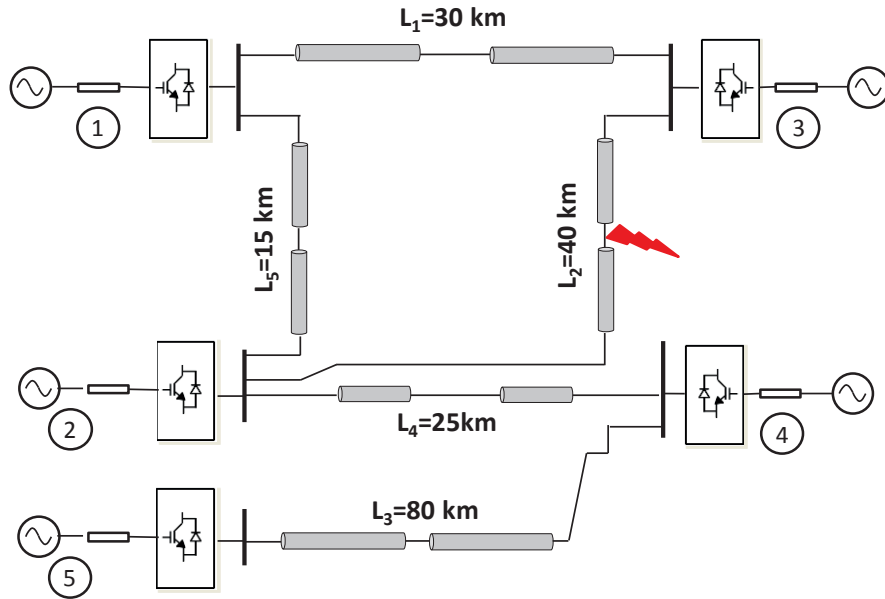


Figure 5.1. Schematic representation of the MTDC network under study.

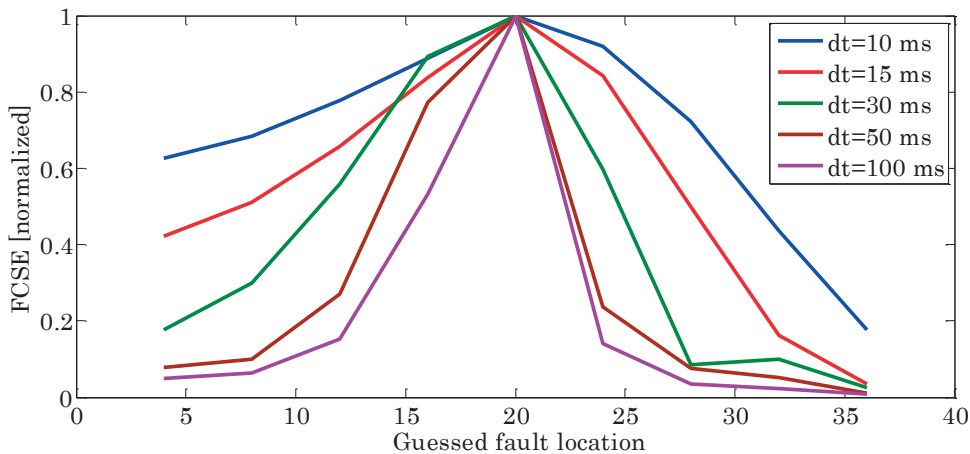


Figure 5.2. Impact of time reversal window length on the accuracy of the proposed EMTR-based fault location method (the real fault location is in line 2 at 20 km).

However, as can be seen by the presented results, window durations compatible with MTDC protection constraints are still adequate to perform the fault location functionality.

We have introduced this example since the possibility to locate faults with short time windows supplying the EMTR fault location is a fundamental property to deploy this fault location process into embedded hardware. The next section discusses such deployment.



### 5.3 Integration of the EMTR with the Developed FPGA-RTS

The aim for the integration of EMTR with the FPGA-RTS is to develop a fault location platform which is able to (i) receive transient signals recorded at a given observation point of a power network, (ii) apply time reversal to the recorded signals, (iii) identify the fault location by applying the EMTR-based fault location procedure through the multiple simulations corresponding to multiple GFL in the network. In what follows the structure of the developed fault location platform is explained.

As described in Chapter 2, the proposed EMTR-based fault location method uses the fault originated transient signals recorded in the given observation point of the network under study. So, the first step is to import the recorded transient signals into the fault location system.

In the developed platform, there are three possibilities to import these signals:

1. The platform can be directly coupled with the network and the signals are imported directly by using voltage/current measurements coupled with FPGA Analog Input (AI) modules. In this case, suitable transient event detection systems are needed to trigger the recording (e.g., [116]).
2. The signals can be imported from the spreadsheet (or text) files generated by the fault recorder or EMTP-RV simulation environment.
3. There is also a possibility to simulate the fault scenario inside the platform using the developed FPGA-RTS and use the simulated signals to perform the fault location process. This option is mainly used to assess the performance of the platform for various fault cases by using an automated procedure, which allows performing numerous accelerated fault scenarios. In this case, for each fault case study, the fault-originated transient signals are recorded at the observation point and saved in a separate spreadsheet file, inside the platform storage.

The imported signals are processed such that only the time window which corresponds to the fault-originated travelling waves before the opening of the line breakers are considered:

$$s_i(t), \quad t \in [t_f, t_f + T_d] \quad (4.21)$$

where  $s_i(t)$  is the processed recorded signal,  $t_f$  is the fault time, and  $T_d$  is, at maximum, the total time required by the protection system and breakers to disconnect the line. Then, these signals are time reversed and shifted in time such that the time reversed signals start from zero.

$$\bar{s}_i(\hat{t}), \hat{t} \in [0, T_d] \quad (4.22)$$

$$\hat{t} = (T_d + t_f) - t \quad (4.23)$$

where  $\bar{s}_i(\hat{t})$  is the time reversed and shifted in time signal resulted from  $s_i(t)$ . The time reversed signals are saved in the memory blocks in order to be transferred to the FPGA solver.

The network data are transferred to the platform to generate the information required by the FPGA-RTS. These data are used to build the EMT model of the considered network being simulated in FPGA. Furthermore, the information from protective relays such as fault type, and the faulty line are also received and used in the fault location process. Before starting the process, a few parameters have to be defined. Among them, the information regarding GFLs (based on the required fault location accuracy) has to be determined.

Furthermore, based on the network parameters and fault data, for each GFL the information required by the FPGA-RTS are re-calculated using network processing unit. In order to have a possibility of applying a fault at an arbitrary location along a line, each line is segmented into two sections. As an example, Figure 5.3 shows a faulty transmission line in a network where the EMTR process is applied.

In this figure,  $L_1^i$  and  $L_2^i$  are the lengths of the two sections of the line and  $x_f$  is the location of the GFL. By moving the position of GFL along the line, the lines length, and as a consequence, the line parameters are changed.

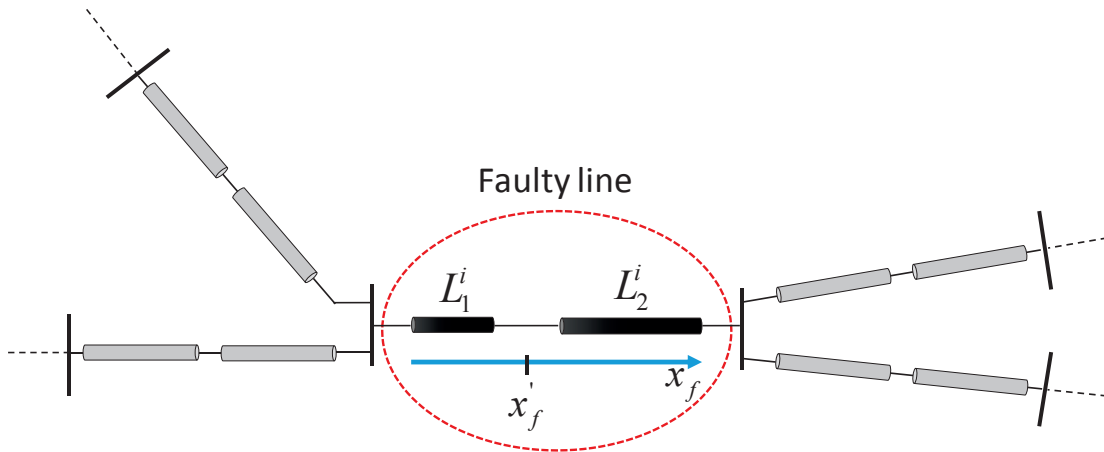


Figure 5.3. A faulty line in a network in which EMTR-fault location is applied.

For each GFL (i.e.,  $x'_f$ ), the lines lengths are recalculated. As a consequence, the coefficients for the RHS computations of the transmission lines ( $K_1^{\rho,i}(x'_f)$ ,  $K_2^{\rho,i}(x'_f)$ ,  $K_3^{\rho,i}(x'_f)$ ,  $K_4^{\rho,i}(x'_f)$ ), the linear interpolation coefficients ( $\alpha_0^{\rho,i}(x'_f)$ ,  $\alpha_1^{\rho,i}(x'_f)$ ), and the circular buffers sizes ( $p^{\rho,i}(x'_f)$ ) are updated. Moreover, the corresponding ANAM is calculated and inverted for the considered GFL (See chapter 4 for more details about the coefficients and the ANAM).

These information are transferred to the FPGA-RTS which simulates the back-propagation model of the network for the specified GFL. The network EMT model is simulated in FPGA-RTS by back-injecting the time-reversed signals from the considered observation point. Each back-propagation simulation corresponds to the simulation of the fault current ( $i_{x'_f}^p(j)$ ) at a GFL resulted from the injection of the time-reversed signals from a given observation point. It is worth noting that, to calculate the fault current, the contribution of each conductor of the line which are involved in the considered fault type is calculated.

For each simulation, the fault current is simulated and the energy of the fault current signal is calculated as:

$$\Gamma(x'_f) = \sum_{p=1}^M \sum_{j=1}^N \left[ i_{x'_f}^p(j) \right]^2, \quad T_d = N\Delta t \quad (4.24)$$

where  $N$  is the number of samples and  $\Delta t$  the sampling time, and  $p$  indicates the number of conductors in the line which are involved in the fault. The calculated energy is transferred back to the **network processing** to perform more assessments. This procedure is done for all the considered GFL and the computed fault current energies are used to identify the exact fault location.

It is worth mentioning that the desired fault location accuracy is determined by the user and the simulations are performed based on the corresponding number of GFLs. The calculated fault current energies associated with the considered GFLs are also saved as a spreadsheet file, allowing the possibility of post-processing them. The structure of the developed fault location platform is shown in Figure 5.4.

As stated before, the developed platform is also capable to simulate numerous fault cases to assess the performance of the platform. In this respect, it is possible, using an automated procedure, to apply different fault types, at different locations of the transmission lines in the network. The user can specify the number of real fault scenarios and required fault location accuracy, which determines the number of back-propagation simulations.

## 5.4 Application of the Developed Fault Location Platform for a Meshed MTDC Network

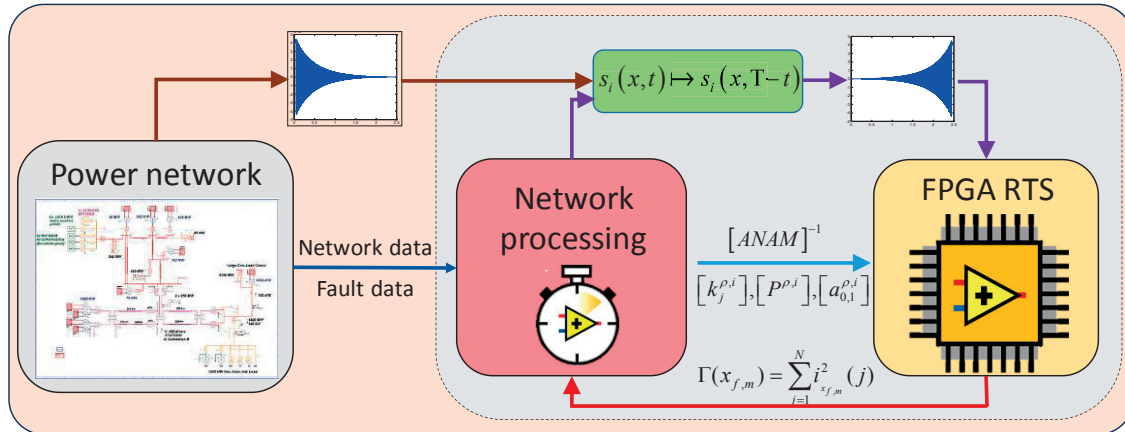


Figure 5.4. Structure of the developed fault location platform.

For each fault case study, the generated transient signals and the fault location results are stored by their corresponding name, which can be accessed for further post-processing.

## 5.4 Application of the Developed Fault Location Platform for a Meshed MTDC Network

The first considered application for the developed fault location platform refers to an MTDC network shown in Figure 5.1.

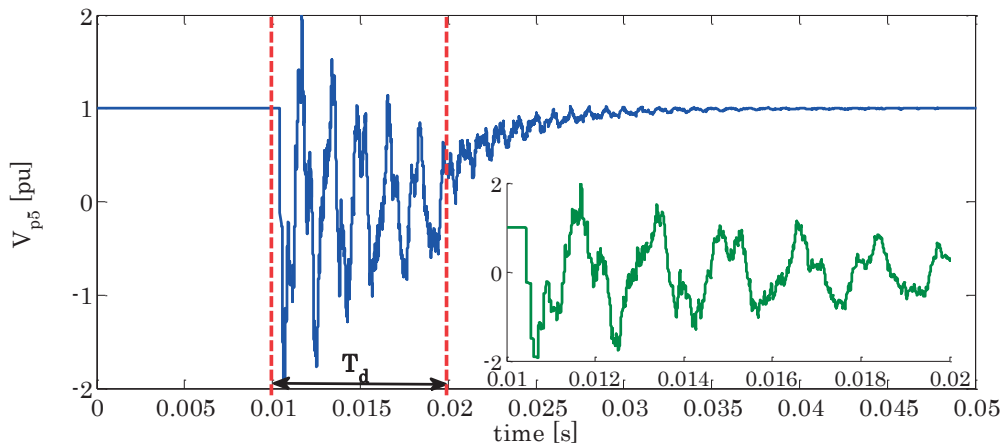
By following the approach presented in Chapter 4, the FPGA-RTS for this network is assessed and validated by comparing its results with EMTP-RV generated simulations. Then, considering the proposed structure presented in Section 5.3, the fault location platform for this network is developed.

The developed fault location system enables the simulation of back-propagation model for different fault types (i.e., p2p, p2g), at an arbitrary position along a considered line. Furthermore, the time reversed transient signals can be back-injected from one of the five observation points located at the five converter stations.

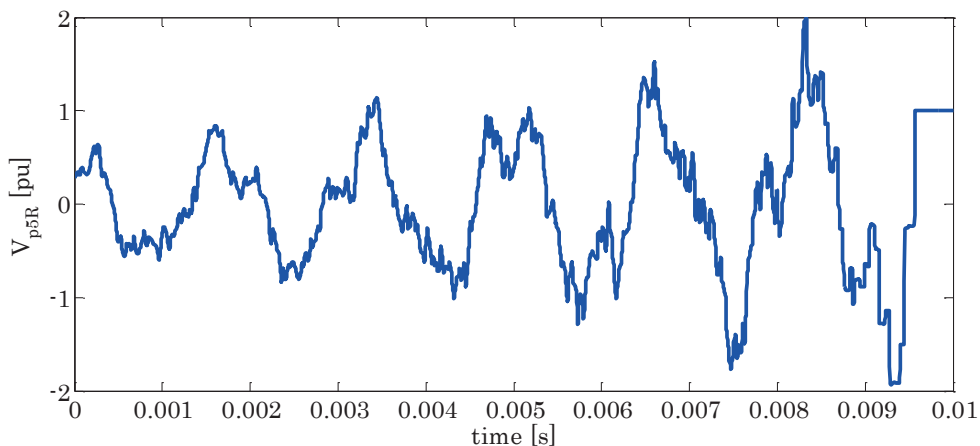
As stated earlier, the fault-originated transient signals recorded at the observation point can be imported from real signals recorded by the fault recorder, fault transients simulated in EMTP-RV simulation environment, or simulated inside by FPGA-RTS. Then, the imported signals are processed and time reversed based on equation (4.22) by considering the fault occurrence time and the total time required by the protection system and the breakers to disconnect the faulty line. In this application example, we use 10 ms for the time reversal window, which is the typical value of the line disconnection time used in the literature (e.g., [147], [156]).

## 5 Integration of the EMTR in the Proposed FPGA-RTS for the Development of a Fast and Efficient Fault Location System

As an example, let consider a p2p fault at 10 km of Line 1. The fault occurs at 10 ms and the line breakers disconnect the line at 20 ms. Figure 5.5 shows the recorded voltage for the positive node in station 5. In this figure, the red lines show the fault occurrence (10 ms) and the breakers disconnection time (20 ms). As stated before, in order to consider only the fault originated travelling waves, the time reversal window is considered from the fault occurrence to the breakers opening. Therefore, only this part of the recorded voltage (which is shown in the expanded view - green waveform) is considered for the EMTR fault location process. Then, this signal is shifted in time by  $t_f$  and time reversed (see equation (4.22)). The time-reversed signal is shown in Figure 5.6. The same process is applied for the recorded signal of the negative pole. Then, the time-reversed signals are saved into DMA-FIFO memories and transferred to the FPGA.



**Figure 5.5.** Recorded transient signals in station 5 for positive pole. The green waveform corresponds to the part of signal from the fault occurrence to the breakers openings.



**Figure 5.6.** Time-reversed voltage signal recorded at station 5 for positive pole. (The reference signal is the one shown Figure 5.5).

### 5.4.1 Performance Assessment With Respect to the Fault Location and Fault Type

To assess the performance of the developed fault location platform, a series of fault cases are considered. Two different fault types (i.e., p2p, and p2g) are considered and the location of the fault is changed by the length step of 1 km. Therefore, the total fault cases for each fault type and for each line are:  $N_f@L_1=29$ ,  $N_f@L_2=39$ ,  $N_f@L_3=79$ ,  $N_f@L_4=24$ ,  $N_f@L_5=14$ .

For each real fault case, the fault is simulated in the FPGA-RTS and the fault-originated transient signals are recorded at the observation points located at all converter stations, processed and time reversed according to the procedure explained before.

In this application example, since the fault location process starts after the protection systems operation, in order to accelerate the fault location process, it is assumed that the faulty line is determined beforehand. Therefore, the GFLs are only considered along the faulty line. For each GFL along the faulty line, the back-propagation model is simulated in FPGA-RTS by considering an observation point which back-injects the time-reversed signals, and the associated fault current at the considered GFL is simulated. Then, the location of GFL is moved by the considered step ( $\Delta x_f$ ), which determines the fault location accuracy and the process is repeated for all GFLs. In this example, we have considered  $\Delta x_f = 1km$ . The energy of the fault current signal simulated for a given GFL is calculated and used as a measure to identify the correct fault point. As an example, Figure 5.7 shows the calculated fault current energies as a function of GFLs along the faulty line and for different observation points. For each observation point, the calculated energies are normalized by its maximum. The real fault is p2p at 20 km of Line 3. As it can be observed, the fault location platform is able to identify the correct fault location by using any of the observation points.

The same process is performed for all the considered real faults, which are moved along all lines with a location step of 1 km. The back-propagation simulations are performed by using the back-injection of the time-reversed signals from the observation point 5. Table 5.1 shows the performance of the developed system for the considered fault cases. As it can be observed, the system is able to identify the correct fault location for the p2p faults at all the lines. For the case of p2g faults there are a limited number of mislocations in line 3 and line 4. In order to compute a correct measure to indicate the errors associated with these mislocation cases, we need to consider the limited number of real fault cases in each line and the fault location accuracy step ( $\Delta x$ ). The fault location error is an integer multiple of  $\Delta x$ .

## 5 Integration of the EMTR in the Proposed FPGA-RTS for the Development of a Fast and Efficient Fault Location System

Therefore, the average location error (ALE) is computed as following:

$$ALE = \frac{\sum_{i=1}^{N_{failure}} k_i \Delta x}{N_{failure}}, k_i = 2, 3 \dots \quad (5.1)$$

where  $k_i \Delta x$  is the error between the real fault location and the identified one for the case failure. We exclude the misestimated fault location that are within one step of the fault location accuracy ( $1\Delta x$ ) since for these cases it falls within the uncertainty region of the fault location process. It is worth mentioning that, for all the misestimated fault location cases, the maximum fault location error is  $3\Delta x$ .

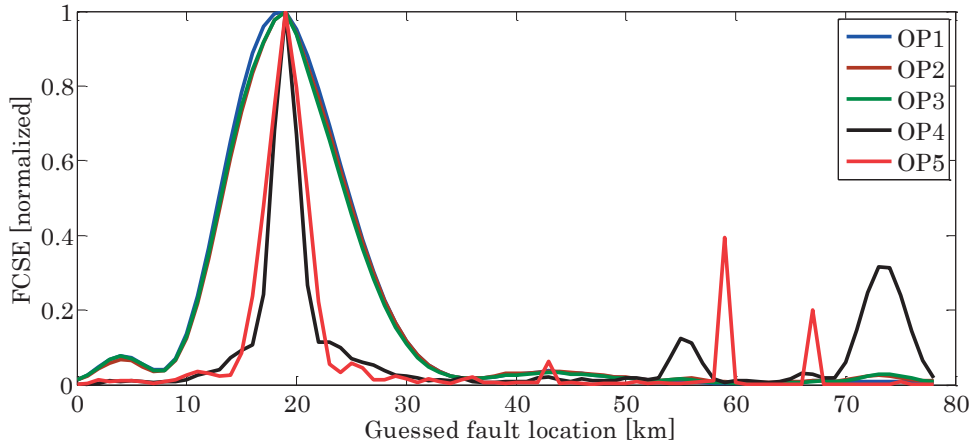


Figure 5.7. Example of FCSE as a function of gussed fault location along the line 3 for different observation point back-injections. The fault is p2p at 20 km.

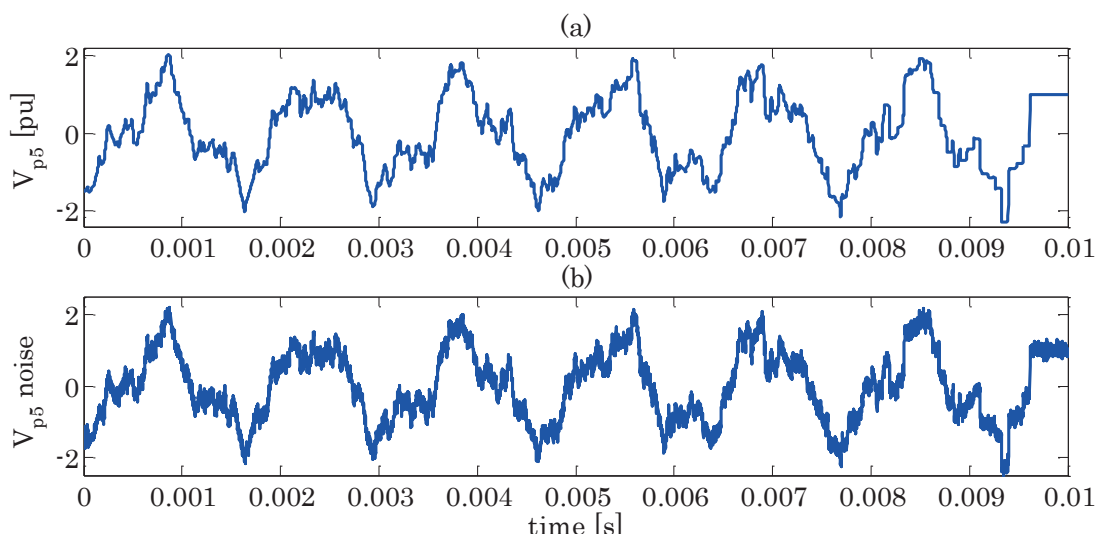
Table 5.1. Performance assessment of the developed fault location platform by considering different fault types at different locations along the lines.

Faulty line	Line length	Fault type	Nr. of faults	Nr. of mislocations	Ave. error/ $\Delta x$
1	30	p2p	29	0	0
		p2g	29	0	0
2	40	p2p	39	0	0
		p2g	39	0	0
3	80	p2p	79	0	0
		p2g	79	4	2
4	25	p2p	24	0	0
		p2g	24	2	2.5
5	15	p2p	14	0	0
		p2g	14	0	0

It is worth mentioning that for the considered network, the average time to simulate a fault simulation for a given GFL is 60 ms. This includes the following computation stages: (i) re-assessment of the network and transmission lines parameters associated with each GFL, (ii) recalculation of the ANAM and computation of the matrix inverse, (iii) transfer the network information as well as the time-reversed transient signals to the FPGA solver, (iv) call the FPGA simulator to start simulation of the back-propagation model, and (iv) and the time required by the FPGA simulator to finished the back-propagation simulation and generated the FCSE (fault current signal energy) corresponding to the GFL.

### 5.4.2 Performance Assessment with Respect to Noise

In order to assess the performance of the system in the presence of the noise, we run the same simulations by adding noise to the time-reversed signals with different Signal to Noise Ratio (SNR): (i) 40 dB, and (ii) 20 dB. Figure 5.8 shows the fault originated transient signal recorded at the station 5 for the positive pole (a) without and (b) with 20 dB noise. The fault is at 10 km of line 2. Table 5.2 and Table 5.3 show respectively, the performance of the developed system with presence of 40 dB and 20 dB SNR levels of the noise added to the time reversed transient signals. As it is observed, the presence of noise does not have an impact on the performance of the developed fault location system and the EMTR-based fault location method is able to identify the correct fault location even in the presence of extremely high measurement noise.



**Figure 5.8. (a) The time-reversed voltage signal recorded at station 5 for positive pole; (b) the same signal by adding 20 dB noise.**



## 5 Integration of the EMTR in the Proposed FPGA-RTS for the Development of a Fast and Efficient Fault Location System

**Table 5.2. Performance assessment of the developed fault location platform by considering different fault types at different locations along the lines. The time-reversed signals are contaminated with 40 dB SNR noise.**

Faulty line	Line length	Fault type	Nr. of faults	Nr. of mislocations	Ave. error/ $\Delta x$
1	30	p2p	29	0	0
		p2g	29	0	0
2	40	p2p	39	0	0
		p2g	39	0	0
3	80	p2p	79	0	0
		p2g	79	4	2
4	25	p2p	24	0	0
		p2g	24	2	2.5
5	15	p2p	14	0	0
		p2g	14	0	0

**Table 5.3. Performance assessment of the developed fault location platform by considering different fault types at different locations along the lines. The time-reversed signals are contaminated with 20 dB SNR noise.**

Faulty line	Line length	Fault type	Nr. of faults	Nr. of mislocations	Ave. error/ $\Delta x$
1	30	p2p	29	0	0
		p2g	29	0	0
2	40	p2p	39	0	0
		p2g	39	0	0
3	80	p2p	79	0	0
		p2g	79	4	2
4	25	p2p	24	0	0
		p2g	24	3	2.33
5	15	p2p	14	0	0
		p2g	14	0	0

### 5.4.3 Performance Assessment of Time-Shifted Time Reversed Windows

Furthermore, the performance of the developed fault location system is analyzed when there is a time delay for the recorded fault-originated transient signal. As known, the first part of the post-fault transient has the highest frequency components since they are damped more rapidly with respect to lowest frequency components. Therefore, it is probable that the measurement systems would not be able to capture this part of the signal. Therefore, the signal recording starts with some time delay. By making reference to equation (4.21), the recorded signal is:

$$s_i(t), \quad t \in [t_f + t_{delay}, t_f + T_d + t_{delay}] \quad (5.2)$$

## 5.4 Application of the Developed Fault Location Platform for a Meshed MTDC Network

where  $t_{delay}$  is the time delay for the signal recording. By applying the time reversal operator and by shifting the signal, we obtain:

$$\bar{s}_i(\hat{t}), \hat{t} \in [0, T_d + t_{delay}] \quad (5.3)$$

$$\hat{t} = (T_d + t_f + t_{delay}) - t \quad (5.4).$$

Table 5.4 and Table 5.5 show the performance of the fault location system by considering  $t_{delay} = 1 \text{ ms}$  and  $t_{delay} = 2 \text{ ms}$ , respectively. It is observed that, shifting the recorded transient signals does not impact significantly the performance of the system.

**Table 5.4. Performance assessment of the developed fault location platform by considering different fault types at different locations along the lines. The measurement systems time delay to start recording the signals is 1 ms.**

Faulty line	Line length	Fault type	Nr. of faults	Nr. of mislocations	Ave. error/ $\Delta x$
1	30	p2p	29	0	0
		p2g	29	0	0
2	40	p2p	39	0	0
		p2g	39	0	0
3	80	p2p	79	0	0
		p2g	79	4	2
4	25	p2p	24	0	0
		p2g	24	2	2.5
5	15	p2p	14	0	0
		p2g	14	0	0

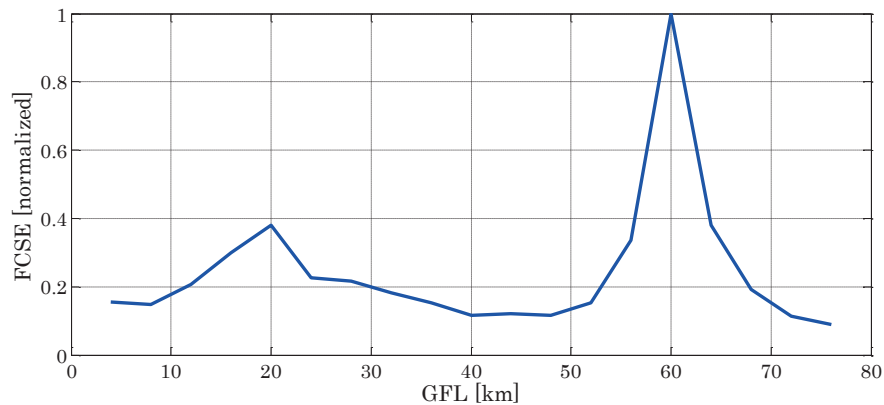
**Table 5.5. Performance assessment of the developed fault location platform by considering different fault types at different locations along the lines. The measurement systems time delay to start recording the signals is 2 ms.**

Faulty line	Line length	Fault type	Nr. of faults	Nr. of mislocations	Ave. error/ $\Delta x$
1	30	p2p	29	0	0
		p2g	29	0	0
2	40	p2p	39	0	0
		p2g	39	0	0
3	80	p2p	79	0	0
		p2g	79	4	2
4	25	p2p	24	0	0
		p2g	24	4	2.5
5	15	p2p	14	0	0
		p2g	14	0	0

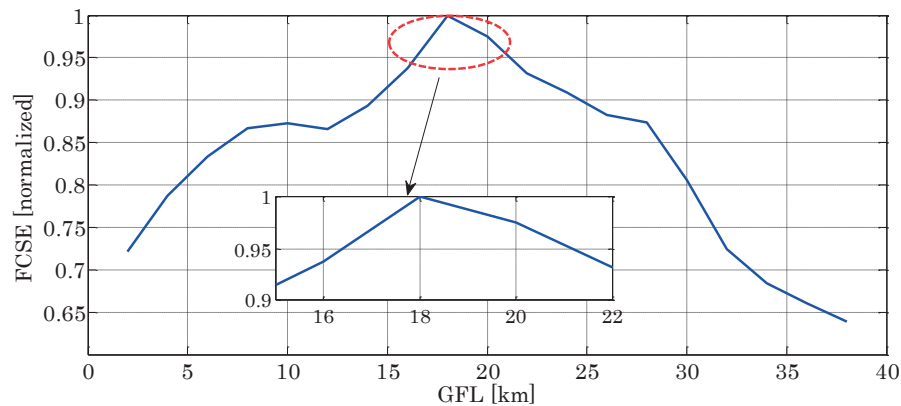
#### 5.4.4 Performance Assessment with Respect to Fault Impedance

As shown in Chapter 2, the proposed EMTR-based fault location method is robust against the fault impedance and in particular, for the case of high impedance faults. Nevertheless, in order to show the performance of the developed fault location system against high impedance faults, three cases are demonstrated. The first fault case is a p2p fault at 60 km of line 3 (line length is 80 km) and the fault impedance is 100  $\Omega$ . The fault location can be clearly identified by observing the fault current energy shown in Figure 5.9.

The second case is a p2g fault at 18 km of line 2 (the line length is 40 km) and the fault impedance is 50  $\Omega$ . Figure 5.10 shows the FCSE as a function of GFL along the line2. The energy is maximized in correspondence of 18 km, which is the real fault location. The third example is a p2p fault at 9km of line 1 and the fault impedance is 50  $\Omega$ . As demonstrated in Figure 5.11, the FCSE is maximum at 9 km compared to the other GFLs.



**Figure 5.9. FCSE as a function of GFL for a p2p fault at 60km of line 3. The fault impedance is 100  $\Omega$ .**



**Figure 5.10. FCSE as a function of GFL for a p2g fault at 18 km of line 2. The fault impedance is 50  $\Omega$ .**

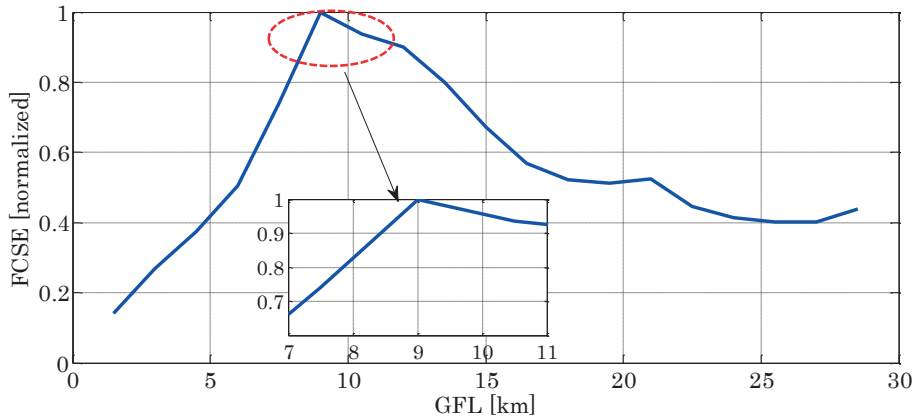


Figure 5.11. FCSE as a function of GFL for a p2p fault at 9km of line 1. The fault impedance is  $50 \Omega$ .

## 5.5 Application of the Developed Fault Location Platform for a Radial ADN

As stated in the introduction, fault location is also a challenging problem for the case of ADNs where there are DGs connected to the feeders along the lines. Travelling wave-based fault location methods are the most suitable ones for these type of networks but, in general, they need multiple-end measurements in order to provide accurate fault location.

In order to assess the performance of the developed fault location platform for this application, the network shown in Figure 5.12 is considered. The network is composed of 5 transmission lines where each line is divided into two segments to provide the possibility of moving the fault location along its length. The fault location system is considered to be installed at the substation where the fault originated travelling waves are recorded. Thus, the fault location process is performed by using a single-end measurement.

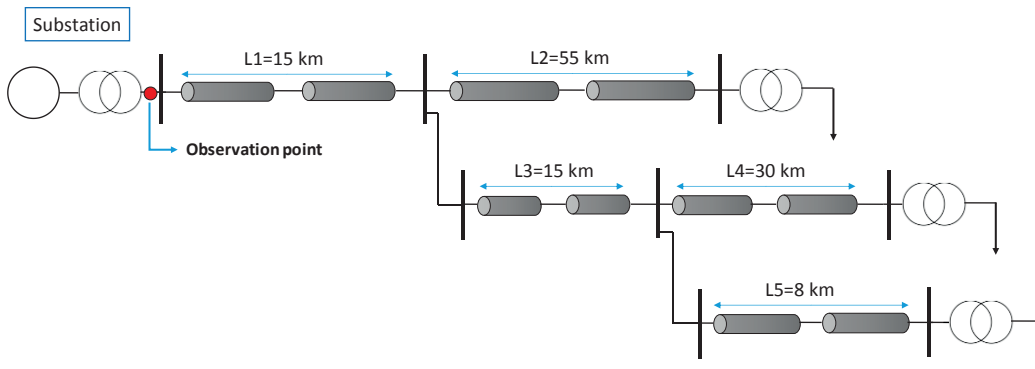
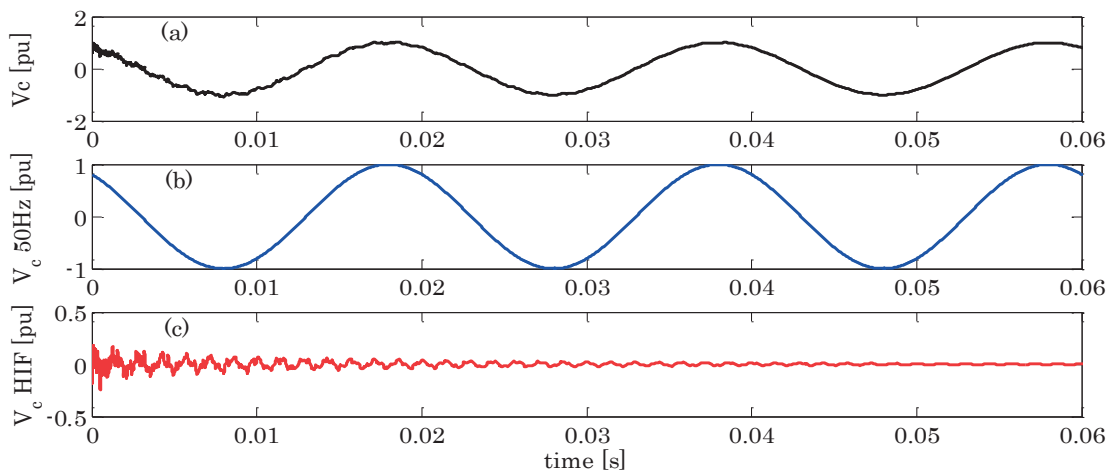


Figure 5.12. Radial distribution network composed of 5 transmission lines.

By following the procedure described earlier, the fault location system is adapted for this network. Moreover, three category of fault types are considered (i.e., three-phase, phase-to-phase, and phase-to-ground) and, for a given fault, the GFLs are considered along all the lines without the need for the knowledge of the faulty line. Furthermore, a longer time reversal window (120 ms) is considered in order to be compatible with the operation time of the protection systems typically used in distribution networks.

For this application, since the fault-originated travelling waves are superimposed with the power system main frequency (50 Hz), first the high-frequency travelling waves transients are extracted from the recorded signals. To this end, the signal characteristics (amplitude, and phase) associated with the 50 Hz component are extracted and a sinusoidal signal based on these characteristics are generated. The process to extract this steady-state frequency component is described in [160]. Then, the high-frequency transients are extracted subtracting the original signal from its corresponding 50Hz. Figure 5.13 shows: (a) the recorded voltage of phase c, (b) the corresponding 50Hz tone, (c) the extracted high frequency transients for an a-b-g fault at 5km of Line1.

As an example, Figure 5.14 and Figure 5.15 show the FCSE as a function of GFLs along all the lines for the case of a-b-g fault at 5 km of Line 1 and a-g fault at 15 km of line 4, respectively. The FCSEs of different lines are normalized by the maximum energy value of the faulty line. As it can be observed, in both cases the real fault location is identified precisely. Furthermore, it is also able to identify the faulty line by performing the process only from a single-end measurement located at the substation. Therefore, it can also be used as a reliable backup protection system since it does not need multi-end measurement points and communication links.



**Figure 5.13.** (a) Observed post-fault voltage waveform for phase c for a a-b-g fault at 5km of Line1, (b) corresponding 50 Hz component, (c) extracted high frequency transients.

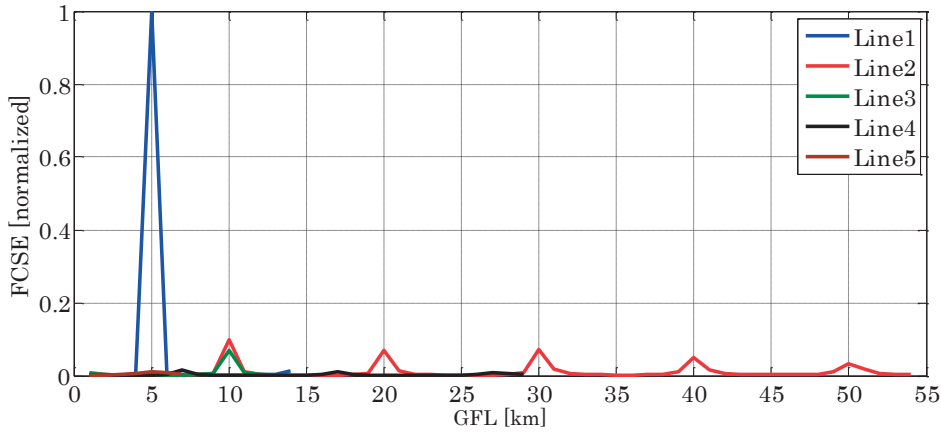


Figure 5.14. FCSE as a function of GFLs along all the lines. The real fault is at 5km of the Line1 and the fault type is a-b-g.

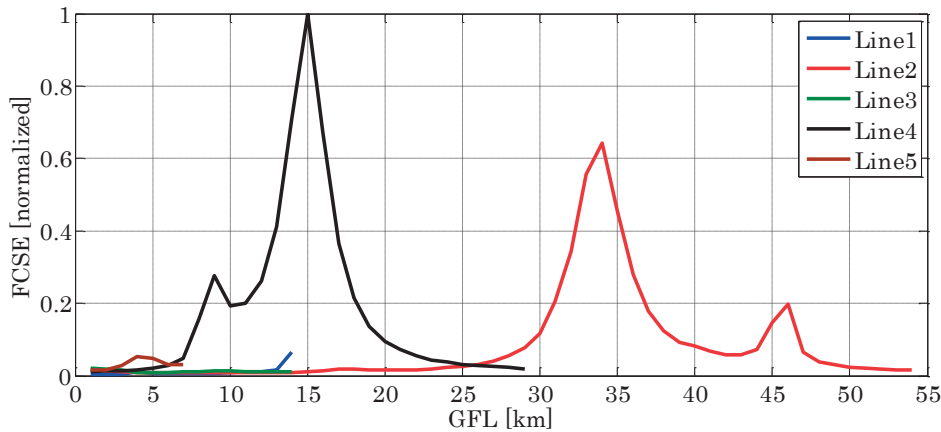


Figure 5.15. FCSE as a function of GFLs along all the lines. The real fault is at 15km of the Line4 and the fault type is a-g.

### 5.5.1 Performance Assessment with Respect to the Fault Location and Fault Type

In order to provide a comprehensive performance assessment of the developed system for this application, similar to the case MTDC network, a series of fault cases are considered in order to assess the accuracy of the identified fault location. For each line, the real fault location is moved with a location step of 1 km and for each real fault location, seven different fault types are considered. For each case, the fault-originated transient signals are recorded at the substation (see Figure 5.12), processed and time reversed. For each considered fault location and type, a number of GFLs are considered along the lines and, by using the back-propagation model of the network being simulated in FPGA-RTS, for each GFL, the time-reversed signals are back-injected into the simulated network. Then, the FCSE is calculated and transferred to the network processor to identify the fault

## 5 Integration of the EMTR in the Proposed FPGA-RTS for the Development of a Fast and Efficient Fault Location System

point. Table 5.6 illustrates the performance of the developed system applied for the considered radial distribution network. The following comments can be derived:

1. The fault location system is able not only to assess the correct fault location but, also, is capable to identify the faulty line. This feature is of particular importance since it is performed by using a single-end measurement at the substation.
2. Among 866 simulated real fault cases, including different fault types at all the lines, only in 10 cases (1.15%), the system failed to correctly estimate the fault location.
3. Concerning the computation time, the average time to simulate a fault simulation for a given GFL is 410 ms. Compared to the MTDC case, this computation time is larger due to the use of longer time reversal window (120 ms). This execution time includes the times needed for: (i) recalculate the network and transmission lines parameters associated with each GFL, (ii) recalculate the ANAM and compute the matrix inverse, (iii) transfer the network information as well as the time-reversed transient signals to the FPGA solver, (iv) call the FPGA simulator to start simulation of the back-propagation model, and (iv) and the time required by the FPGA simulator to finished the back-propagation simulation and generated the FCSE corresponding to the GFL.

**Table 5.6. Performance assessment of the developed fault location platform for the case of ADN by considering different fault types at different locations along the lines.**

Faulty line	Line length	Fault type	Nr. of faults	Nr. of mislocations
1	15	3ph	14	0
		ph-ph	3*14=52	0
		ph-g	3*14=52	0
2	55	3ph	54	2
		ph-ph	3*54=162	6
		ph-g	3*54=162	2
3	15	3ph	14	0
		ph-ph	3*14=52	0
		ph-g	3*14=52	0
4	30	3ph	29	0
		ph-ph	3*29=87	0
		ph-g	3*29=87	0
5	8	3ph	7	0
		ph-ph	3*7=21	0
		ph-g	3*7=21	0

**5.5.2 Performance Assessment with Respect to Noise**

In order to assess the performances of the system in the presence of noise, the same simulations are performed again by adding noise to the time-reversed signals with different SNRs: (i) 40 dB, (ii) 20 dB. Table 5.7 and Table 5.8 show respectively, the performance of the developed system with presence of 40 dB and 20 dB SNR levels.

**Table 5.7. Performance assessment of the developed fault location platform for the case of ADN by considering different fault types at different locations along the lines. The recorded transient signals are contaminated with 40 dB noise.**

Faulty line	Line length	Fault type	Nr. of faults	Nr. of mislocations
1	15	3ph	14	0
		ph-ph	3*14=52	0
		ph-g	3*14=52	0
2	55	3ph	54	2
		ph-ph	3*54=162	6
		ph-g	3*54=162	2
3	15	3ph	14	0
		ph-ph	3*14=52	0
		ph-g	3*14=52	0
4	30	3ph	29	0
		ph-ph	3*29=87	0
		ph-g	3*29=87	0
5	8	3ph	7	0
		ph-ph	3*7=21	0
		ph-g	3*7=21	0

**Table 5.8. Performance assessment of the developed fault location platform for the case of ADN by considering different fault types at different locations along the lines. The recorded transient signals are contaminated with 20 dB noise.**

Faulty line	Line length	Fault type	Nr. of faults	Nr. of mislocations
1	15	3ph	14	0
		ph-ph	3*14=52	0
		ph-g	3*14=52	0
2	55	3ph	54	2
		ph-ph	3*54=162	7
		ph-g	3*54=162	3
3	15	3ph	14	0
		ph-ph	3*14=52	0
		ph-g	3*14=52	0
4	30	3ph	29	0
		ph-ph	3*29=87	0
		ph-g	3*29=87	0
5	8	3ph	7	0
		ph-ph	3*7=21	0
		ph-g	3*7=21	1



As it can be observed, the presence of noise does not have a significant impact on the performance of the developed fault location system and the method is robust against the high level of noise contamination in the transient signals.

### 5.5.3 Performance Assessment of Time-Shifted Time Reversed Windows

Similar to the case of MTDC network, the performance of the developed system is analyzed by considering a time delay for the measurement system to record the fault originated transient signals. To this end, two scenarios are considered by assuming 1ms and 2ms time delay for the recorded signals. As it can be inferred by observing Table 5.9 and Table 5.10, the measurement system time delay slightly impacts the performances of the fault location platform. The number of misestimated fault location increases mostly for the faults nearby the observation point. For these cases, the durations of the fault-originated transient signals are extremely short and large time delay may result in losing the whole post-fault transient.

**Table 5.9. Performance assessment of the developed fault location platform for the case of ADN by considering different fault types at different locations along the lines. The measurement systems time delay to start recording the signals is 1 ms.**

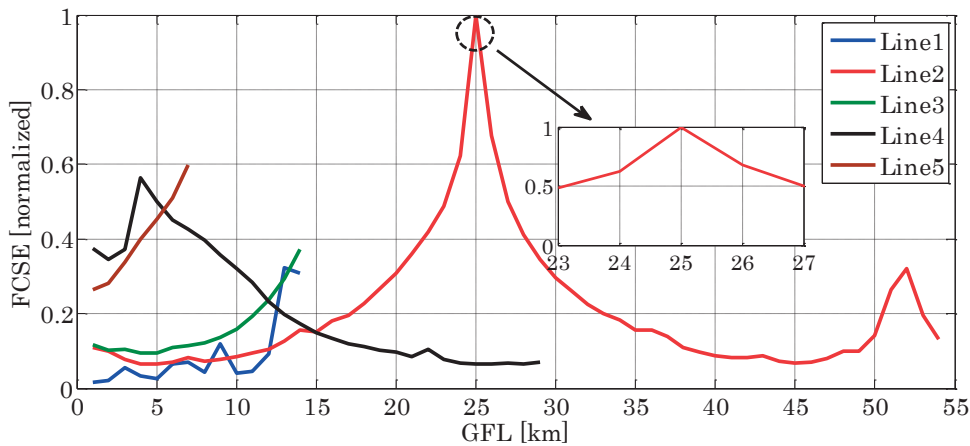
Faulty line	Line length	Fault type	Nr. of faults	Nr. of mislocations
1	15	3ph	14	0
		ph-ph	3*14=52	2
		ph-g	3*14=52	1
2	55	3ph	54	3
		ph-ph	3*54=162	6
		ph-g	3*54=162	3
3	15	3ph	14	0
		ph-ph	3*14=52	0
		ph-g	3*14=52	1
4	30	3ph	29	0
		ph-ph	3*29=87	0
		ph-g	3*29=87	1
5	8	3ph	7	0
		ph-ph	3*7=21	0
		ph-g	3*7=21	0

**Table 5.10. Performance assessment of the developed fault location platform for the case of ADN by considering different fault types at different locations along the lines. The measurement systems time delay to start recording the signals is 2 ms.**

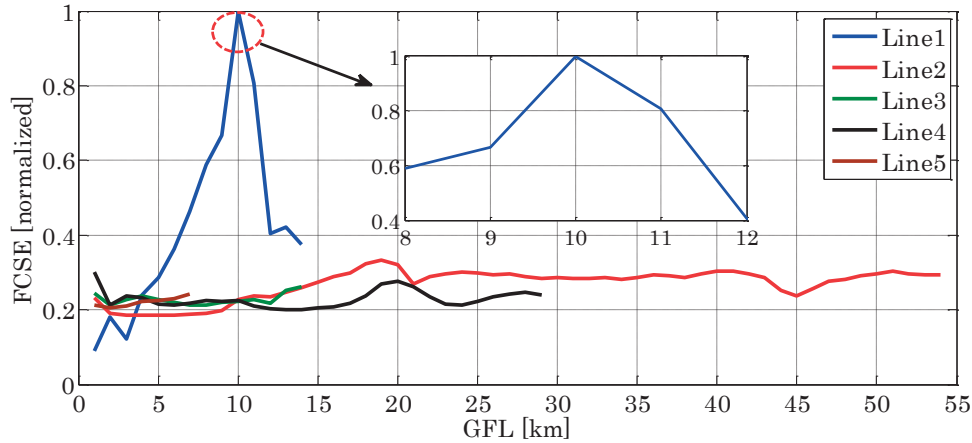
Faulty line	Line length	Fault type	Nr. of faults	Nr. of mislocations
1	15	3ph	14	1
		ph-ph	3*14=52	3
		ph-g	3*14=52	3
2	55	3ph	54	0
		ph-ph	3*54=162	6
		ph-g	3*54=162	5
3	15	3ph	14	0
		ph-ph	3*14=52	0
		ph-g	3*14=52	0
4	30	3ph	29	0
		ph-ph	3*29=87	2
		ph-g	3*29=87	2
5	8	3ph	7	0
		ph-ph	3*7=21	0
		ph-g	3*7=21	2

### 5.5.4 Performance Assessment with Respect to Fault Impedance

The performances of the system is also assessed for the case of high impedance faults. As an example, Figure 5.16 and Figure 5.17 show the FCSE for a 3ph and ph-ph faults at correspondence of 25km of line 2 and 10 km of line 1, respectively. The fault impedance is 100 Ω. For both illustrated cases, the real fault location can be identified by observing the FCSE curve.



**Figure 5.16. FCSE as a function of GFL for a 3ph fault at 25km of line 2. The fault impedance is 100 Ω.**



**Figure 5.17. FCSE as a function of GFL for a ph-ph fault at 10km of line 1. The fault impedance is 100  $\Omega$ .**

## 5.6 Conclusion

This chapter presented the developed fault location platform applied to power networks. The platform is developed by integrating the EMTR-based fault location method presented in Chapter 2 and the FPGA-RTS presented in Chapter 4. The developed platform takes advantage of the fast EMT simulation capability of the proposed FPGA-RTS to perform the fault location process within short computation time. The developed fault location system is validated by making reference to two applications: (i) an MTDC-HVDC network and (ii) an ADN.

For the case of MTDC network, first the possibility of applying EMTR-based fault location method with limited time reversal window is explored. This analysis is essential for these networks since the protection systems are required to act in much lower time scales compared to conventional systems for AC grids. Therefore, it is difficult to observe the full window of the fault-originated transient signals up to their damping. By taking advantage of specific peculiarities of the time reversal theory for closed reflecting media, it has been shown that it is possible to apply the fault location method by considering a limited time reversal window. The performance of the developed platform were analyzed by examining a series of different fault cases with different fault types and locations along the network and the estimated fault location accuracy was assessed with respect to the fault type, presence of the noise, measurement systems delay, and fault impedance. It was shown that the developed system is able to identify the correct fault location and exhibit excellent robustness against uncertainties such as noise, measurement delays and fault impedance.

The developed platform was also applied for the case of an ADN where the process is performed by using a single-end measurement system located at the primary

## 5.6 Conclusion

---

substation. Similarly to the case of an MTDC network, the performance of the platform was assessed by considering various fault cases with different fault types at different locations along the line. It was shown that estimated fault locations match with the real ones and the fault location accuracy was not affected by the type of the fault, the presence of the noise, measurement systems delay, and fault impedance.

## 6.1 Summary and Conclusions

The problem of fault location in power networks has been seriously reconsidered with the development of active distribution and MTDC-HVDC networks.

This thesis proposes a new concept for the fault location in AC/DC systems and its deployment in chip-scale real-time simulation hardware realized by FPGAs. The development of the proposed fault location platform is done in two steps. First, an original fault location method based on the Electromagnetic Time Reversal (EMTR) theory is proposed. The proposed method is validated for the case of various power networks topologies and a comprehensive assessment of its performances is also carried out. Then, a new automated FPGA-based RTS is proposed. The developed FPGA-RTS is able to simulate EMT phenomena taking place in power converters and travelling wave propagation in power grids within very small simulation time steps. In what follows, a summary of the studies that have been accomplished to develop the proposed fault location platform is presented.

### 6.1.1 Fault Location in Power Networks Based on EMTR Theory

Chapter 2 of the thesis presented the principles and the validation of a novel fault location method for power networks. First, the chapter summarized the Time Reversal (TR) focusing process by explaining the time reversal cavity and time reversal mirror concepts. Next, the application of the TR theory to Maxwell's equations in general, and to telegraphers' equations in particular, was illustrated. By taking advantage of the time reversal invariance of the telegraphers' equations, an original and efficient fault location method for power networks was presented.

Using transmission line equations in the frequency domain, analytical expressions were derived in order to infer the location of the fault. A time-domain implementation of the EMTR-based fault location technique was also proposed.

As the telegraphers' equations are invariant under a time-reversal transformation only for lossless lines, the impact of the losses on the performance of the proposed fault location method was also discussed. Three different models of back-propagation to address the issue of losses were considered: (i) inverted-loss, (ii) lossless, and (iii) lossy models. It has been shown through a numerical example related to a single-wire line above a conducting ground that, as expected, an inverted-loss model for the back-propagation results in a perfect estimation of the fault location. However, it is shown that, a back-propagation model in which the losses are included results also in a perfect estimation of the fault location, even though in this case the telegrapher's equations are not strictly time-reversal invariant.

The proposed method was validated by means of reduced scale experiments considering two topologies. In both cases, the proposed EMTR-based approach was able to correctly identify the location. Furthermore, several validation examples were performed by making reference to different types of power networks including (i) inhomogeneous network composed of mixed overhead-coaxial cable lines, (ii) radial distribution network, (iii) series-compensated transmission line. The resulting fault location accuracy and robustness against uncertainties (e.g., fault impedance, fault type, network topology) was tested and, in this respect, the proposed method appears to be very promising for real applications.

The main advantages of the proposed method, compared to the existing ones, are as following:

- The method is straightforwardly applicable to inhomogeneous media that, in our case, are represented by mixed overhead and coaxial cable lines.
- It is based on single-end measurement and requires the measurement of the fault-originated voltage/current transient signals only at one observation point in the network. Therefore, it does not need complex communication links and synchronization between multiple observation points.
- Its performances are not influenced by the topology of the system, fault type and impedance, presence of series compensation, and presence of measurement noise.

### 6.1.2 Efficient EMT Simulations Based on FAMNM

One of the common simulation approaches adopted by the existing FPGA-RTSs is the ADC model to represent the switches. This particular model allows the definition of a fixed nodal admittance matrix irrespective of the switch states, and acceleration of the simulation process by avoiding the matrix manipulations associated with each switch states. Therefore, the nodal admittance matrix is defined a-priori, inversed and used by the FPGA solver. Nevertheless, from the accuracy point of view, such simulation technique introduces artificial transients and errors in the simulation results. In Chapter 3, it is shown that the value of the conductance associated with the ADC model can dramatically impact the simulation results accuracy. The existing FPGA-RTSs do not take into account the impact of the ADC model on the accuracy of the simulated results, and the value of the ADC conductance is selected without quantitative error assessments.

In Chapter 3 of the thesis, a novel method for the optimal assessment of the ADC model parameter was presented. The proposed method is based on the minimization of the Euclidian distance between the eigenvalues of the network admittance matrix based on FAMNM, and those associated with the admittance matrices of reference networks corresponding to the all possible switching permutations. To prove the correctness of the proposed method, a comparison between the proposed metric and specific defined error functions was presented and discussed.

The proposed method was validated by making reference to several validation examples including RLC circuits composed of single or two switches, networks including transmission lines, single-phase inverter, and two-level three-phase inverter. The proposed method was proven to be correct in identifying the optimal conductance of the discrete-time switch model. The results of the proposed method minimizes: (i) the differences with reference-model current/voltage waveforms, and (ii) losses in the discrete-time switch conductance.

### 6.1.3 Automated FPGA-RTS for Power Electronics and Power Systems EMTs Simulations

In Chapter 4 of this thesis, an automated FPGA-based RTS for power electronics and power systems applications was presented. The proposed FPGA-RTS is implemented in an industrial real-time embedded system and has the following features: (i) it makes use of the MANA method, (ii) it integrates the FAMNM together with the optimal selection of the switch conductance parameter, (iii) it uses an efficient sparse matrix to vector multiplier which improves which improves the efficiency while significantly decreasing the FPGA hardware usage, (iv) it enables the possibility to accurately reproduce electromagnetic switching

transients taking place in power electronic switching devices together with electromagnetic waves propagation in transmission lines, and (v) it enables to reach extremely low integration time steps and provides an automated procedure to directly translate the schematic representation of the electrical circuits designed in EMTP-RV to the relevant FPGA solver.

Three validation examples were considered. They refer to (i) a two-level three-phase inverter, (ii) a multi-terminal HVDC network, and (iii) three-phase AC network. The comparison of the obtained results with respect to offline benchmark ones and the HIL validation showed an excellent agreement together with high computation efficiency. The proposed FPGA RTS exhibits remarkable performance in terms of the achieved simulation time step and the accuracy of the simulation results.

#### **6.1.4 FPGA-Based Fault Location Platform Based on the EMTR**

An original fault location platform was proposed in Chapter 5. The platform is developed by integrating the EMTR-based fault location method presented in Chapter 2 and the FPGA-RTS presented in Chapter 4. The developed platform takes advantage of the fast EMT simulation capability of the proposed FPGA-RTS to perform the fault location process within short computation time. The developed fault location system was validated by making reference to two applications: (i) an MTDC-HVDC network and (ii) an ADN.

For the case of MTDC network, the platform is developed such that it is compatible with the constraints associated with the time scales required by these grids protections. By taking advantage of specific peculiarities of the time reversal theory for closed reflecting media, the application of the proposed EMTR fault location method was adapted using a limited time reversal window for the measured fault-originated transient signals. The performances of the developed platform were analyzed by considering the substantial factors might impact the fault location accuracy. It was shown that the developed system is able to identify the correct fault location and exhibit excellent robustness against uncertainties such as noise, measurement delays and fault impedance.

The developed platform was also applied for the case of an ADN where the process is performed by using a single-end measurement system located at the primary substation. The performances of the platform were assessed by considering numerous fault cases with different fault types at different locations along the line. It was shown that estimated fault locations match with the real ones and the fault location accuracy was not affected by the type of the fault, the presence of the noise, measurement systems delay, and fault impedance.



## 6.2 Contributions

The main contributions of the thesis are as summarized below:

- Development of a novel and efficient fault location method based on the EMTR theory. Validation by means of reduced-scale experimental setup and simulations of power grids with various topologies and characteristics.
- Analysis of the impact of losses on the accuracy of the EMTR fault location method by considering different back-propagation models.
- Development of an original method for the optimal assessment of the ADC conductance value used in the FPGA-RTSs in order to minimize the simulation errors.
- Development of a new automated FPGA-RTS for the EMT simulations of the power electronics devices and power system grids with propagative multi-conductor transmission lines.
- Validation of the proposed FPGA-RTS by performing a dedicated Hardware-in-the-Loop (HIL) test and quantitative error easements by comparing the FPGA-RTS results with the benchmark one obtained by means of offline simulations and the measurements from a real inverter.
- Analysis of the applicability of the proposed EMTR fault location method using limited time reversal window to comply with the requirements characterizing MTDC networks.
- Development of a new type of fault location platforms by integrating the proposed EMTR fault method with the developed FPGA-RTS.

## 6.3 Future Works

In the continuation of this work, the following topics are suggested for further studies and potential industrial applications:

1. The proposed EMTR-based fault location method in Chapter 2 can be complemented by considering the following aspects.
  - 1.1. The method relies on the placement of several guessed fault locations (GFL), which requires numerous back-propagation simulations in order to identify the fault location. This method can be improved by considering a procedure which avoids the need for inspection of different GFLs.

- 1.2. Sensitivity assessments to analyze the impact of the accuracy of the network model on the fault location method.
- 1.3. Considering the frequency dependent transmission line models instead of a constant-parameter model.
2. The method proposed in Chapter 3 to assess the optimal ADC switch model parameter can be applied for more complex topologies with multiple switches by considering a dedicated conductance value for each switch.
3. The performance of the proposed FPGA-RTS in Chapter 4 can be improved by:
  - 3.1. Considering a floating point representation of the solver variables.
  - 3.2. Considering more accurate transmission line models such as FD model.
4. The proposed fault location platform in Chapter 5 can be extended to consider the following aspects.
  - 4.1. Development of a systematic procedure to determine the minimum time reversal window duration to provide accurate fault location results.
  - 4.2. Design and implementation of the fault triggering system which initiates the recording of the fault-originated transient signals and activates the fault location system.
  - 4.3. Analysis of the limitations associated with the measurement systems (e.g., delays, bandwidth, saturation, etc.) on the performance of the fault location system.
  - 4.4. Filtering disturbances other than the fault-originated ones (induced voltages, load energizing/de-energizing, etc.)
  - 4.5. Implementing a fully automated algorithm which enables the straightforward application of the platform for a given network.
  - 4.6. Development of the communication protocols to interact with other control/protection system.

## Bibliography

- [1] M. M. Saha, J. J. Izykowski, and E. Rosolowski, *Fault Location on Power Networks*, vol. 25. Springer Science & Business Media, 2009.
- [2] F. P. P.M. van Oirsouw, “Fault Localisation in an MV Distribution Network,” *Phase to Phase report*, 2003. [Online]. Available: <http://www.phasetophase.nl>.
- [3] “IEEE Guide for Determining Fault Location on AC Transmission and Distribution Lines.” 2005.
- [4] T. W. Stringfield, D. J. Marihart, and R. F. Stevens, “Fault Location Methods for Overhead Lines,” *Trans. Am. Inst. Electr. Eng. Part III Power Appar. Syst.*, vol. 76, no. 3, pp. 518–529, Apr. 1957.
- [5] T. Takagi, Y. Yamakoshi, M. Yamaura, R. Kondow, and T. Matsushima, “Development of a New Type Fault Locator Using the One-Terminal Voltage and Current Data,” *IEEE Trans. Power Appar. Syst.*, vol. PAS-101, no. 8, pp. 2892–2898, Aug. 1982.
- [6] L. Eriksson, M. M. Saha, and G. D. Rockefeller, “An Accurate Fault Locator with Compensation for Apparent Reactance in the Fault Resistance Resulting from Remote-End Infeed,” *IEEE Power Eng. Rev.*, vol. PER-5, no. 2, pp. 44–44, Feb. 1985.
- [7] C. E. M. Pereira and L. C. Zanetta, “Fault Location in Transmission Lines Using One-Terminal Postfault Voltage Data,” *IEEE Trans. Power Deliv.*, vol. 19, no. 2, pp. 570–575, Apr. 2004.
- [8] T. Kawady and J. Stenzel, “A Practical Fault Location Approach for Double Circuit Transmission Lines Using Single End Data,” *IEEE Trans. Power Deliv.*, vol. 18, no. 4, pp. 1166–1173, Oct. 2003.

- [9] M. Kezunovic and B. Perunicic, "Automated Transmission Line Fault Analysis Using Synchronized Sampling at Two Ends," in *Proceedings of Power Industry Computer Applications Conference*, 1995, pp. 407–413.
- [10] A. A. Girgis, D. G. Hart, and W. L. Peterson, "A New Fault Location Technique for Two- and Three-Terminal Lines," *IEEE Trans. Power Deliv.*, vol. 7, no. 1, pp. 98–107, 1992.
- [11] D. Novosel, D. G. Hart, E. Udren, and J. Garitty, "Unsynchronized Two-Terminal Fault Location Estimation," *IEEE Trans. Power Deliv.*, vol. 11, no. 1, pp. 130–138, 1996.
- [12] A. L. Dalcastagne, S. N. Filho, H. H. Zurn, and R. Seara, "An Iterative Two-Terminal Fault-Location Method Based on Unsynchronized Phasors," *IEEE Trans. Power Deliv.*, vol. 23, no. 4, pp. 2318–2329, Oct. 2008.
- [13] J. Izykowski, E. Rosolowski, P. Balcerek, M. Fulczyk, and M. M. Saha, "Accurate Noniterative Fault-Location Algorithm Utilizing Two-End Unsynchronized Measurements," *IEEE Trans. Power Deliv.*, vol. 26, no. 2, pp. 547–555, Apr. 2011.
- [14] T. Nagasawa, M. Abe, N. Otsuzuki, T. Emura, Y. Jikihara, and M. Takeuchi, "Development of a New Fault Location Algorithm for Multi-Terminal two Parallel Transmission Lines," *IEEE Trans. Power Deliv.*, vol. 7, no. 3, pp. 1516–1532, Jul. 1992.
- [15] G. Manassero, E. C. Senger, R. M. Nakagomi, E. L. Pellini, and E. C. N. Rodrigues, "Fault-Location System for Multiterminal Transmission Lines," *IEEE Trans. Power Deliv.*, vol. 25, no. 3, pp. 1418–1426, Jul. 2010.
- [16] T. Funabashi, H. Ootoguro, Y. Mizuma, L. Dube, and A. Ametani, "Digital Fault Location for Parallel Double-Circuit Multi-Terminal Transmission Lines," *IEEE Trans. Power Deliv.*, vol. 15, no. 2, pp. 531–537, Apr. 2000.
- [17] S. M. Brahma, "Fault Location Scheme for a Multi-Terminal Transmission Line Using Synchronized Voltage Measurements," *IEEE Trans. Power Deliv.*, vol. 20, no. 2, pp. 1325–1331, Apr. 2005.
- [18] Chih-Wen Liu, Kai-Ping Lien, Ching-Shan Chen, and Joe-Air Jiang, "A Universal Fault Location Technique for N-Terminal Transmission Lines," *IEEE Trans. Power Deliv.*, vol. 23, no. 3, pp. 1366–1373, Jul. 2008.
- [19] J. Izykowski, R. Molag, E. Rosolowski, and M. M. Saha, "Accurate Location of Faults on Power Transmission Lines With Use of Two-End Unsynchronized Measurements," *IEEE Trans. Power Deliv.*, vol. 21, no. 2, pp. 627–633, Apr. 2006.

- 
- [20] Y. Liao and N. Kang, "Fault-Location Algorithms Without Utilizing Line Parameters Based on the Distributed Parameter Line Model," *IEEE Trans. Power Deliv.*, vol. 24, no. 2, pp. 579–584, Apr. 2009.
- [21] Y. G. Paithankar and M. T. Sant, "A New Algorithm for Relaying and Fault Location Based on Autocorrelation of Travelling Waves," *Electr. Power Syst. Res.*, vol. 8, no. 2, pp. 179–185, Mar. 1985.
- [22] P. McLaren and S. Rajendra, "Travelling-Wave Techniques Applied to the Protection of Teed Circuits:- Multi-Phase/Multi-circuit Systsem," *IEEE Trans. Power Appar. Syst.*, vol. PAS-104, no. 12, pp. 3551–3557, Dec. 1985.
- [23] A. O. Ibe and B. J. Cory, "A Travelling Wave-Based Fault Locator for Two- and Three-Terminal Networks," *IEEE Trans. Power Deliv.*, vol. 1, no. 2, pp. 283–288, 1986.
- [24] A. M. Ranjbar, A. R. Shirani, and A. F. Fathi, "A New Approach for Fault Location Problem on Power Lines," *IEEE Trans. Power Deliv.*, vol. 7, no. 1, pp. 146–151, 1992.
- [25] F. H. Magnago and A. Abur, "Fault location using wavelets," *IEEE Trans. Power Deliv.*, vol. 13, no. 4, pp. 1475–1480, 1998.
- [26] G. B. Ansell and N. C. Pahalawaththa, "Maximum Likelihood Estimation of Fault Location on Transmission Lines using Travelling Waves," *IEEE Trans. Power Deliv.*, vol. 9, no. 2, pp. 680–689, 1994.
- [27] A. Borghetti, M. Bosetti, M. Di Silvestro, C. A. Nucci, and M. Paolone, "Continuous-wavelet transform for Fault Location in Distribution Power Networks: Definition of Mother Wavelets Inferred From Fault Originated Transients," *IEEE Trans. Power Syst.*, vol. 23, no. 2, pp. 380–388, 2008.
- [28] Y. Zhang, N. Tai, and B. Xu, "Fault Analysis and Traveling-Wave Protection Scheme for Bipolar HVDC Lines," *IEEE Trans. Power Deliv.*, vol. 27, no. 3, pp. 1583–1591, 2012.
- [29] E. H. Shehab-Eldin and P. G. McLaren, "Travelling Wave Distance Protection-problem Areas and Solutions," *IEEE Trans. Power Deliv.*, vol. 3, no. 3, pp. 894–902, Jul. 1988.
- [30] D. J. Spoor and J. G. Zhu, "Improved Single-Ended Traveling-Wave Fault-Location Algorithm Based on Experience With Conventional Substation Transducers," *IEEE Trans. Power Deliv.*, vol. 21, no. 3, pp. 1714–1720, Jul. 2006.
- [31] M. Ando, E. Schweitzer, and R. Baker, "Development and Field-Data

- Evaluation of Single-End Fault Locator for Two-Terminal HVDC Transmission Lines-Part 2: Algorithm and Evaluation,” *IEEE Trans. Power Appar. Syst.*, vol. PAS-104, no. 12, pp. 3531–3537, Dec. 1985.
- [32] F. V. Lopes, K. M. Silva, F. B. Costa, W. L. A. Neves, and D. Fernandes, “Real-Time Traveling-Wave-Based Fault Location Using Two-Terminal Unsynchronized Data,” *IEEE Trans. Power Deliv.*, vol. 30, no. 3, pp. 1067–1076, Jun. 2015.
- [33] M. B. Dewe, S. Sankar, and J. Arrillaga, “The Application of Satellite Time References to HVDC Fault Location,” *IEEE Trans. Power Deliv.*, vol. 8, no. 3, pp. 1295–1302, 1993.
- [34] C.-S. Yu, “An Unsynchronized Measurements Correction Method for Two-Terminal Fault-Location Problems,” *IEEE Trans. Power Deliv.*, vol. 25, no. 3, pp. 1325–1333, Jul. 2010.
- [35] a Borghetti, M. Bosetti, C. a Nucci, M. Paolone, and a Abur, “Integrated Use of Time-Frequency Wavelet Decompositions for Fault Location in Distribution Networks: Theory and Experimental Validation,” *Power Deliv. IEEE Trans.*, vol. 25, no. 4, pp. 3139–3146, 2010.
- [36] A. Borghetti, S. Corsi, C. A. A. Nucci, M. Paolone, L. Peretto, and R. Tinarelli, “On the Use of Continuous-Wavelet Transform for Fault Location in Distribution Power Systems,” *Int. J. Electr. Power Energy Syst.*, vol. 28, no. 9, pp. 608–617, Nov. 2006.
- [37] M. Vetterli and C. Herley, “Wavelets and Filter Banks: Theory and Design,” *IEEE Trans. Signal Process.*, vol. 40, no. 9, pp. 2207–2232, 1992.
- [38] F.-C. Lu, Y. Chien, J. P. Liu, J. T. Lin, P. H. S. Yu, and R. R. T. Kuo, “An Expert System for Locating Distribution System Faults,” *IEEE Trans. Power Deliv.*, vol. 6, no. 1, pp. 366–372, 1991.
- [39] K. K. Kuan and K. Warwick, “Real-Time Expert System for Fault Location on High Voltage Underground Distribution Cables,” vol. 139, no. 3. pp. 235–240, 1992.
- [40] J.-C. Maun, “Artificial neural network approach to single-ended fault locator for transmission lines,” in *Proceedings of the 20th International Conference on Power Industry Computer Applications*, 1997, pp. 125–131.
- [41] J. Gracia, A. J. Mazon, and I. Zamora, “Best ANN Structures for Fault Location in Single- and Double-Circuit Transmission Lines,” *IEEE Trans. Power Deliv.*, vol. 20, no. 4, pp. 2389–2395, Oct. 2005.

- 
- [42] B. Bogert, "Demonstration of Delay Distortion Correction by Time-Reversal Techniques," *IEEE Trans. Commun.*, vol. 5, no. 3, pp. 2–7, Dec. 1957.
- [43] K. E. Schreiner, H. L. Funk, and E. Hopner, "Automatic Distortion Correction for Efficient Pulse Transmission," *IBM J. Res. Dev.*, vol. 9, no. 1, pp. 20–30, Jan. 1965.
- [44] J. Kormylo and V. Jain, "Two-Pass Recursive Digital Filter with Zero Phase Shift," *IEEE Trans. Acoust.*, vol. 22, no. 5, pp. 384–387, Oct. 1974.
- [45] M. Fink, C. Prada, F. Wu, and D. Cassereau, "Self Focusing in Inhomogeneous Media with Time Reversal Acoustic Mirrors," in *Proceedings, IEEE Ultrasonics Symposium*, 1989, pp. 681–686.
- [46] M. Fink, "Time Reversal of Ultrasonic Fields. I. Basic Principles.," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 39, no. 5, pp. 555–66, Jan. 1992.
- [47] F. Wu, J.-L. Thomas, and M. Fink, "Time Reversal of Ultrasonic Fields--- Part II: Experimental Results," *IEEE Transactions Ultrason. Ferroelectr. Freq. Control*, vol. 39, no. 5, pp. 567–578, 1992.
- [48] D. Cassereau and M. Fink, "Time-reversal of Ultrasonic Fields---III: Theory of the Closed Time-Reversal Cavity," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 39, no. 5, pp. 579–592, 1992.
- [49] G. Lerosey, J. de Rosny, A. Tourin, A. Derode, G. Montaldo, and M. Fink, "Time Reversal of Electromagnetic Waves," *Phys. Rev. Lett.*, vol. 92, no. 19, p. 193904, May 2004.
- [50] D. Liu, G. Kang, L. Li, Y. Chen, S. Vasudevan, W. Joines, J. Krolik, and L. Carin, "Electromagnetic Time-Reversal Imaging of a Target in a Cluttered Environment," *IEEE Trans. Antennas Propag.*, vol. 53, no. 9, pp. 3058–3066, Sep. 2005.
- [51] H. Zhai, S. Sha, V. K. Shenoy, S. Jung, M. Lu, K. Min, and E. Al., "An Electronic Circuit System for Time-Reversal of Ultra-Wideband Short Impulses Based on Frequency-Domain Approach," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 1, pp. 74–86, Jan. 2010.
- [52] J. D. Jackson, *Classical Electrodynamics*, 3rd ed. New York, USA: Wiley, 1999.
- [53] R. Snieder, "Time-Reversal Invariance and the Relation Between Wave Chaos and Classical Chaos," in *In Imaging of complex media with acoustic and seismic waves*, Springer Berlin Heidelberg, 2002, pp. 1–16.

- [54] F. Rachidi and M. Rubinstein, "Time Reversal of Electromagnetic Fields and its Application to Lightning Location," in *2013 International Symposium on Lightning Protection (XII SIPDA)*, 2013, pp. 378–383.
- [55] G. Lugrin, N. M. Parra, F. Rachidi, M. Rubinstein, and G. Diendorfer, "On the Location of Lightning Discharges Using Time Reversal of Electromagnetic Fields," *IEEE Trans. Electromagn. Compat.*, vol. 56, no. 1, pp. 149–158, Feb. 2014.
- [56] M. Fink, G. Montaldo, and M. Tanter, "Time-reversal Acoustics in Biomedical Engineering.," *Annu. Rev. Biomed. Eng.*, vol. 5, pp. 465–97, Jan. 2003.
- [57] W. R. Alam, M., McClellan, J. H., Norville, P. D., & Scott Jr, "Time-Reverse Imaging for Detection of Landmines," in *In Defense and Security*, 2204, pp. 167–174.
- [58] N. Mora, F. Rachidi, and M. Rubinstein, "Application of the Time Reversal of Electromagnetic Fields to Locate Lightning Discharges," *Atmos. Res.*, vol. 117, pp. 78–85, Nov. 2012.
- [59] R. Razzaghi, G. Lugrin, H. M. Manesh, C. Romero, M. Paolone, and F. Rachidi, "An Efficient Method Based on the Electromagnetic Time Reversal to Locate Faults in Power Networks," *IEEE Trans. Power Deliv.*, vol. 28, no. 3, pp. 1663–1673, Jul. 2013.
- [60] H. M. Manesh, G. Lugrin, R. Razzaghi, C. Romero, M. Paolone, and F. Rachidi, "A new method to locate faults in power networks based on Electromagnetic Time Reversal," in *2012 IEEE 13th International Workshop on Signal Processing Advances in Wireless Communications (SPAWC)*, 2012, pp. 469–474.
- [61] A. Greenwood, *Electrical transients in power systems*. New York: John Wiley and Sons, 1991.
- [62] A. Borghetti, M. Bosetti, C. A. Nucci, M. Paolone, and A. Abur, "Fault Location in Active Distribution Networks by Means of the Continuous-Wavelet Analysis of Fault-Originated High Frequency Transients," in *Proc. of the Cigré General Session*, 2010.
- [63] F. Rachidi, C. A. Nucci, M. Ianoz, and C. Mazzetti, "Influence of a Lossy Ground on Lightning-Induced Voltages on Overhead Lines," *IEEE Trans. Electromagn. Compat.*, vol. 38, no. 3, pp. 250–264, 1996.
- [64] F. Rachidi, "A Review of Field-to-Transmission Line Coupling Models With Special Emphasis to Lightning-Induced Voltages on Overhead Lines," *IEEE*



- 
- Trans. Electromagn. Compat.*, vol. 54, no. 4, pp. 898–911, Aug. 2012.
- [65] L. Gaspard, R. Razzaghi, F. Rachidi, and M. Paolone, “Electromagnetic Time Reversal Applied to Fault Detection: the Issue of Losses,” in *Joint IEEE International Symposium on Electromagnetic Compatibility and EMC Europe*, 2015.
- [66] C. A. Nucci and F. Rachidi, “Interaction of Electromagnetic Fields Generated by Lightning with Overhead Electrical Networks,” in *The Lightning Flash*, V. Cooray, Ed. London: IET, 2004, pp. 559–610.
- [67] H. Dommel, “Digital Computer Solution of Electromagnetic Transients in Single- and Multiphase Networks,” *IEEE Trans. Power Appar. Syst.*, vol. PAS-88, no. 4, pp. 388–399, Apr. 1969.
- [68] J. Mahseredjian, S. Lefebvre, and X.-D. Do, “A New Method for Time-Domain Modelling of Nonlinear Circuits in Large Linear Networks,” in *Proc. of 11th Power Systems Computation Conference PSCC*, 1993.
- [69] J. Mahseredjian, S. Denetière, L. Dubé, B. Khodabakhchian, and L. Gérin-Lajoie, “On a New Approach for the Simulation of Transients in Power Systems,” *Electr. Power Syst. Res.*, vol. 77, no. 11, pp. 1514–1520, Sep. 2007.
- [70] W. H. Kersting, “Radial Distribution Test Feeders,” in *2001 IEEE Power Engineering Society Winter Meeting. Conference Proceedings (Cat. No. 01CH37194)*, 2001, vol. 2, pp. 908–912.
- [71] Chi-Shan Yu, Chih-Wen Liu, Sun-Li Yu, and Joe-Air Jiang, “A New PMU-Based Fault Location Algorithm for Series Compensated Lines,” *IEEE Trans. Power Deliv.*, vol. 17, no. 1, pp. 33–46, 2002.
- [72] P. Jena and A. K. Pradhan, “A Positive-Sequence Directional Relaying Algorithm for Series-Compensated Line,” *IEEE Trans. Power Deliv.*, vol. 25, no. 4, pp. 2288–2298, Oct. 2010.
- [73] J. Izykowski, E. Rosolowski, P. Balcerek, M. Fulczyk, and M. M. Saha, “Fault Location on Double-Circuit Series-Compensated Lines Using Two-End Unsynchronized Measurements,” *IEEE Trans. Power Deliv.*, vol. 26, no. 4, pp. 2072–2080, Oct. 2011.
- [74] N. Watson and J. Arrillaga, *Power Systems Electromagnetic Transients Simulation*. The Institution of Engineering and Technology, Michael Faraday House, Six Hills Way, Stevenage SG1 2AY, UK: Institution of Engineering and Technology, 2003.
- [75] W. A. Radasky and M. W. Wik, “IEC Standardization of Immunity to High

- Altitude Nuclear Electromagnetic Pulse (HEMP),” in *Proceedings of International Symposium on Electromagnetic Compatibility ELMAGC-97*, 1997, pp. 40–42.
- [76] M. R. N. Mora, F. Vega, G. Lugrin, F. Rachidi, “Study and Classification of Potential IEMI Sources,” *System Design and Assessment Notes, Note 41*, 2014.
- [77] J. Mahseredjian, “Computation of Power System Transients: Overview and Challenges,” in *2007 IEEE Power Engineering Society General Meeting*, 2007, pp. 1–7.
- [78] J. Mahseredjian, V. Dinavahi, and J. A. Martinez, “Simulation Tools for Electromagnetic Transients in Power Systems: Overview and Challenges,” *IEEE Trans. Power Deliv.*, vol. 24, no. 3, pp. 1657–1669, 2009.
- [79] H. W. Dommel, *EMTP Theory Book*. Bonneville Power Administration, 1984.
- [80] L. O. Chua and P. M. Lin, *Computer-Aided Analysis of Electronic Circuits: Algorithms & Computational Techniques*. Prentice-Hall, 1975.
- [81] R. M. Mathur and X. Wang, “Real-Time Digital Simulator of the Electromagnetic Transients of Power Transmission Lines,” *IEEE Trans. Power Deliv.*, vol. 4, no. 2, pp. 1275–1280, Apr. 1989.
- [82] X. Wang and R. M. Mathur, “Real-time Digital Simulator of the Electromagnetic Transients of Transmission Lines with Frequency Dependence,” *IEEE Trans. Power Deliv.*, vol. 4, no. 4, pp. 2249–2255, 1989.
- [83] M. Kezunovic, M. Aganagic, V. Skendzic, J. Domaszewicz, J. K. Bladow, D. M. Hamai, and S. M. McKenna, “Transients Computation for Relay Testing in Real-Time,” *IEEE Trans. Power Deliv.*, vol. 9, no. 3, pp. 1298–1307, Jul. 1994.
- [84] A. E. Hakimi, H. Le-Huy, C. Dufour, and I. Kamwa, “Real-Time Methods for Power-Transmission Networks Simulation,” in *ICDS '95. First International Conference on Digital Power System Simulators*, 1995, p. 287.
- [85] C. Dufour, J. C. Soumagne, and A. El Hakimi, “Real-Time Simulation of Power Transmission Lines Using Marti Model with Optimal Fitting on Dual-DSP Card,” *IEEE Trans. Power Deliv.*, vol. 11, no. 1, pp. 412–419, 1996.
- [86] J. Marti, “Accurate Modelling of Frequency-Dependent Transmission Lines in Electromagnetic Transient Simulations,” *IEEE Trans. Power Appar. Syst.*, vol. PAS-101, no. 1, pp. 147–157, Jan. 1982.
- [87] J. R. Marti and L. R. Linares, “Real-time EMTP-based transients

- simulation,” *IEEE Trans. Power Syst.*, vol. 9, no. 3, pp. 1309–1317, 1994.
- [88] Y. Fujimoto, Y. Bin, H. Taoka, H. Tezuka, S. Sumimoto, and Y. Ishikawa, “Real-Time Power System Simulator on a PC-Cluster,” in *Proc. of the International Conference on Power Systems Transients (IPST 1999)*, 1999.
- [89] J. a. Hollman and J. Martí, “Real time network simulation with PC-cluster,” *Power Syst. IEEE Trans.*, vol. 18, no. 2, pp. 563–569, May 2003.
- [90] L.-F. Pak, M. O. Faruque, X. Nie, and V. Dinavahi, “A Versatile Cluster-Based Real-Time Digital Simulator for Power Engineering Research,” *IEEE Trans. Power Syst.*, vol. 21, no. 2, pp. 455–465, May 2006.
- [91] L. Fabre, G. Lanz, T. Kyriakidis, D. Sallin, I. Nagel, R. Cherkaoui, and M. Kayal, “An Ultra-High Speed Emulator Dedicated to Power System Dynamics Computation Based on a Mixed-Signal Hardware Platform,” *IEEE Trans. Power Syst.*, vol. 28, no. 4, pp. 4228–4236, Nov. 2013.
- [92] I. Nagel, L. Fabre, M. Pastre, F. Krummenacher, R. Cherkaoui, and M. Kayal, “High-Speed Power System Transient Stability Simulation Using Highly Dedicated Hardware,” *IEEE Trans. Power Syst.*, vol. 28, no. 4, pp. 4218–4227, Nov. 2013.
- [93] P. G. McLaren, R. Kuffel, R. Wierckx, J. Giesbrecht, and L. Arendt, “A Real Time Digital Simulator for Testing Relays,” *IEEE Trans. Power Deliv.*, vol. 7, no. 1, pp. 207–213, 1992.
- [94] P. Forsyth, T. Maguire, and R. Kuffel, “Real Time Digital Simulation for Control and Protection System Testing,” in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, 2004, vol. 1, pp. 329–335.
- [95] “RTDS Technologies.” [Online]. Available: <http://www.rtds.com>.
- [96] V. Q. Do, J. C. Soumagne, G. Sybille, G. Turmel, P. Giroux, G. Cloutier, and S. Poulin, “HYPERSIM, an Integrated Real-Time Simulator for Power Network and Control Systems,” in *Proc. of International Conference on Digital Power System Simulators (ICDS 1999)*, 1999.
- [97] D. Pare, G. Turmel, J.-C. Soumagne, V. Q. Do, S. Casoria, M. Bissonnette, B. Marcourx, and C. McNabb, “Validation Tests of the HYPERSIM Digital Real Time Simulator with a Large AC-DC Network,” in *Proc. of the International Conference on Power Systems Transients (IPST 2003)*, 2003.
- [98] J. Belanger, V. Lapointe, C. Dufour, and L. Schoen, “eMEGAsim: An Open High-Performance Distributed Real-Time Power Grid Simulator,

- Architecture and Specification,” in *Proc. of the International Conference on Power Systems (ICPS 2007)*, 2007.
- [99] J. Belanger, L. A. Snider, J. N. Paquin, C. Pirolli, and W. Li, “A Modern and Open Real-Time Digital Simulator of Contemporary Power Systems,” in *Proc. of the International Conference on Power Systems Transients (IPST 2009)*, 2009.
- [100] I. Etxeberria-Otadui, V. Manzo, S. Bacha, and F. Baltes, “Generalized Average Modelling of FACTS for Real Time Simulation in ARENE,” in *IEEE 2002 28th Annual Conference of the Industrial Electronics Society. IECON 02*, 2002, vol. 2, pp. 864–869.
- [101] M. Matar and R. Iravani, “FPGA Implementation of the Power Electronic Converter Model for Real-Time Simulation of Electromagnetic Transients,” *IEEE Trans. Power Deliv.*, vol. 25, no. 2, pp. 852–860, Apr. 2010.
- [102] Y. Chen and V. Dinavahi, “FPGA-Based Real-Time EMTP,” *IEEE Trans. Power Deliv.*, vol. 24, no. 2, pp. 892–902, Apr. 2009.
- [103] C. Dufour, S. Cense, V. Jalili-Marandi, and J. Belanger, “Review of State-of-the-Art Solver Solutions for HIL Simulation of Power Systems, Power Electronic and Motor Drives,” in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–12.
- [104] M. Matar and R. Iravani, “Massively Parallel Implementation of AC Machine Models for FPGA-Based Real-Time Simulation of Electromagnetic Transients,” *IEEE Trans. Power Deliv.*, vol. 26, no. 2, pp. 830–840, Apr. 2011.
- [105] M. Matar and R. Iravani, “The Reconfigurable-Hardware Real-Time and Faster-Than-Real-Time Simulator for the Analysis of Electromagnetic Transients in Power Systems,” *IEEE Trans. Power Deliv.*, vol. 28, no. 2, pp. 619–627, Apr. 2013.
- [106] C. Dufour, S. Cense, T. Ould-Bachir, L. A. Gregoire, and J. Belanger, “General-Purpose Reconfigurable Low-Latency Electric Circuit and Motor Drive Solver on FPGA,” in *IECON Proceedings (Industrial Electronics Conference)*, 2012, pp. 3073–3081.
- [107] T. Ould Bachir, C. Dufour, J. Bélanger, J. Mahseredjian, and J. P. David, “A Fully Automated Reconfigurable Calculation Engine Dedicated to the Real-Time Simulation of High Switching Frequency Power Electronic Circuits,” *Math. Comput. Simul.*, vol. 91, pp. 167–177, 2012.
- [108] J. Bélanger, P. Venne, and S. Member, “The What , Where and Why of Real-

- Time Simulation,” pp. 37–49.
- [109] G. G. Parma and V. Dinavahi, “Real-Time Digital Hardware Simulation of Power Electronics and Drives,” *IEEE Trans. Power Deliv.*, vol. 22, no. 2, pp. 1235–1246, Apr. 2007.
- [110] M. Matar, H. Karimi, A. Etemadi, and R. Iravani, “A High Performance Real-Time Simulator for Controllers Hardware-in-the-Loop Testing,” *Energies*, vol. 5, no. 12, pp. 1713–1733, Jun. 2012.
- [111] A. Myaing and V. Dinavahi, “FPGA-Based Real-Time Emulation of Power Electronic Systems With Detailed Representation of Device Characteristics,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 358–368, Jan. 2011.
- [112] H. F. Blanchette, T. Ould-Bachir, and J. P. David, “A State-Space Modeling Approach for the FPGA-Based Real-Time Simulation of High Switching Frequency Power Converters,” *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4555–4567, Dec. 2012.
- [113] “eFPGAsim Power Electronic Real-Time Simulator.” [Online]. Available: <http://www.opal-rt.com/new-product/efpgasim-power-electronic-real-time-simulator>.
- [114] D. Majstorovic, I. Celanovic, N. D. Teslic, N. Celanovic, and V. A. Katic, “Ultralow-Latency Hardware-in-the-Loop Platform for Rapid Validation of Power Electronics Designs,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4708–4716, Oct. 2011.
- [115] “Typhoon HIL.” [Online]. Available: <https://www.typhoon-hil.com/>.
- [116] R. Razzaghi, C. Foti, M. Paolone, and F. Rachidi, “A Method for the Assessment of the Optimal Parameter of Discrete-Time Switch Model,” *Electr. Power Syst. Res.*, vol. 115, pp. 80–86, Oct. 2014.
- [117] M. Matar and R. Iravani, “The Reconfigurable-Hardware Real-Time and Faster-Than-Real-Time Simulator for the Analysis of Electromagnetic Transients in Power Systems,” *IEEE Trans. Power Deliv.*, vol. 28, no. 2, pp. 619–627, Apr. 2013.
- [118] J. R. Marti and J. Lin, “Suppression of Numerical Oscillations in the EMTP Power Systems,” *IEEE Trans. Power Syst.*, vol. 4, no. 2, pp. 739–747, May 1989.
- [119] C. A. Thompson, “A Study of Numerical Integration Techniques for use in the companion circuit method of transient circuit analysis,” 1997.
- [120] T. T. Hartley, G. O. Beale, and S. P. Chicatelli, *Digital Simulation of*

- Dynamic Systems: A Control Theory Approach*. NJ, USA: Prentice-Hall, Inc., 1994.
- [121] R. J. LeVeque, *Finite Difference Methods for Ordinary and Partial Differential Equations: Steady-State and Time-Dependent Problems*. Siam, 2007.
- [122] A. Morched, B. Gustavsen, and M. Tartibi, "A Universal Model for Accurate Calculation of Electromagnetic Transients on Overhead Lines and Underground Cables," *IEEE Trans. Power Deliv.*, vol. 14, no. 3, pp. 1032–1038, Jul. 1999.
- [123] A. Semlyen and A. Dabuleanu, "Fast and Accurate Switching Transient Calculations on Transmission Lines with Ground Return using Recursive Convolutions," *IEEE Trans. Power Appar. Syst.*, vol. 94, no. 2, pp. 561–571, Mar. 1975.
- [124] A. Tavighi, J. Martí, and J. A. G. Robles, "Comparison of the fdLine and ULM Frequency Dependent EMTP Line Models with a Reference Laplace Solution," in *International Power Systems Transients Conference (IPST)*, 2015.
- [125] L. Bergeron, *Du coupde bélier en hydraulique au coupde foudre en électricité*. Paris, France: Dunod, 1949.
- [126] H. Jin, "Behavior-Mode Simulation of Power Electronic Circuits," *IEEE Trans. Power Electron.*, vol. 12, no. 3, pp. 443–452, May 1997.
- [127] H. Wu and W. Feng, "Efficient simulation of switched networks using reduced unification matrix," *IEEE Trans. Power Electron.*, vol. 14, no. 3, pp. 481–494, May 1999.
- [128] S. Y. R. Hui and C. Christopoulos, "A Discrete Approach to the Modeling of Power Electronic Switching Networks," *IEEE Trans. Power Electron.*, vol. 5, no. 4, pp. 398–403, 1990.
- [129] S. Y. R. Hui and S. Morrall, "Generalised Associated Discrete Circuit Model for Switching Devices," *IEE Proc. - Sci. Meas. Technol.*, vol. 141, no. 1, pp. 57–64, Jan. 1994.
- [130] P. Pejovic and D. Maksimovic, "Method for fast time-domain simulation of networks with switches," *IEEE Trans. Power Electron.*, vol. 9, no. 4, pp. 449–456, 1994.
- [131] J. A. Gutiérrez-Robles, L. A. Snider, J. L. Naredo, and O. Ramos-Leanos, "An Investigation of Interpolation Methods Applied in Transmission Line Models

- for EMT Analysis,” in *International Conference on Power Systems Transients (IPST2011)*, 2011, pp. 1–6.
- [132] R. Razzaghi, C. Foti, M. Paolone, and F. Rachidi, “A Novel Method for the Optimal Parameter Selection of Discrete-Time Switch Model,” in *International Power Systems Transients Conference (IPST)*, 2013.
- [133] T. Maguire and J. Giesbrecht, “Small Time-Step (<2 us) VSC Model for the Real Time Digital Simulator,” in *International Power Systems Transients Conference (IPST)*, 2005.
- [134] M. Matar and R. Iravani, “An FPGA-Based Real-Time Digital Simulator for Power Electronic Systems,” in *International Conference on Power Systems Transients (IPST)*, 2007.
- [135] M. Matar, H. Karimi, A. Etemadi, and R. Iravani, “A High Performance Real-Time Simulator for Controllers Hardware-in-the-Loop Testing,” *Energies*, vol. 5, no. 12, pp. 1713–1733, Jun. 2012.
- [136] M. P. Kazmierkowski and L. Malesani, “Current Control Techniques for Three-Phase Voltage-Source PWM Converters: a Survey,” *IEEE Trans. Ind. Electron.*, vol. 45, no. 5, pp. 691–703, 1998.
- [137] V. TK, Y. Y, D. S, J. J, and S. H, “The CIGRE B4 DC Grid Test System,” 2013.
- [138] Y. Zhang, N. Tai, and B. Xu, “Fault Analysis and Traveling-Wave Protection Scheme for Bipolar HVDC Lines,” *IEEE Trans. Power Deliv.*, vol. 27, no. 3, pp. 1583–1591, Jul. 2012.
- [139] H. Bahirat, H. Hoidalén, and B. Mork, “Thevenin Equivalent of Voltage Source Converters for DC Fault Studies,” *IEEE Trans. Power Deliv.*, vol. PP, no. 99, pp. 1–1, 2015.
- [140] J. Descloux, “Protection Contre les Courts-Circuits des Reseaux a Courant Continu de Forte Puissance,” Université de Grenoble, 2013.
- [141] D. Van Hertem and M. Ghandhari, “Multi-Terminal VSC HVDC for the European Supergrid: Obstacles,” *Renew. Sustain. Energy Rev.*, vol. 14, no. 9, pp. 3156–3163, 2010.
- [142] G. Shi, Z. Chen, and X. Cai, “Overview of multi-terminal VSC HVDC transmission for large offshore wind farms,” in *2011 International Conference on Advanced Power System Automation and Protection*, 2011, vol. 2, pp. 1324–1329.
- [143] P. Bresesti, W. L. Kling, and R. Vailati, “Transmission Expansion Issues for

- Offshore Wind Farms Integration in Europe,” in *2008 IEEE/PES Transmission and Distribution Conference and Exposition*, 2008, pp. 1–7.
- [144] C. M. Franck, “HVDC Circuit Breakers: A Review Identifying Future Research Needs,” *IEEE Trans. Power Deliv.*, vol. 26, no. 2, pp. 998–1007, Apr. 2011.
- [145] V. T. K. T.-O. R. E, L. B, and T. M. Haileselassie, “The North Sea Super Grid - A Technical Perspective,” in *International Conference on AC and DC Power Transmission*, 2010.
- [146] J. Yang, J. E. Fletcher, and J. O’Reilly, “Multiterminal DC Wind Farm Collection Grid Internal Fault Analysis and Protection Design,” *IEEE Trans. Power Deliv.*, vol. 25, no. 4, pp. 2308–2318, 2010.
- [147] J. Descloux, B. Raison, and J. B. Curis, “Protection Strategy for Undersea MTDC Grids,” *2013 IEEE Grenoble Conf. PowerTech, POWERTECH 2013*, 2013.
- [148] N. Ahmed, A. Haider, D. Van Hertem, L. Zhang, and H.-P. Nee, “Prospects and Challenges of Future HVDC SuperGrids with Modular Multilevel Converters,” *Power Electron. Appl. (EPE 2011), Proc. 2011-14th Eur. Conf.*, pp. 1–10, 2011.
- [149] L. Tang and B.-T. Ooi, “Locating and Isolating DC Faults in Multi-Terminal DC Systems,” *IEEE Trans. Power Deliv.*, vol. 22, no. 3, pp. 1877–1884, Jul. 2007.
- [150] K. De Kerf, K. Srivastava, M. Reza, D. Bekaert, S. Cole, D. Van Hertem, and R. Belmans, “Wavelet-Based Protection Strategy for DC Faults in Multi-Terminal VSC HVDC Systems,” *IET Gener. Transm. Distrib.*, vol. 5, no. January, p. 496, 2011.
- [151] L. T. L. Tang and B.-T. O. B.-T. Ooi, “Protection of VSC-Multi-Terminal HVDC Against DC Faults,” *2002 IEEE 33rd Annu. IEEE Power Electron. Spec. Conf. Proc. (Cat. No.02CH37289)*, vol. 2, pp. 719–724, 2002.
- [152] A. E. B. Abu-Elanien, A. A. Elserougi, A. S. Abdel-Khalik, A. M. Massoud, and S. Ahmed, “A Differential Protection Technique for Multi-Terminal HVDC,” *Electr. Power Syst. Res.*, vol. 130, pp. 78–88, Jan. 2016.
- [153] O. M. K. K. Nanayakkara, A. D. Rajapakse, and R. Wachal, “Traveling-wave-based line fault location in star-connected multiterminal HVDC systems,” *IEEE Trans. Power Deliv.*, vol. 27, no. 4, pp. 2286–2294, Oct. 2012.
- [154] J. Yang, J. E. Fletcher, and J. O’Reilly, “Short-Circuit and Ground Fault



- Analyses and Location in VSC-Based DC Network Cables,” *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3827–3837, Oct. 2012.
- [155] J. Suonan, S. Gao, G. Song, Z. Jiao, and X. Kang, “A Novel Fault-Location Method for HVDC Transmission Lines,” *IEEE Trans. Power Deliv.*, vol. 25, no. 2, pp. 1203–1209, Apr. 2010.
- [156] W. Leterme and D. Van Hertem, “Classification of Fault Clearing Strategies for HVDC Grids,” in *Cigre*, 2015.
- [157] C. Draeger and M. Fink, “One-Channel Time Reversal of Elastic Waves in a Chaotic 2D-Silicon Cavity,” *Phys. Rev. Lett.*, vol. 79, no. 3, pp. 407–410, Jul. 1997.
- [158] C. Draeger, J.-C. Aime, and M. Fink, “One-Channel Time-Reversal in Chaotic Cavities: Experimental Results,” *J. Acoust. Soc. Am.*, vol. 105, no. 2, p. 618, Feb. 1999.
- [159] M. Fink, “Time-Reversal Acoustics in Complex Environments,” *Geophysics*, vol. 71, no. 4, p. SI151, 2006.
- [160] P. Romano and M. Paolone, “Enhanced Interpolated-DFT for Synchrophasor Estimation in FPGAs: Theory, Implementation, and Validation of a PMU Prototype,” *IEEE Trans. Instrum. Meas.*, vol. 63, no. 12, pp. 2824–2836, Dec. 2014.



# Curriculum Vitae

## REZA RAZZAGHI

Distributed Electrical Systems Laboratory (DESL)  
École Polytechnique Fédérale de Lausanne (EPFL)

Born in 19<sup>th</sup> July, 1987, Maragheh, Iran

Email: [r.razzaghi87@gmail.com](mailto:r.razzaghi87@gmail.com)

Tel : +41 78 907 5556

Address: Avenue d'Ouchy 64, CH-1006  
Lausanne, Switzerland

### Education

---

- |           |  |
|-----------|--|
| 2011-2015 | <b>Ph.D. in Electrical Engineering</b> , <i>Swiss Federal Institute of Technology (EPFL)</i> , Switzerland.<br><b>Thesis:</b> Fast simulation of Electromagnetic Transients in power systems: numerical solvers and their coupling with the Electromagnetic Time Reversal process. |
| 2009-2011 | <b>Master of Science in Electrical Power Engineering</b> , <i>University of Tehran</i> , Iran.<br><b>Thesis:</b> Dynamic response of distributed generators (DGs) to system faults and perturbations, protection against transient instability.                                    |
| 2005-2009 | <b>Bachelor of Science in Electrical Engineering</b> , <i>University of Tehran</i> , Iran.   |

### Professional Experience

---

- |           |   |
|-----------|---|
| 2011-2015 | <b>Doctoral assistant</b> , Distributed Electrical Systems Laboratory (DESL)-EPFL, Lausanne, Switzerland. |
| 2009-2010 | <b>Consultant engineer</b> , Faraniroo Engineering Company, Tehran, Iran.                                 |

### Research Interests

---

- Power system protection and fault location.
- Power system modeling and simulation.
- Real-time simulation of electromagnetic transients in power electronics and power systems.

### Language Skills:

---

- Azerbaijani (native)
- Persian (Native)
- English (Fluent, IBT: 99/120)
- French (Intermediate, B1)
- German (Beginner, A2)

## Awards and Scientific Recognitions

---

- |      |  |
|------|--|
| 2015 | Distinguished PhD research presented at <a href="#">EPFL homepage</a> , <a href="#">EPFL-TV interview</a> , <b>24 Heures</b> newspaper, and <b>RTS radio</b> . |
| 2015 | Best Poster award at EPFL-EDEE scientific exchange day.  |
| 2013 | Basil Papadias Best Paper award at the 2013 IEEE PowerTech, Grenoble, France.  |
| 2009 | Ranked 2 <sup>nd</sup> among nearly 12000 participants in the nation wide universities entrance Exam for MSc Degree.   |
| 2005 | Ranked 91 <sup>st</sup> among nearly 400,000 participants in the nation wide universities entrance Exam for BSc Degree.  |

## Scientific Visits and Collaboration

---

- |      |  |
|------|--|
| 2015 | <b>École Polytechnique de Montréal, Canada</b> , Real-time simulation of Modular Multilevel Converters using FPGAs.                  |
| 2014 | <b>L2EP, Ecole Centrale de Lille, France</b> , Hardware-in-the-loop validations using FPGA-based real-time simulator.                |
| 2014 | <b>HES-SO Valais-Wallis, Switzerland</b> , General purpose FPGA-based real-time simulator for electromagnetic transient simulations. |
| 2014 | <b>National Instruments, Austin, USA</b> , Efficient real-time simulation of power electronics and power systems using FPGAs.        |
| 2013 | <b>G2Elab, Grenoble University, France</b> , Fault location in multi-terminal HVDC networks.   |

## Publications

---

### Book Chapter

---

“Electromagnetic Time Reversal: Application to Electromagnetic Compatibility and Power Systems” Chapter 7: Electromagnetic Time Reversal Applied to Fault Detection in Power Networks. Wiley (in preparation).

### Patent

---

M. Paolone, F. Rachidi, H. Manesh, **R. Razzaghi**, G. Lugrin “Efficient Method Based on the Electromagnetic Time Reversal to Locate Faults in Power Network,” US20140300370 A1.

## Journal Papers

---

- 1- **R. Razzaghi**, M. Davarpanah, M. Sanaye-Pasand, "A Novel Protective Scheme to Protect Small Scale Synchronous Generators against Transient Instability," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, April, 2013.
- 2- **R. Razzaghi**, G. Lugrin, H. Manesh, C. Romero, M. Paolone, and F. Rachidi, "An Efficient Method Based on the Electromagnetic Time Reversal to Locate Faults in Power Networks," *IEEE Transactions on Power Delivery*, vol. 28, no. 3, pp. 1663–1673, Jul. 2013.
- 3- **R. Razzaghi**, C. Foti, M. Paolone, F. Rachidi, "A Method for the Assessment of the Optimal Parameter of Discrete-Time Switch Model," *Electric Power Systems Research*, vol. 115, p.p. 80-86, October 2014.
- 4- **R. Razzaghi**, M. Mitjans, F. Rachidi, M. Paolone, "An Automated FPGA Real-Time Digital Simulator for Power Electronics and Power Systems Electromagnetic Transients," Submitted to *IEEE Transactions on Power Delivery*, 2015.

## Conference Proceedings

---

- 1- H. Manesh, G. Lugrin, **R. Razzaghi**, C. Romero, M. Paolone, and F. Rachidi, "A new Method to Locate Faults in Power Networks Based on the Electromagnetic Time Reversal," *IEEE 13th International Workshop on Signal Processing Advances in Wireless Communications (SPAWC)*, Cesme, June, 2012.
- 2- **R. Razzaghi**, C. Foti, M. Paolone, F. Rachidi, "A Novel Method for the Optimal Parameter Selection of Discrete-Time Switch Model," *10th International Conference on Power Systems Transients (IPST2013)*, Vancouver, Canada, July 18-20, 2013.
- 3- **R. Razzaghi**, G. Lugrin, M. Paolone, F. Rachidi, "On the Use of Electromagnetic Time Reversal to Locate Faults in Series-Compensated Transmission Lines," *Proceedings of the 2013 IEEE Grenoble PowerTech, Grenoble, France, June, 2013. The paper obtained the Basil Papadias best paper award of the conference.*
- 4- **R. Razzaghi**, M. Paolone, F. Rachidi, "A General Purpose FPGA-Based Real-Time Simulator for Power Systems Applications," in *2013 4th IEEE/PES Innovative Smart Grid Technologies Europe, Copenhagen, Denmark, Oct. 2013.*
- 5- **R. Razzaghi**, M. Paolone, F. Rachidi, J. Descloux, B. Raison, N. Retiere, "Fault Location in Multi-Terminal HVDC Networks Based on Electromagnetic Time Reversal with Limited Time Reversal Window," *Proceedings of the Power Systems Computation Conference*, Wroclaw, Poland, Aug. 18-22, 2014
- 6- **R. Razzaghi**, F. Colas, X. Guillaud, M. Paolone, F. Rachidi, "Hardware-in-the-Loop Validation of an FPGA-Based Real-Time Simulator for Power Electronics Applications," *Proceedings of International Conference on Power Systems Transients (IPST2015)*, Cavtat, Croatia, June 15-18, 2015.
- 7- G. Lugrin, **R. Razzaghi**, F. Rachidi, M. Paolone, "Electromagnetic Time Reversal Applied to Fault Detection: the Issue of Losses," *Proceedings Joint IEEE International Symposium on Electromagnetic Compatibility and EMC Europe, Dresden, Germany, August, 2015.*