A Correlated Multiple Sampling Passive Switched Capacitor Circuit for Low Light CMOS Image Sensors

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***Abstract*—After a brief review of the principle of correlated multiple sampling (CMS) and its implementation techniques in CIS readout chains, a simple CMS passive circuit that (i) requires no additional active circuitry, (ii) has no impact on the output dynamic range and (iii) does not need multiple analog-to-digital conversions (faster) is presented. The proposed circuit uses n switched capacitors to perform a CMS on 2^n samples. It is validated using transient noise simulations on a CIS readout chain based on a 4T pixel, designed with a 180nm CIS process. For a line readout time of 35 μs and a column amplifier bandwidth of 256 kHz, the proposed circuit reduces the input-referred noise as expected by an ideal CMS.**

***Keywords*—Noise; CMOS; image sensors; CMS; passive; switched-capacitor.**

I. Introduction

It is known that for low light CMOS image sensors (CIS) based on pinned photodiodes, the combined 1/f and thermal readout circuit noise becomes the dominant source in low light conditions [1]. Thermal noise can be drastically reduced using column level amplification and bandwidth control. 1/f noise originating from the in-pixel source follower, despite the impact of the correlated double sampling (CDS), remains the dominant noise source in low light CIS readout chains. In the last few years, correlated multiple sampling (CMS) has been used at column level for more efficient 1/f and thermal noise reduction. Two main implementations have been introduced, one using additional column level active circuitry to integrate multiple samples in one capacitor [2] and the other one performs the CMS after the analog-to-digital conversion using multiple conversions [3]. This paper presents a new simple analog implementation of CMS that (i) requires no additional active circuitry, (ii) has no impact on the output dynamic range and (iii) does not need multiple analog-to-digital conversions.

This paper is organized as follows. Section II reviews the CMS principle and its impact on $1/f$ and thermal noise. Section III reports the current implementations of CMS in state-of-the-art CIS readout chains. Section IV presents the new circuit implementation and, in Section V, the proposed circuit implementation of CMS is validated using transient noise simulations.

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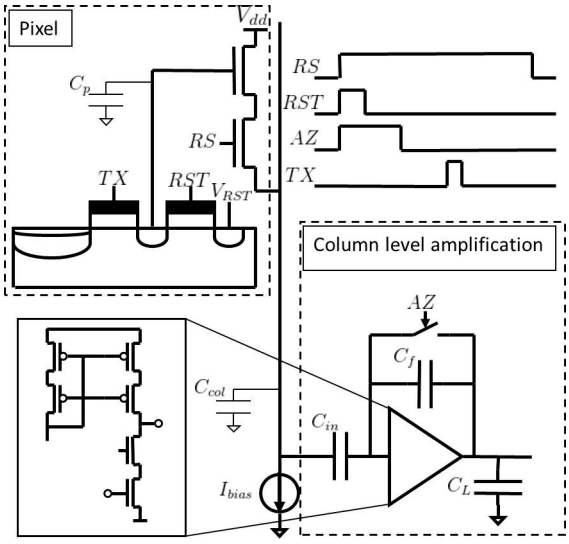

Fig. 1. Schematic of a classical CIS readout chain showing the pixel-level and column-level- amplification circuits with the timing diagram

II. Correlated Multiple Sampling in CIS

Fig. 1 shows a classical CIS readout chain based on a classical 4T pixel with a pinned photodiode and a column level amplifier. The row selector is first turned on (RS high) to select the pixel. Then, the sense node is reset to a voltage V_{RST} higher than the pinning voltage. The transfer gate is clocked down to sink photo-generated electrons in the sense node. After auto-zeroing of the column amplifier, the reset voltage level is sampled at the output of the column amplifier. Then, the transfer gate (TX) is activated to allow the charge transfer from the pinned photodiode to the sense node. The voltage drop in the sense node is amplified and sampled at the column level amplifier output. The first (reset) and second (transfer) samples are then differentiated. This CDS process cancels the reset kTC thermal noise and reduces the $1/f$

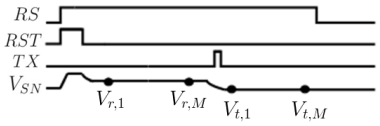

Fig. 2. Timing diagram of aclassical pixel showing the reset and transfer samples used for a correlated mutiple sampling of order M

noise. Moreover, the pinned photodiode is emptied of charges at each transfer showing no frozen noise. Correlated multiple sampling (CMS) is a generalized form of CDS. It combines the CDS with averaging. The CMS consists in the difference between the average of M samples at the reset level and the average of M samples after transferring the charge to the sense node. Fig. 2 shows the timing diagram of a 4T pixel and times of the different samples of the CMS. the voltage at the output of the CMS is given by

$$V_{CMS} = \frac{1}{M}\sum_{i=1}^{M} V_{r,i} - \frac{1}{M}\sum_{i=1}^{M} V_{t,i} \tag{1}$$

In order to evaluate the impact of CMS on thermal noise, we consider, at the input of the CMS stage, a thermal noise voltage source with a PSD N_{th} band-limited at the first order with a cut-off frequency f_c. The corresponding autocorrelation is given by [4]

$$R(\tau) = \pi f_c N_{th} e^{-2\pi f_c|\tau|}. \tag{2}$$

Thus, the correlation between each two different samples of the $2M$ is lower than $R(T_{CMS})$. For enough settling of the signal between the samples $2\pi f_c T_{CMS}$ must be higher than 5. Thus the correlation between two different samples is lower than e^{-5} and can therefore be neglected. Thus, the samples can be considered uncorrelated. Consequently, the variance of the thermal noise voltage at the output of the CMS stage can be derived using (1) as

$$< V_{CMS}^2 >= \frac{2}{M} R(0) = \frac{2}{M}\pi f_c N_{th}. \tag{3}$$

Note that $\pi f_c N_{th}$ is the thermal noise variance at the input of the CMS stage. Thus CMS results in a thermal noise reduction by $\frac{2}{M}$.

The impact of CMS on $1/f$ noise has been discussed in previous works [5] [2], we only recall the result. Consider at the input of the CMS stage a $1/f$ noise voltage source with a PSD of $\frac{N_{1/f}}{f}$ band limited at the first order with a cut-off frequency f_c. The 1/f noise variance at the output of the CMS is calculated numerically and plotted as a function of $2\pi f_c T_{CMS}$ in Fig. 3 together with the normalised thermal noise variance. The $1/f$ noise reduction efficiency increases with the CMS order M and reaches a plateau for M higher than 8, especially when $2\pi f_c T_{CMS}$ is high.

III. Overview of CMS implementations

A. Analog CMS

A CMS of order M can be implemented using a SC amplifier that accumulates M consecutive samples in its feedback capacitor [2]. The drawback of this technique is that accumulation of voltages reduces the dynamic range of the readout chain by a factor of M. An alternative of the analog integration technique is the folding integration technique [2]. It allows performing CMS without reducing the dynamic range at the cost of adding two voltage references, one comparator, and some control logics. This additional circuitry introduces a feedback effect in order to prevent the output of the SC amplifier from saturation.

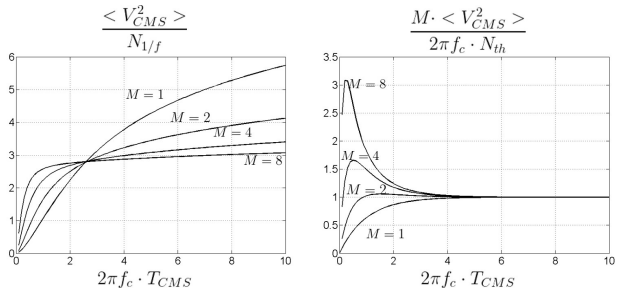

Fig. 3. Impact of CMS on 1/f and thermal noise variance

B. Digital CMS

Another implementation of the CMS is used in [3][6]. It consists in the addition of the first M samples (reset) after analog-to-digital conversion and then subtract consecutively the next M ones (transfer). The main drawback of this technique is the fact that analog-to-digital conversion has to be performed $2M$ times during each readout.

IV. A new CMS implementation

In this Section, an alternative to the CMS implementations reported above is presented. It avoids using additional active circuitry or multiple analog-to-digital conversions. It is based on the passive SC network using an optimal number of capacitors. Consider two capacitors, C_1 and C_2, each one holding respectively voltages V_1 and V_2. When connecting both capacitors, the charges held in C_1 and C_2 are shared

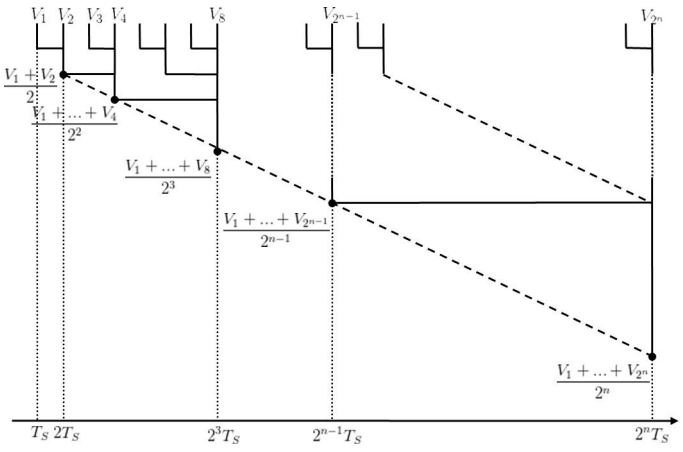

Fig. 4. Illustration of the progressive processing of the average of 2^n consecutive samples with a sampling frequency T_S

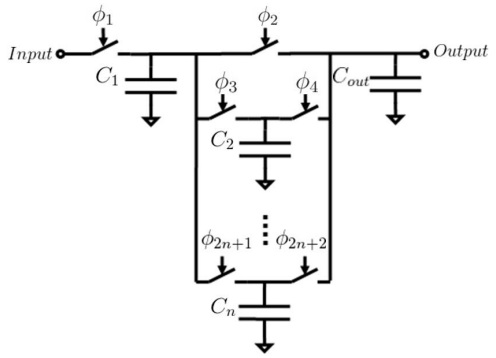

Fig. 5. Passive switched capacitors circuit averaging 2^n samples using n capacitors

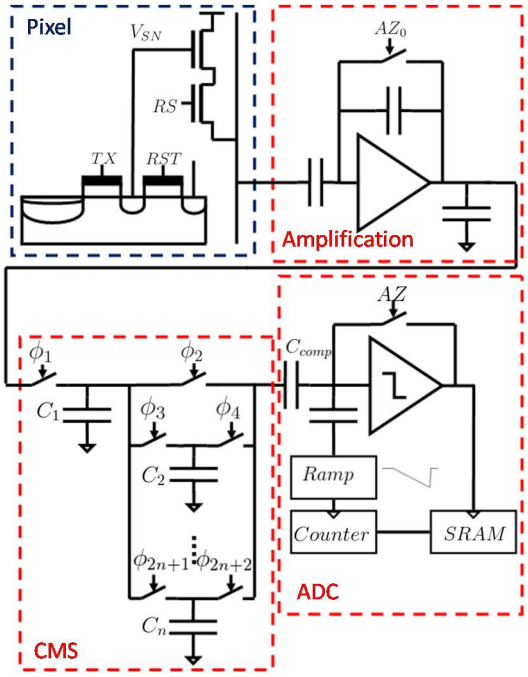

Fig. 6. Implementation of the new circuit performing a 2^n order CMS using n switched capacitors in a classical CIS readout chain

leading to a common voltage V across both capacitors given by

$$V = \frac{C_1V_1 + C_2V_2}{C_1 + C_2} \overset{C_1=C_2}{=} \frac{V_1 + V_2}{2} \tag{4}$$

The simplest way to perform an average of M samples using switched capacitors consists of holding M consecutive samples with a period of sampling T_S in M capacitors and connecting them all, at MT_S, to obtain the average. This process is faster than the state-of-the-art techniques reported in the previous Section at the cost of silicon area occupied by the sampling capacitors. In order to use less capacitors to average the same number of samples, one has to process the average progressively and hold the intermediate results in the capacitors instead of holding the initial samples. Consider the case where $M = 2^n$. One can find that the average of the 2^n consecutive samples can be calculated recursively. In fact

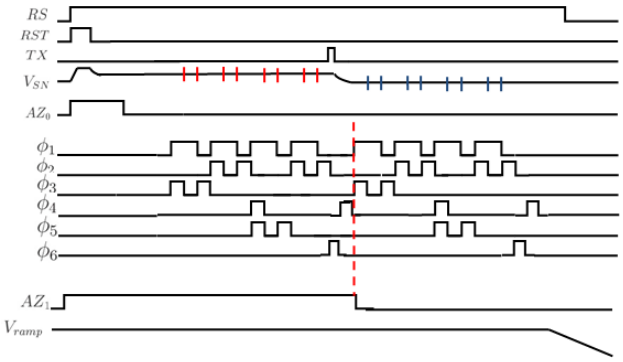

Fig. 7. Timing digram for the CIS readout chain of figure 7 that incompass the new CMS circuit of order 8 ($n = 3$)

the average of 2^n samples is calculated by connecting two capacitors, each one storing the average of 2^{n-1} consecutive samples as

$$\frac{1}{2^n}\sum_{i=1}^{2^n} V_i = \frac{1}{2}\left(\frac{1}{2^{n-1}}\sum_{i=1}^{2^{n-1}} V_i + \frac{1}{2^{n-1}}\sum_{i=2^{n-1}}^{2^n} V_i\right). \tag{5}$$

Fig. 4 illustrates the progressive processing of the samples average over the duration needed to sample and process the total 2^n samples (2^nT_S). Equation (5) and Fig. 4 show that at 2^nT_S, the average of 2^n samples is processed by connecting two capacitors, one storing the average of the first 2^{n-1} samples processed at $2^{n-1}T_S$, and the other one storing the average of the next 2^{n-1} samples. One can notice that the capacitors used to compute the average of the first 2^{n-1} samples are not all needed to hold this value during the processing of the next samples. Only one capacitor is needed to hold the average of the first 2^{n-1} samples and the other capacitors can be reused to process the next samples. Consequently, if one considers U_{n-1}, the number of capacitors needed to calculate the average of 2^{n-1} consecutive samples. The average of 2^n samples can be calculated using $U_{n-1} + 1$. Thus

$$U_n = U_{n-1} + 1. \tag{6}$$

Finally, the number of capacitors needed to calculate the average of 2^n consecutive samples is given by

$$U_n = n + 1. \tag{7}$$

This result is very important because it shows that a CMS of order 2^n can be performed using $n+1$ capacitors instead of 2^n. Therefore, the implementation of CMS using this technique results in CMS layout footprint reduction of order $\frac{2^n}{n}$.
Fig. 5 shows a passive SC circuit implementing this technique. It uses $n + 1$ identical capacitors. Consider the case $n = 2$. First, switches Φ_1 and Φ_2 are closed. Φ_2 is opened to hold a sample V_1 in C_{out}. Then Φ_1 is opened after T_S in order to hold the next sample V_2 in C_1. Φ_1 is closed to calculate the average and opened to hold a voltage $\frac{1}{2}(V_1+V_2)$ in C_{out}. The same process is iterated with capacitors C_1 and C_2 and ends with a voltage $\frac{1}{2}(V_3 + V_4)$ held in capacitor C_2. Finally Φ_4

is closed to connect C_2 and C_{out} and then opened to hold a voltage $\frac{1}{4}(V_1 + V_2 + V_3 + V_4)$ in C_{out}.
Fig. 6 shows the implementation of the averaging circuit presented in Fig. 5 in a classical CIS readout chain to perform CMS of order 2^n. Notice that the input capacitor of the ADC comparator C_{comp} is used as C_{out}. The corresponding timing diagram for the case $n = 3$ is depicted in Fig. 7. the voltage at the input of the comparator corresponds to the difference between the voltage levels before and after opening the auto-zeroing switch (AZ). The same averaging circuit computes the average of 2^n samples during the reset phase and the average is stored in capacitor C_{comp}. Then, the auto-zeroing switch (AZ) is opened and the voltage at the input of the comparator becomes the difference between the average current output and the average calculated at the reset phase. Once the average of the 2^n samples of the transfer phase is calculated, the ramp is activated together with the counter as shown in Fig. 7 for the case $n = 3$. Compared to a classical CIS readout chain, only two additional capacitors are needed with no active circuitry. The logic circuit needed to control the switches is common to all the columns of the imager, thus its footprint is not significant.

V. Transient noise simulation results

In order to validate the new CMS circuit presented in this paper. The CIS readout chain presented in Fig. 6, using the analog averager for the case $n = 3$ to perform a CMS of order 8, is simulated using ELDO transient noise simulation. The line readout time is set to $35\mu s$ for a column amplifier bandwidth of 265 kHz and gain of 8 (in order to minimize the contribution of the ADC comparator to the input referred noise). The design kit used for this simulation is a 180 nm process dedicated to CIS. Simulations of $1/f$ and thermal noise are performed separately. Note that the averaging circuit can perform CMS of orders from 1 (correponding to the simple CDS) up to 8. Fig. 8 shows the input-referred thermal noise as a function of the CMS order M together with a $1/\sqrt{M}$ theoretical decrease expectation curve. This figure shows that, as expected, thermal noise reduction follows a $1/\sqrt{M}$ decrease. Fig. 9 shows the $1/f$ component of the input referred noise for M varying between 1 and 8. It shows that CMS reduces $1/f$ noise by about 30% for a CMS of order 4 and 33% for order 8. Thus for $1/f$ noise using CMS of orders higher than 4 does not bring any significant decrease.

VI. Conclusion

In a CIS readout chain based on a 4T pixel, a CMS of order M reduces thermal noise by $\frac{2}{M}$. CMS is a general case of CDS. Thus it reduces significantly $1/f$ noise and offset. The $1/f$ noise reduction using CMS increases with M and reaches a plateau at $M = 8$. In state-of-the-art CIS readout chains, CMS is performed after analog-to-digital conversion or using analog active circuitry.
In this paper, a new implementation of CMS is introduced. It uses only n additional switched capacitors at the bottom of each column to perform a CMS of order 2^n. The proposed

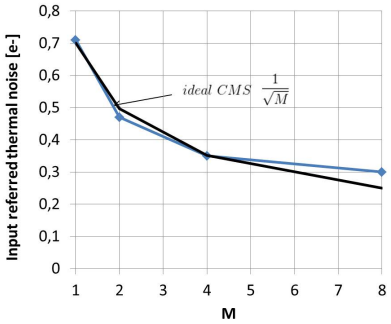

Fig. 8. Simulations of the input-referred thermal noise rms charge of the CIS readout chain presented in Fig. 6 using the proposed CMS circuit

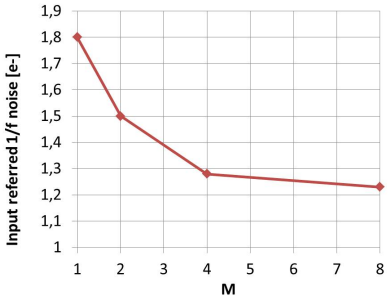

Fig. 9. Simulations of the input-referred $1/f$ noise rms charge of the CIS readout chain presented in Fig. 6 using the proposed CMS circuit

CMS circuit (i) requires no additional active circuitry, (ii) has no impact on the output dynamic range and (iii) does not need multiple analog-to-digital conversions. The new implementation is validated by transient noise simulations for the case of an 8^{th} order CMS. The simulation results confirm the theoretical results. They show that the thermal noise is decreased as expected as $\frac{1}{\sqrt{M}}$, whereas the $1/f$ noise is reduced by 30% for $M = 4$ but no significant additional decrease occurs for M larger than 8.

References

[1] Y. Chen, X. Wang, A. Mierop, and A. Theuwissen, "A cmos image sensor with in-pixel buried-channel source follower and optimized row selector," *Electron Devices, IEEE Transactions on*, vol. 56, no. 11, pp. 2390–2397, 2009.

[2] S. Suh, S. Itoh, S. Aoyama, and S. Kawahito, "Column-parallel correlated multiple sampling circuits for cmos image sensors and their noise reduction effects," *Sensors*, vol. 10, no. 10, pp. 9139–9154, 2010.

[3] Y. Chen, Y. Xu, Y. Chae, A. Mierop, X. Wang, and A. Theuwissen, "A 0.7e rms-temporal-readout-noise cmos image sensor for low-light-level imaging," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, 2012, pp. 384–386.

[4] A. Papoulis and S. U. Pillai, *Probability, random variables, and stochastic processes*. McGRAW-HILL, 2002.

[5] A. Boukhayma, A. Peizerat, A. Dupret, and C. Enz, "Design optimization for low light cmos image sensors readout chain," in *New Circuits and Systems Conference (NEWCAS), 2014 IEEE 12th International*, June 2014, pp. 241–244.

[6] Y. Lim, K. Koh, K. Kim, H. Yang, J. Kim, Y. Jeong, S. Lee, H. Lee, S.-H. Lim, Y. Han, J. Kim, J. Yun, S. Ham, and Y.-T. Lee, "A 1.1e-temporal noise 1/3.2-inch 8mpixel cmos image sensor using pseudo-multiple sampling," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, 2010, pp. 396–397.