A low-voltage CMOS-compatible time-domain photodetector, device & front end electronics

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"What I cannot create, I do not understand. Know how to solve every problem that has been solved."
–Richard Feynman

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Abstract

During the last decades, the usage of silicon photodetectors, both as stand-alone sensor or integrated in arrays, grew tremendously. They are now found in almost any application and any market range, from leisure products to high-end scientific apparatuses, including, among others, industrial, automotive, and medical equipment. The impressive growth in photodetector applications is closely linked to the development of CMOS technology, which now offers inexpensive and efficient analog and digital signal processing capabilities. Detectors are often integrated with their respective front end and application-specific digital circuit on the same silicon die, forming complete systems on chip. In some cases the detector itself is not on the same chip but often part of the same package.

However, this trend of co-integration of analog front end and digital circuits complicates the design of the analog part. The ever-decreasing supply voltage and the smaller transistors in advanced processes (which are driven by the development of digital circuits) negatively impact the performance of the analog structures and complicates their design. For photodetector systems, the effect most importantly translates into a degradation of dynamic range and signal-to-noise ratio.

One way to circumvent the problem of low supply voltages is to shift the operation from voltage domain to time domain. By doing so, the signal is no longer constrained by the supply rails and analog amplification is avoided. The signal takes the form of a time-based modulation, such as pulse-width modulation or pulse-frequency modulation. Another advantage is that the output signal of a time-domain photodetection system is directly interfaceable with digital circuits.

In this work, a new type of CMOS-compatible photodetector displaying intrinsic light-to-time conversion is proposed. Its physical structure consists of a MOS gate interleaved with a PN junction. The MOS structure is acting as a photogate. The depletion region shrinks when photogenerated carriers fill the potential well. At some point, the anode of the PN structure is de-isolated from the rest of the detector and triggers a positive-feedback effect that leads to a very steep current increase through the PN-junction. This translates into a signal of very high amplitude and independent from light-intensity, which can be almost directly interfaced with digital circuits. This simplifies the front end circuit compared to photodiode-based systems.

The physical behavior of the device is analyzed with the help of TCAD simulations and simple behavioral and shot-noise models are proposed. The device has been co-integrated with its driver and front end circuit in a standard CMOS process and its characteristics have been measured with a custom-made measurement system. The effect of bias parameters on the performance of the sensor are also analyzed. The limitations of the device are discussed, the most important ones being dark current and linearity. Technological solutions, such as the implementation of the detector on Silicon-on-Insulator technology, are proposed to overcome the limitations.

Finally, some application demonstrators have been realized. Other applications that could benefit from the detector are suggested, such as digital applications taking advantage of the latching behavior of the device, and a Photoplethysmography (PPG) system that uses a PLL-based control loop to minimize the emitting LED-current.

Keywords

Silicon Photodetectors, Sensor Front ends, CMOS integrated circuits, Pulse Modulation, Silicon-on-insulator

Résumé

Au cours des dernières décennies, l'utilisation des photodétecteurs, que ce soit comme composant individuel ou intégré en matrice, s'est considérablement développé. On les retrouve désormais dans toutes les gammes d'applications et dans tous les marchés, allant des produits destinés aux loisirs, jusqu'aux appareils scientifiques haut de gamme, en passant par l'équipement industriel, automobile, et médical. L'impressionnant élargissement des domaines applications des photodétecteurs est étroitement lié au développement de la technologie CMOS, qui offre aujourd'hui des possibilités de traitement de signal analogique et numérique efficaces et à bas prix. Les détecteurs sont souvent intégrés avec leurs circuits de front end respectifs et les circuits numériques propres à leur application sur la même puce de silicium.

Cependant, cette tendance à la co-intégration du front end analogique et des circuits digitaux complique la conception de la partie analogique du système. La diminution continue des tensions d'alimentation ainsi que de la taille des transistors dans les technologies avancées (poussées par le développement des circuits numériques) réduit sur les performances des structures analogiques et complique leur conception. Pour les systèmes de photodétecteurs, l'effet se traduit principalement par une diminution de la plage dynamique et du rapport signal sur bruit.

Un moyen de d'affranchir du désavantage introduit par les tensions d'alimentation réduits est de convertir le fonctionnement du domaine des tensions au domaine temporel. Il n'est ainsi plus contraint par les rails d'alimentations et l'amplification analogique n'est plus nécessaire. Le signal prend alors la forme d'une modulation temporelle, telle que la modulation de largeur d'impulsions (PWM), ou la modulation de fréquence d'impulsions (PFM). Un second avantage réside dans le fait que le signal de sortie d'un système de photodétection dans le domaine temporel est directement interfaçable avec des circuits numériques.

Dans ce travail, un nouveau type de photodétecteur compatible CMOS effectuant intrinsèquement une conversion lumière-temps est proposé. Sa structure physique consiste en une grille MOS entrelacée avec une jonction PN. La structure MOS joue le rôle de « photogate ». La zone de déplétion se réduit quand les porteurs photogénérés remplissent le puit de potentiel. À un certain point, l'anode de la jonction PN n'est plus isolée du reste du détecteur et initie un effet de réaction positive conduisant à une augmentation subite du courant à travers la jonction PN. Ce phénomène se traduit par un signal de très forte amplitude et indépendant de l'intensité lumineuse, pouvant être presque directement interfacé avec des circuits numériques. Cela simplifie la conception du circuit de front end en comparaison des systèmes conventionnels basés sur des photodiodes.

Le comportement physique du composant est analysé à l'aide de simulations TCAD. Des modèles simples décrivant son comportement ainsi que le bruit quantique sont proposés. Le composant a été intégré avec son circuit de détection dans une technologie CMOS standard et ses caractéristiques ont été mesurées avec un système de mesure dédié. Les effets des paramètres de polarisation sur les performances du capteur sont analysés et les limitations du composant sont discutées, les plus importantes concernant le courant d'obscurité ainsi que la linéarité. De nouvelles solutions, comme l'implémentation du détecteur sur des procédés de silicium-sur-isolant (SOI), sont proposées afin d'outrepasser ses limitations.

Finalement, des démonstrateurs d'applications ont été conçus et fabriqués. D'autres applications qui pourraient bénéficier des caractéristiques spécifiques au détecteur proposé sont suggérées, telles que des applications numériques tirant parti du comportement en « verrou » du capteur, ainsi qu'un système de photopléthysmographie (PPG) utilisant une boucle de contrôle basée sur une boucle à verrouillage de phase (PLL) pour minimiser le courant de la LED émettrice.

Mots-clés

Photodétecteurs sur silicium, front ends de capteurs, circuits intégrés CMOS, modulation d'impulsions, silicium-sur-isolant (SOI)

Contents

List of Figures

List of Tables

Chapter 1 Introduction

Photodetectors are nowadays ubiquitous. During the past decades, their range of applications have experienced a massive growth, both as stand-alone sensors or integrated into arrays for 2D and 3D imaging. They are now present in virtually any market, ranging from toys and leisure appliances to high-end scientific equipment and including, among others, industrial, automotive, and health-monitoring applications. This tremendous development has been driven by the relentless progress and cost reduction in CMOS technologies, allowing for higher integration and more and more sophisticated digital signal processing as well as, very often, co-integration of sensors and CMOS circuits.

Development of CMOS technologies and their versatility has permitted to meet the specific requirements in terms of cost, power consumption, and performance of the detection system on both ends of the range of applications. For example, compact proximity sensors are present in every smartphone. CMOS imagers, thanks to co-integration of detectors and circuits and therefore smaller costs, have supplanted CCDs in almost every application, including high-end photography.

Exotic technologies are nowadays limited to telecommunications (for wavelength reasons: low-bandgap semiconductors, for speed reasons: avalanche photodiodes), extreme sensitivity requirements (single photon avalanche photodiode (SPAD), photomultiplier), or extremely low noise and low dark current applications (low-temperature CCD imagers).

The impressive development of digital CMOS circuits in terms of feature size and power consumption unfortunately comes with a price. The decrease in supply voltage and size of the transistors, with the related parasitic effects, have made analog design more challenging over the years. In the domain of photodetection, lower supply voltages translate into degraded dynamic range and non-ideal transistors make the design of amplifiers and analog-to-digital converters (ADC) more difficult, leading to degraded noise and linearity characteristics.

One way to avoid the performance limitations due to very low supply voltage, analog amplification, and digital conversion is to shift the signal from voltage or current domain to time domain. In such a system, photogenerated carriers are accumulated in a capacitance. Depending on the chosen modulation method, the information might be encoded in frequency, duty-cycle, or pulse density and is therefore unconstrained by supply voltage.

In this thesis, a new type of CMOS-compatible photodetector is presented. Its particularity is to feature in-device charge integration and comparison, and a current output whose magnitude is independent of light intensity. These properties make it an ideal candidate for time-based detection systems. The device-level charge accumulation and comparison avoids the use of a comparator, and the high magnitude output makes it easy to interface with CMOS logic circuits. The switching behavior of the device makes its operation comparable to the operation of a SPAD, and from which the design of the driver and readout circuit is inspired.

This work is organized as follows. The rest of this chapter introduces the physical concepts behind photodetection, and defines some important parameters. It also reviews the existing types of semiconductor-based photodetectors and their operation. In chapter 2 the structure and the operation of the new photodetector, called the Hybrid MOS-PN device, are presented. Physical behavior is explained and confirmed with TCAD simulations, and parameters are derived. In Chapter 3 the design of the co-integrated front end circuit and the measurement system is detailed. It also presents measurement results and analyzes the effects of bias voltages of the device parameters. In Chapter 4 potential technological solutions that could improve the performances and modify the behavior of the device are explored. In chapter 5, some application demonstrators are presented as well as potential applications taking advantage of the detector properties. A summary of achieved results and the next research steps are discussed in chapter 6.

1.1 Photodetection

Photodetection describes the general process of detecting incident light into a so called *photodetector*. To do so, almost every photodetector uses the quantum physical effect of ionization by absorption of a photon (*photoionization*). This phenomenon is also known as the photoelectric effect. It was first observed by Heinrich Rudolf Hertz in 1887 and explained by Albert Einstein in 1905 [1], who introduced the hypothesis that electromagnetic energy is only emitted or absorbed in discrete packets (*Energiequanten*) that are nowadays called photons. For his work on the photoelectric effect, Einstein was awarded the Nobel Prize for physics in 1921.

Historically, the photoelectric effect referred to the emission of electrons from a metal when bombarded with photons of sufficient energy. However, in semiconductor-based photodetectors, the energy from the absorption of a photon is used to transfer an electron from the valence band to the conduction band, creating an electron-hole pair resulting in a voltage buildup on the electrodes. In order to be able to so, the energy of the absorbed photon ($E_{phot} = h\nu = \frac{hc}{\lambda}$) must be higher than the band gap of the semiconductor material.

For silicon, the bandgap energy at 300K is approximately 1.1eV, corresponding to an equivalent wavelength of 1.11µm. This is an important physical parameter which restricts the useful range of any silicon-based photodetector to the near-infrared region and above, excluding the long range mono-mode fiber-optics telecommunication range at 1.3 and 1.5µm.

Some photodetectors, mainly photomultipliers, Avalanche Photodiodes (APD), and phototransistors display internal gain. The physical principles involved vary between different types of devices. For APD and photomultipliers, gain appears when a free electron created from the absorption of a photon gains sufficient energy to create other free carriers which in their turn will create more free carriers.

In photomultipliers, the free electron is accelerated in an electric field and hits a plate called a *dynode*. In the so-called process of *secondary emission*, new electrons are emitted and accelerated to the next dynode and so on and so forth, until they reach the anode.

In Avalanche photodiodes, this happens in the material with a process called *impact ionization* leading to the famous *avalanche multiplication*.

In phototransistors, gain is created by the *transistor effect*. In this case, photons are absorbed in a region corresponding to the base of a bipolar transistor. The local variation of potential modulates the current flowing through the collector, like a “normal” transistor.

1.2 Important physical parameters

1.2.1 Quantum Efficiency and Responsivity

Quantum Efficiency (QE) is roughly defined as the ratio between the number of photo-generated carrier over the number of available photons [2]. More precisely, Quantum Efficiency can be defined in two ways. First, Internal Quantum Efficiency (QE_{int}) is defined as the number of photo-generated carriers over the number of absorbed photons. In practice and for silicon, this ratio is very close to one.

$$QE_{int} = \frac{Nb\ of\ photogenerated\ carriers}{Nb\ of\ absorbed\ photons}$$

Second, External Quantum Efficiency (QE_{ext}) is defined as the number of collected photo-generated carriers over the number of incident photons on the detector.

$$QE_{ext} = \frac{Nb\ of\ collected\ carriers}{Nb\ of\ incident\ photons}$$

The latter definition is the one that is useful in practice. QE_{ext} is in general smaller than QE_{int}, but can be >1 in the case of photodetectors that display gain. Several factors can participate in the decrease of QE_{ext} of a detector, such as reflection at the surface due to the refractive index difference, thin-film interference in the cover layers, photon absorption in the cover layers, recombination or trapping of the photo-generated carriers at interface between oxide and semiconductor, absorption deep in the semi-conductor or non-absorption.

Responsivity describes the electro-optical transfer characteristic of the detector. It is defined as the ratio between the photogenerated current and the received power.

$$R = \frac{I_0}{P_r}\ [A/W]$$

Since one photon can only generate one free carrier (for visible light), and since the energy of a photon is inversely proportional to its wavelength ($E_{phot} = \frac{hc}{\lambda}$), the number of photons absorbed per second for a given incident power is directly proportional to the wavelength, and so is the responsivity. In the ideal case, where every incident photon generate one carrier, the ideal responsivity is given by

$$R_{ideal} = \frac{q}{hc}\lambda = 0.807\lambda_{\mu m}\ [A/W]$$

The ratio between the actual responsivity and the ideal responsivity is defined by the external *quantum efficiency* (QE_{ext}) of the device.

$$QE_{ext}(\lambda) = \frac{R(\lambda)}{R_{ideal}(\lambda)}$$

Consequently, responsivity and external quantum efficiency are two equivalent ways of describing the efficiency of a photodetector. They are linked by the following relation.

$$R(\lambda) = \frac{q}{E_{phot}}QE_{ext}(\lambda) = \frac{q \cdot \lambda}{hc}QE_{ext}(\lambda)$$

1.2.2 Photon Absorption depth

Photons propagating in the semiconductor ϕ(x) are absorbed exponentially according to Beer-Lambert law and depending on the absorption coefficient α(λ) and travelled distance x.

$$\phi(x) = \phi_0 \cdot \exp(-\alpha(\lambda) \cdot x)\ [cm^{-2} \cdot s^{-1}]$$

In silicon, the absorption coefficient α(λ) strongly depends on the wavelength λ (Fig. 1-1). The longer the wavelength, the smaller the absorption coefficient, and the longer the distance travelled by photons before being absorbed. As stated in the previous sub-section, this effect can introduce a drop in QE_{ext} if photons are absorbed too deeply in the silicon layer and don't have time to travel back (usually, by diffusion) to the depletion layer of the detector to be collected before recombination. It was also stated that QE_{ext} drops when photons are absorbed in the cover layers. One of them is polysilicon used in MOS gates and that features the same absorption coefficient as silicon. Fig. 1-1 shows that for short wavelengths (below 500nm), the material starts to be very absorptive and, as a consequence, can deteriorates the quantum efficiency of the detector if present on the photon path.

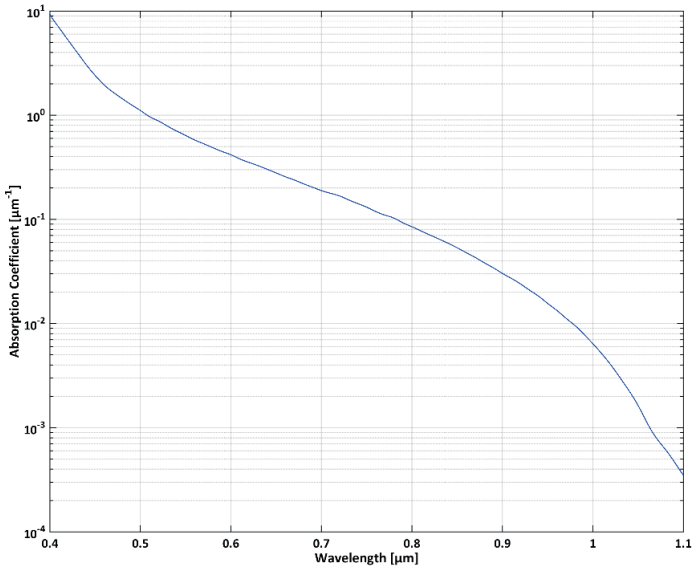

Fig. 1-1: Silicon absorption coefficient versus wavelength

From the derivative of the photon flux ($d\varphi(x)/\,dx$), the photo-generation rate G(x) can be defined. It expresses the number of generated photo-carriers per volume and per time unit.

$$G(x) = -\frac{d\phi(x)}{dx} = \phi_0 \cdot \alpha(\lambda) \cdot \exp(-\alpha(\lambda) \cdot x)\ [cm^{-3} \cdot s^{-1}]$$

1.2.3 Poissonian Noise

The electromagnetic energy is quantized and forms photons. Each photon forming the incident light on a detector is statistically independent from any other and arrives stochastically. As a consequence, the number of incident photons in a given time follows a Poisson distribution, with the property that the variance of a Poisson random variable is equal to its mean [3]. This is the Photon Noise, also called shot noise, or Poissonian noise.

$$\sigma_{photon} = \sqrt{N_{photon}}$$

The signal to noise ratio of incident light for a given time interval can be defined as the ratio between the mean number of incident photons over its standard deviation (σ_{photon}).

$$SNR_{photon} = \frac{N_{photon}}{\sigma_{photon}} = \sqrt{N_{photon}}$$

Each incident photon has a QE_{ext} probability to be converted into a collected photo-generated carrier. Each collection is statistically independent. The binomial selection theorem states that the binomial selection of a Poisson random variable is a Poisson random variable and that the mean of the output of the selection process is the mean of the input times the probability of selection.

$$N_{collected} = QE_{ext} \cdot N_{photon}$$

$$SNR_{collected} = \sqrt{QE_{ext} \cdot N_{photon}}$$

This signal to noise ratio is a physical limit rooted in the stochastic process of photon arrival. Consequently, the ways to increase this signal to noise ratio at the output of a detector for a given light intensity are, to have QE_{ext} as close as possible to 1, to increase the active area of the detector, or to increase the detection time (averaging).

In practice, SNR can be degraded by dark current, as well as circuit-related noise such as Johnson noise, flicker noise, reset noise, etc. Those external noise sources can be minimized by careful circuit design or, depending on the system, techniques such as correlated double sampling. Section 2.1.7 discusses SNR in more details.

1.3 Types of photodetectors

In this section, a non-exhaustive list of semiconductor-based photodetectors that are relevant to our research is presented. They are summarized in Table 1-1.

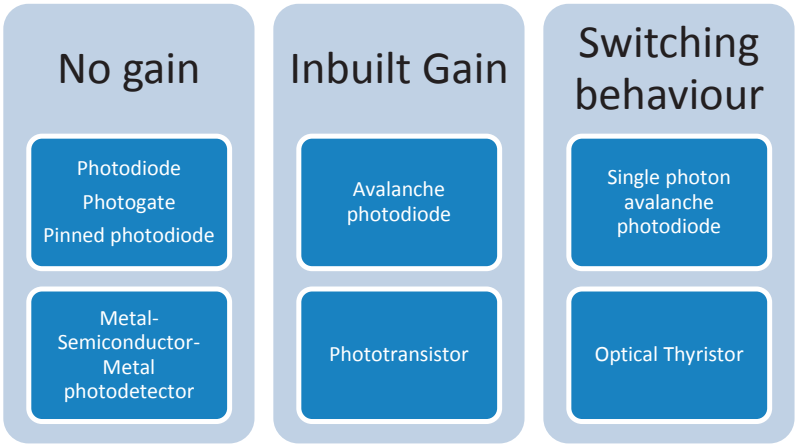

Table 1-1: Classification of some photodetectors

1.3.1 P-N and P-I-N photodiode

This is the simplest kind of semiconductor based photodetector and probably the most used. The applications range from power solar panels to low noise photodetectors, and including telecom applications [4, 5].

For efficient detection, photons must be absorbed in the depletion region of the PN junction, where the electric field is high. Free carriers created this way are accelerated and form a drift current that is quickly collected at the electrodes. Carriers generated outside the depletion region form a diffusion current component and are way slower and have a high chance of recombination. Slow carriers impair the linearity and speed of photodiode-based detectors, and several techniques exist to suppress their effect [6].

Adding an intrinsic region to the PN junction has two advantages. By increasing the depletion region, the junction capacitance is reduced, leading to smaller RC delays and faster operation of the detector. The increased depletion region also improves quantum efficiency by increasing the number of "useful" carriers generated in the high field region. Hence, P-I-N photodiodes are superior to P-N ones.

PIN photodiodes are widely used because of their simplicity of structure, CMOS-compatibility, higher linearity, higher quantum efficiency and lower cost compared to other photodetectors with gain.

1.3.2 Photogate and pinned photodiode

The photogate is the principal component of charge coupled device (CCD) sensors and some CMOS image sensors (CIS). Basically, it is a MOS structure, with usually a polysilicon gate and a SiO_2 oxide. Applying a voltage on the gate creates a depletion region and a potential well in the substrate, in which photocharges are accumulated. Charges are then transferred directly to a floating diffusion and converted into voltage at pixel level (CIS), or transferred from gate to gate to a single floating diffusion and amplifier (CCD).

In CIS, having the sensing node and the read-out node separated allows the implementation of correlated double sampling (CDS), a technique that reduces fixed pattern noise (FPN) across the sensor by cancelling reset noise and mismatch from one pixel to another.

However, photogate sensors suffer from two main drawbacks. First, the interface between silicon and the oxide presents traps that lead to carrier recombination, decreasing quantum efficiency and increasing noise. Second, light absorption in the polysilicon of the gate stack at short wavelengths degrades the blue response of the detector in the case of front-side illumination [7].

The pinned photodiode (PPD) solve those problems [8]. In that case, the potential well is not created by a gate but with the doping profile. In consists of a sandwich between an n+ diffusion on a p substrate, and a very shallow p+ diffusion on top of the n+ one. The n+ diffusion creates a potential well below the surface of the semiconductor. The read-out is performed the same way as with photogate sensors. Special care must be given to the doping profiles between the PPD, the transfer gate and the floating diffusion in order to ensure a complete charge transfer. Pinned photodiodes are nowadays present in the majority of CMOS image sensors [9].

1.3.3 Metal-Semiconductor-Metal photodetector

Another kind of widespread photodetector is the Metal-Semiconductor-Metal (MSM) detector [4]. That device is constituted of two back-to-back connected Schottky barriers. When applying a voltage between the electrodes, the electric field creates a depletion area in the substrate where photogenerated carriers car drift to the electrodes, thus generating a photocurrent.

The MSM photodetector has the advantage of being compatible with standard CMOS processes. Another advantage is the smaller capacitance compared to an equivalent P-I-N photodiode, enabling high-frequency applications, such as fiber-optics communication. The drawback is that dark current levels are higher than for an equivalent photodiode.

1.3.4 Avalanche Photodiode (APD)

An avalanche photodiode has a similar structure to a P-N or P-I-N photodiode. It is reverse biased under very high voltage to take advantage of impact ionization and avalanche multiplication. This in-built gain is extremely useful for high-sensitivity and high-speed applications. Using the intrinsic gain of the detector, the gain requirements of the front end electronics can be relaxed and consequently a higher bandwidth is achievable [10].

One of the principal drawbacks of APDs is the relatively large noise generated in the avalanche multiplication, which is a random process [11]. The noise comes from the fact that each generated carrier doesn't generate a deterministic number of other carriers.

The response time of an APD depends of the avalanche buildup. This response time increases linearly with gain and the gain-bandwidth product (GPW) remains constant, and can reach up to 400GHz [12].

Although some APD can reach bias voltages of several hundreds of volts and are built in specific technologies, CMOS compatible APD in proportional mode with relatively low bias (~10V) have been reported. Epitaxial growth of Germanium allows it to operate in the 1.5µm telecommunication range [13].

1.3.5 Phototransistor

The structure of a standard phototransistor is more or less similar to the one of a bipolar transistor, but the base is floating [14]. Holes created by incident photons in the depletion region separating base and collector flow to the energy maximum and are trapped in the base and raise its potential, allowing a large number of electrons to flow from the emitter and to be collected by the collector (Fig. 1-2).

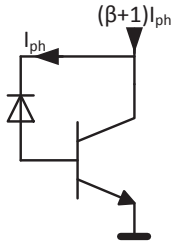

Fig. 1-2: Model of the NPN phototransistor

Advantages of phototransistors are the low cost, compatibility with bipolar technology, and high gain. However, the gain of a photo-transistor is not constant with light intensity and its speed is limited by the RC constants of the transistor and cannot reach the one of an APD.

Moreover, bipolar phototransistors are not suitable for low light applications. At low light intensity, their current gain (β) collapses because of carrier recombination in the base.

MOSFET type photodetectors with high gain have been proposed, using either a floating gate [15], or a photodiode-effect in the bulk [16]. SOI-based MOSFET-type detectors based on body -charge have also been proposed [17].

1.3.6 Single Photon Avalanche Photodiode

A Single Photon Avalanche Photodiode (SPAD), or Geiger mode avalanche photodiode, is a type of APD biased above its breakdown voltage. In this mode of operation, the device cannot extract the avalanche generated carriers at a sufficient rate, leading to a rapid switching of the device into a conductive state. A single photon can trigger the switching, making this device useful for very low intensity applications in offering an alternative to photomultiplier tubes [18].

An important parameter of a SPAD is the dark count rate (DCR), which is the rate (frequency) of “false” detections triggered by thermally excited carriers. DCR depends on the Excess Bias Voltage and, of course, on temperature. This value is in the order of several tens of kilohertz.

Photon Detection Probability (PDP) corresponds to the ratio between detected photons and incident photons.

The timing resolution of a SPAD can be assessed defining its full-width at half-maximum (FWHM) resolution. It describes the time range in which half of the photon detections have occurred (The smaller, the better). A good time domain resolution is important for applications such as time-of-flight measurement. The very high time resolution of SPADs makes them useful for applications requiring extremely fast detection of a weak signal, such as time-of-flight 3d cameras [19-23], but also fluorescence measurement [24] and optical communication [25].

CMOS compatible SPAD have been proposed [26-29]. They can feature a relatively low breakdown voltage (10V), a DCR of 100 kHz, a PDP of 41% and a FWHM of 144ps [30].

1.3.7 Optically controlled thyristor

The optically controlled thyristor is a type of semiconductor switch that is triggered between its OFF and ON state by incoming light.

The structure of this device is the one of the standard thyristor [31]. This P-N-P-N structure can be understood as two cross-coupled transistors (Fig. 1-3).

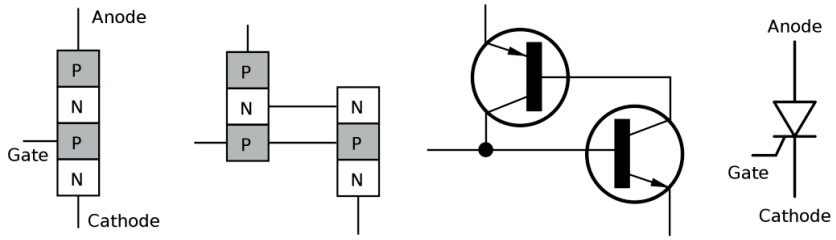

Fig. 1-3: Structure of the Thyristor [32]

In forward bias, the application of a pulse on the second P diffusion can be seen as turning the NPN transistor on, which then turns on the PNP transistor. The device will then remain in its conductive state as long as the current is above a certain threshold. Hence, the thyristor is a semi-controlled switch (Fig. 1-4). Conceptually, in the case of the optically controlled Thyristor, the gate isn't controlled by an externally applied current pulse, but by the photogenerated current.

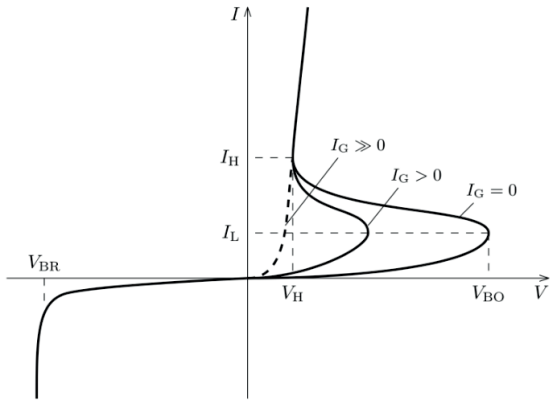

Fig. 1-4: I-V characteristics of the standard Thyristor [32]

The *optical thyristor* is not a widespread device in the field of Photodetection. It is a more commonly used device in the field of power electronics. The goal here is to provide galvanic isolation between the control system and the power component.

Nevertheless, thyristor-like photodetectors have been proposed in the past. One of them, [33] is based on the metal-insulator-semiconductor thyristor (m.i.s.t) which is basically a tunnel-diode in series with a PN junction.

One other, for which differential detection circuits have been developed [34], is based on a thyristor-like structure (P-N-P-N) in exotic semiconductor materials.

It will be shown in chapter 2 that the device of interest can be viewed as field-induced optical thyristor.

1.4 Front End Circuits

This section presents some detection circuits that are of interest for this research. Mainly, it compares the respective circuits of the two big families of detectors: the linear ones, converting light intensity into current or voltage, and the switching ones, converting light intensity into switching time.

1.4.1 Trans-Impedance Amplification

The standard concept of interfacing circuits for photodiodes and avalanche photodiodes are current-to-voltage converters, also called transimpedance amplifier (Fig. 1-5). Usually, those are implemented with operational amplifiers (Op Amp). This detection method allows for very linear and/or very fast circuits [35] and the analog processing of complex modulations of the signal , but at the price of a relatively large [36, 37] silicon area and power consumption. Moreover, the design of such circuits becomes more and more difficult with the diminution in supply voltage, with adverse effects on noise performance and dynamic range.

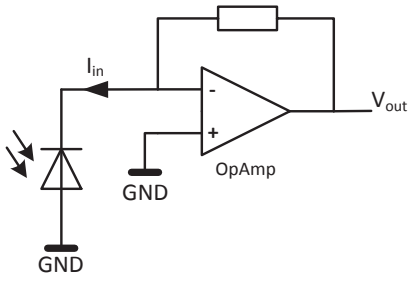

Fig. 1-5: Basic transimpedance amplifier

1.4.2 Source-follower voltage conversion

When used in a CMOS image sensor, photocharges are simply transformed into Voltage on the gate capacitance of a source follower readout transistor [38]. Here again, SNR and dynamic range are limited by the supply voltage.

The simplest form of pixel circuit in shown in Fig. 1-6. It consists of only three transistors, a row selection switch, a source follower, and a reset transistor (3T-pixel). A voltage amplifier and an ADC are found at the end of each column. It is interesting to note that the reset transistor is an NMOS. There are two main reasons for using an NMOS transistor. First, using a PMOS would increase the pixel size and decrease the fill factor, since an N-well would have to be placed in each pixel, with the associated separation constraints between N and PMOS transistors. Second, the NMOS transistor stays in saturation for almost all the reset sequence (soft reset), which divides the voltage noise by a factor $\sqrt{2}$ with respect to the same operation with a PMOS transistor in triode region, that would perform a so called "hard reset" [39]. The disadvantage of soft reset is that it introduces image lag (reset value is dependent on the previous detection) [40, 41]. Several techniques can be used to alleviate the lag. In general, they consist in performing first a hard reset to reduce the lag, and then a soft reset to ensure low noise [42].

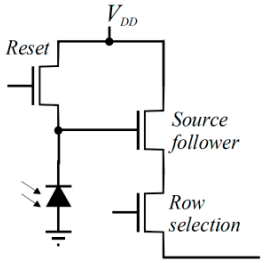

Fig. 1-6: Three transistors (3T) pixel [43]

For low light intensities, the 3T pixel noise is dominated by circuit noise, especially reset noise, but also flicker noise and read noise. A very efficient technique that can be used to cancel reset noise and flicker noise is correlated double sampling (CDS). This is used extensively in CCD sensors but cannot be used with the simple 3T pixel sensor, because the read-out diffusion needs to be separated from the detection node.

CDS is however made possible with the introduction of photogate-based or pinned-photodiode-based pixels (4T pixels). Fig. 1-7 shows that the pinned photodiode is separated from the read-out floating diffusion by the so called transfer gate. This setup can be seen as an "in-pixel CCD".

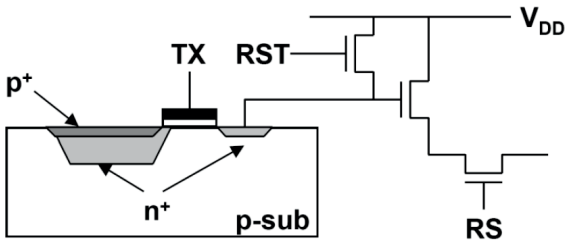

Fig. 1-7: Pinned photodiode (4T) pixel [43]

In CDS, the voltage of the read-out diffusion is sampled just after reset, and once again after the photocharges from the pinned photodiode (or photogate), the difference between those two samples is then taken, effectively cancelling reset noise, and offset fixed pattern noise (FPN), flicker noise (because both samples are taken a very short time apart), at the expense of doubling read noise. Typical dynamic range of imagers with CDS is of about 80dB.

More complicated schemes including averaging, such as correlated multiple sampling (CMS) can effectively reduce read-noise and are useful for very low light applications. SNRs approaching the shot noise limit with only 1.12 dB loss were reported on systems implementing CMS [44].

Techniques to furthermore improve dynamic range exist [45], such as output signal compression, for example in linear-logarithmic sensors [46]. Dynamic ranges of 10 decades are even reported for sensors with complex read-out systems [47].

The performance of sensors with complex noise-reduction and read-out techniques is now good enough to compete with CCDs on high end applications [48] such as, for example, to implement bioluminescence labs-on-chips [44], but also applications requiring extreme temporal precision and sensitivity such as time-of-flight measurement [49], or fluorescence measurement [50, 51].

1.4.3 SPAD driver

In the case of single photon avalanche photodiodes, the detection circuit provides a so called *quench and reset* operation.

That kind of circuits is of particular interest for this research because the proposed photodetector also needs a reset action directly after sensing.

When detection occurs, the current in the SPAD increases very rapidly and must be stopped (quenched) as soon as possible to avoid self-destruction of the device. The SPAD must then be reset (or recharged) to its nominal bias voltage to allow the next detection.

The simplest quenching circuit is the passive one (Fig. 1-8). When avalanche occurs, the rapid increase in current is translated into a voltage on the resistor. Consequently, with a sufficiently large resistor, the voltage on the SPAD decreases below the breakdown voltage and the avalanche stops. The device then resets itself to its nominal voltage with a RC time constant depending on the quenching resistor and the SPAD capacitance.

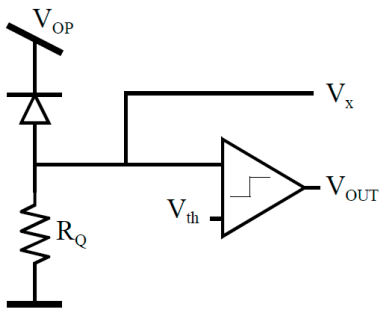

Fig. 1-8: Passive quenching circuit [13]

This time constant, along with along with the after pulses phenomenon, which are subsequent avalanches occurring during the recovery paralyzing the device, constitute fundamental limitations of passive quenching circuits.

In order to overcome those limitations, Active quenching circuits have been developed. When an avalanche is detected, it is actively stopped (e.g. by switching the device supply). Then, after a dead time (generated e.g. by a multivibrator or a ring oscillator (Fig. 1-9)) the device is reset by reapplying the nominal bias voltage.

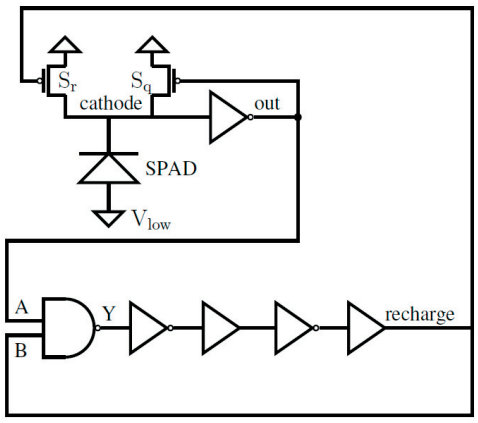

Fig. 1-9: Ring oscillator-based SPAD circuit [52]

Since the dead time is constant, well defined, and smaller compared to passive circuits, those active circuits show higher detector response linearity.

There are also Hybrid systems, using passive quenching and active recharge [53], or active quenching and passive recharge [18].

1.4.4 Time-domain photodetection

It was shown previously that SNR and dynamic range of CMOS image sensors are limited by voltage headroom and the characteristics of the source follower transistor. Techniques improving the dynamic range often include a non-linear response.

Dynamic range can be greatly improved by shifting the signal from voltage to time domain [54]. To do so, photocharges are integrated on the capacitance of the detection node and its voltage compared with a reference voltage by a comparator. The integration time between the end of the reset sequence and the switching of the comparator is measured. The generic name of this technique is Pulse Modulation (PM) detection (Fig. 1-10).

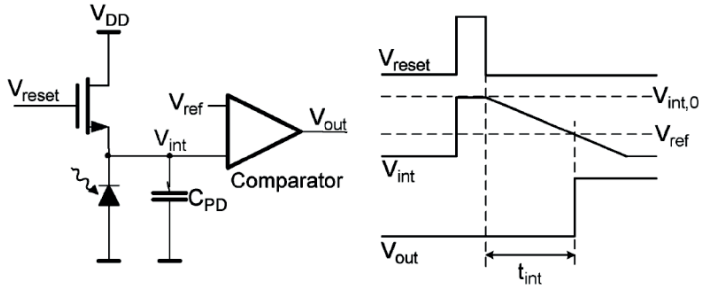

Fig. 1-10: General principle of pulse modulation (PM) photodetection [54]

There are basically two categories of PM systems, Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM).

In PWM, the information about light intensity is carried in the time between reset and the switching of the comparator. There is an inversely proportional (1/x) relation between integration time and light intensity. The higher the intensity, the shorter the integration time. The dynamic range of such a system is defined by the measurable integration time range.

In PFM, the information about light intensity is carried in the frequency of the reset pulses, which is a linear function of light intensity. Here, dynamic range of the system is mainly constrained by the resolution of the counter, but also by the duration of the reset pulse and the quality of the reset-circuit [55]. PFM can be understood as a sequence of PWM measurements. As a consequence, noise is decreased by the averaging effect over multiple measurements. In PM systems, performance and power consumption are largely determined by the design of the comparator. OTA-based comparators usually offer the best matching [56], thus reducing FPN at the price of static power-consumption.

Fig. 1-11 presents the information encoding in PWM and PFM. More detail about their respective characteristics are given in chapter 2.

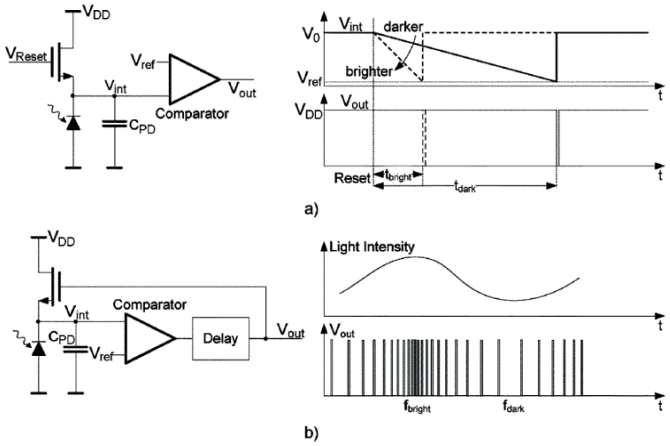

Fig. 1-11: Principle of a a) PWM pixel, b) PFM pixel [57]

Both detection schemes, PFM and PWM, can be used in high dynamic range imagers, with different combination of reset and read-out strategies depending on the chosen modulation and targeted application. However, the different types of sensors can be roughly classified in two big categories. First, the Digital Pixel Sensors (DPS) [58-61] in which each pixel features its own memory and the read-out is performed for the whole frame at once after the detection. Second, the Address Event Representation (AER) [57, 62, 63] in which each pixel sends a signal when integration is completed. The timing information corresponding to each pixel is then written in a central memory. The big limitation of DPS sensors is that each pixel has its own memory, with very negative consequences on pixel-size and fill factor, which also limits the size of the memory. AER-based sensors don't have this problem, but their design complexity is shifted to the handshake circuit and/or bus-arbitration system that must be able to handle the asynchronous behavior of the pixels. Pixel collision is an important problem of such systems, especially for featureless or uniformly illuminated scenes, where every pixel tends to finish integration at the same time. This introduces imprecisions in timing measurement and, hence, noise. Imagers with a dynamic range of more than 140dB were reported [57, 64].

As previously stated, PM sensors suffer from FPN due to comparator mismatch, as well as reset noise, and coupled digital noise. In order to alleviate noise coupling, isolation techniques are used during the layout, as well as coding techniques, such as Grey encoding [58]. PM systems implementing CDS [57] in order to cancel FPM and reset noise were reported.

It is worth noting that stand-alone PFM detectors, also called Light-to-Frequency converters, are very practical to be directly interfaced with microcontrollers due to their digital output. Such sensor systems are inexpensive, compact, and widely available as commercial products [65, 66].

1.5 Summary

This chapter presented the general construction of this thesis, which is about a new type of photodetector featuring intrinsic light-to-time conversion and switching behavior.

General concepts of photodetection were introduced, as well as some photodetectors and their associated circuits that are of interest for this research. It especially showed that shifting the signal to time domain, such as in pulse modulation (PM) imaging, is an interesting alternative to standard CMOS sensors, especially in terms of dynamic range. A time-domain output is also practical for interfacing the sensor with digital circuits.

It is going to be presented in the next chapters that the device of interest for this thesis could advantageously be used in pulse modulation sensors or imagers.

Chapter 2 Hybrid MOS-PN photodetector

In this chapter, a new type of photodetector that is referred to as “Hybrid MOS-PN photodetector” is proposed [67, 68]. The structure and physical operation of the device are described in section 2.1. TCAD simulations are used to explore the impact of technological and electrical parameters on the operation of the device. In section 2.2 the use of the photodetector at system level is described. Different schemes for photo-signal processing are analyzed and their impact on the overall system performances highlighted.

2.1 Device Level analysis

2.1.1 Device structure

The structure of the Hybrid MOS-PN photodetector consists of a combined MOS and PN structure on a low-doped p substrate. As for a standard diode, the p+ and n+ diffusions are called anode and cathode, respectively. The anode is surrounded by a MOS gate. A second P+ diffusion, acting as a ground anchor, is necessary to set the potential of the substrate (Fig. 2-1).

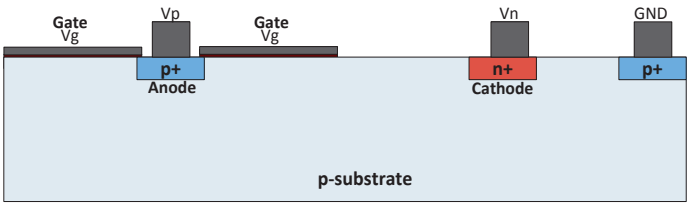

Fig. 2-1: Structure of the Hybrid MOS-PN device

In standard modern CMOS implementations, this basic structure is completed with Shallow Trench Isolation (STI) between the different diffusions. P+ diffusions on each side of the gate are added as a CMOS fabrication requirement. (Fig. 2-2).

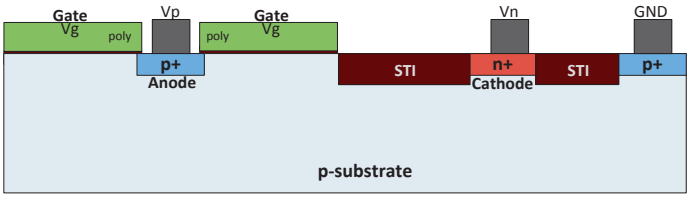

Fig. 2-2: Structure of the device with polysilicon

2.1.2 Operation

The operation of the detector starts by applying a positive voltage step on the gate. This creates a space-charge region due to the carrier depletion induced by the electric field. At the same time, a positive voltage is applied on the anode and the cathode is kept grounded (or at a low voltage). However, no current flows through the PN structure because the anode is isolated by the depletion region and the cathode to bulk junction still reverse based thanks the ground node (Fig. 2-3).

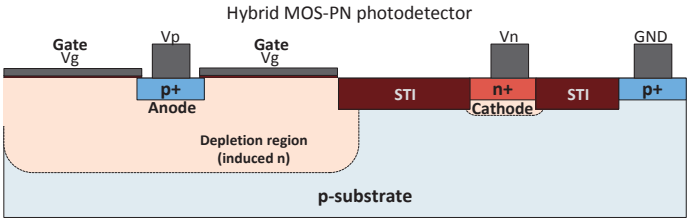

Fig. 2-3: Structure with space-charge region

Under illumination, photo-generated electron-hole pairs are separated by the electric field. Electrons drift under the gate and holes are evacuated to the cathode and ground connections. Over time, the accumulation of electrons under the gate starts to shield the electric field. Consequently, the depletion region shrinks and de-isolates the anode, which in turn emits holes that lower the barrier on the cathode side by locally increasing the potential (Fig. 2-4).

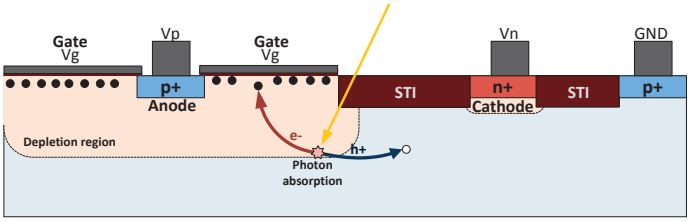

Fig. 2-4: Photon absorption, photoelectron accumulation

In turn, the cathode starts to emit electrons which add up to the charges under the gate, de-isolating the anode even more and increasing the hole current. This leads to a positive feedback effect with a very sharp increase in current magnitude between the anode and cathode (Fig. 2-5).

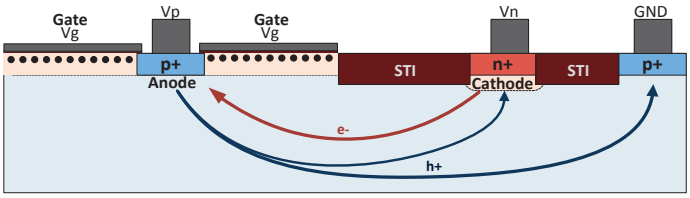

Fig. 2-5: Positive feedback effect

Another way to look at the physical behavior of the device is to look at the potential barriers across it. Fig. 2-6 presents the potential along the red cutline of (a). It can be seen that the potential barrier disappears after the triggering of the device.

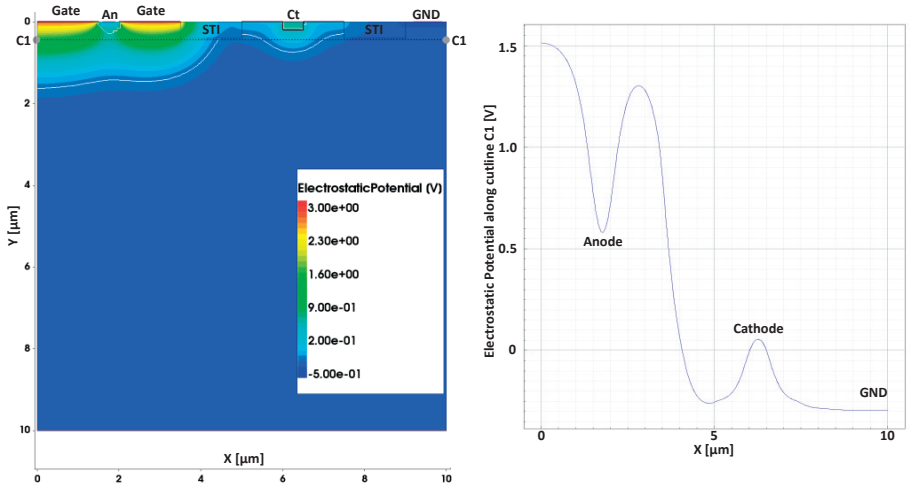

Fig. 2-6: Simulation of the electrostatic potential before triggering in a bulk device a) 2D visualization, b) potential along the cutline C1. V_g =3.0V, V_{an} = 0.8V, V_{ct} = 0.1V.

In summary, the forward biased PN diode becomes conducting (turns on) after a certain amount of charges is accumulated under the gate. The accumulation rate of the charges is directly proportional to light intensity, which means that the time to turn on, also called the triggering time, is inversely proportional to light intensity. The photo-detector thus acts as a charge integrator and comparator, which can be understood as a light-to-time converter (Fig. 2-7). It is also worth noting that the final current magnitude is independent of light intensity.

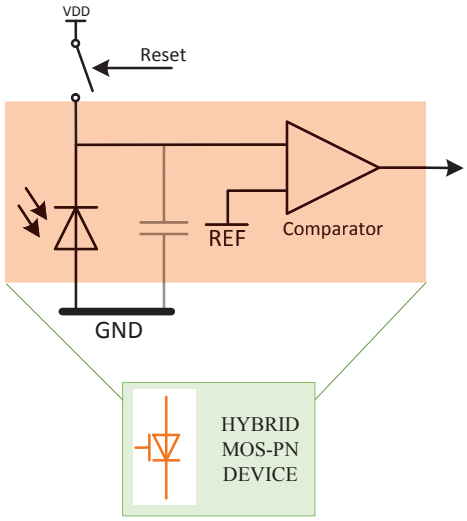

Fig. 2-7: Conceptual equivalent circuit of the photodetector

For a given technology, the amount of charges needed for the device to trigger is mostly determined by gate voltage and geometry. The higher the voltage, the stronger the electric field and thus the higher the number of electrons needed to shrink the depletion region enough for the device to trigger. Concurrently, a larger gate also increases the amount of needed carriers due to the bigger space-charge region thus created. Technological parameters such as oxide thickness and substrate doping have a direct influence on the amount of charge needed to trigger the device.

Once the device has triggered, it needs to be reset in order to evacuate the electrons under the gate as well as the carriers at the PN junction. In order to do so, the Gate is grounded so that the accumulated carriers recombine and/or are evacuated to the anode, and the polarity of the PN junction is reversed in order to evacuate the carriers at the PN junction. The device is then ready for the next detection sequence.

2.1.3 Dark current

In reality, parasitic effects add to the aforementioned operation of the detector. The most notable of them is dark current, which in the case of the Hybrid MOS-PN device refers to the accumulation of non-photogenerated carriers (Fig. 2-8). These carriers participate in the accumulation process and thus to the triggering. The time needed for the detector to trigger due to the dark current alone (i.e. in complete darkness) is called “self-triggering time”.

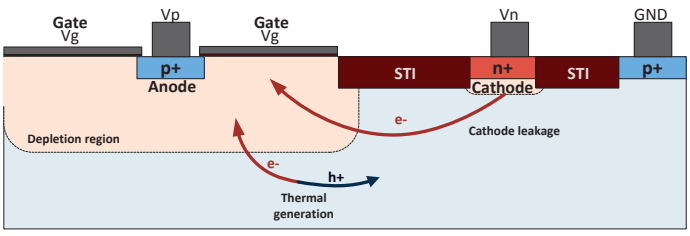

Fig. 2-8: Dark current sources

In the device of interest, dark current comes from two main sources. The first dark current component is thermogenerated electron-hole pairs in the substrate (i_{dark}). This component is not specific to the device of interest, but is common to any charge based photodetector. The second component is specific to the device, and is due to electrons (minority carriers) emitted from the cathode over the junction with the p+ substrate (i_{leak}).

$$i_{dark} = i_{thermal} + i_{leak} \tag{2-1}$$

Cathode to anode leakage comes from the low potential barrier between the n+ diffusion and substrate. The mechanism giving rise to this leakage is as follows. For standard substrate doping levels (N_a = 10^{15} cm^{-3}) and/or low gate voltages, the depletion region is not deep enough to completely engulf the anode. Consequently, there is a resistive path from the anode to the substrate where a hole-current is free to flow. Those free holes end up in the substrate and diffuse towards the cathode where they locally increase the substrate voltage (i.e. decrease the potential barrier).This effect can be alleviated by a good electrostatic control of the substrate through a ground anchor close to the device, as shown in Fig. 2-9. This anchor keeps the voltage around the cathode close to zero. Concurrently, biasing the cathode to a few hundreds of mV, instead of zero, also increases the barrier and reduces the leakage exponentially [69]. This effect is studied in section 3.6.1.

Fig. 2-9 presents a simulation of the electrostatic potential across the device with and without a ground anchor. As expected, without a ground connection, the barrier on the cathode side is inexistent and the anode-side depletion region is smaller.

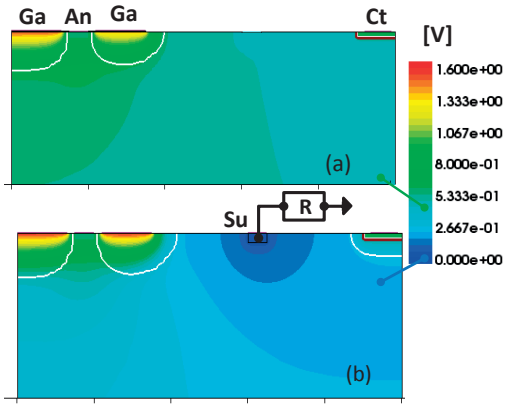

Fig. 2-9: Electrostatic potential without (top) and with (bottom) ground anchor

The closer the ground anchor to the device, the better the electrostatic control and thus the smaller the leakage. In Fig. 2-10, the variation in distance to the ground connection is emulated by varying the value of the series resistor shown in Fig. 2-9. The smaller the series resistance, i.e. the closer the ground anchor, the longer the self-triggering time.

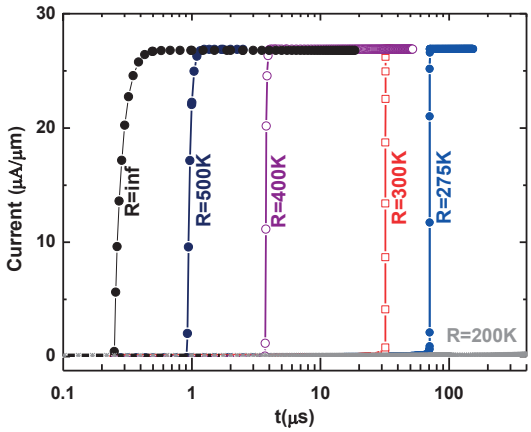

Fig. 2-10: Effect of ground-anchor resistance on self-triggering time

2.1.4 Temperature dependence

A simulation of the temperature dependence of the inverse of self-triggering time for different gate voltages is plotted in Fig. 2-11. Several effects can be observed [70].

First, the higher the gate voltage, the longer the self-triggering time. This is partly due to the fact that the amount of carriers needed to turn the device on increases with gate voltage, but also that leakage current increases for lower gate voltages because of the higher holes injection from the anode due to the shallower depletion region.

Second, the slope of the characteristic (i.e. the exponential factor) is not constant. For low gate voltages, the self-triggering time is divided by two at a higher rate than every 5 to 7 Kelvin corresponding to thermal generation [71]. This is due to the dominance of the cathode leakage variation component over thermal generation at low gate voltage.

Finally, it is interesting to note that the slope suddenly increases at high temperature for low gate voltages (1.4V and 1.6V). At those voltages and temperatures, the depletion layer (and thus the isolation of the anode) does not seem to form properly, leading to a very fast triggering of the device.

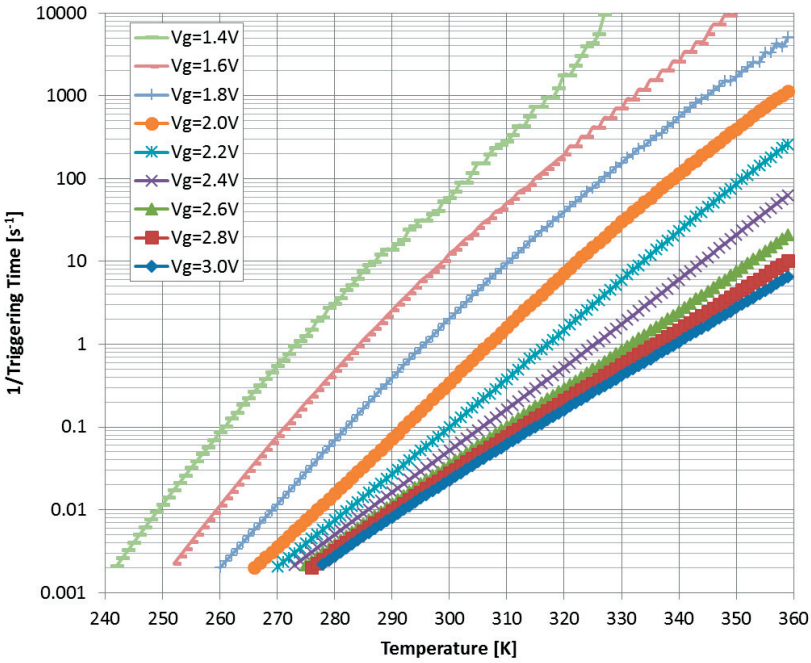

Fig. 2-11: Simulated temperature dependence of the device V_{anode} = 0.8V, $V_{cathode}$ = 0.1V

2.1.5 Linearity: Slow carriers and recombination current

There are two categories of photogenerated electron-hole pairs in the photodetector. First, when a photon is absorbed in the depletion region, the photogenerated electrons drift in the strong electric field of the depletion, accumulate under the gate and almost certainly participate in the photodetector operation. The second category of photocarrier are the ones generated outside of the depletion region. Due to the absence of strong electric field, these carriers are quite slow and reach the depletion only after a certain delay. The proportion of these slow carriers increases with the absorption depth of the photons (i.e. their wavelength) and with the area outside the gates (i.e. the area where no depletion occurs). Fig. 2-12 presents the magnitude of the electric field across the device and shows that the field quickly decreases out of depletion regions.

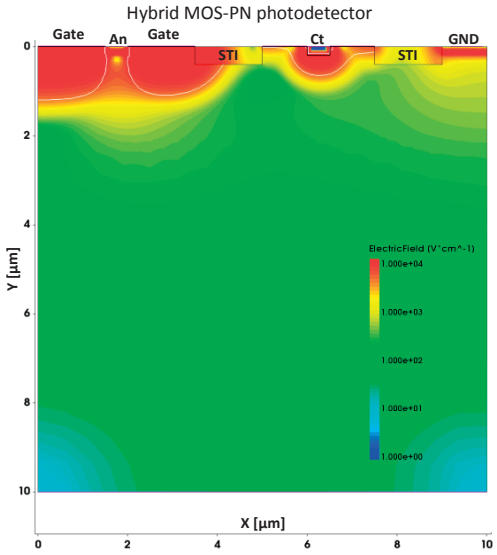

Fig. 2-12: Simulated magnitude of the electric field in the device. V_g = 1.8V, V_{an} = 0.8V, V_{ct} = 0.1V

The time taken by slow carriers to reach the depletion region introduces non-linearities. Indeed, not all the slow carriers have time to reach the depletion region and the time at their disposal depends on light intensity. The higher the intensity, the shorter the triggering time and the smaller the amount of carriers able to reach the depletion region.

Consequently, the useful area around the depletion region decreases when light intensity increases. This translates into a diminution of active area and thus a diminution of the sensitivity of the detector. It also translates into a diminution of quantum efficiency, especially for long wavelengths, for which the majority of the photons are absorbed deep into the silicon (Fig. 2-13).

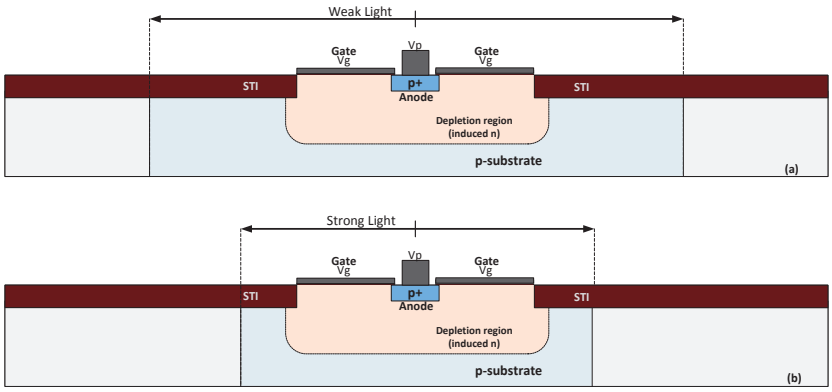

Fig. 2-13: Active area shrink with respect to light intensity

Fig. 2-14 shows the simulated derivative of the inverse of triggering time triggering time with respect to light intensity, which corresponds to the sensitivity of the device. It can be seen that it is decreasing for high intensities, showing the reduction in effective active area (oscillations are due to numerical imprecisions). It is also worth noting that, as a general trend, the sensitivity is higher for lower gate voltages. This is due to the fact that the amount of carriers needed to trigger the device is smaller at low gate voltages, leading to a steeper characteristic. This effect is measured and analyzed in section 3.6.2.

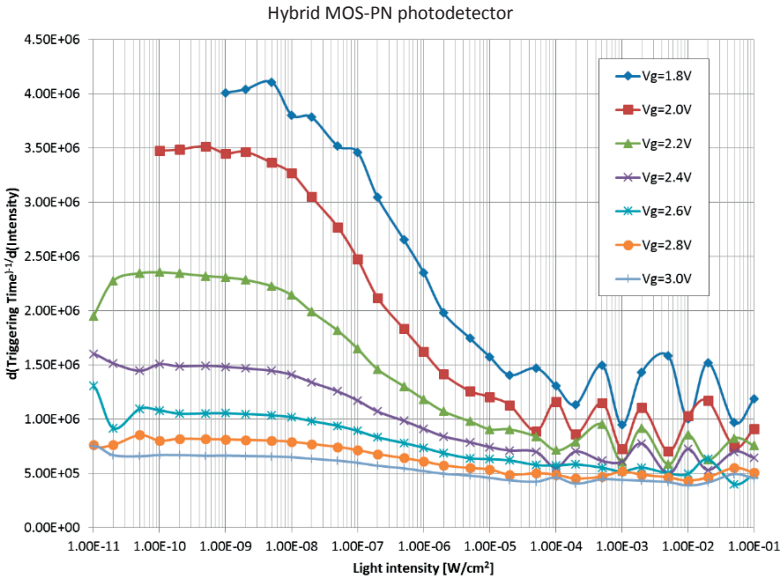

Fig. 2-14: Simulated derivative of the inverse of triggering time versus light intensity. V_{anode} = 0.8V, $V_{cathode}$ = 0.1V, λ = 500nm

By plotting the same relation with respect to triggering time, it can be seen that the sensitivity mostly decreases in a linear way with time, confirming that the main changing parameter is active area (Fig. 2-15).

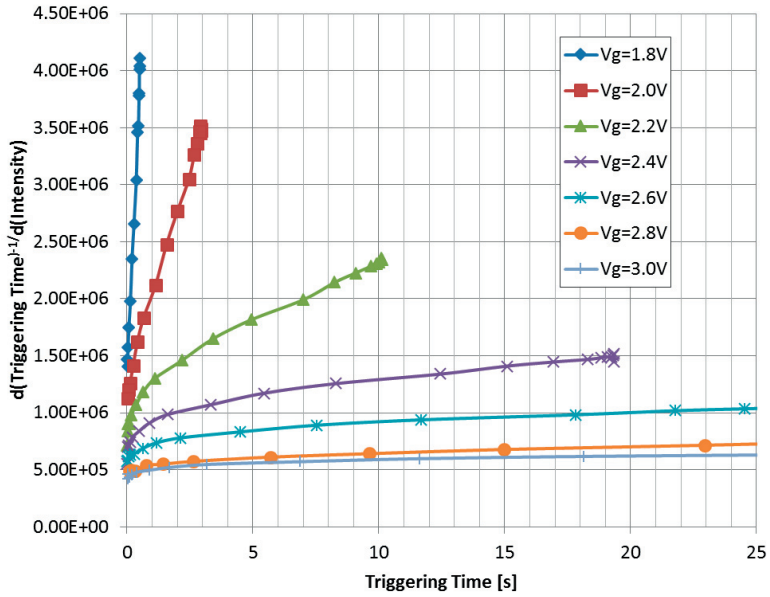

Fig. 2-15: Simulated derivative of the inverse of triggering time versus Triggering Time. V_{anode} = 0.8V, $V_{cathode}$ = 0.1V, λ = 500nm.

This slow carrier effect can be cancelled by effectively blocking the slow carriers, so that they don't have a chance to reach the depletion region. For example, by fabricating the device on a Silicon-on-Insulator technology, as presented in section 4.4.

2.1.6 Input-Output Relation

In this section we propose to derive the basic equations describing the light to time conversion of the proposed photodetector. Under the assumption that the amount of accumulated carriers needed to trigger the device (N_{tot}) doesn't depend on light intensity and that the accumulation rate of charges doesn't change during the integration time (i.e. Light intensity varies slowly in comparison of triggering time), the relation between triggering time, dark current, and photocurrent is given by .

$$\frac{1}{T_{trig}} = \frac{1}{N_{tot}}\left(n_{phot} + n_{dark}\right)\ [s^{-1}] \qquad (2\text{-}2)$$

Where $n_{phot} = \frac{i_{phot}}{q}$ = number of integrated photogenerated charges per second. [s^{-1}];

$n_{dark} = \frac{i_{dark}}{q}$ = dark carrier generation by temperature and cathode leakage [s^{-1}];

T_{trig} = triggering time [s];

$N_{tot} = \frac{Q_{tot}}{q}$ = Number of carriers needed for triggering;

The variable n_{phot}, and thus the triggering time, can be expressed in function of light intensity (I_{light}), active area (A), quantum efficiency for a giver wavelength (QE_λ), and wavelength (λ), as:

$$\frac{1}{T_{trig}} = \frac{1}{N_{tot}}\left(\underbrace{\frac{A \cdot QE_\lambda \cdot \lambda}{hc} I_{light}}_{n_{phot}} + n_{dark}\right) = \frac{1}{N_{tot}}\left(\underbrace{\frac{A \cdot QE_\lambda}{E_{phot}} I_{light}}_{n_{phot}} + n_{dark}\right) \quad (2\text{-}3)$$

This relation can also be written in function of responsivity (R_λ), knowing that:

$$R_\lambda = \frac{q \cdot QE_\lambda \cdot \lambda}{hc} \left[{}^{A}/_{W} = {}^{C}/_{J}\right] \quad (2\text{-}4)$$

Yielding:

$$\frac{1}{T_{trig}} = \frac{1}{Q_{tot}}\left(\underbrace{A \cdot R_\lambda \cdot I_{light}}_{i_{phot}} + i_{dark}\right) \quad (2\text{-}5)$$

These theoretical expressions show that T_{trig}^{-1} varies linearly light intensity, if all the parameters are constants with respect to light intensity.

In order to verify the limit of this characteristic, TCAD simulations are performed. Section 2.1.5 has shown that it's not actually the case and that the effective active area of the photodetector (A) varies with light intensity.

From the previous relations, an expression of self-triggering time (T_0) can be derived.

$$T_0 = \frac{Q_{tot}}{i_{dark}} \quad (2\text{-}6)$$

2.1.7 Signal-to-Noise Ratio

In order to derive the expression of the signal-to-noise ratio (SNR) of the proposed device, its operation is first compared to the one of a CCD. Indeed, the detection principle of the Hybrid MOS-PN photodetector shows similarities with the one of a CCD pixel. In both cases, carriers are accumulated in a depletion region. Our calculation is thus inspired by the SNR expression of CCDs [72]:

$$SNR_{CCD} = \frac{\varphi}{\sigma} = \frac{\varphi}{\sqrt{\sigma_{dark}^2 + \sigma_{light}^2 + \sigma_{read}^2}} \quad (2\text{-}7)$$

φ : signal. Number of photocharges

σ_{dark} : dark carriers shot noise

σ_{light} : photocharges shot noise. Equals to $\sqrt{\varphi}$

σ_{read} : readout noise (extrinsic noise)

The main difference between a CCD and our device is that, with a CCD, a variable amount of charge is integrated during a fixed time, whereas with our device, a fixed amount of charges is integrated during a variable time. The intrinsic noise of our device is thus given by:

$$SNR_{intrinsic} = \frac{N_{phot}}{\sqrt{\sigma_{dark}^2 + \sigma_{phot}^2}} = \frac{N_{phot}}{\sqrt{N_{dark} + N_{phot}}} \quad (2\text{-}8)$$

Knowing that

$$N_{tot} = N_{phot} + N_{dark} \tag{2-9}$$

$$N_{dark} = n_{dark} \cdot T_{trig} \tag{2-10}$$

$$\frac{1}{T_{trig}} = \frac{1}{N_{tot}}(n_{dark} + n_{phot}) \tag{2-11}$$

It is possible to express N_{dark} in function of N_{phot} or N_{tot}:

$$N_{dark} = n_{dark} \cdot T_{trig} = n_{dark} \frac{N_{tot}}{n_{dark}+n_{phot}} = n_{dark} \cdot \frac{N_{phot}}{n_{phot}} \tag{2-12}$$

The expression for intrinsic SNR can thus be rewritten in function of the amount of charges needed to trigger the device (N_{tot}), n_{phot}, and n_{dark} as:

$$SNR_{intrinsic} = \frac{\sqrt{N_{phot}}}{\sqrt{\frac{n_{dark}}{n_{phot}}+1}} = \sqrt{N_{tot}} \frac{\sqrt{\frac{n_{phot}}{n_{dark}+n_{phot}}}}{\sqrt{\frac{n_{dark}+n_{phot}}{n_{phot}}}} = \frac{\sqrt{N_{tot}}}{\frac{n_{dark}}{n_{phot}}+1} \tag{2-13}$$

This expression shows that the intrinsic noise of the device converges to $\sqrt{N_{tot}}$ for high light intensities (large n_{phot}). In low light conditions, the detrimental effect of dark current (n_{dark}) is more important. Notably, cathode leakage must be minimized.

The expression of the SNR can be rewritten in terms of light intensity (I_{light}), active area (A), and Responsivity (R_λ) or quantum efficiency (QE_λ) and wavelength (λ) as:

$$SNR_{intrinsic} = \frac{\sqrt{N_{tot}}}{\frac{n_{dark}}{n_{phot}}+1} = \frac{\sqrt{N_{tot}}}{\frac{i_{dark}}{A \cdot R_\lambda \cdot I_{light}}+1} = \frac{\sqrt{N_{tot}}}{\frac{n_{dark} \cdot hc}{A \cdot QE_\lambda \cdot \lambda \cdot I_{light}}+1} \tag{2-14}$$

Under the assumption that the device is linear, i.e. that its parameters don't change with light intensity, the same expression can be rewritten with respect to triggering time (T_{trig}) and self-triggering time (T_0), using the following relation.

$$\frac{n_{dark}}{n_{phot}} = \frac{\frac{N_{tot}}{T_0}}{\left(\frac{1}{T_{trig}} - \frac{1}{T_0}\right)N_{tot}} = \frac{T_{trig}}{T_0 - T_{trig}} \tag{2-15}$$

The expression for the intrinsic SNR can thus be rewritten.

$$SNR_{intrinsic} = \sqrt{N_{tot}} \frac{1}{\frac{n_{dark}}{n_{phot}}+1} = \sqrt{N_{tot}}\left(1 - \frac{T_{trig}}{T_0}\right) \tag{2-16}$$

In order to complete the noise characterization of the whole photodetector system, the following extrinsic sources have to be considered:

σ_{read}: read noise of the front end electronics. Expected to be very low, since the readout is almost fully digital.

σ_{gate}: voltage noise on the gate.

σ_{anode}: voltage noise on the anode

$\sigma_{cathode}$: voltage noise on the cathode

The SNR can thus be written as

$$SNR_{total} = \frac{N_{phot}}{\sqrt{\sigma_{dark}^2 + \sigma_{phot}^2 + \underbrace{\sigma_{read}^2 + \sigma_{gate}^2 + \sigma_{anode}^2 + \sigma_{cathode}^2}_{Noise_{ext}}}} = \frac{N_{phot}}{\sqrt{N_{dark} + N_{phot} + Noise_{ext}}} \tag{2-17}$$

By using the same calculations than previously, the expression for the total SNR can be derived:

$$SNR_{total} = \frac{\sqrt{N_{phot}}}{\sqrt{\frac{n_{dark}+n_{phot}}{n_{phot}} + \frac{Noise_{ext}}{N_{phot}}}} = \frac{\sqrt{N_{tot}}\frac{1}{n_{dark}}+1}{\sqrt{1+\frac{Noise_{ext}}{N_{tot}}}} = \frac{\sqrt{N_{tot}}(1-\frac{T_{trig}}{T_0})}{\sqrt{1+\frac{Noise_{ext}}{N_{tot}}}} \quad (2\text{-}18)$$

It is interesting to note that, in order to reduce the impact of the external noise component, the size of the integrator (N_{tot}) must be increased.

2.2 System-level design and analysis

In this section, several detection schemes and modulations suitable for the Hybrid MOS-PN photodetector are presented and their advantages and drawbacks are analyzed.

2.2.1 Pulse Width Modulation (PWM) Scheme

Pulse Width Modulation (PWM) is one of the most natural ways to use the device of interest. In this mode of operation, the device is alternating between forward biasing (sensing) and reverse biasing (reset) at a fixed frequency (Fig. 2-16). In this case, the information about light intensity is contained in the duration of the forward biasing sequence before triggering, i.e. triggering time (T_{trig}).

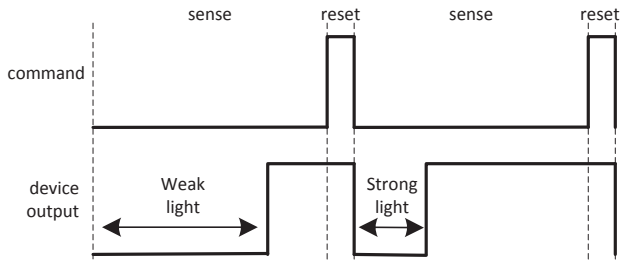

Fig. 2-16: Pulse Width Modulation (PWM)

This time can be measured by a digital counter, Time to Digital Converter (TDC) such as a delay line or a combination of the two to maximize dynamic range [73]. The time measured in this case corresponds to the inverse of light intensity, since:

$$T_{trig} = \frac{N_{tot}}{n_{phot}+n_{dark}} \; [s] \quad (2\text{-}19)$$

The measurement can optionally be linearized. Depending of the application, this can be done at conversion time using a look-up table, varying the frequency of the clock signal driving the measurement counter [58].

Another simple method to linearize the measurement is to integrate the triggering time. This can be done analogically on a capacitor or numerically on an accumulator. An example of an analog implementation is presented in Fig. 2-17. In that case, the imprecisions in the measurement mainly come from charge injection of the switch and leakage of the capacitor.

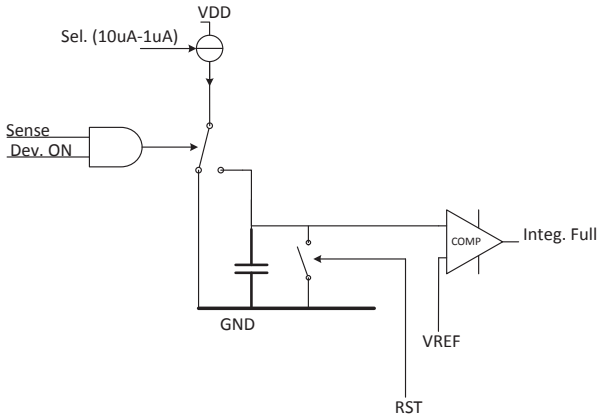

Fig. 2-17: Simple implementation of a time integrator

The behavior of the analog integrator can be modelled as follows.

$$T_{int} = \int_0^{V_{ref}} \frac{C}{\alpha \cdot I_{set}} dV \tag{2-20}$$

With

$$\alpha = \frac{T_{trig}}{T_0} = \frac{1}{1+\frac{n_{phot}}{n_{dark}}} \tag{2-21}$$

Which yields

$$T_{int} = \int_0^{V_{ref}} \frac{C}{I_{set}} \left(1 + \frac{n_{phot}}{n_{dark}}\right) dV = \frac{V_{ref} \cdot C}{I_{set}} \left(1 + \frac{n_{phot}}{n_{dark}}\right) [s] \tag{2-22}$$

T_{int} is thus linear with respect to n_{phot}.

The dynamic range of the PWM detection system depends on the maximum and minimum measurable triggering times. In this case, T_{max} corresponds to the self-triggering time (T_0), which is defined by dark current. T_{min} corresponds to the minimum measurable triggering time, which depends on the speed of the electronics (i.e. the technology node) and on the measurement and digital conversion technique.

$$DR_{PWM} = \frac{T_{max}}{T_{mim}} = \frac{T_0}{T_{min}} \tag{2-23}$$

In practice, the dynamic range of the implemented device can be evaluated to about 140dB (7 decades), assuming a minimum measurable time of 1ns and a self-triggering time of 10ms (section 3.6.1).

In PWM mode (not linearized), the expression of the sensitivity is given by

$$S_{PWM} = \left|\frac{dT_{trig}}{dn_{phot}}\right| = \frac{N_{tot}}{\left(n_{phot}+n_{dark}\right)^2} \; [s^2] \tag{2-24}$$

The expression can be rewritten in terms of light intensity (I_{light})

$$S_{PWM} = \left|\frac{dT_{trig}}{dI_{light}}\right| = \frac{N_{tot} \cdot A \cdot QE_\lambda \cdot \lambda}{hc} \cdot \frac{1}{\left(\frac{A \cdot QE_\lambda \cdot \lambda}{hc} I_{light} + n_{dark}\right)^2} \; [\frac{m^2 \cdot s^2}{J} = \frac{s^4}{kg}] \tag{2-25}$$

It is interesting to note that the sensitivity decreases for higher light intensities, introducing a compression effect which can be interesting in high dynamic range applications. The equation also reveals that the dark current decreases the sensitivity of the device.

2.2.2 Pulse frequency modulation (PFM) Scheme

The Hybrid MOS-PN photodetector is also usable in a pulse frequency modulation (PFM) scheme (Fig. 2-18). In that case, the device is immediately resetted for a fixed reset time (T_{reset}) after each triggering (T_{trig}).

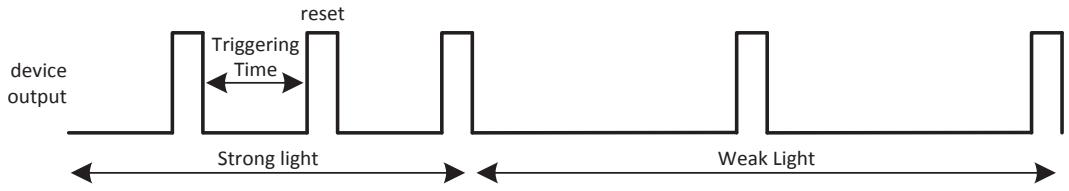

Fig. 2-18: Pulse Frequency Modulation (PFM)

There is therefore a linear dependence between triggering frequency and light intensity. The frequency is easily measured and directly digitized with a simple pulse counter at the output of the detection system. In the ideal case, where $T_{reset} << T_{trig}$, the output frequency is given by

$$f_{PFM} = \frac{1}{T_{trig}} = \frac{1}{N_{tot}} \left(n_{phot} + n_{dark}\right) [Hz] \tag{2-26}$$

From which the sensitivity can be calculated

$$S_{PFM} = \left| \frac{d\frac{1}{T_{trig}}}{dn_{phot}} \right| = \frac{1}{N_{tot}} \; [] \tag{2-27}$$

The expression can also be rewritten in terms of light intensity (I_{light})

$$S_{PFM} = \left| \frac{d\frac{1}{T_{trig}}}{dI_{light}} \right| = \frac{A \cdot QE_{\lambda} \cdot \lambda}{hc \cdot N_{tot}} \; [\frac{m^2}{J} = \frac{s^2}{kg}] \tag{2-28}$$

It is interesting to note that in this case, the sensitivity neither depends on light intensity nor on dark current, but only on physical parameters.

Another interesting aspect of the PFM detection is the averaging effect. During a measurement timeframe (T_{frame}), the number of measurements that are effectively being performed is equal to $f_{PFM} \cdot T_{frame}$. In other words, $f_{PFM} \cdot T_{frame} \cdot N_{tot}$ carriers are being accumulated, which changes the SNR formulation as follows.

$$SNR_{intrinsic,PFM} = \frac{\sqrt{f_{PFM} \cdot T_{frame} \cdot N_{tot}}}{\frac{n_{dark}}{n_{phot}}+1} = \frac{\sqrt{T_{frame}(n_{phot}+n_{dark})}}{\frac{n_{dark}}{n_{phot}}+1} = \frac{\sqrt{T_{frame}} \cdot n_{phot}}{\sqrt{n_{dark}+n_{phot}}} \tag{2-29}$$

In this case the SNR is not constrained by N_{tot} anymore and tends to $(T_{frame} \cdot n_{phot})^{1/2}$ for high intensities or small dark current. This equation also shows that, theoretically, an arbitrary SNR can be achieved with a long enough measurement timeframe.

However, if the assumption $T_{reset} << T_{trig}$ is not verified, which is the case for strong light intensities, the expression for the output frequency becomes:

$$f_{PFM} = \frac{1}{T_{trig}+T_{reset}} = \frac{n_{phot}+n_{dark}}{N_{tot}+T_{reset}(n_{phot}+n_{dark})} \; [Hz] \tag{2-30}$$

Which gives the following formula for sensitivity:

$$S_{PFM} = \left| \frac{d\frac{1}{T_{trig}}}{dn_{phot}} \right| = \frac{N_{tot}}{\left(N_{tot}+T_{reset}(n_{phot}+n_{dark})\right)^2} \; [] \tag{2-31}$$

The sensitivity now depends on light intensity and dark current, and that tends to zero for high intensities or large T_{reset}. As expected, this expression reverts to the previous one when T_{reset} tends to zero.

The dynamic range of the PFM system is defined by the maximum and minimum achievable frequencies. The maximum frequency is constrained by T_{reset}, and the minimum frequency is constrained by self-triggering time (T_0), which gives the expression:

$$DR_{PFM} = \frac{f_{max}}{f_{min}} = \frac{\frac{1}{T_{reset}}}{\frac{1}{T_0+T_{reset}}} = \frac{T_0+T_{reset}}{T_{reset}} = \frac{N_{tot}}{n_{dark} \cdot T_{reset}} + 1 \tag{2-32}$$

In practice, due to the relatively long reset time of the implemented Hybrid MOS-PN device, dynamic range is limited to about 40dB, assuming a self-triggering time of 10ms (section 3.6.1) and a reset time of about 100µs (section 3.6.5).

2.2.3 Pulsed voltage operation

As presented is sub section 2.1.3, a significant part of dark current originates from cathode leakage, which is due to the incomplete shielding of the anode of forward biased PN junction. Holes thus injected in the substrate lower the barrier on the cathode side, which in turn emits electrons that are integrated under the gate. Fig. 2-19 reveals that the electron current density increases by several orders of magnitude when the PN structure is forward biased (b) compared to the case when it is tied to ground (a), which translates into a decreased self-triggering time.

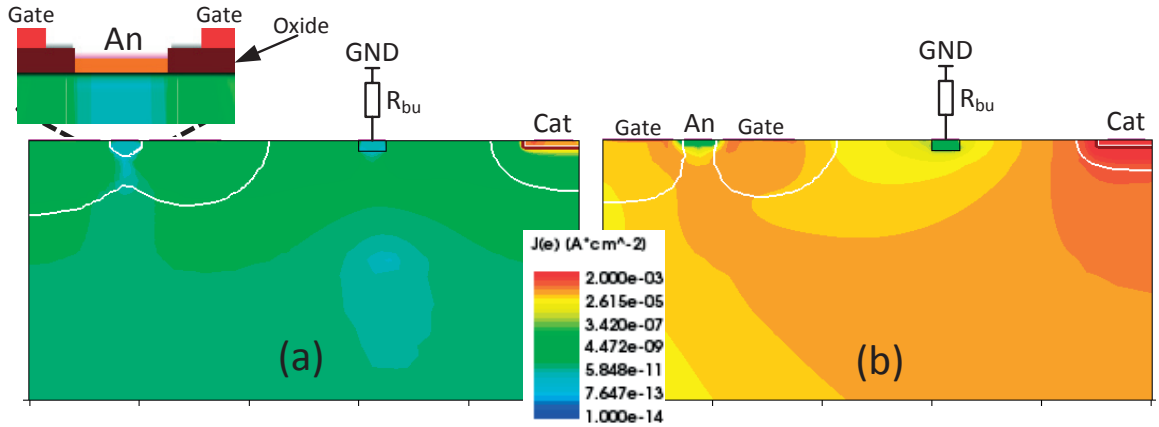

Fig. 2-19: Simulation of the electron current density with (a) V_{an} = 0V and (b) V_{an} = 1V. In both cases, V_{ct} = 0.2V, V_{gate}=2V, R_{bu} = 400kΩ.

Two strategies were used in [67] and [69] to effectively counteract this detrimental effect, yet both present limitations. In [67], low substrate doping (around 10^{14} cm^{-3}) increases the depletion depth. However, such low doping is incompatible with standard CMOS processes (nominal substrate doping around 10^{15} cm^{-3}). In [69], the cathode potential barrier is increased using a specific biasing of the device. This technique, however, significantly attenuates the dark current only when the cathode voltage is raised to a sufficiently high level. This obviously results in a drop of the triggering current with a greater detection difficulty.

On the other hand, the detrimental continuous forward biasing is not necessary during charge integration. In fact, the sole function of the forward bias is to generate the positive feedback and, in turn, the triggering when the integrated charge reaches a given N_{tot}. In other words, the device acts as a comparator [74]. By biasing the PN junction during short lapses of time instead of with a DC voltage, cathode leakage can effectively be decreased. By applying a pulsed voltage of duty cycle D, the expression of the dark current becomes

$$n_{dark\_pulsed} = n_{thermal} + D \cdot n_{leak} \tag{2-33}$$

Consequently, triggering time is increased. In the ideal case, it is given by

$$\frac{1}{T_{trig\_pulsed}} = \frac{1}{N_{tot}}(D \cdot n_{leak} + n_{thermal} + n_{phot}) \tag{2-34}$$

Most importantly, the SNR of the device is also improved. The following expression is valid in the ideal case.

$$SNR_{intrinsic\_pulsed} = \frac{\sqrt{N_{tot}}}{\frac{D \cdot n_{leak} + n_{thermal}}{n_{phot}} + 1} \tag{2-35}$$

Fig. 2-20 demonstrate the increase of triggering time for small values of D = T_h/T. As expected, the self-triggering time is inversely proportional to the duty cycle. For instance, dividing T_h by 10 (from 5 to 0.5 µs) leads to a change in time triggering from 3.6 to 36 ms.

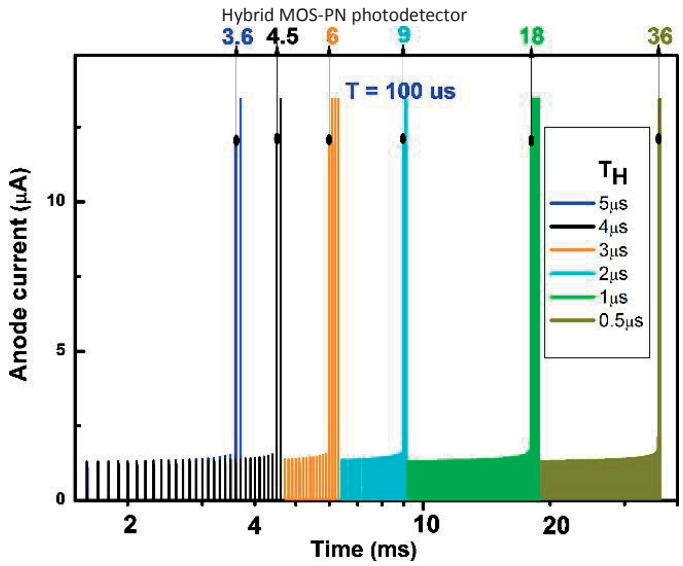

Fig. 2-20: Anode current versus time for different duty-cycle values. f_{pulse} = 10kHz, Vg = 2V, V_{an} = 1V, V_{ct} = 0.2V

Nevertheless, in real operation, each rising edge of the anode voltage might introduce recombination. Let's assume that each rising edge entails the recombination of a fixed amount of carriers N_{recomb}. The total amount of "lost" carriers during one detection windows is proportional to the number of rising edges of the anode signal, which depends on the ratio between triggering time (T_{trig}) and the period of the anode signal T_{pulse}.

$$N_{lost} = \frac{T_{trig}}{T_{pulse}} N_{recomb} \tag{2-36}$$

Those lost charges must be compensated and add up to the number of carriers needed to turn the device on. The expression of triggering time is thus modified.

$$\frac{1}{T_{trig}} = \frac{n_{phot}+n_{dark\_pulsed}}{N_{tot}+N_{lost}} = \frac{1}{N_{tot}}\left(n_{phot} + n_{dark\_pulsed} - \underbrace{\frac{N_{recomb}}{T_{pulse}}}_{n_{recomb}}\right) \tag{2-37}$$

The effect of recombination can thus be modelled as a current n_{recomb} which is subtracted to the photocurrent and dark current. An adverse effect of this current is that it adds up to the noise of the photodetector through shot noise and degrades the SNR.

$$SNR_{intrinsic\_recomb} = \frac{N_{phot}}{\sqrt{\sigma^2_{dark\_pulsed}+\sigma^2_{phot}+\sigma^2_{recomb}}} = \frac{\sqrt{N_{tot}}}{\frac{D\cdot n_{leak}+n_{thermal}+\frac{N_{recomb}}{T_{pulse}}}{n_{phot}}+1} \tag{2-38}$$

From this expression, it appears that the best SNR is reached for small values of D and large values of $T_{pulse.}$ However, applying an anode signal of long period introduces quantization noise (not modelled in the expression) that increases with T_{pulse}. There must therefore be an optimum of SNR with respect to T_{pulse}.

An important and beneficial consequence of the pulsed operation of the device is that it acts as a direct digital conversion. By counting the number of pulses before triggering, a thermometer scale digital converter is created (Fig. 2-21).

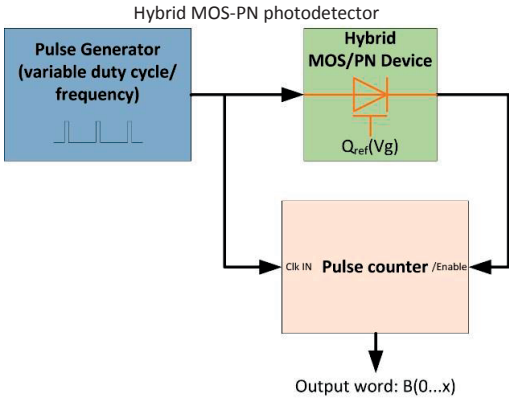

Fig. 2-21: Concept of a pulse-counting converter

Of course, that kind of conversion scheme has several disadvantages. First, the digital word thus obtained corresponds to the inverse of light intensity. Second, in order to reach a high resolution, the pulse period (T_{pulse}) must be very small, with the aforementioned disadvantages in terms of noise. In order to linearize the conversion and to alleviate the recombination problem, the device can be driven with a variable frequency, generated for example via a look-up table, as presented in section 2.2.1.

2.2.4 Binary search

Another way to use voltage pulses to cancel cathode leakage without introducing the recombination problem is to perform a binary search algorithm on the triggering time.

Instead of driving the anode of the device with an AC signal of small duty cycle, only one voltage pulse is applied after some predetermined integration time. Depending on whether current flows through the device during the voltage pulse, the integration time of the next detection is either decreased or increased. A binary search algorithm is thus created, and an N-bits analog to digital conversion is performed in N detection cycles. A SAR-ADC is thus created (Fig. 2-22).

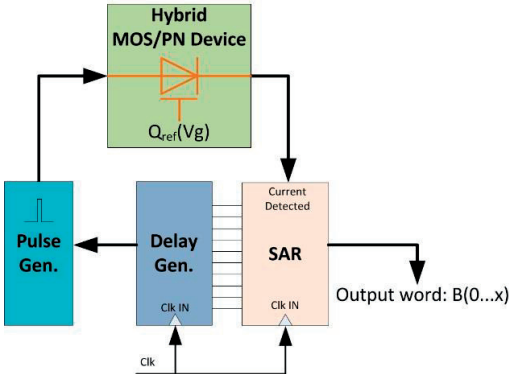

Fig. 2-22: Concept of a Successive Approximation Register (SAR) based converter

With this detection scheme, cathode leakage current during detection is completely cancelled (instead of being multiplied by D), and the potential recombination problem introduced by the rising edge of the anode voltage does not exist either, because the device is resetted after each pulse. The drawback of such a detection scheme is mainly conversion speed. As previously stated, an N bit conversion requires N detection periods, and requires light intensity to be constant during the conversion.

Here as well, a look-up table can be used to linearize the conversion by generating “pre-distorted” delays. The precision of the whole system is mainly constrained by the quality of the delay generator, which must generate very precise and reproducible delays, especially for strong light intensities.

It is also worth noting that there is a physical limit to the precision of the conversion due to shot noise. For a one sigma precision on the LSB, for m-bits, N_{tot} in the ideal case (no leakage) can be expressed

$$\sqrt{N_{tot\_min}} = 2^m \tag{2-39}$$

This number is a theoretical minimum. In practice, due to dark current and other noises, N_{tot_min} is larger and the photodetector has to be designed consequently. This limit is not specific to the pulse-operated binary search algorithm, but valid for any analog to digital conversion scheme.

2.3 Electrical model of the device

In order to be able to device a control and read-out circuit for the Hybrid MOS-PN device, it is important to have a model describing the electrical behavior of the device.

The model of the device must take in account both its operating states and non-ideal parameters, which are presented in Fig. 2-23. When the device is off, most of the leakage current consists of a hole-current flowing from the anode to ground (R_{leak}). The electron current emitted from the cathode and participating in the dark current of the detection is negligible compared to the current through R_{leak} and is not represented. It is important to understand that the hole-current between anode and ground does not participate to the dark current of the detection (i.e. it does not accumulate under the gate). When the device is on, the anode current has two components, one diode current between anode and cathode with a small series resistor R_s, and a hole current to ground of a way bigger magnitude than before (R_{hole}<<R_{leak}).

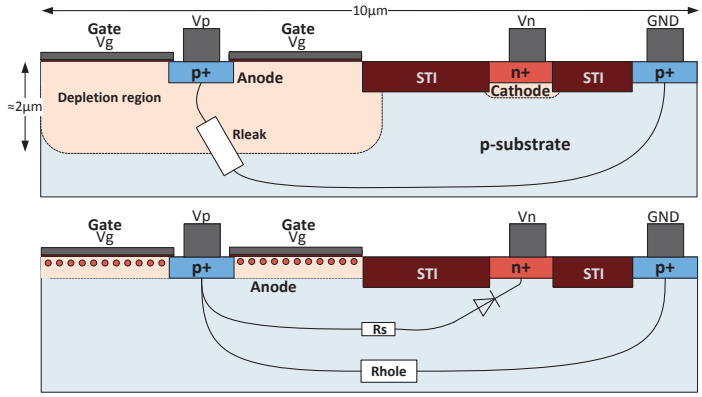

Fig. 2-23: Current paths before (top) triggering and after (bottom) triggering

A more complete model must take into account the reverse biased diode between cathode and ground, which introduces a small reverse leakage current. Fig. 2-24 presents an equivalent circuit of the device. The transition between the OFF and ON state is done by closing the ideal switch.

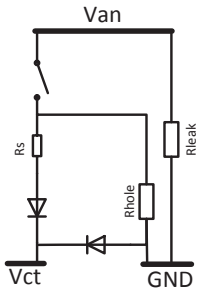

Fig. 2-24: Simple equivalent circuit of the device

The dynamic behavior of the device strongly depends on the parasitic capacitances between the different terminals, which are introduced in the complete model presented in Fig. 2-25.

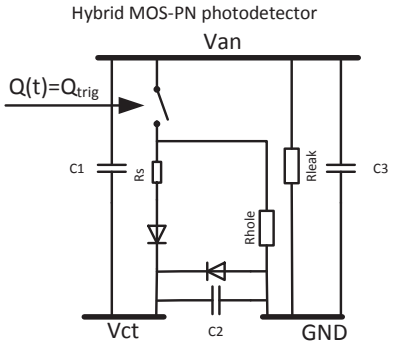

Fig. 2-25: Equivalent circuit with parasitic capacitances

It is difficult to determine the values of components and the diode parameters without a proper semiconductor-level modelling of the device. Nevertheless, the values in Table 2-1 were used for circuit design, and the diode areas were chosen according the the size of the N+ diffusion.

Parameter	Value
Rs	10-100 Ω
Rhole	0.1-1 MΩ
Rleak	10-100 MΩ
C1	10 fF
C2	1 fF
C3	1 fF

Table 2-1: Device model parameters

The resistance R_{hole} introduces a resistive path in parallel to the diode current. Depending on the resistance value and the diode forward voltage, the resistive current path can dominate. Fig. 2-26 shows that diode voltage (V_{an}-V_{ct}) must be higher than 0.5-0.6 V in order to dominate. Nevertheless, this simple model doesn't take into account the electrostatic effects of the ground anchor on the diode characteristics depending on the geometrical arrangement between the cathode and the anchor and can therefore only provide qualitative results.

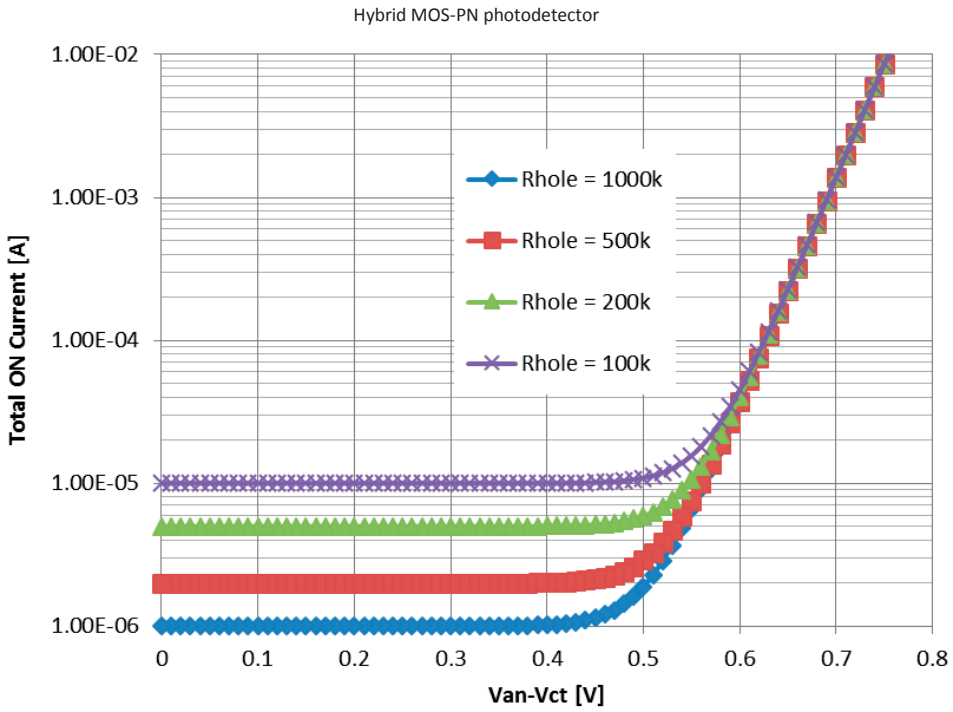

Fig. 2-26: Modelled device current versus diode forward voltage or different R_{hole} resistances

From a system point of view, one can argue that knowing which is current the dominant one has no importance, as long as the positive feedback effect takes place and produces the steep current step during triggering and that total current is sufficiently high to be easily detectable. The next chapter is going to present circuits taking advantage of the device characteristics.

2.4 Summary

This chapter presented the Hybrid MOS-PN device and its use as a photodetector. Its structure and physical operation were presented and its behavior analyzed. In particular, the triggering time of the device is proportional to the inverse of light intensity. The performances of the device strongly depend on substrate doping levels as well as the distance to the nearest ground anchor (i.e. the electrostatic control of the substrate).

Several detection schemes usable with the device were then presented and analyzed, such as PWM and PFM. The performances in PFM mode suffer from the relatively long reset time. It is shown that pulsed operation of the device can reduce leakage and thus improve SNR, and can also be used as a method for light-to-digital conversion.

Finally, a circuit-equivalent model on the device is presented, taking in account leakage and parasitic capacitances. Such a model is useful for efficient circuit design.

Chapter 3 Front end circuit design and experimental validation

This chapter presents the design and validation of the light detection system using the Hybrid MOS-PN device as photodetector. Several implementations of the driver and front end circuits are presented, as well as the microcontroller-based control and measurement system. Measurements of the device characteristics using the detection system are then presented and analyzed. Finally, an implementation of the pulsed operation of the detector is presented.

3.1 Circuit principle

Chapter 2 showed that the Hybrid MOS-PN photodetector behaves as a device-level charge integrator and comparator that triggers with a sudden current step when a certain amount of charge is reached. The front end circuit must efficiently take advantage of this behavior while minimizing silicon area and power consumption. Concurrently, the circuit must drive the detector to the correct voltages, switching it between a reverse and forward bias.

Basically, the front end circuit has to detect a step in current. However, directly measuring a current is complicated and may involve a transimpedance amplifier, which is exactly the kind of circuit that is used in standard photodiode-based detection and that the device of interest is supposed to avoid. A simpler method was thus selected, which consists in directly converting the diode current into voltage by discharging (or charging) the anode (or cathode) node capacitance.

The design of the circuit is inspired by the active quench-and-reset circuits used with single photon avalanche photodiodes (SPAD). However, the operation is more complex. In the case of the SPAD, the detector simply has to be resetted (biased to a reverse voltage higher than the breakdown voltage) after each detection. In the case of the Hybrid MOS-PN photodetector, there is one more step in the operation during which the device is reverse biased and the free carriers evacuated. The device is then forward biased in order to be ready for the next detection. Finally, the anode (or cathode) is put in high impedance, allowing the triggering of the device to discharge (or charge) the node capacitance.

With a standard bulk CMOS implementation, the substrate is always grounded and is the most negative potential. It is therefore impossible to apply a negative voltage to the device in order to reverse bias it. Instead, the polarity of the device is reversed by applying a high voltage on the cathode while grounding the anode. Once cleaned of free carriers, the device is then forward biased before the detection node being put in high impedance. Fig. 3-1 presents the three operating phases of the detection circuit, here presented with detection on the anode side.

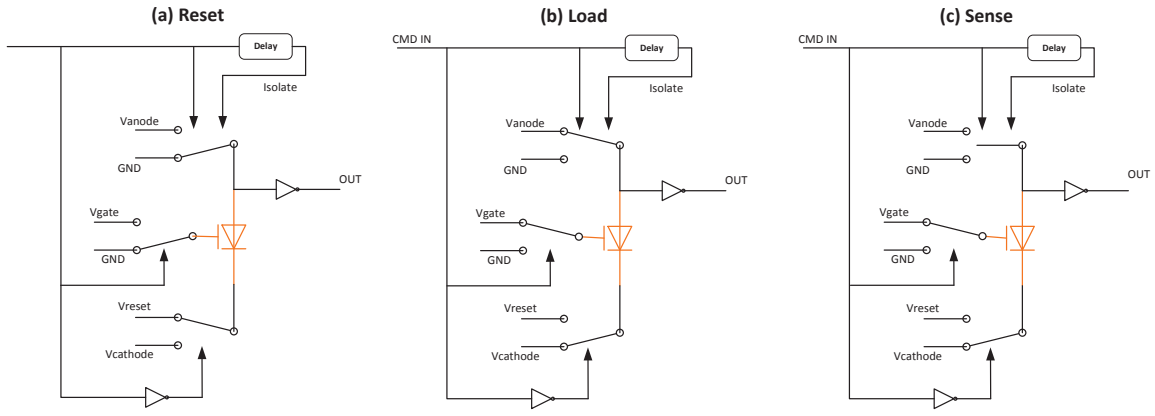

Fig. 3-1: Operating principle of the driver circuit in three phases

The forward current of the device after triggering follows an exponential behavior with respect to forward voltage that can be modelled by the Shockley diode equation. This current charges the capacitance of the detection node. In order to express the time-varying voltage on the capacitance, the circuit of Fig. 3-2 must be solved.

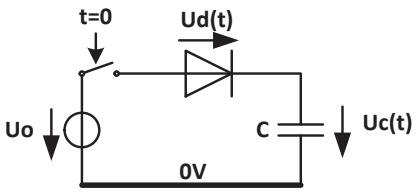

Fig. 3-2: Charge of a capacitance through a junction-diode

Knowing the equation of the capacitor

$$I(t) = C\frac{dU_c(t)}{dt} \tag{3-1}$$

And the Shockley diode equation

$$I(t) = I_s\left(\exp\left(\frac{U_d(t)}{nU_t}\right) - 1\right) = I_s\left(\exp\left(\frac{U_0 - U_c(t)}{nU_t}\right) - 1\right) \tag{3-2}$$

Which combine into the following ordinary differential equation.

$$\frac{dU_c(t)}{dt} - \frac{I_s}{C}\left(\exp\left(\frac{U_0 - U_c(t)}{nU_t}\right) - 1\right) = 0 \tag{3-3}$$

Which can be solved for the initial condition $U_c(0)=0V$.

$$U_c(t) = nU_t \cdot \ln\left(exp\left(\frac{U_0}{nU_t}\right) - \left(exp\left(\frac{U_o}{nU_t}\right) - 1\right) \cdot exp\left(-\frac{I_s}{C \cdot nU_t}t\right)\right) \tag{3-4}$$

This logarithmic behavior of the capacitor voltage entails that, for a fast and noiseless detection, i.e. a detection where the slope of the voltage is very steep, it is important to have a low detection-voltage threshold (Fig. 3-3). The next sections detail the design on the detection circuits.

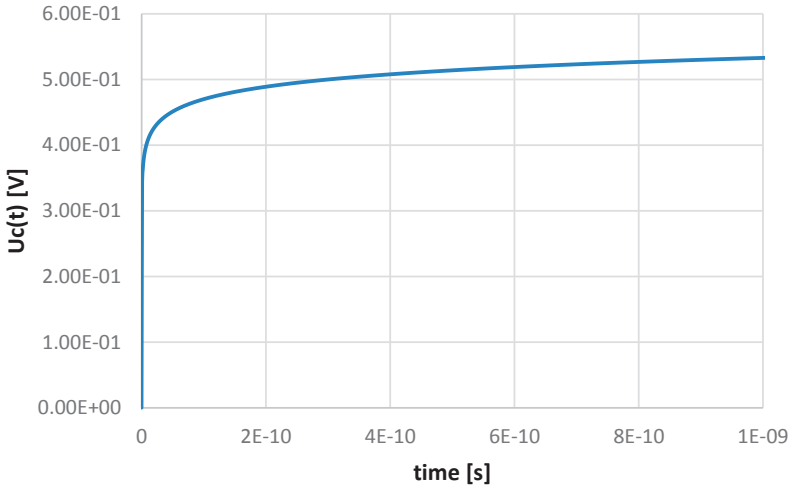

Fig. 3-3: Evaluation of Uc(t) with Is=1e-14A, n=1.05, Ut=26mV, C=10fF

3.2 Anode-side read-out

Using the anode as detection node presents some advantages, notably in terms of reset sequence. Indeed, Fig. 3-1 showed that during reset, the anode is connected to ground, whereas the cathode is connected to V_{reset}, which is a positive voltage. Having the read-out transistor on the anode side allows to apply a high voltage on the cathode (3.3V) while using low-voltage transistors on the anode side without risk of breakdown. For this reason, this configuration was the first to be implemented in the UMC 180nm CMOS technology.

The driving circuitry is simply constituted of an inverter and a tri-state inverter on the cathode and anode side, respectively. The tri-state gate is here to put the anode in a high impedance state after having biased the PN structure in forward mode. A small programmable delay between the forward biasing and the high-impedance mode is generated by a chain of inverters, as presented in Fig. 3-4. The inverters chain can generate a maximum delay of about 8.8 ns with 73 inverters.

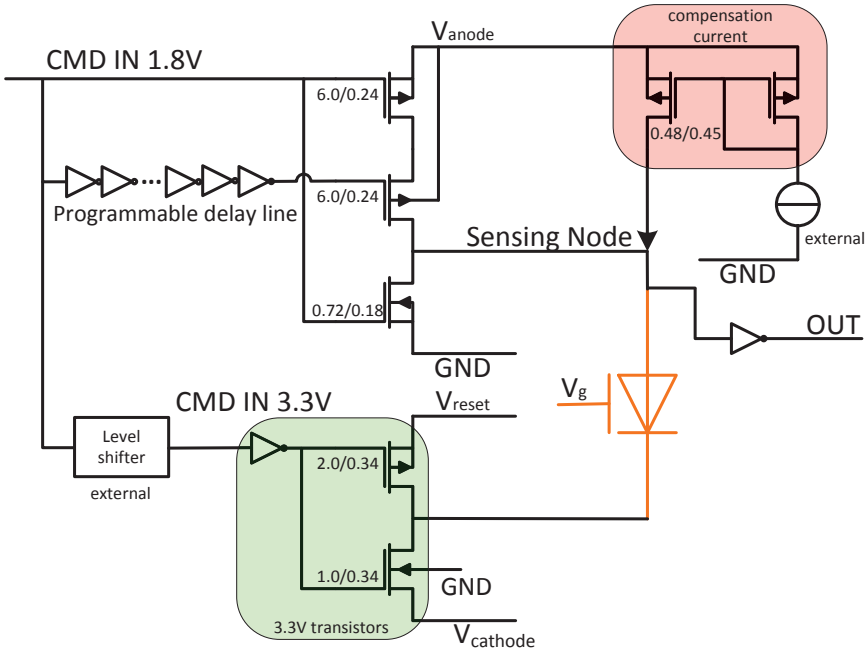

Fig. 3-4: Implementation of the driver circuit with anode as sensing node

Fig. 3-4 also shows a compensation-current circuit. It was chosen to implement this circuit due to the poor understanding of the device at the time of the circuit design and due to the foreseen leakage current thought the NMOS transistor of the anode driving circuit. Eventually, the compensation current proved itself very useful, due to the imperfect shielding of the anode and the associated hole-leakage current. For any system using anode-side read-out, anode leakage would have to be compensated. With good device modelling, the leakage current can be characterized and the compensation circuit made simpler, without external bias, for example with a resistor or a small diode-connected PMOS transistor. The compensation current is based on an external tunable current reference.

In this implementation of the circuit, the level-shifter for the control signal (CMD_IN) as well as the gate voltage (V_g) control circuits are implemented at board level with discrete components and circuits.

The front end circuit itself is basically a level-shifter that converts the swing of the sensing node to a CMOS 1.8V logic signal (Fig. 3-5). The design challenge of this circuit is to minimize the parasitic capacitance on the sensing node, allowing for a steep discharge and thus read-noise minimization, while having a fast-enough front end circuit that minimizes the signal delay and allows a precise read-out in fast-triggering conditions.

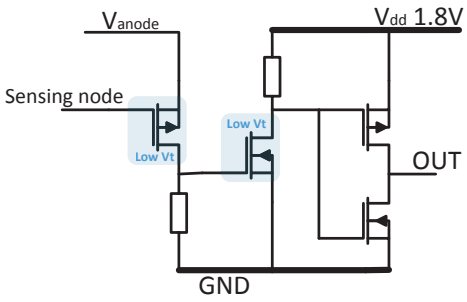

Fig. 3-5: Simplified schematic of the anode-side read-out circuit

In order to minimize the capacitance and knowing that the circuit only needs to detect a falling-edge transition, it was decided to use an “asymmetrical” scheme, with only one low-Vt PMOS transistor connected to the sensing node. The pull-down and pull-up components were implemented as fixed-bias transistors with a high resistance. To ensure a quick and clean reset of the voltages after detection, reset transistors are added. Those are activated during the “load” phase of the system and are controlled by the same delay generator as the anode driver. The sizing of the transistors was performed by parametric analysis in order to minimize the propagation delay between the triggering and the output signal (Fig. 3-6). The optimized delay is of about 650ps.

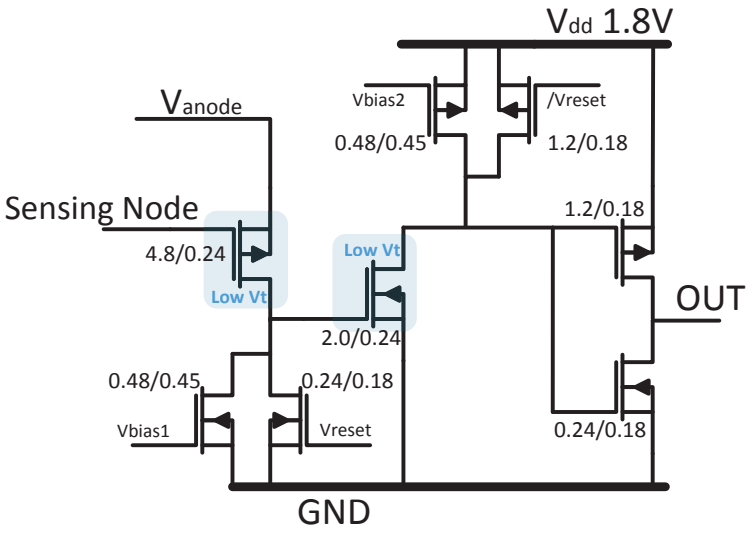

Fig. 3-6: Complete schematic of the anode-side read-out circuit

Per chip, four different front end circuits were implemented and their inputs and outputs multiplexed in order to be able to test four different detectors. The total circuit area is about 150µm x 75µm. The complete chip size is 1.5mm x 1.5mm. In the example presented in Fig. 3-6, only three devices are connected to the circuit. The fourth front end circuit is not connected to any device and is there to test the functionality in case of problems. In that case, the detection node is connected to an NMOS transistor that simulate the triggering of the device.

The layout of the entire chip is presented in Fig. 3-7. In this first implementation, the detectors were placed far away from the circuit in order to avoid any interference.

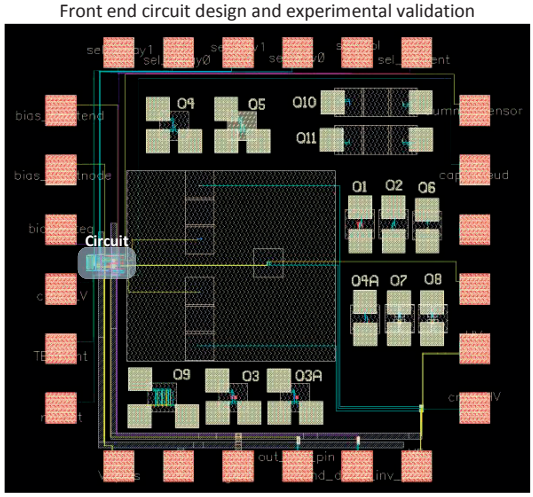

Fig. 3-7: Layout of the entire chip (UMC 0.18µm)

The characteristics of the circuits are summarized in Table 3-1

Parameter	Value
Technology	UMC 0.18 µm
Chip Area	2.25 mm^2
V_{dd}	1.8 V
$V_{reset,\ max}$	3.3 V
Number of pads	24
Total circuit area	11’250 µm^2
Number of detection circuits	4
Detection node	anode
Static consumption	Yes (compensation current and bias)
t_d	650 ps
V_{th}	-160 to -200 mV

Table 3-1: Characteristics of the anode-side circuit implementation

A potential detection problem that can arise from the circuit design is that due to the very small threshold voltage of the first transistor, the circuit might trigger itself before the device has triggered, especially for leaky photodetectors. In order to avoid this problem is to carefully tune the compensation current as well as the bias of the load transistors of the detection circuit. A solution to avoid this problem altogether is not to use a low-Vt PMOS transistor on the detection node but a standard PMOS transistor (V_{th} ≈ -490 mV) at the price of a longer detection time.

3.3 Cathode side read-out

It was shown in the previous section that one of the main disadvantages of the anode-side read-out circuit is that it has to compensate for the anode-leakage current, which introduces static consumption as well as a risk of self-triggering. A solution to this problem is to use the cathode as detection node [74]. This section presents the design of two different implementations of a cathode-side front end circuit.

3.3.1 Implementation with delay generator

The first implementation of the cathode-side front end circuit follows the same principle as the one presented in the previous section. It was designed and realized on the ON-semiconductor 0.18µm CMOS technology.

The driver circuit is the same as previously, but with the tri-state gate on the cathode-side, which is now the sensing node (Fig. 3-8). With this configuration, the compensation current is now unneeded, since the leakage on the cathode side is almost negligible. The drawback of this configuration is that reset can now only be performed with a maximum voltage (V_{reset}) of 1.8V. This is due to the fact that the front end circuit consists of low-voltage low-Vt transistors, whose gate oxide might break down for higher voltages. Consequently, the tri-state gate also consists of low-voltage transistors, with the same voltage requirements. Another particularity of this driver circuit is the introduction of body effect on the NMOS transistors of the tri-state gate, due to the fact that $V_{cathode}$ can be higher than ground. Consequently, these transistors were designed with a wider gate in order to compensate for the larger on-resistance (R_{ON}) introduced by the body effect. The gate driver circuit (V_g) is implemented externally.

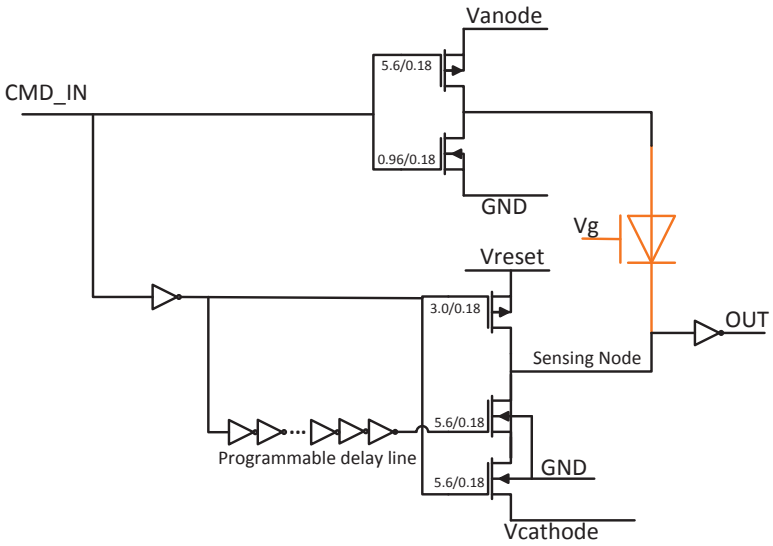

Fig. 3-8: Implementation of the first driver circuit with cathode as sensing node

The principle of the front end circuit is a reverted version of the previous one, and its goal is also to convert the triggering of the photodetector into a CMOS logic signal (Fig. 3-9). The selected technology (On-semi 0.18µm) does not implement low-Vt transistors of PMOS type. Consequently, a standard low-voltage PMOS transistor was used

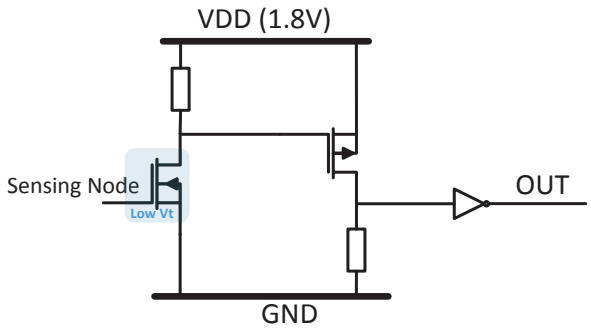

Fig. 3-9: Simplified schematic of the cathode-side read-out circuit

The design procedure of the read out circuit is the same as the previous one, but simplified. In order to avoid any external bias, the loads of the “level shifter” were implemented as diode-connected transistors with low-gm (long transistors). Like before, quick and correct reset of the circuit is ensured by reset transistors acting during the “load” phase of the system (Fig. 3-10). Due to the unavailability of low-Vt PMOS transistors, the detection-delay time is longer than previously, with a delay t_d = 1.6 ns.

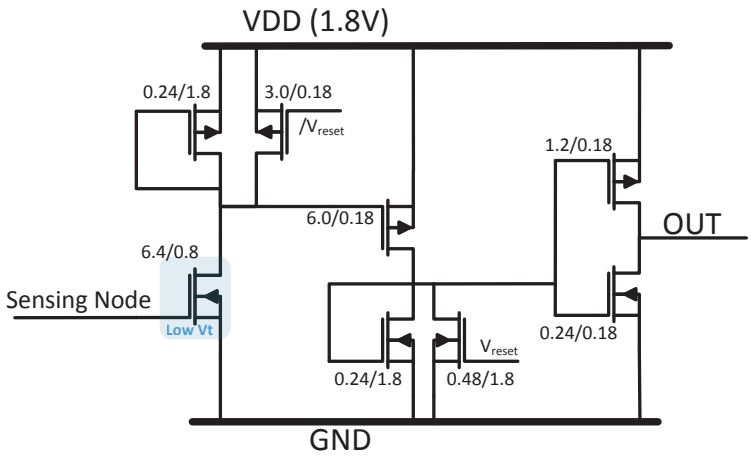

Fig. 3-10: Complete schematic of the first cathode-side read-out circuit

Two independent detection circuits were implemented per chip, which allows to test two detectors. Due to time constraints, the multiplexing circuitry was implemented externally with discrete components. Fig. 3-11 shows the layout of a complete driver and front end circuit. It is worth noting that ¾ of the area are occupied by the delay generator. The total area of one detection circuit is about 1400 µm².

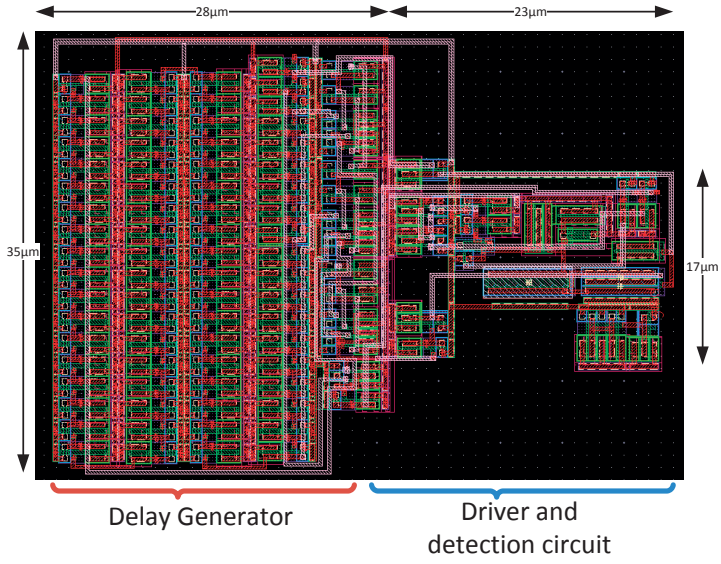

Fig. 3-11: Layout of the detection circuit (cathode read-out, first version)

The complete chip has a size of about 1.3 mm x 1.3 mm and also contains test devices. Fig. 3-12 presents the layout of such a chip.

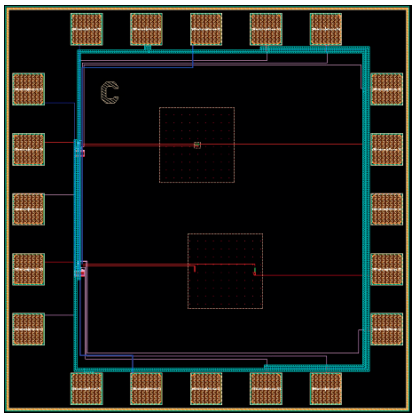

Fig. 3-12: Layout of the entire chip (cathode read-out, first version)

Table 3-2 summarizes the characteristics of the circuit.

Parameter	Value
Technology	ON-semi 0.18 µm
Chip Area	1.69 mm^2
V_{dd}	1.8 V
$V_{reset,\ max}$	1.8 V
Number of pads	20
Total circuit area	2x 1'400 μm^2
Number of detection circuits	2
Detection node	cathode
Static consumption	Yes when triggered
t_d	1600 ps
V_{th}	150 to 180 mV

Table 3-2: Characteristics of the first cathode-side circuit implementation

The detection circuit was fabricated and tested, and it was remarked that the circuit itself suffers from self-triggering. Off-current in the PMOS transistor of the cathode-driving gate (Fig. 3-8) was overlooked during design. A test circuit that is not connected to any photodetector was used to measure the self-triggering of the circuit itself in function of $V_{cathode}$. Fig. 3-13 shows that the worst case appears for $V_{cathode}$ = 0V. Indeed, the higher the voltage drop on the PMOS transistor, the higher the leakage current in the off transistor. Several solutions can be implemented in order to alleviate this problem. For example, The PMOS transistor can be made smaller, at the price of a higher R_{on} and slower transition of the Photodetector into reset mode. Another solution is to improve the circuit by adding a system that disconnects the PMOS transistor from the power supply during detection.

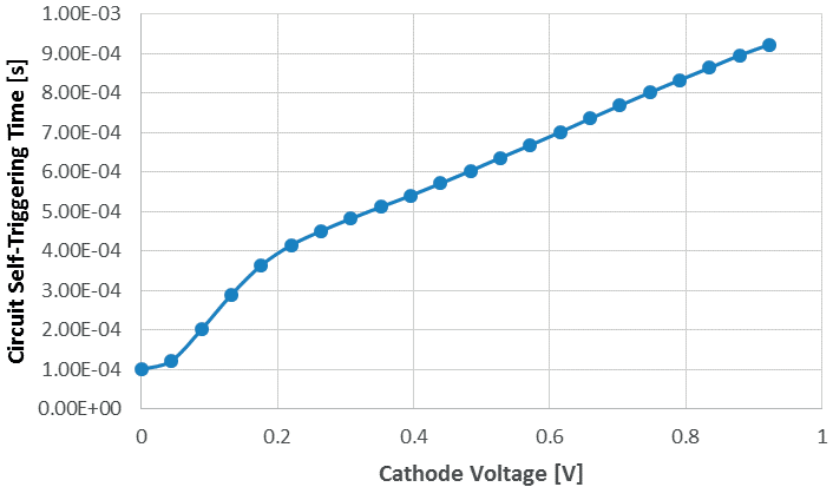

Fig. 3-13: Measurement of circuit self-triggering with respect to cathode voltage

3.3.2 Implementation with feedback system

A second version of the cathode-side front end circuit was developed. Its main goals are to test a new concept of "load" phase without delay generator, optimize the design of the read-out circuit, and fix the flaws discovered on the first implementation, notably self-triggering due to off leakage.

The previous section showed that the ¾ of the driver and front end circuit area are in fact occupied by the delay generator used for the "load" phase of the photodetector. Avoiding the delay generator would not only spare silicon area, but also power consumption. In order to avoid the use of a delay generator, a feedback system that uses the information about the state of the sensing node in order to control the driver circuit is proposed. Fig. 3-14 presents that, basically, the sensing node is put in high impedance when a certain voltage is reached.

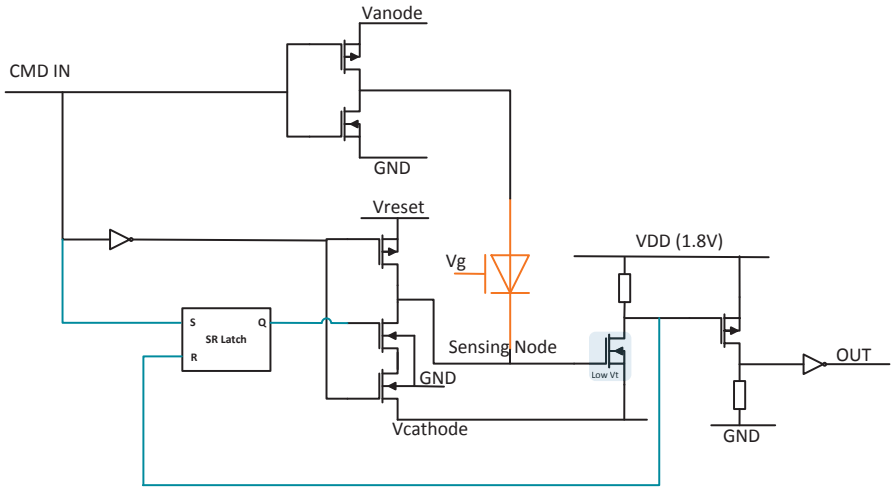

Fig. 3-14: Concept of the "load" sequence feedback system

The new circuit was designed during a semester project and its general schematic is presented in Fig. 3-15. It consists of a driver circuit (*Reset cathode*), a Front end (*Readout*), and a feedback block that controls the "load" phase of the detector as well as a positive feedback effect on the front end circuit. It was designed on a UMC 0.18µm CMOS technology.

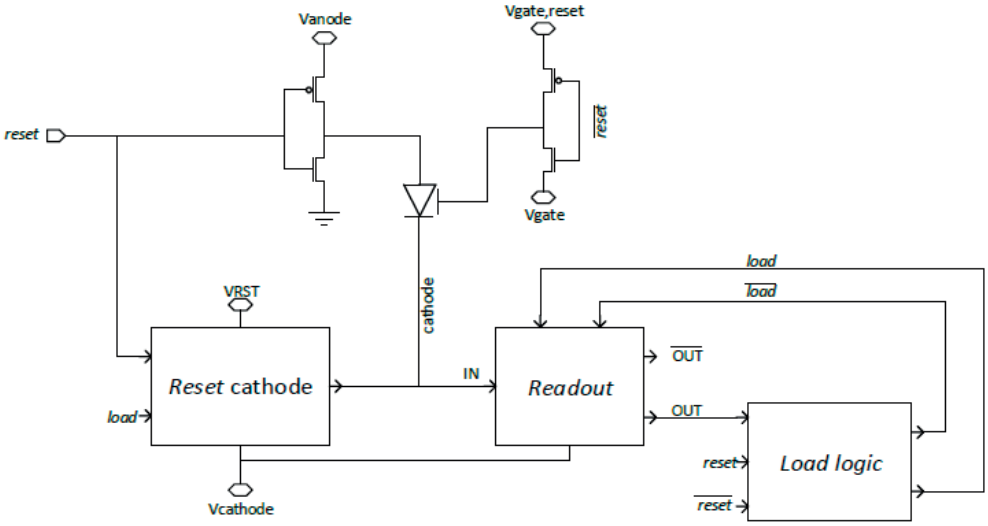

Fig. 3-15: High-Level schematic of the second cathode-side detection system [75]

The *Reset cathode* block solves the leakage problem of the previous circuit by disconnecting the reset PMOS transistor from the V_{reset} voltage during the sense phase, cancelling the voltage drop on it (Fig. 3-16). The IN node corresponds to the sensing node.

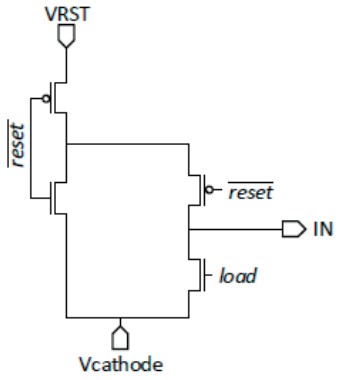

Fig. 3-16: Leakage cancellation circuit [75]

The *Readout* block operates on the same principle as the previous one, but it incorporates a feedback system that turns off the passive loads and thus cancels the static power consumption when the circuit has triggered (Fig. 3-17). It also incorporate a "load" system to ensure that the logic levels are well defined before the "sense" phase. The first NMOS transistor (the one connected to the sensing node (IN) has a low-Vt. All other transistors are of standard type. The delay time (t_d) between triggering of the photodetector and the change in the output signal is of 1.5 ns.

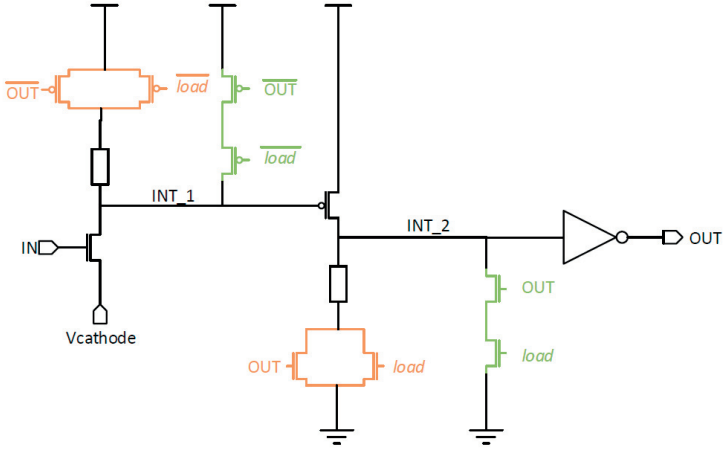

Fig. 3-17: Principle of the read-out circuit with feedback (cathode-side, second version) [75]

The *load* signal is generated with the following circuit (Fig. 3-18). During the reset phase, *reset = 1* and *OUT = 0*. Therefore, the intermediate signal *RL = 1* and *load = 0*. When *reset* goes from 1 to 0, *RL* stays 1 until *OUT* goes to 1, during this time *load = 1*. In other words, the system exists the "load" phase when the output is back to the correct state. The feedback system has the advantage that the duration of the "load" phase is automatically adapted to the speed of the sensing node and the front end circuit.

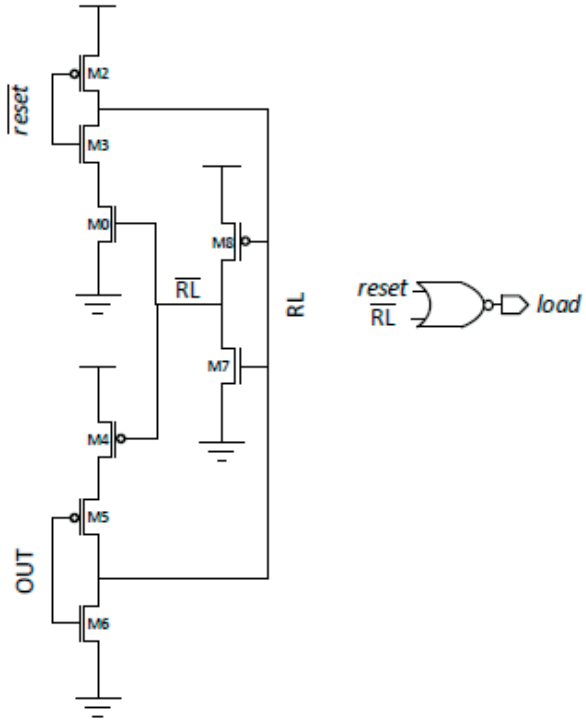

Fig. 3-18: "load" signal generator [75]

The feedback system turning off the passive loads of the front end circuit means that the complete system does not suffer from any static consumption. This is clear in the $i_{readout}$ graph of Fig. 3-19, which only has a current peak during triggering and load. It is also worth noting that the circuit does not suffer from self-triggering. The leakage cancellation technique is therefore efficient.

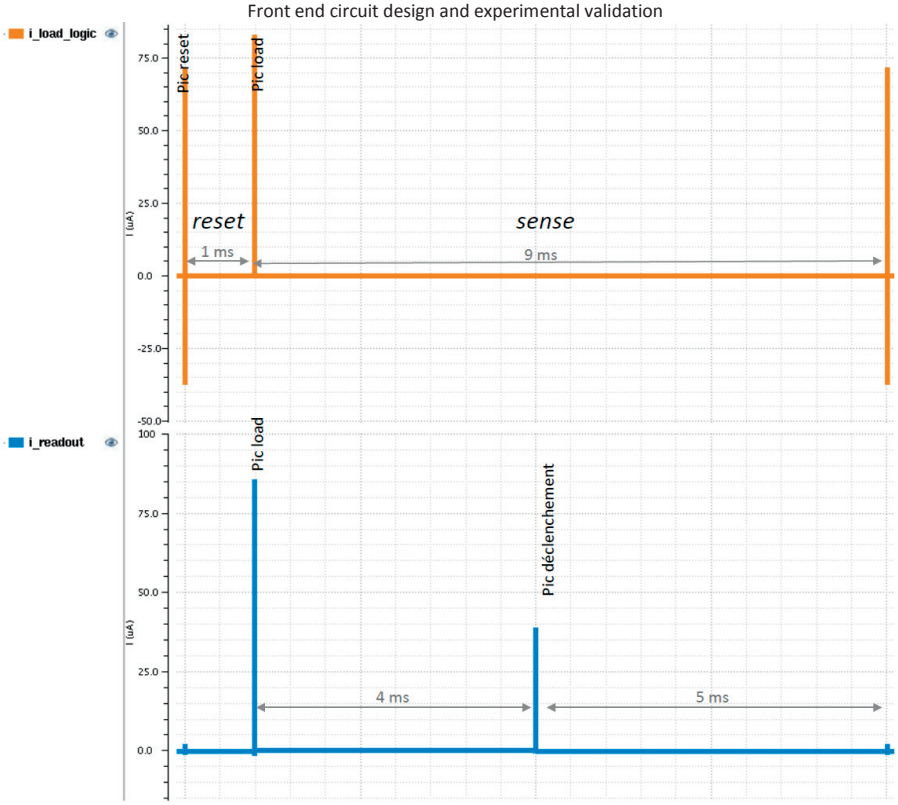

Fig. 3-19: Simulation of the current consumption of the detection circuit [75]

Fig. 3-20 presents the layout of the complete circuit. The total silicon area of one detection circuit is 840 µm^2. It can be easily seen that this area can be decreased by optimizing the layout. By comparing this area with the one of the previous circuit (1400 µm^2), the gain of not having a delay generator is clear.

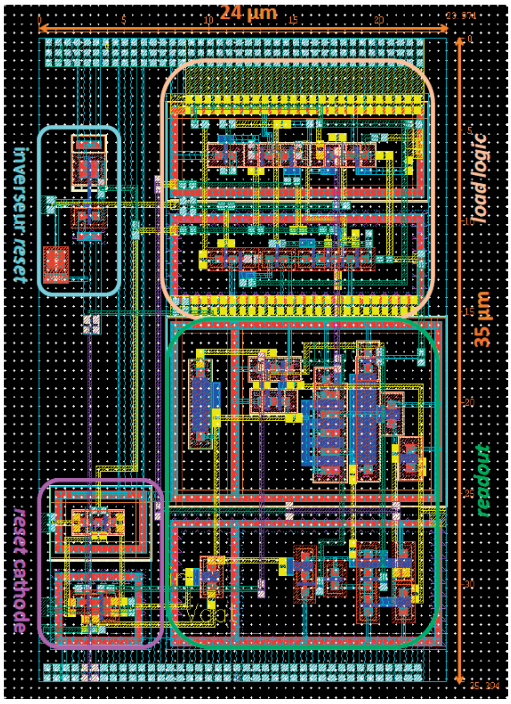

Fig. 3-20: Layout of the driver and read-out circuit (cathode-side, second version) [75]

Fig. 3-21 presents the complete layout of the circuit. Four driver and front end circuits were implemented and multiplexed, with four different detectors.

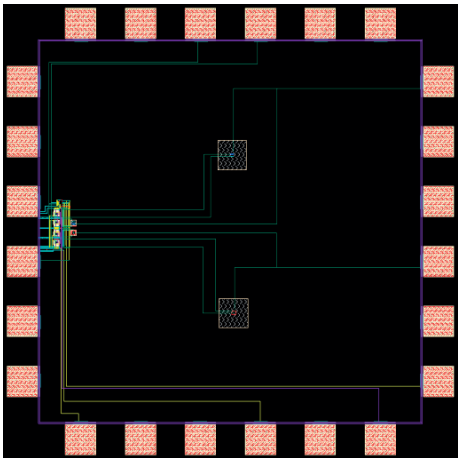

Fig. 3-21: Layout of the entire chip (cathode-side read-out, second version)

The characteristics of the device are summarized in Table 3-3

Parameter	Value
Technology	UMC 0.18 µm
Chip Area	2.25 mm^2
V_{dd}	1.8 V
$V_{reset,\ max}$	1.8 V
Number of pads	24
Total circuit area	5775 μm^2
Number of detection circuits	4
Detection node	cathode
Static consumption	No
t_d	1500 ps
V_{th}	150 to 180 mV

Table 3-3: Characteristics of the second cathode-side circuit implementation

3.4 Device Implementation

The Hybrid MOS-PN devices are implemented on the same chip as the driver and front end circuits. It is directly implemented on the substrate with standard design rules. A “p-well block” layer is drawn on and around the device to ensure that no additional p-type dopant is implanted in the substrate below the device and therefore that its doping stays low (substrate doping of the UMC 0.18µm technology is evaluated around $N_A = 8 \cdot 10^{14}\ cm^{-3}$). In addition, the metal-filler layers are opened above the devices so that light can reach them and be absorbed in the substrate.

Fig. 3-22 presents the layout of a Hybrid MOS-PN photodetector. In order for a thin gate oxide to be fabricated, it is necessary (on the used CMOS technologies) to draw the gate-anode assembly as a PMOS transistor. It means that the p+ diffusion on the anode is present on both sides of the gate and is left floating on the outer side. If the device is not built that way, no thin gate oxide is built

under the gate, but thick field oxide instead, and the device does not work. The reference device that was used for all the characterizations is the one presented in Fig. 3-22, which consists of 10 µm long anode and cathode that are placed 7 µm apart, with 1.1 µm wide gate on each side of the anode.

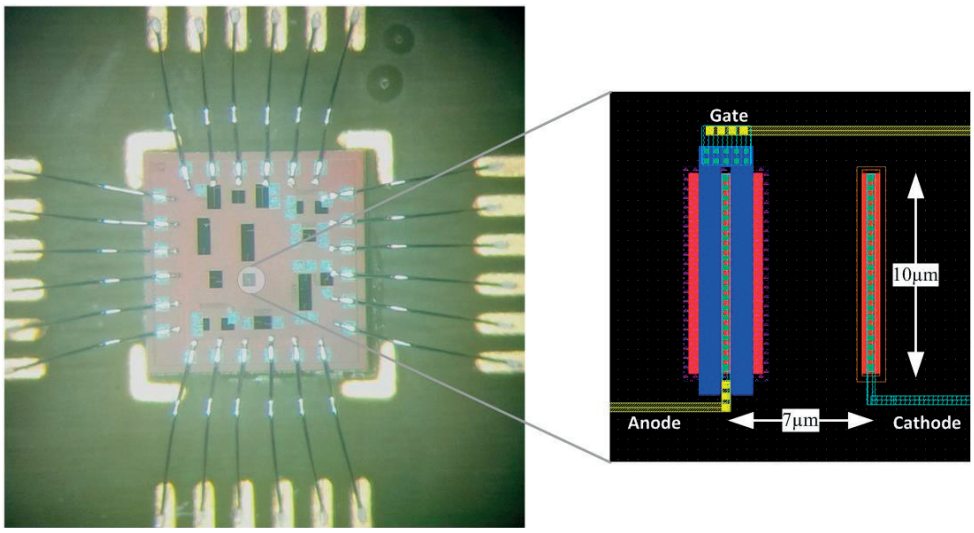

Fig. 3-22: Picture of a wire-bonded chip and layout example of the device

Several different device geometries were implemented, with different distances between anode and cathode as well as some circular geometries.

3.5 Complete measurement system

The aforementioned driver and front end circuits are part of a complete measurement system which is able to send the required signals to the device under test as well as measure the triggering time of the photodetector. The measurement system is connected via USB to a computer and uses this link to receive commands and send back measurement results.

The central component of the measurement system is an ARM-based STM32F4 microcontroller (MCU) with a clock frequency at 84MHz. This MCU drives the DACs that generate the anode, cathode, and gate voltages as well as programmable resistors that tune current references for the anode compensation current and bias of the front end circuit (section 3.2). Fig. 3-23 presents a simplified schematic of the measurement system with the principal components

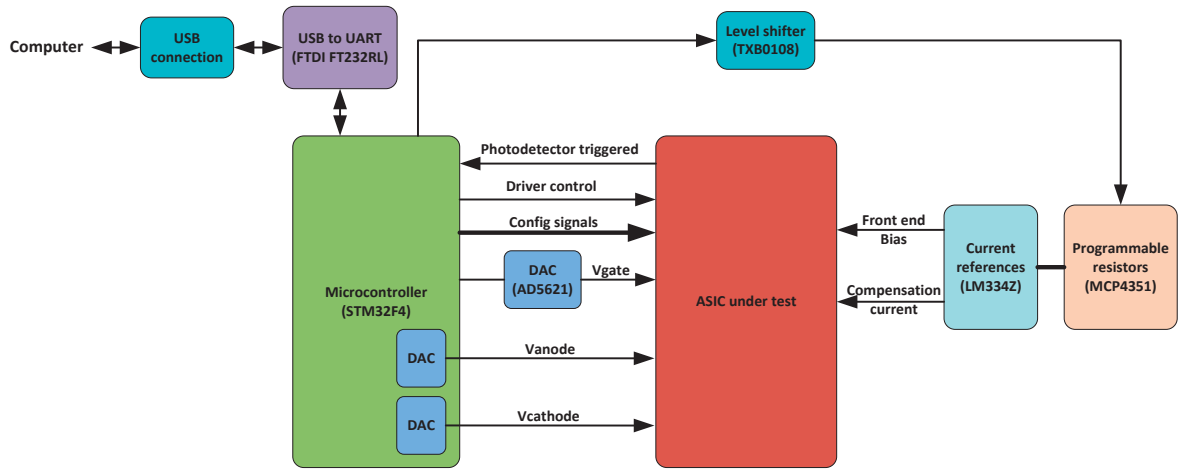

Fig. 3-23: Concept of the complete measurement system

The system was fabricated on a double-layer printed circuit board (PCB). Power is supplied through USB and linear regulators provide 1.8 V and 3.3 V stabilized voltages. Coaxial cable connectors are present in order to output signals to an oscilloscope for precise

characterization of the hybrid MOS-PN photodetector. The circuit is also designed with provisions for a proximity sensing demonstrator (Fig. 3-24). The size of the PCB is 130.8mm x 47mm (5150mil x 1850mil) and the minimum track width and clearance is 150µm.

The chip with driver and front end circuits as well as photodetectors is wire-bonded on a small removable PCB, which allows for the characterization of multiple devices. The size of the removable PCB is 21.1mm x 21.1mm (830mil x 830mil). The design of the small PCB can be modified in order to accommodate the different versions of the chip without modifying the whole system.

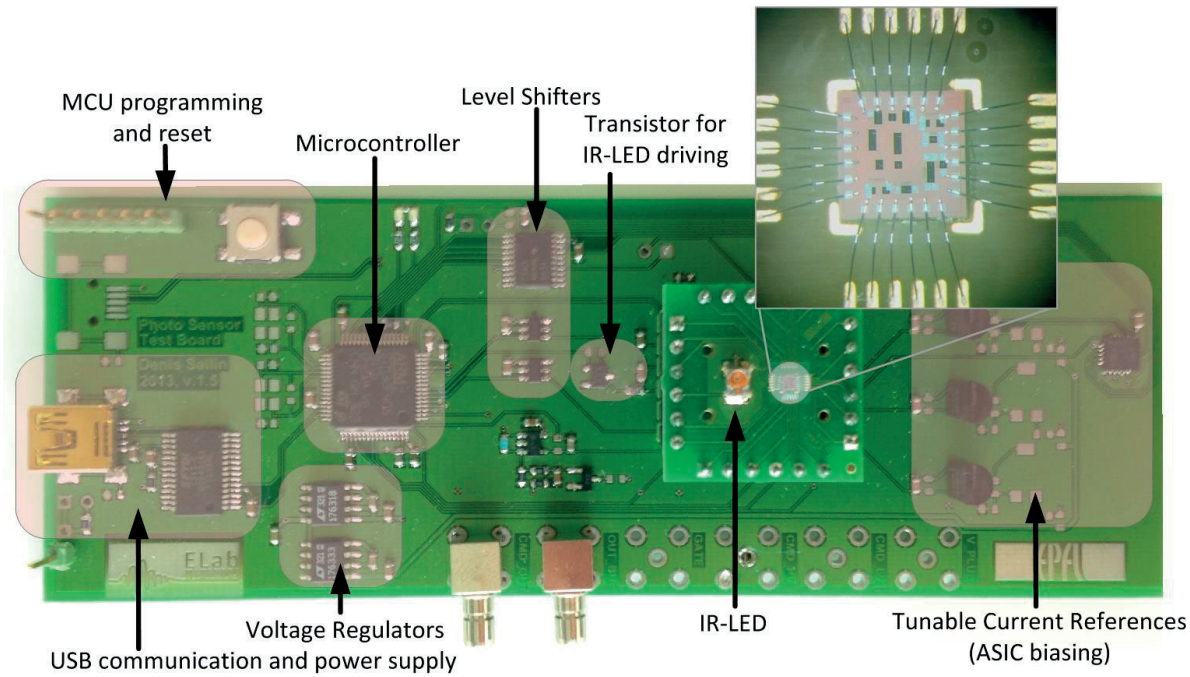

Fig. 3-24: Picture of the detection system PCB

The system uses a FTDI USB-to-UART converter chip to communicate via USB with the computer. The selected MCU also implements a native USB2 controller, but it was chosen not to use it because of the needed development time and because the high performances of the USB2 were not needed in this application. Instead, the FTDI chip emulates an RS-232 serial port on the computer and allows commands to be transmitted over a virtual COM port. A small communication protocol was developed in order to send configuration commands to the measurement system and to get light measurement results.

3.6 Experimental Study

The driver and front end circuit presented in section 3.2 was used to characterize the behavior of the Hybrid MOS-PN device for different biasing conditions and in function of light intensity [69]. The device used for all the following measurements is the one shown in Fig. 3-22. Unless otherwise specified, the light source is a Thorlabs S1FC635 fiber coupled laser with a wavelength of 635nm. The oscilloscope used for measurements is an Agilent MSO6034A.

3.6.1 Effect of cathode voltage

It was presented in section 2.1.3 that cathode leakage is responsible for the majority of dark current. This is due to the small potential barrier between cathode and substrate. This barrier can be increased by biasing the cathode to a positive voltage with respect to the substrate.

Measurements in darkness are presented in Fig. 3-25 and show that the triggering time, and therefore dark current, depends exponentially on cathode voltage. An increase of 100mV in cathode voltage translates into an increase of more than one order of magnitude in self-triggering time. Those measurements also show that the higher the gate voltage (V_g), the longer the triggering time. This is because the number the accumulated carriers needed to trigger the device increases with gate voltage.

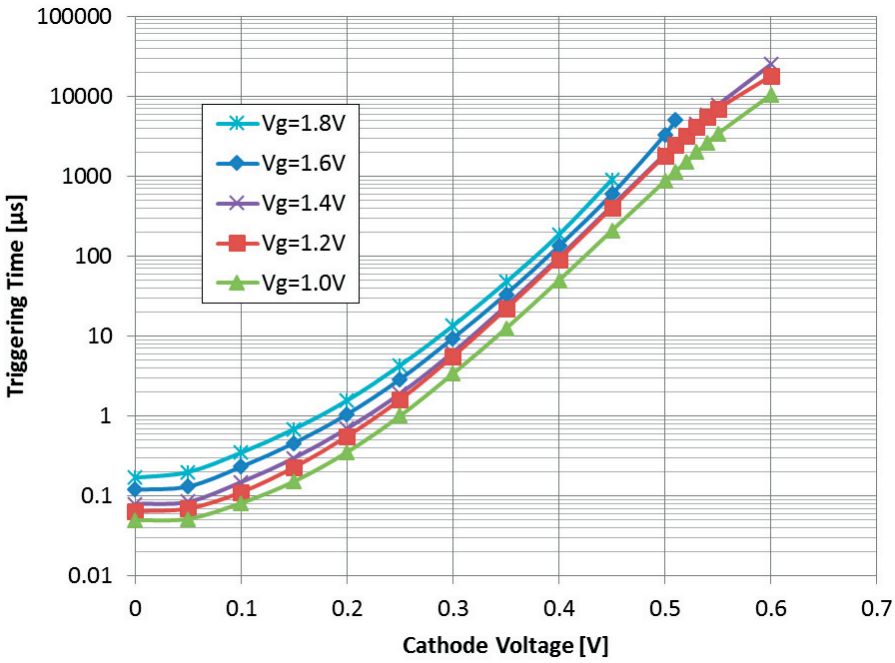

Fig. 3-25: Measurement of the effect of cathode voltage on self-triggering time for different gate voltages. Van=1V.

Measurement of the inverse of triggering time versus light intensity for different cathode voltages (Fig. 3-26) shows that the slope of the characteristic does not change with cathode voltage. This means that varying cathode voltage only acts on dark current, but neither on the amount of carriers needed to trigger the device, nor on the active area.

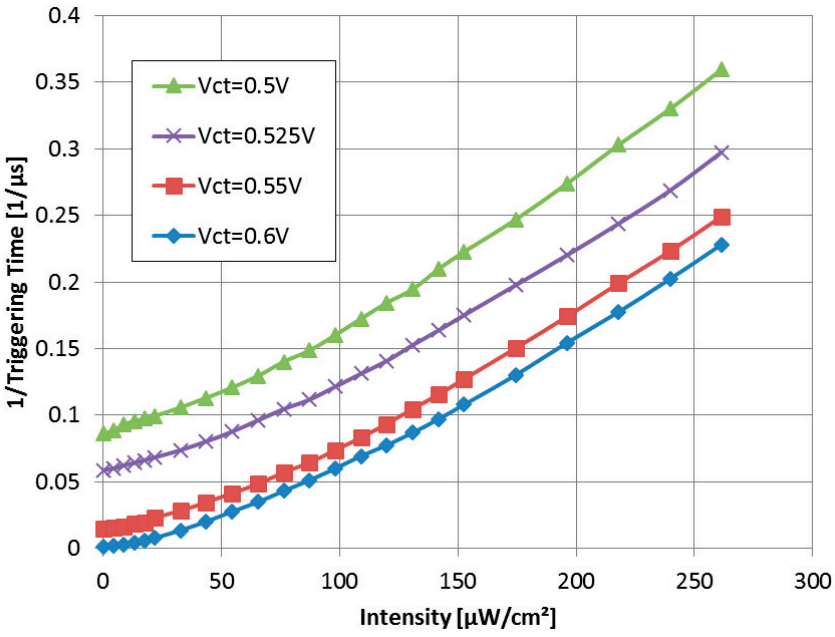

Fig. 3-26: Measurement of the effect of light on triggering time for different cathode voltages. Van=1V, Vg=1.2V

Basically, the cathode voltage acts on the potential barrier of the cathode. Under the assumption that triggering of the device is solely due to cathode leakage and that the behavior of the leakage current corresponds to the one of a forward biased PN junction, it is clear that the variation of triggering time with respect to cathode voltage should be exponential.

$$T_{trig} = \frac{q \cdot N_{tot}}{I_{leak}} = \frac{q \cdot N_{tot}}{I_s} \exp\left(-\frac{V_F}{n \cdot U_t}\right) = \frac{q \cdot N_{tot}}{I_s} \exp\left(\frac{V_{ct} - V_p}{n \cdot U_t}\right) \; [s] \tag{3-5}$$

It is difficult to determine the actual value of V_F. It of course depends on cathode voltage, but also on the potential drop across the depletion region as well as on the position of the ground anchor and substrate doping. Fig. 3-27 shows a trend line for the region where the characteristic is truly exponential.

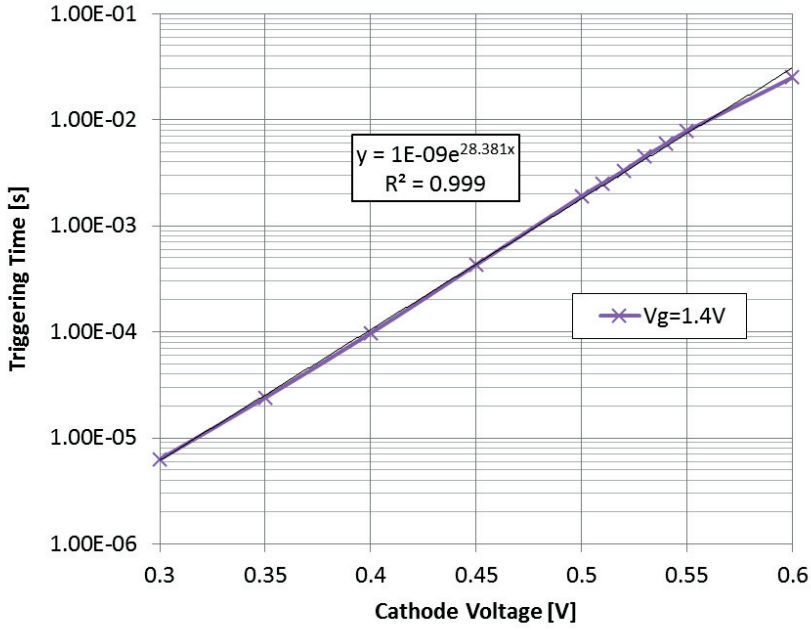

Fig. 3-27: Exponential fitting of the self-triggering time versus cathode voltage measurement

The fact that the variation in triggering time is indeed due to the forward voltage of the diode structure is confirmed by measuring the variation in triggering time due to the anode voltage (Fig. 3-28). Here, the relation is more complicated because the anode voltage acts on both the leakage current and the size of the accumulator. However, the exponential component dominates.

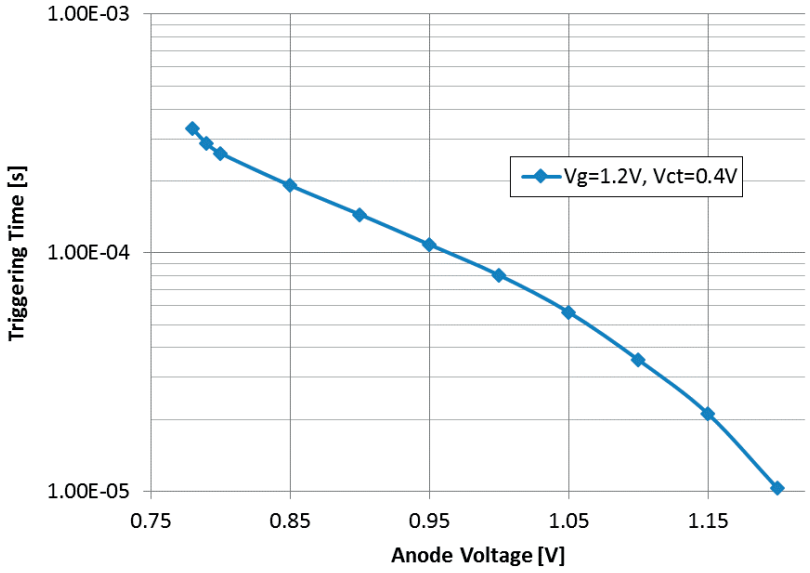

Fig. 3-28: Measurement of the effect of anode voltage on self-triggering time. Vg=1.2V, Vct=0.4V.

3.6.2 Effect of gate voltage

It was presented in section 2.1.5 that sensitivity of the device can be tuned by changing the gate voltage. By increasing the voltage at the gate, the depletion region deepens, the anode is better isolated, and the amount of charges needed to trigger the conduction is higher. Here also, the impact on the self-triggering time, shown in Fig. 3-29, is significant. Note that approximately below 1 V, the triggering time decreases dramatically. This can be considered as the minimum gate voltage for which the anode can be engulfed by the depletion region and the forward-biased PN diode blocked.

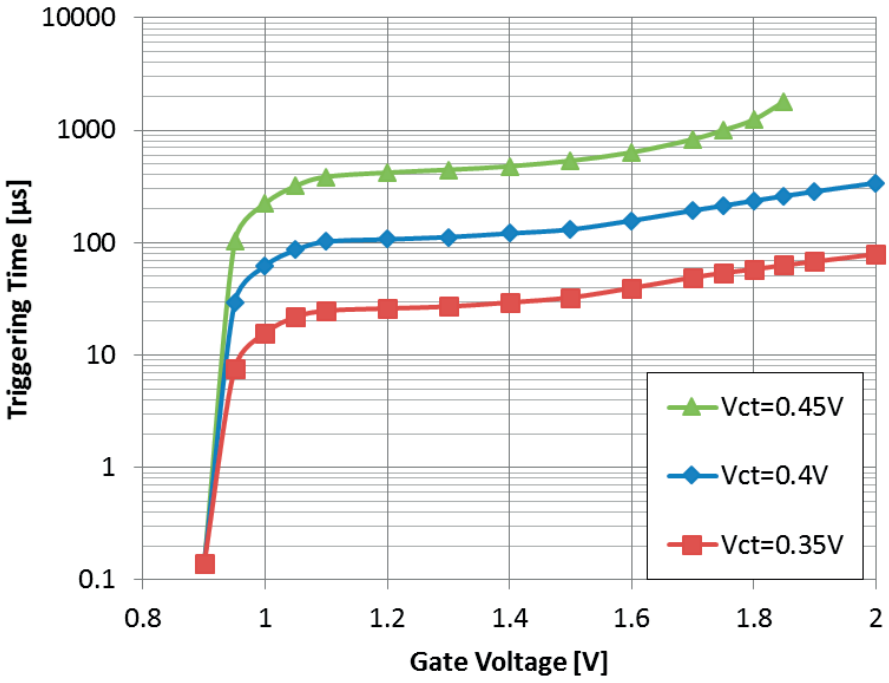

Fig. 3-29: Measurement of the effect of gate voltage on self-triggering time for different cathode voltages. Van=1V.

In Fig. 3-30, the characteristic of self-triggering time versus gate voltage is plotted on a linear scale. In the voltage region where the depletion region is deep enough to efficiently isolate the anode (V_g > 1.1 V), it can be analyzed that the relation seems to be quadratic with respect to voltage. It means that the amount of carriers needed for the device to trigger increases quadratically with gate voltage. One hypothesis that can be put forward to explain this behavior is that a higher gate voltage not only increases N_{tot}, but also decreases the leakage current by improving the isolation of the anode. Indeed, a more resistive path between the anode and the substrate leads to fewer holes injected into the substrate and, in consequence, a lower potential on the cathode side which leads to a smaller dark current. Both effects, higher N_{tot} and smaller i_{leak} occur at the same time, leading to a quadratic behavior.

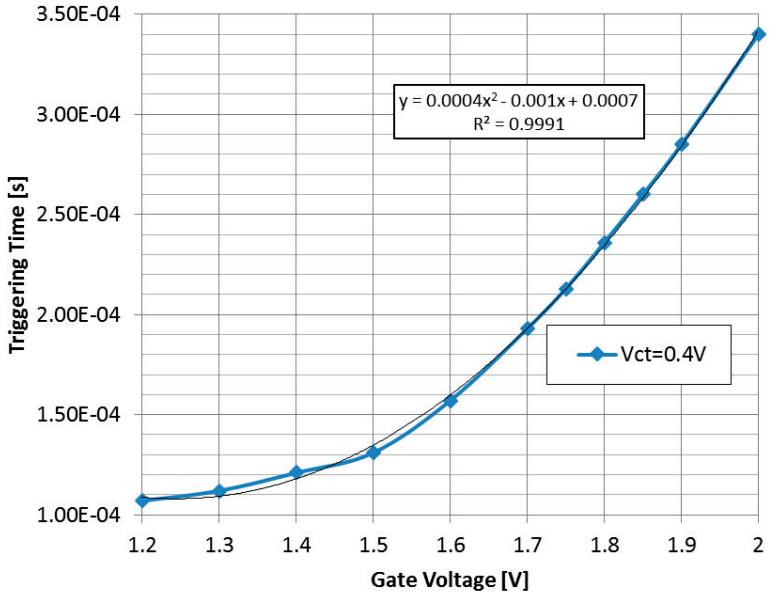

Fig. 3-30: Quadratic fitting of the self-triggering time versus gate voltage measurement

The variation of the number of charges needed to trigger the device with respect to V_g is easily seen when light is applied onto the photodetector. The higher number of carriers needed to trigger the device translates into a less steep slope of the inverse of triggering time versus light intensity (Fig. 3-31). In other terms, the sensitivity (as defined in section 2.2.2) decreases with higher gate voltages.

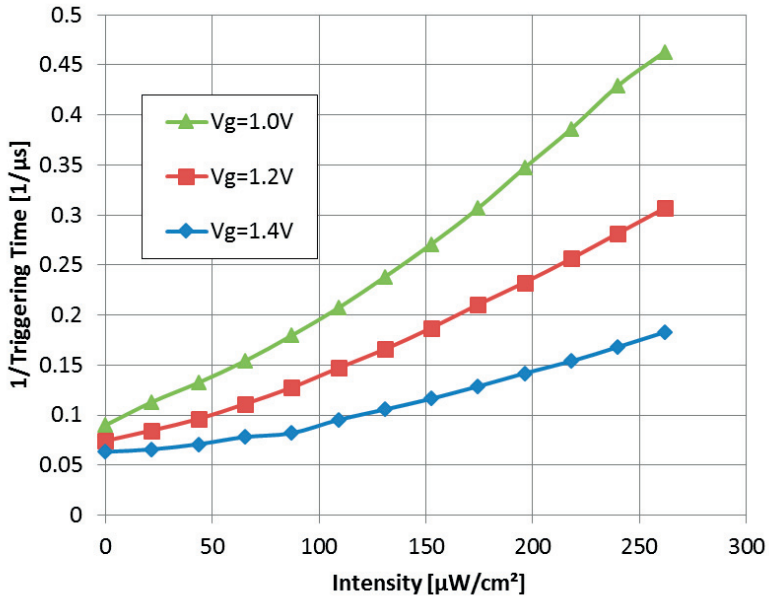

Fig. 3-31: Measurement of the effect of light on triggering time for different gate voltages. Van=1V, Vct=0.525V

From Fig. 3-26 and Fig. 3-31, it is clear that the behavior of the device is non-linear with light intensity. Moreover, its sensitivity seems to increase with high light intensities. This is not in agreement with the TCAD simulations presented in section 2.1.5, in which the sensitivity decreases for high intensities. One hypothesis that can be put forward to explain those discrepancies is that recombination current due to traps at the interfaces is not taken into account in the simulation. Nevertheless, in real life, this current can be non-negligible, especially for low intensities, due to the STI isolation for which the interface is not expected to be clean and smooth. Indeed, in standard CMOS circuits, no current is supposed to flow and no carriers are supposed to be accumulated under the STI and

its interface is thus not designed to be of very good quality. However, in our case, electrons indeed flow around the STI and can even be accumulated under it.

3.6.3 Noise Measurements

One way to confirm the findings presented under sections 3.6.1 and 3.6.2 is to analyze the noise characteristics of the measurements. It was shown in section 2.1.7 that, in the ideal case, the noise of the device is only due to shot noise. In that condition, the variance of the total amount of carriers (N_{tot}) is equal to N_{tot} (E(X) = Var(X)).

In practice, the noise translates into variations of triggering time from one measurement to another. The oscilloscope used for timing measurements features statistical functions that allow to evaluate the standard deviation of triggering time over many measurement samples. Under the assumption that shot noise is the dominant noise source, N_{tot} can be evaluated from noise measurements.

$$\frac{T_{trig}}{\sigma_{T_{trig}}} = \frac{N_{tot}}{\sigma_{N_{tot}}} = \frac{N_{tot}}{\sqrt{N_{tot}}} = \sqrt{N_{tot}} \tag{3-6}$$

Under the assumption that the noise of the entire system is dominated by shot noise, the fact that N_{tot} does not depend on cathode voltage (section 3.6.1) should translate into a nearly constant T_{trig}/σ_{Ttrig} ratio independent of V_{ct}. Fig. 3-32 confirms it by showing a nearly constant ratio.

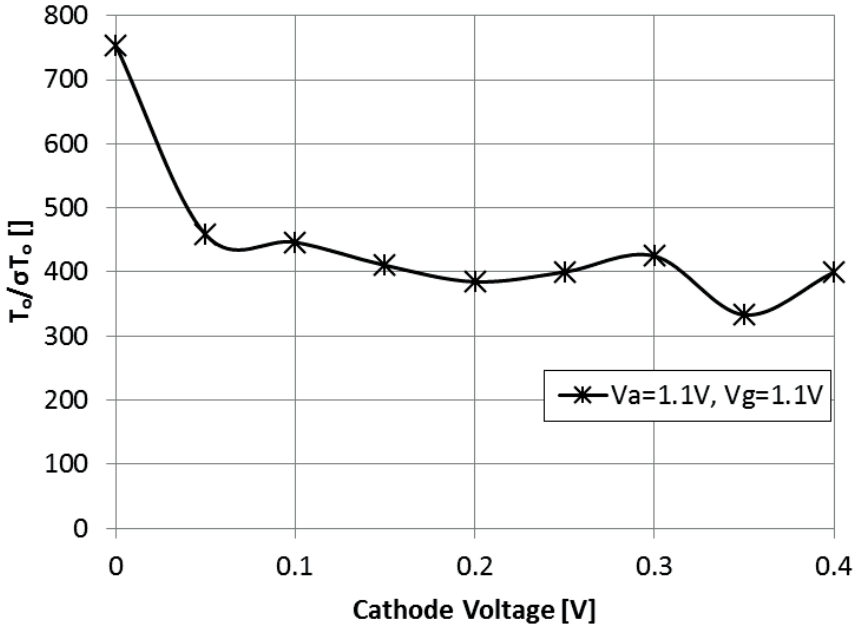

Fig. 3-32: Measurement of the effect of cathode voltage on relative triggering noise

The same reasoning, the evaluation of T_{trig}/σ_{Ttrig} when varying V_g should show an increase in the ratio for larger gate voltages. Indeed, it was shown in section 3.6.2 that N_{tot} directly depends on V_g. This is confirmed by Fig. 3-33.

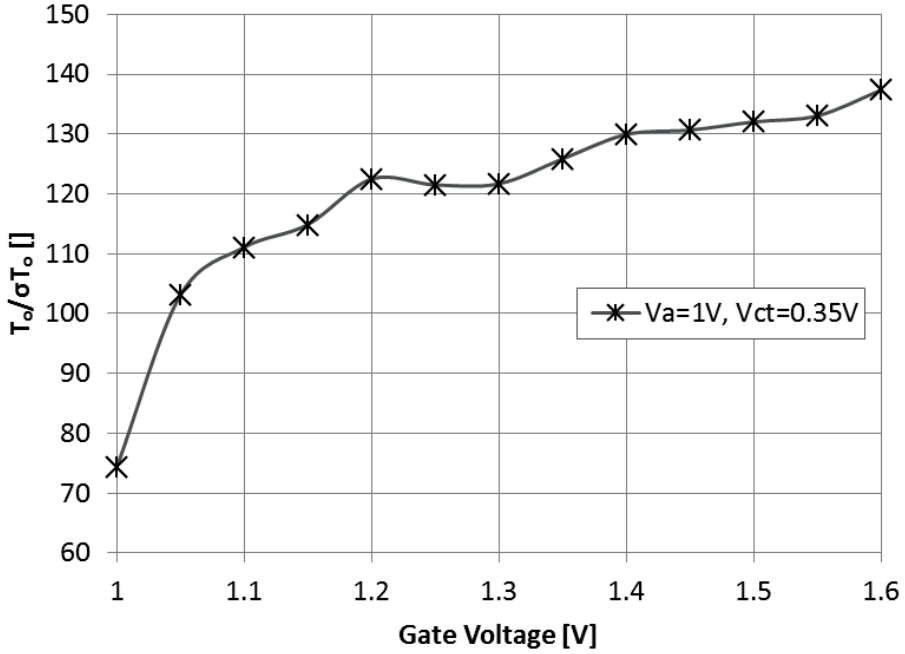

Fig. 3-33: Measurement of the effect of gate voltage on relative triggering noise

Under the assumption that the total noise of the system is only due to shot noise, squaring the T_{trig}/σ_{Ttrig} ratio yields the N_{tot}. In practice, many other noise sources add to shot noise, but evaluating $(T_{trig}/\sigma_{Ttrig})^2$ gives some hints about the evolution of N_{tot} with gate voltage. Fig. 3-34 presents this evolution, and shows that it is more or less linear for $V_g > 1.1V$. Comparing it with the quadratic behavior of triggering time versus gate voltage (Fig. 3-30) confirms the hypothesis that V_g not only acts on N_{tot}, but also on I_{leak}.

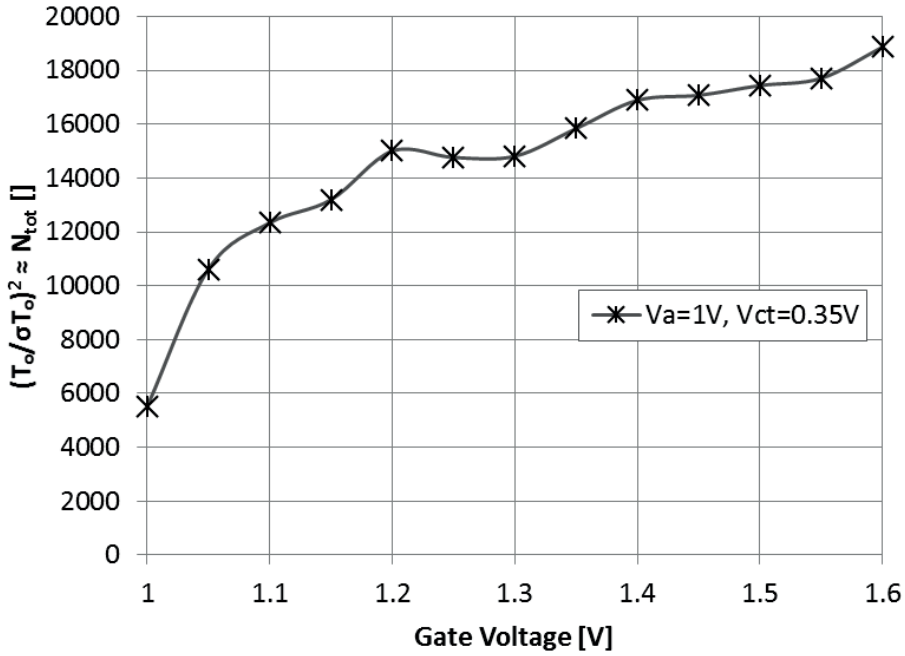

Fig. 3-34: Evaluation of the total amount of accumulated carriers needed for triggering versus gate voltage

Evaluating the T_{trig}/σ_{Ttrig} ratio with respect to anode voltage (V_a) confirms that this voltage not only acts on leakage current (i_{leak}), but also on the number of carriers needed to trigger the device (N_{tot}). Fig. 3-35 shows that the T_{trig}/σ_{Ttrig} ratio decreases when V_a increases, confirming the results presented in 3.6.1.

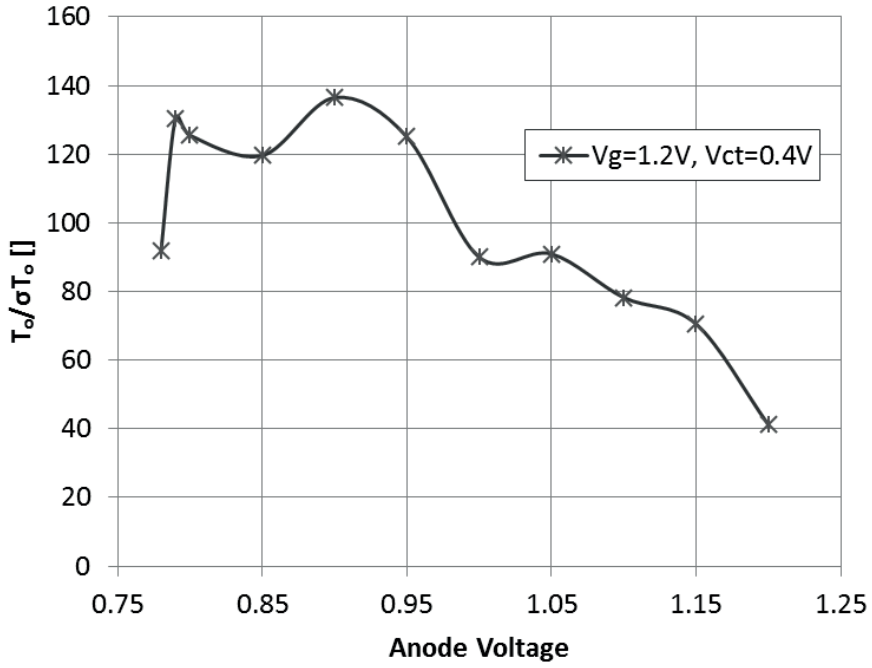

Fig. 3-35: Measurement of the effect of anode voltage on relative triggering noise

3.6.4 Spectral response

It is interesting to measure the response of the sensor with respect to the wavelength of incident light. Under the assumption that the response of the photodetector is linear, a value proportional to the quantum efficiency of the device can be obtained by normalizing the triggering time with respect to the number of incident photons per second per cm² (n_{ph}.[$s^{-1}cm^{-2}$]).

$$QE \propto \frac{\frac{1}{T_{trig}}-\frac{1}{T_0}}{n_{ph}} = \frac{\left(\frac{1}{T_{trig}}-\frac{1}{T_0}\right)\cdot hc}{I_{light}\cdot\lambda} \; [] \tag{3-7}$$

Measurements were performed by placing a monochromator having a bandwidth of 10nm in front of a “white” light source. Light intensity was measured by the use of a beam-splitter and a calibrated photodiode. Results are presented in Fig. 3-36.

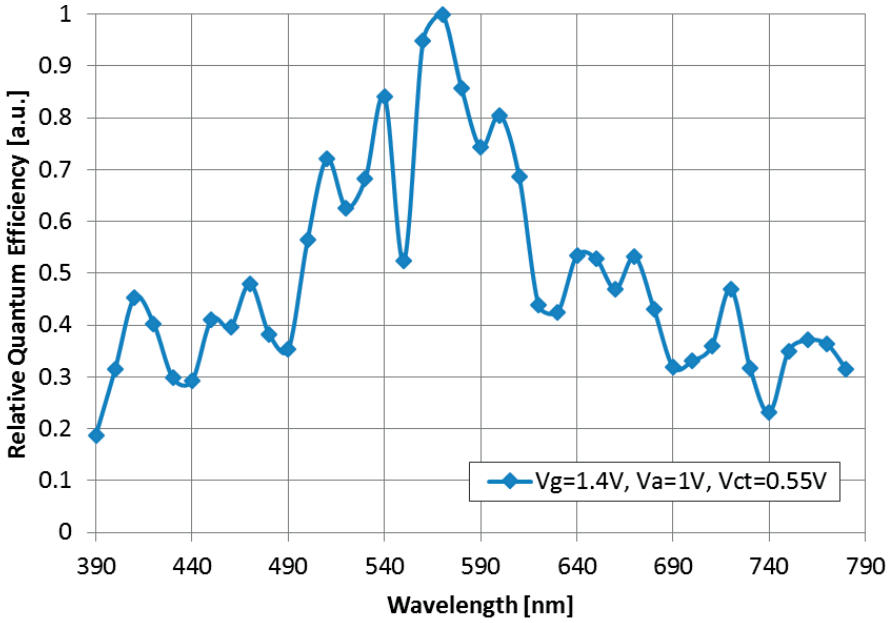

Fig. 3-36: Measurement of the spectral response of the photodetector

The analysis of those measurements puts forward some interesting features. First, the characteristic is not monotonous but there is ripple in the quantum efficiency with respect to wavelength. This is due to interference in the metal stack as well as in the gate stack and shallow trench isolation. Second, a degradation of the efficiency is observed for short as well as for long wavelengths, with a peak efficiency around 560nm.

The degradation for long wavelengths can be explained by the diminution of the absorption coefficient of silicon for longer wavelengths, leading to a deeper absorption of the photons. Fig. 3-37 presents the absorption depth according to Beer-Lambert law with respect to wavelength. For wavelengths above 600nm, a sizable portion of the photons may be absorbed outside the depletion region, entailing a diminution in efficiency.

For short wavelengths, the absorption depth becomes very shallow, and a sizable proportion of photons are absorbed in the polysilicon gate without reaching the active area. On the UMC 0.18µm CMOS technology, the gate-polysilicon thickness is 200nm. Fig. 3-37 shows that such a thickness is sufficient for it to become quite absorptive for wavelengths shorter than 500nm. More details about polysilicon absorption and how to avoid it are presented in section 4.4.5.

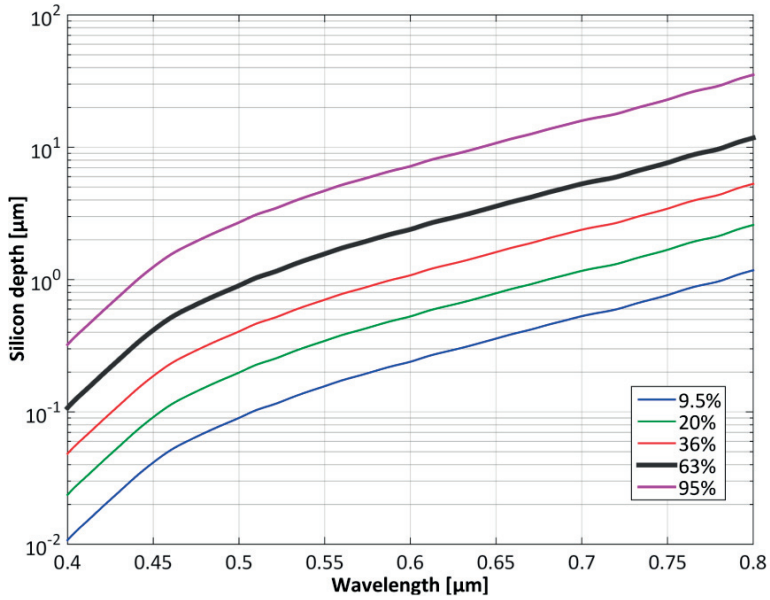

Fig. 3-37: Simulated photon absorption depth in silicon with respect to wavelength

3.6.5 Impact of reset duration

After each detection, the device needs to be resetted in order to evacuate the accumulated charges under the gate and at the forward-biased junction. This process, however, is not instantaneous and the quality of the reset depends on the duration of the reset phase [76]. This is partly due to the well-known problem of diode reverse recovery [11]. If the PN-junction is not reverse-biased for a long-enough time after having conducted, excess majority carriers at the junction are not completely evacuated, lowering the potential barrier on the cathode-side and increasing leakage current for the next detection. The other carriers that need to be evacuated during reset are the minority carriers under the gate, on the anode-side.

Fig. 3-38 presents measurements of the self-triggering time with respect to reset time. The relation between reset time and self-triggering time seems to fit a logarithmic function. This hints that, during reset, accumulated carriers under the gate are in fact not evacuated but slowly recombine when the gate voltage is put to zero with a minority carrier lifetime τ. In that case, self-triggering time would be due to residual carriers under the gate, reducing the number of carriers to be accumulated before triggering.

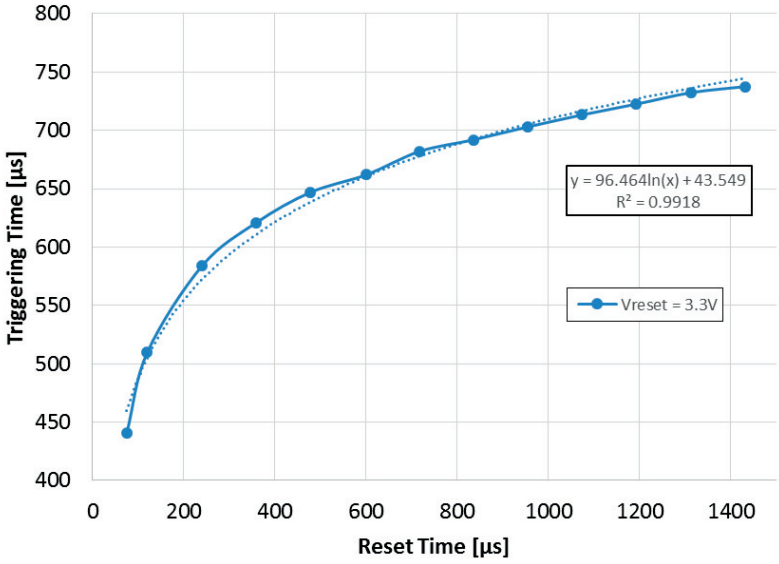

Fig. 3-38: Measurement of the effect of reset rime on self-triggering time (with logarithmic fitting)

The aforementioned hypothesis is confirmed by the measurement of the inverse of triggering time versus light intensity for different reset-phase durations. Fig. 3-39 shows that varying the reset time does not significantly change the leakage current but instead acts on the sensitivity of the device, which depends on the amount of carriers that need to be accumulated before the device triggers.

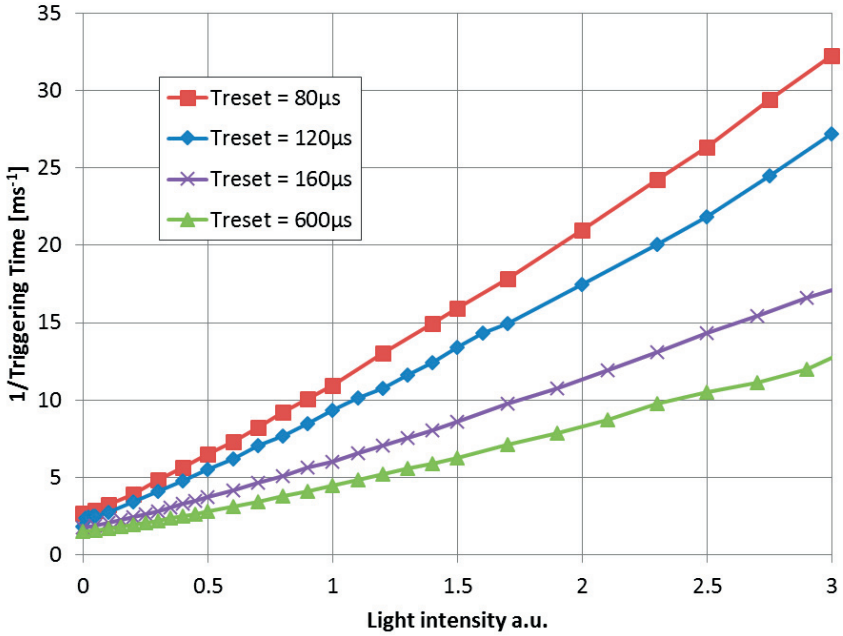

Fig. 3-39: Measurement of the effect of light on triggering time for different reset times. Vg,=1.2V, Van=1V, Vct=0.525V.

The equation of the device can thus be rewritten by taking in account the residual carriers $N_{residual}$, which depends on reset duration.

$$\frac{1}{T_{trig}} = \frac{(i_{phot}+i_{dark})}{q\cdot(N_{tot}-N_{residual})} \tag{3-8}$$

According to those findings, it seems that the reset strategy used until now is not the most efficient one. For now, gate and anode voltages are put to 0V during the reset phase, while cathode voltage is put to a positive reset voltage. Consequently, most of the accumulated carriers stay in the bulk near the anode and wait for recombination, which takes time in a low doped substrate. It may be possible to speed-up the reset process by keeping the anode voltage positive after putting the gate voltage to 0V. In that case, minority carriers would drift towards the anode and be quickly recombined in the highly-doped p+ diffusion.

3.6.6 Effect of pulsed operation

It was presented in section 2.2.3 that the performances of the device in terms of dark current and power consumption can be improved by pulsing the anode voltage during light sensing. In practice, this is realized by slightly modifying the circuit in order to drive the anode and the cathode independently [74]. Fig. 3-40 presents the operation of the driver circuit in pulsed mode.

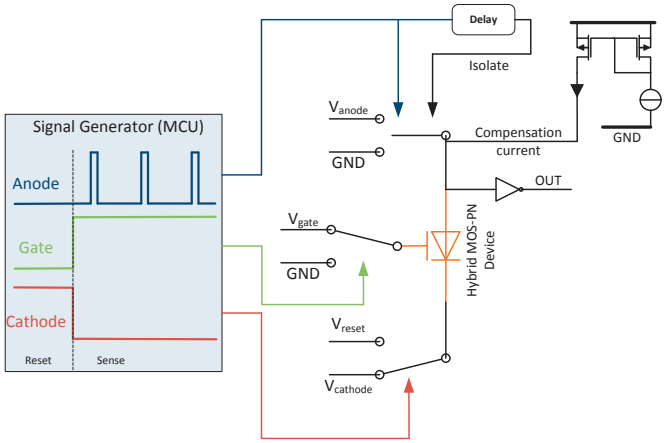

Fig. 3-40: Pulsed operation of the driver circuit

The measured triggering time versus light intensity is presented in Fig. 3-41. For comparison, both the results for pulsed operation and non-pulsed operation are illustrated. The performance improvement is obvious, with an increase of triggering time for a given light intensity of more than two orders of magnitude, principally due to the diminution in dark current.

However, the linearity is not as high as in the TCAD simulations and, in practice, is worse than the one with normal operation. The causes of the non-linearity are multiple. Some of them are rooted in the circuit, with the injection of the leakage compensation current, whose goal is to stabilize the anode voltage for long triggering times. This stabilization is, however, not instantaneous and introduces a non-linearity when the pulse duration is short. Another source of non-linearity is rooted in the operation of the device itself. As explained in section 2.2.3, pulsed operation increases minority carrier recombination due to the pulsed anode in the middle of the depletion layer. However, the amount of recombined carriers at each voltage pulse might not be constant, and might depend on the amount of already accumulated carriers, introducing non-linearity. Another source of non-linearity, common to both operation modes, may be recombination due to traps at the interface between silicon and STI, as explained in section 3.6.2.

Higher recombination current in pulsed operation also increases the noise level, and introduces quantization noise due to the discrete nature of the operation (section 2.2.3).

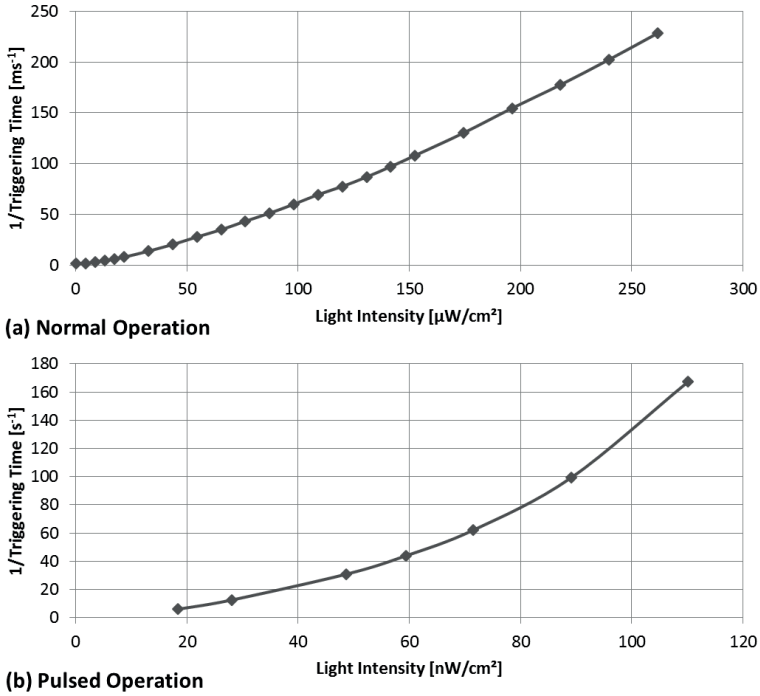

Fig. 3-41: Measured triggering time versus light intensity for DC (a) and pulsed (b) operation. V_{anode}= 1V, $V_{cathode}$=0.6V, V_{gate}=1.2V.

In order to improve the performance of the system, especially in terms of recombination and linearity, it might be interesting to pulse the cathode voltage instead of the anode voltage. This would greatly reduce recombination in the depletion layer. However, in that case, the hole-leakage current through the depletion layer from the anode to ground would still be present, increasing the power consumption of the detector.

3.7 Summary

This chapter presented both the circuit design of the detection system as well as a characterization of the Hybrid MOS-PN photodetector using the said detection circuit.

The general principle of the detection system is to measure the (dis)charge of the parasitic capacitance of a high-impedance node when the device triggers. The design challenge is to minimize the parasitic capacitance while having a fast and efficient detection. Several circuits with different detection strategies were designed and co-integrated with the sensors on standard CMOS technologies. The complete measurement system consists of a printed circuit board with a microcontroller sending signals to the chip and communicating with a computer via USB.

Characterization of the device using the measurement system confirmed that sensitivity of the device depends on gate voltage, and that the leakage component of the dark current strongly depends on the forward voltage of the PN structure.

Pulsed operation of the device was performed, and performance improvements in terms of dark current were confirmed.

Characterization of the device with respect to the wavelength of incident light showed a dropped in efficiency for short wavelengths, certainly due to polysilicon absorption, as well as for long wavelengths, due to the deeper absorption of the photons.

Analysis of the impact of reset duration showed that a too short reset time does not introduce leakage, but residual carriers staying under the gate for the next detection phase.

Chapter 4 Prospective technological solutions

This chapter explores some technological solutions that can potentially address some limitations of the Hybrid MOS-PN device that were presented in the previous chapters.

4.1 Multi-gate implementation

It was presented in chapters 2 and 3 that the amount of carriers needed for the device to trigger (N_{tot}), and thus sensitivity, is controlled by gate voltage. However, it was also shown that the tunable range is limited to about a factor two, which is not very interesting if one want to use this feature to tune the sensitivity for high dynamic range measurements.

A solution that could be implemented to increase the tunability is to build a device with multiple gates that can be turned on and off in an onion ring manner. The size of the depletion region can thus be controlled. The more gates are turned on, the larger N_{tot}.

On a standard CMOS process, such a structure must be built as a series of transistors, or a transistor with multiple fingers. Consequently, gates are separated from one another with a floating P+ diffusion. The multi-gate implementation only works under the assumption that electrons are free to move in the whole depletion region and that the whole accumulated charge averages out over the entire gate area. For this to be valid, the floating P+ diffusions must be small enough so that electrons can cross it with a low probability of recombination in the high doping region. On a standard 180nm CMOS, such small diffusions are 200-300nm wide, which is small enough for electrons to pass through with a low recombination probability. Fig. 4-1 presents such a structure.

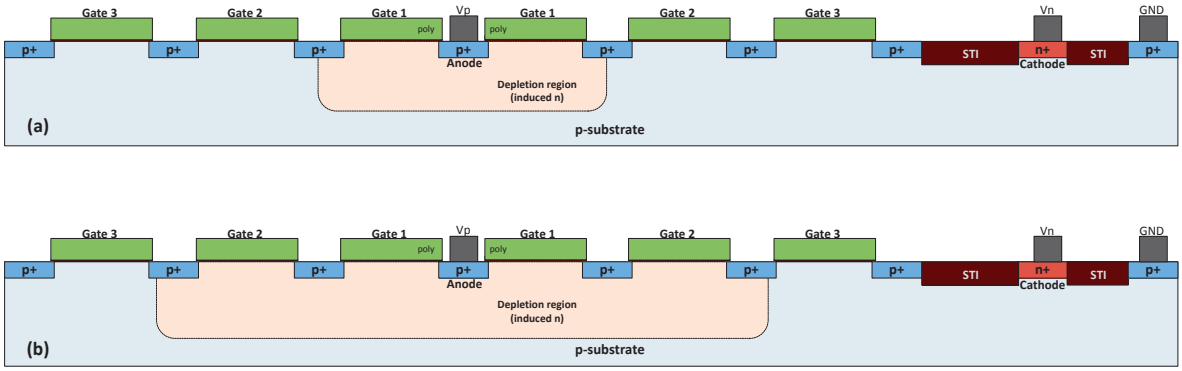

Fig. 4-1: Structure of the multi-gate device with one activated gate (a) and two activated gates (b)

4.2 Ambient light cancellation

In many applications, such as for example light curtains, proximity sensing, or heart-rate monitoring, a small signal variation must be detected on top of a large constant ambient light signal that can be up to 4 or 5 orders of magnitude stronger. This introduces a detection challenge in keeping the input-stage of the detection chain unsaturated while having a sufficiently high gain to detect the signal. In order to avoid this problem, detections systems usually try to cancel the ambient light component before amplification, by the use of a high-pass filter [77] or by subtracting the ambient light photocurrent [78-80].

Of course, in the case of the Hybrid MOS-PN photodetector, it is not possible to simply filter-out the constant component of the photocurrent. However, it might be possible to subtract charges from the depletion layer by changing a bit the structure of the detector. By adding an n+ diffusion connected to a current source directly in the space-charge region, photocurrent as well as dark-current could be effectively cancelled. By integrating the current source into a control loop, the cancellation current (i_{cancel}) can be

tuned in function of the average triggering time ($T_{trig, avg}$) in order to keep the detector in a state where detection is easy, i.e. a state of relatively long triggering time or low frequency. Fig. 4-2 presents the modification to the device structure and one way of controlling i_{cancel}.

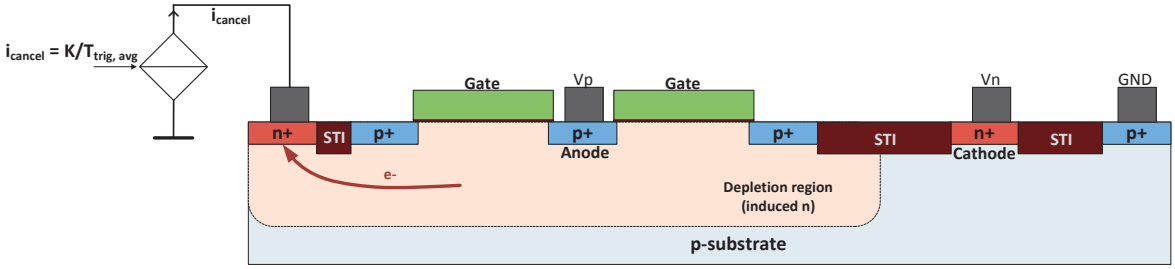

Fig. 4-2: Modified structure of the device with cancellation current

One simple way of implementing the ambient light cancellation control loop is to use the sensor in PFM mode. In that case, the cancellation current is controlled via a PLL (Fig. 4-3). If the low-pass filter of the PLL is designed in such a way that it completely filters out the AC due to the light signal (I_{SIG}), the average frequency of the FM signal at the output of the detector is equal to the reference frequency. Consequently, the relative amplitude of the modulation is increased, the sensor is guaranteed to operate at a favorable frequency ($f_{FM} << 1/T_{reset}$), and the FM demodulator has the information about the center-frequency of the signal at its disposal, allowing for a more efficient demodulation.

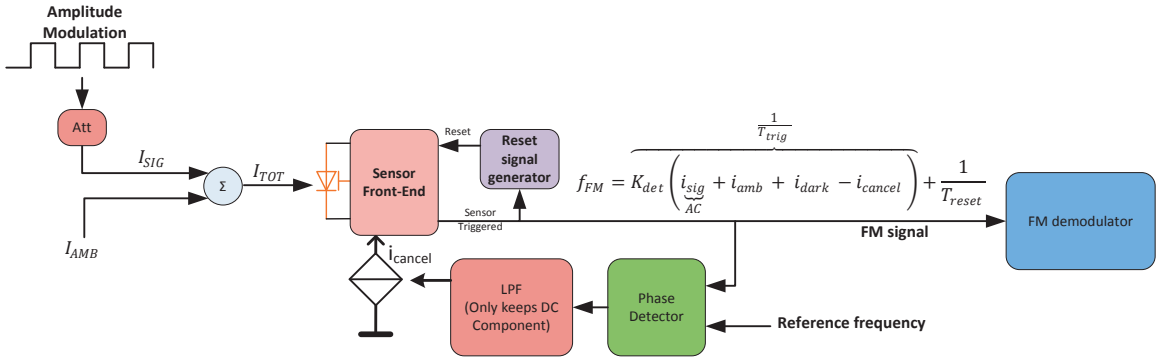

Fig. 4-3: Proposed ambient light and dark current cancellation control loop

Such a system would also provide an automatic temperature compensation, by subtracting the dark current. However, one has to keep in mind that even though such a system would cancel ambient and dark currents, it would not cancel their associated noise. Indeed, the shot noise components associated with the different current still add up, even if the currents cancel-out.

$$\sigma_{tot} = \sqrt{\sigma_{sig}^2 + \sigma_{amb}^2 + \sigma_{dark}^2 + \sigma_{cancel}^2} \tag{4-1}$$

The same kind of control loop can be implemented in time domain, using timing information instead of phase information.

4.3 Triple Well process

Most modern CMOS processes feature a triple well (TWELL) option. It refers to the possibility of having a p-well inside of a so called deep n-well. The advantage of this technique is that the p-well is isolated from the substrate by the deep n-well, and can therefore be biased to a different voltage than ground. This section presents the potential applications and advantages of a triple well process for the Hybrid MOS-PN photodetector.

4.3.1 Device isolation

Theoretically, triple well is a very interesting solution for device isolation. By building the devices in p-wells inside a deep n-well, one could first ensure that there is no crosstalk between devices as well as no substrate noise coupling. Fig. 4-4 presents the concept of triple-well isolation of the devices.

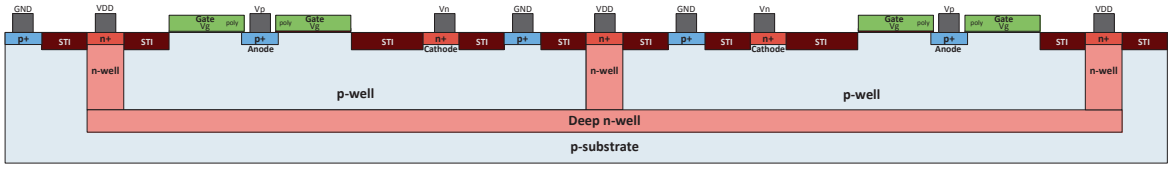

Fig. 4-4: Structure of two devices implemented on a triple-well process

Building the devices in triple wells would also improve their linearity by blocking the diffusion of slow carriers generated away from the depletion region or deeper in the substrate. A good quantum efficiency can be assured even for longer wavelengths of the visible spectrum or near infrared by having a sufficiently deep local p-well.

However, this technique cannot be used in practice with standard CMOS processes due to the doping of the local p-well, which in is in the order of $N_a = 10^{17}$ cm^{-3}. In those conditions, it's impossible to generate a deep enough depletion region to isolate the anode of the detector.

4.3.2 Bulk biasing and isolated circuit

It was showed in previous chapters that in order to limit dark current, the cathode needs to be biased to a slightly positive voltage with respect to the substrate. Usually, the substrate is connected to ground and the cathode is connected to a slightly positive voltage.

A triple well process can be used to bias the whole substrate instead of the cathode. The idea is to put the complete read-out and driving circuitry inside a triple well and keep the devices in the substrate. The circuit would thus be isolated from the substrate, which could then be biased to a negative voltage while keeping the cathode connected to ground.

Another advantage of having the circuit isolated in a triple well is avoidance of parasitic coupling through the substrate that could add noise to the detection. This is especially useful in our case, where the read-out and subsequent circuits are of digital nature, with fast switching and current peaks.

4.4 Silicon-on-Insulator

Chapters 2 and 3 presented some limitations of the Hybrid MOS-PN photodetector. The main non-ideal effects are cathode leakage due to poor electrostatic control of the substrate and non-linearity with respect to light intensity due to slow carriers generated in the substrate.

Silicon-on-Insulator (SOI) technology can alleviate those issues [81]. It is shown in this chapter that adding a buried oxide (BOX) to the device structure has many positive effects in terms of electrostatics and linearity with respect to light intensity [82]. The BOX also introduces interesting optical effects that can be used in certain applications [83].

Some specificities of SOI technology can be advantageously used for device isolation in the context of an array as well as a method to increase quantum efficiency by implementing backside illumination.

The modelling of an equivalent device structure on fully-depleted SOI is proposed in [84].

Unless otherwise specified, all the TCAD simulations whose results are presented in this chapter were performed with a silicon layer depth of 500nm, a BOX thickness of 1µm, and a substrate doping of $N_a=10^{15}$ cm^{-3} (Fig. 4-5).

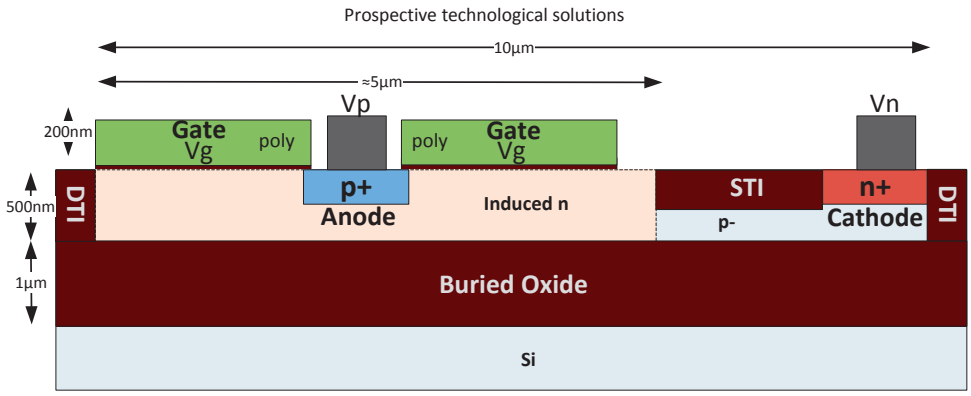

Fig. 4-5: Structure of the SOI-implemented device used in TCAD simulations

4.4.1 Leakage cancellation

It was shown in section 2.1.3 that on standard CMOS implementations, incomplete anode shielding and poor electrostatic control lead to cathode leakage, which accounts for the majority of dark current in the device. On bulk CMOS, it is needed to add a third contact connected to ground and to bias the cathode to a positive voltage in order to create a good enough potential barrier.

On SOI, the addition of an isolating BOX greatly improve the leakage characteristics of the structure. By setting the BOX depth to a few hundreds of nm (500 nm in most of the simulations), the depth of the depletion region created by the gate electric field is constrained by the BOX. There is no room for the formation of a path for holes to the rest of the device. This, in turn, cancels the cathode leakage dark current. In such a structure, the potential of the substrate of the device is no longer fixed by a ground anchor, but with the so called back-gate. By connecting the wafer below the BOX to ground (or any other voltage), the BOX itself acts as a very thick transistor gate, and thus imposes the potential of the device.

The electrical potential across the device is shown in Fig. 4-6. It confirms that the potential well is constrained by the BOX, effectively isolating the anode from the rest of the structure. By comparing those results with the potential barriers of the bulk device presented in Fig. 2-6, it is clear that the quality of the barriers are better in the SOI case, even for a smaller gate voltage. Leakage current is greatly reduced as a consequence.

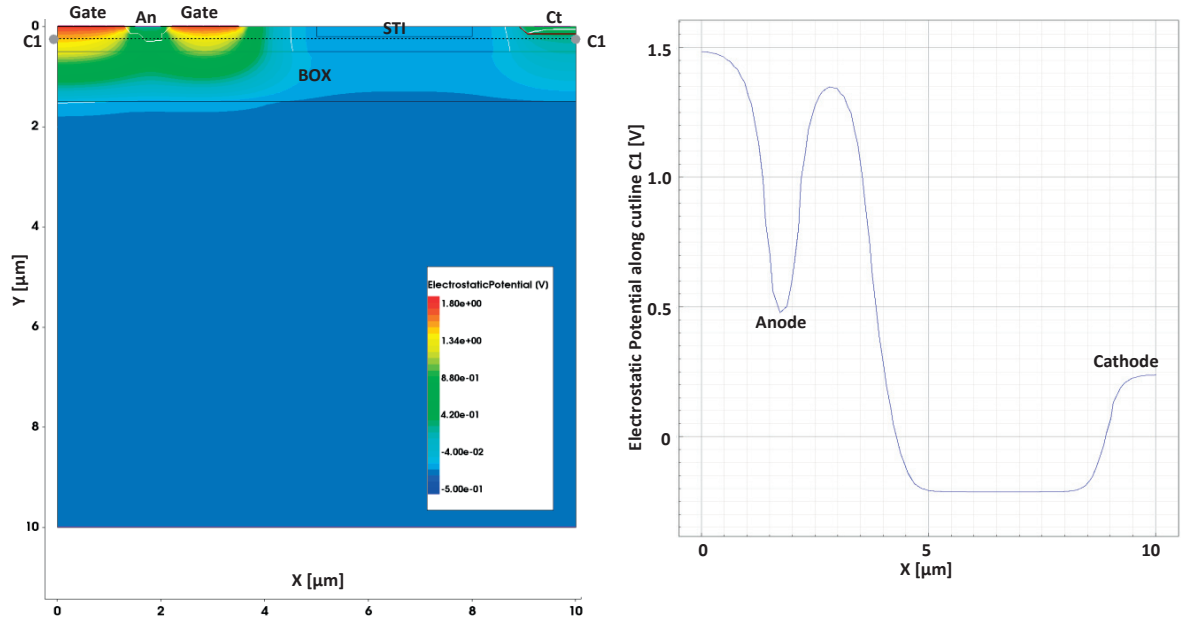

Fig. 4-6: Simulation of the electrostatic potential before triggering in a SOI device a) 2D visualization, b) potential along the line. V_g =1.8V, V_{an} = 0.8V, V_{ct} = 0.1V, V_{bg} = 0V.

TCAD simulations of self-triggering time show that the introduction of the BOX is extremely beneficial, especially for “practical” gate voltages (<2V). For Vg = 1.8V, an increase of self-triggering time by a factor 20 is observed, proving the efficiency of the technique (Fig. 4-7).

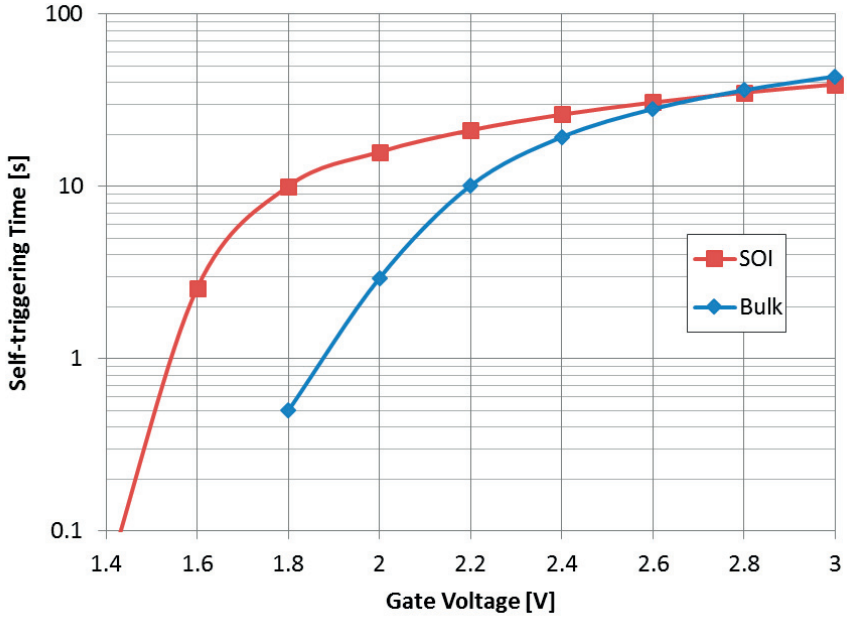

Fig. 4-7: Simulated self-triggering time versus gate voltage for bulk and SOI implementations. Van=0.8V, Vct=0.1V

Of course, the effect of the BOX strongly depends on its depth. Lower gate voltages require a shallower silicon region to achieve the same leakage cancellation. The effect of silicon thickness is illustrated in Fig. 4-8, where a thicker silicon region leads to a shorter self-triggering time. It shows that, in practice and for a substrate doping level of 10^{15} cm^{-3}, silicon thickness should be smaller than about 700nm for the device to be usable. On the other end, shallower silicon regions have disadvantages in terms of light absorption, especially for long wavelengths, as analyzed in section 3.6.4.

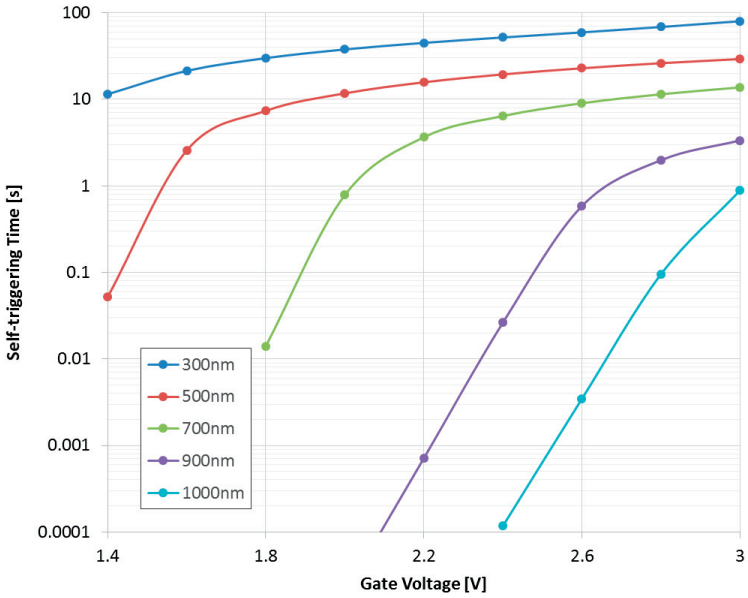

Fig. 4-8: Simulated self-triggering time versus gate voltage for different silicon layer thicknesses V_{an} = 0.7V, V_{ct} = 0V, V_{bg} = 0V.

4.4.2 Effect of back-gate

A feature of SOI technology is that the BOX can behave as a gate oxide with the silicon bulk under being polarized at a voltage different than 0V. Doing so influences the electrostatics of the device and changes its behavior. In particular, it has an effect on i_{dark} and N_{tot}. Fig. 4-9 shows that negative voltage biasing of the back gate can increase self-triggering time (T_0) and that there is an optimum voltage for which the triggering time is maximized, depending on gate voltage.

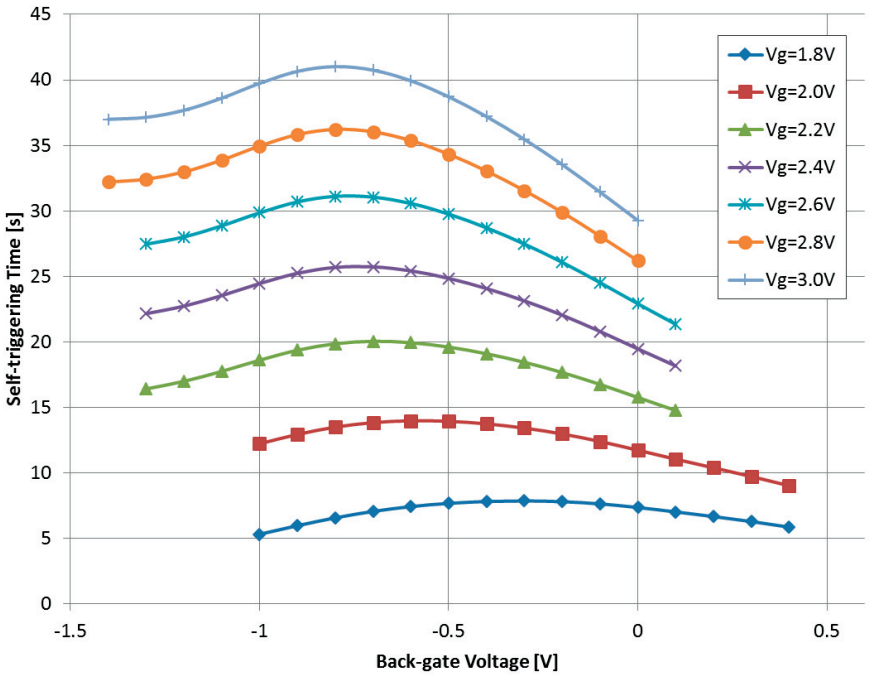

Fig. 4-9: Simulated effect of back-gate voltage on self-triggering time for different gate voltages. Van = 1V, Vct = 0.1V.

By applying light on the device and using the sensitivity formula from section 2.2.2, the total amount of charges necessary to turn the device on (N_{tot}) can be evaluated.

$$S_{PFM} = \left| \frac{d\frac{1}{T_{trig}}}{dI_{light}} \right| = \frac{A \cdot QE_{\lambda} \cdot \lambda}{hc \cdot N_{tot}} \left[\frac{m^2}{J} = \frac{s^2}{kg} \right] \quad (4\text{-}2)$$

N_{tot} can be evaluated under the assumption that the active area doesn't significantly vary with gate voltage (Vg) and that recombination current is negligible. QE is evaluated taking in account the reflection at silicon interface and absorption of photons at λ=500nm in a silicon thickness of 500nm. The derivative was evaluated by calculating the slope for an illumination between 0 and 1e-9 W/cm². What is important here is not the exact value of N_{tot}, but how it varies with Vbg. It is interesting to note that the maximum of N_{tot} does not appear at the same Vbg as the maximum of T_0 (Fig. 4-10).

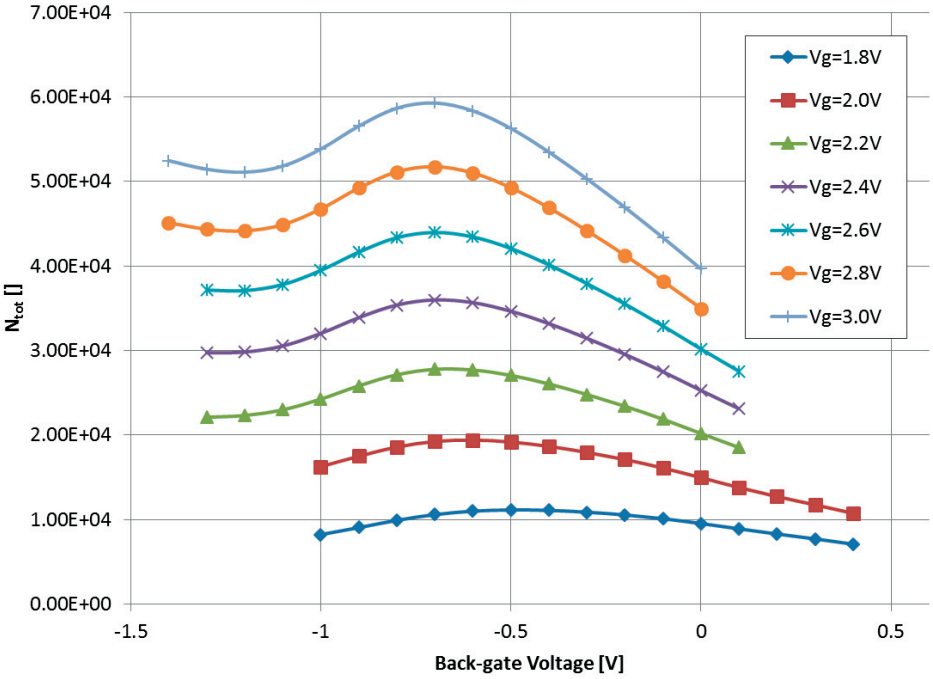

Fig. 4-10: Evaluation of N_{tot} with respect to back-gate voltage for different gate voltages

It is now possible to evaluate i_{dark}, knowing from section 2.1.6 that $T_0 = N_{tot}/i_{dark}$, as shown in Fig. 4-11.

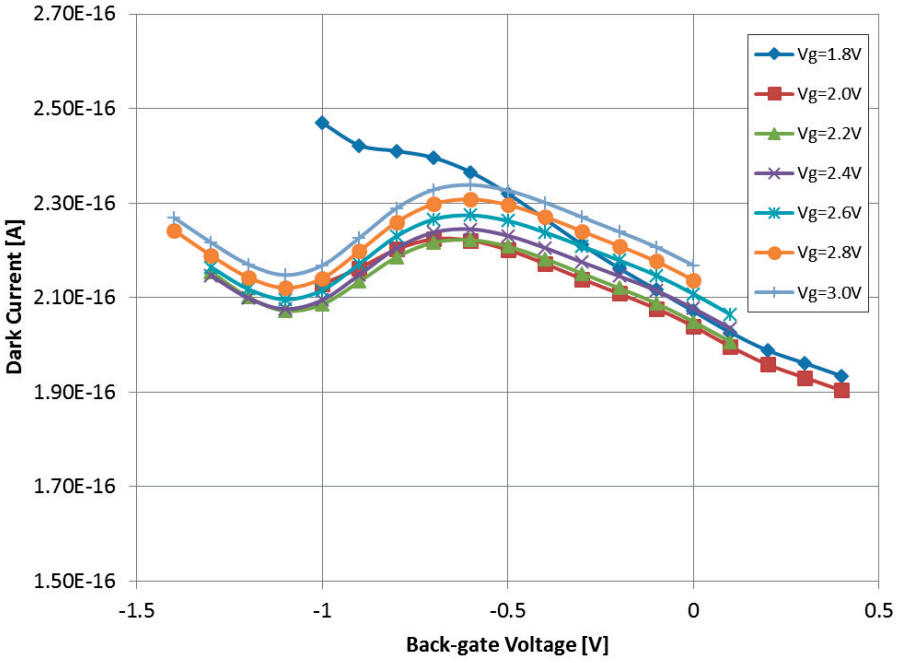

Fig. 4-11: Evaluation of dark current with respect to back-gate voltage for different gate voltages

The behavior of dark current for Vg = 1.8V seems to indicate that it is a limit case for which the electric field forming the depletion layer is not strong enough to cancel the leakage completely under Vbg biasing.

Once N_{tot} and i_{dark} are evaluated, it is possible to evaluate the SNR for I_{light} = 1e-9 W/cm^2, presented in Fig. 4-12.

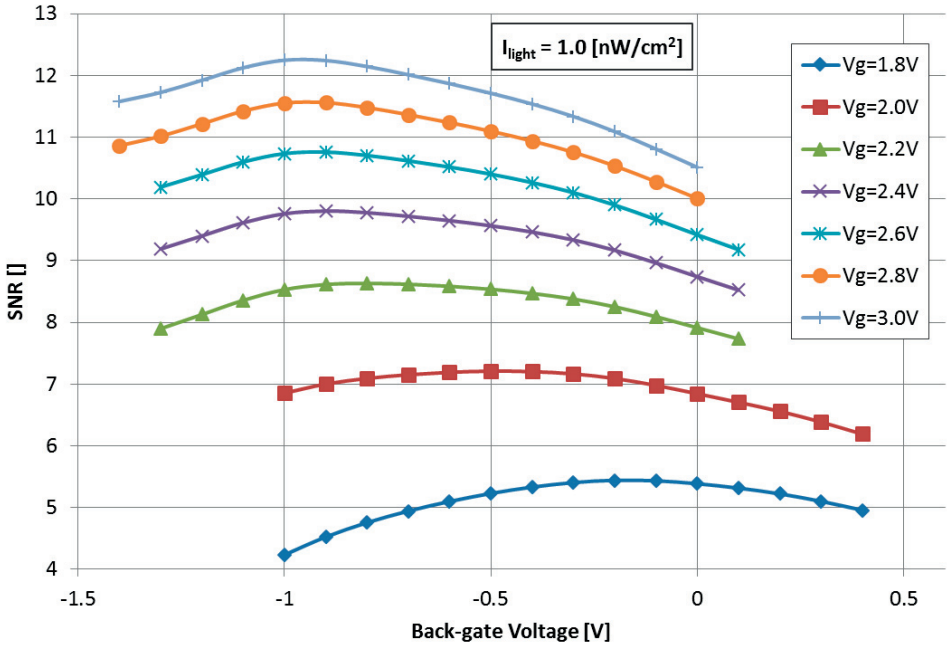

Fig. 4-12: Evaluation of dark current with respect to back-gate voltage for different gate voltages. I_{light} = 1nW/cm²

It is interesting to note that, for such a low light intensity, the achievable optimized value of the SNR with back gate biasing with respect to 0V is about 15% in the best case. One has to evaluate if such a small increase in SNR is worth the added complexity of a backside biasing system.

4.4.3 Linearity

Section 2.1.5 showed that, in the case of a bulk CMOS implementation of the device, slow carriers generated in the substrate impair the linearity of the device with respect to light intensity. On SOI, most of these carriers are blocked by the BOX and cannot reach the depletion layer of the device. Fig. 4-13 shows the derivative of the inverse of triggering time with respect to light intensity.

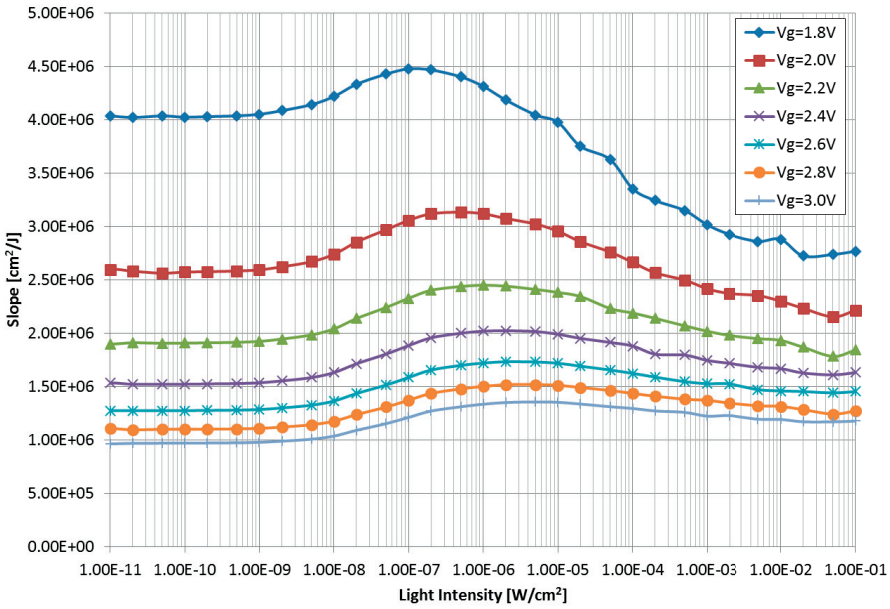

Fig. 4-13 : Simulated derivative of the inverse of triggering time versus light intensity for SOI

Compared with Fig. 2-14 of section 2.1.5, linearity is improved, with a maximal variation of about 40% over 10 orders of magnitude of light intensity, compared to a factor 3 in bulk implementation.

There is a maximum of sensitivity for some values of light intensity (depending on Vg). The drop in sensitivity for lower values of light intensities can be explained by recombination at the anode.

On the other end of dynamic range, for strong light intensities, the drop in sensitivity can be explained by the fact that not all the slow carriers are eliminated by the BOX, and carriers generated in the silicon layer but outside of the depletion region don't have time to reach the depletion region under small triggering time, leading to the same effect as the one described in section 2.1.5.

4.4.4 Optical effect of the SOI stack

Building the device on SOI technology also changes the optical properties of the photodetector. First, a shallow silicon layer has a negative effect on photon absorption, especially for long wavelength [85]. Photons in silicon diffuse according to Beer-Lambert law before being absorbed and the absorption coefficient of silicon strongly varies with wavelength. This translates into a drop in quantum efficiency for a given silicon thickness when wavelength increases, as it was shown in Fig. 3-37.

Nevertheless, due the difference in refractive indexes between the silicon ($n_{si} \approx 4.3$) and silicon dioxide ($n_{SiO2} \approx 1.5$) and the layer stack of the SOI process (Fig. 4-14), a light confinement effect appears and resonates for certain wavelengths, depending on the thicknesses of the different layers [81, 86].

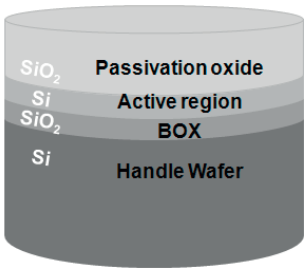

Fig. 4-14: Layer stack of a SOI process

The resonance translates into a peak in quantum efficiency at a certain wavelength, and a drop for the adjacent ones, as shown in Fig. 4-15.

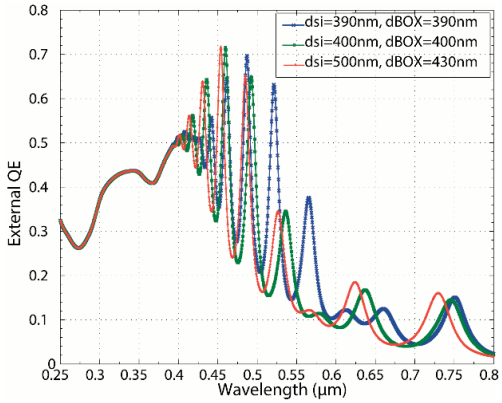

Fig. 4-15: Wavelength tuning for different SOI parameters

By tuning the thickness of the different layers, the resonance can be tuned to appear at a particular wavelength. Fig. 4-16 presents the variation in quantum efficiency for the upper spectrum of visible light with respect to BOX thickness, for an active region thickness of 395nm.

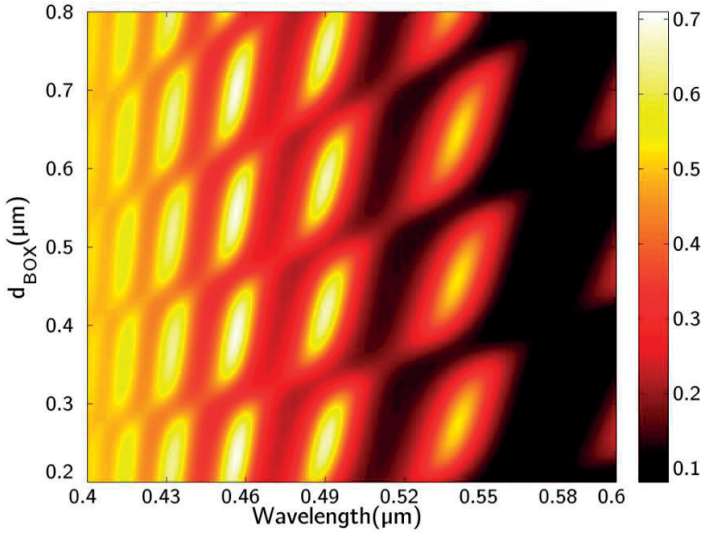

Fig. 4-16: External quantum efficiency for a silicon active region thickness of 395nm versus Box thickness (d_{BOX}) and wavelength

In some specific applications, such as bioluminescence measurement, the signal is present at one particular wavelength. In the case of bioluminescence, it is either at 480nm or 560nm, depending on whether it involves *renilla luciferase* or *firefly luciferase*, respectively. Fig. 4-17 presents the variation of quantum efficiency for λ=480nm, with respect to BOX thickness and active region depth. It is interesting to note that the resonance wavelength is more dependent on silicon thickness than BOX thickness.

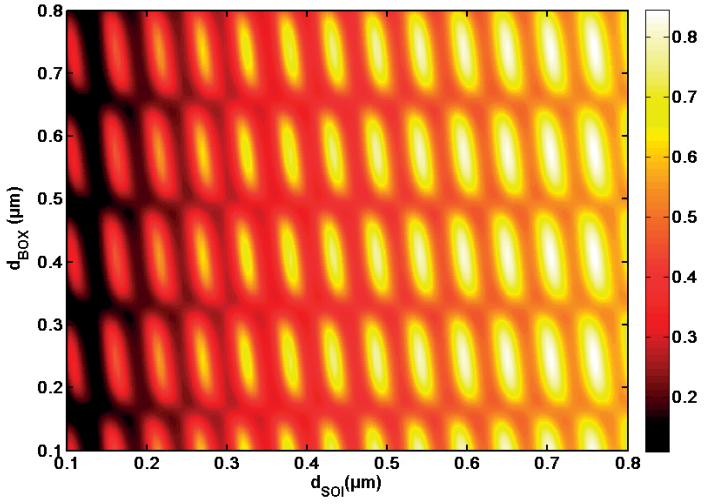

Fig. 4-17: External QE vs thickness of SOI layer (d_{SOI}) and BOX layer (d_{BOX}) for wavelength of 480nm

Those results show that the Hybrid MOS-PN photodetector built on SOI can be an interesting candidate for fully integrated biomedical systems such as bioluminescence labs-on-chip. Such a detector, being tuned to be sensitive to the wavelength of interest but too shallow to absorb efficiently huge parts of the spectrum, behaves like a bandpass filter and can effectively cancel background noise (in the form of ambient light) without any added optical filter. This may be interesting for low cost and/or in-vivo applications, where the system should be disposable and/or very compact.

4.4.5 Polysilicon absorption and Backside illumination

A common problem with photogate-based sensors, such as the Hybrid MOS-PN device, is polysilicon absorption. Polysilicon is a very absorptive material and the gate stack thickness (≈200nm in 0.18µm CMOS technology) is sufficient to absorb almost all the photos for wavelengths shorter than 500nm [86] (Fig. 4-18).

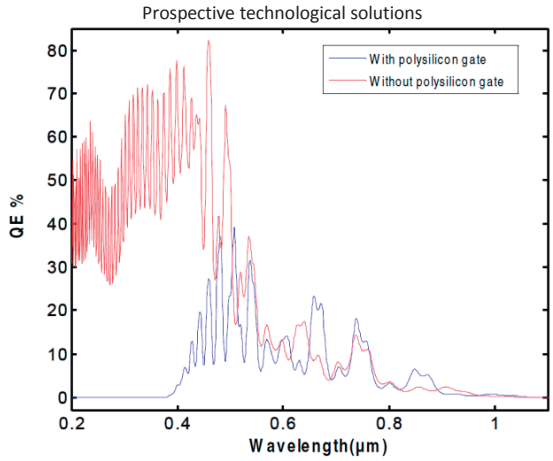

Fig. 4-18: Simulated effect of polysilicon gate on Quantum Efficiency, d_{SOI} and d_{BOX} = 400nm

Absorption in the gate stack reduces the overall efficiency of the detector by reducing its effective active area. One technological solution that can be used to overcome this problem is backside illumination, for which SOI is a suitable technology [87, 88].

The simplified fabrication process of an SOI-based backside illumination sensor (Fig. 4-19) starts by mounting the previously fabricated SOI circuit (a) on a handle wafer for mechanical stability (b). The silicon on the backside is then selectively etched, and replaced by a passivation layer, anti-reflective coatings (c), and possibly color filters and micro-lenses.

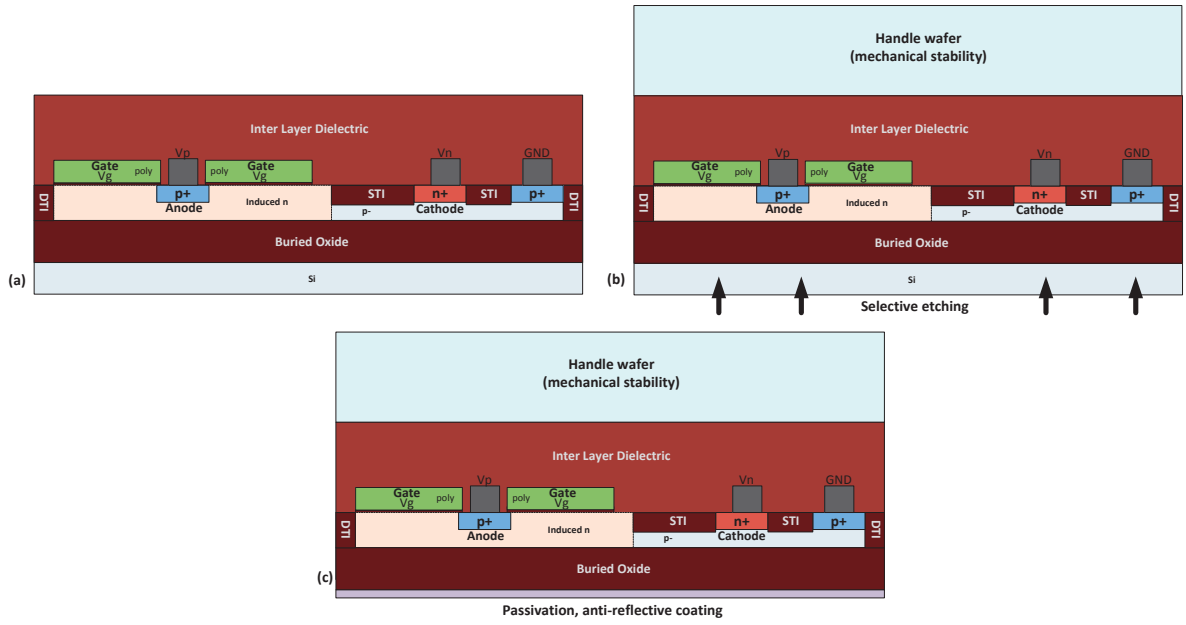

Fig. 4-19: Simplified fabrication process of a back-side illuminated sensor on SOI

It is shown in Fig. 4-17 that the resonance wavelength of detection is less sensitive to BOX thickness than to active region depth. This is positive, because it means that even in the event of a small over-etching of the silicon region underneath the BOX, a small diminution in BOX thickness would not destroy the resonance effect.

Another general advantage of backside illumination is the avoidance of the interference effects due to reflection in the multiple metal and inter-metal dielectric layers that are usually present for front-side illumination sensors and that were measured in Fig. 3-36.

Unfortunately, for back-side illumination, there is no possibility of fixing the substrate potential by the use of a back-gate. It is thus necessary to add a ground anchor to the device, as in a bulk implementation. This could introduce problems for fixing the potential when the silicon layer is shallow.

4.4.6 Isolation and multi-pixel implementation

Another advantage of SOI technology is the possibility to completely isolate the devices from one another, which is useful to ensure that there is no crosstalk between devices in the case of an array implementation. This is possible due to Deep Trench Isolation (DTI), which consists of trenches filled with dielectric penetrating completely through the silicon layer, down to the BOX (Fig. 4-20). As a consequence, every device has its own silicon, and no charges are exchanged between them.

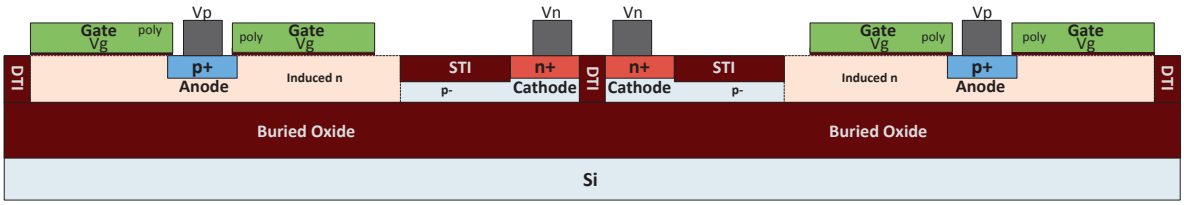

Fig. 4-20: Structure of two devices implemented on a SOI process

4.5 Summary

This chapter presented several techniques aimed at alleviating or solving some limitations of the device of interest.

A Multi-gate implementation can improve the tunability of the sensitivity.

A modification of the structure of the device could allow a subtraction of the dark current as well as ambient light, which can be very useful for some industrial or medical applications.

A triple-well process could help for device isolation if a low doping of the p-well can be achieved. It could also be used to isolate the circuit from the device.

Building the device on SOI would drastically reduce dark current and would be beneficial in terms of device isolation. It could also improve the linearity of the device by blocking the slow carriers.

Resonance effects in SOI create a built-in band-pass filter and can be useful for applications requiring the detection of a well defines wavelength, such as bioluminescence.

Finally, backside illumination would solve the problem of gate polysilicon absorption and interference due to metallic layers

.

Chapter 5 Case Study and Potential Applications

This chapter presents some realized application demonstrators using the Hybrid MOS-PN photodetector, as well as some propositions for potential applications.

5.1 Realized demonstrators

This section presents two different application demonstrators that were realized using the test circuit presented in chapter 3. They consist of a proximity sensor and a light barrier system.

5.1.1 Proximity sensor

By adding a LED to the detection system presented in chapter 3, it is possible to transform it into a reflection-based proximity sensor (Fig. 5-1). Such a system is found in every smartphone and is used to inhibit the touchscreen during a phone call when the phone is held against the head in order not to accidentally press buttons.

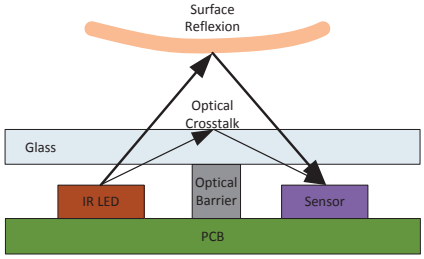

Fig. 5-1: Structure of a reflected intensity-based proximity sensor

The system works by comparing ambient light to reflected light from a collinear LED. When the LED is on, part of the emitted light can be reflected by a nearby object. The closer the object, the stronger the intensity of the reflected light and the bigger the difference in intensity between ambient light and reflected light (Fig. 5-2).

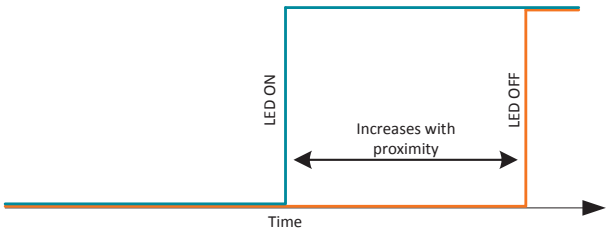

Fig. 5-2: Output signal of the detection system with LED on and LED off

In the case of the Hybrid MOS-PN device as a detector, an infrared LED is turned ON every second detection period. The difference in light intensity translates into a difference in triggering time. By measuring this difference, the distance to the object can be evaluated. It is not possible to perform an absolute distance measurement because reflected power depends on the type and color of the surface of the object. Nevertheless, the ratio between reflected power after subtraction of ambient illumination (P_{data}) and emitted power (P_{pulse}) is proportional to the inverse of the squared distance (D) [89].

$$\frac{P_{data}}{P_{pulse}} \sim \frac{1}{D^2} + Crosstalk + Offset \quad (5\text{-}1)$$

Crosstalk arises from the direct feed of LED emitted light to the detector (Fig. 5-1). This can be avoided by good geometrical design of the system. Offset refers to the electrical offset on the subtraction of ambient light.

With the assumption that crosstalk and offset are negligible, P_{data} can be obtained using the relation of section 2.1.6 by subtracting the ambient light intensity (I_{AMB}) to reflected light intensity (I_{refl}).

$$\underbrace{\frac{1}{T_{LED}} - \frac{1}{T_{AMB}}}_{P_{data}} = \frac{1}{N_{tot}}\left(\alpha I_{refl} + \alpha I_{AMB} + n_{dark}\right) - \frac{1}{N_{tot}}\left(\alpha I_{AMB} + n_{dark}\right) = \frac{\alpha}{N_{tot}} I_{refl} \quad (5\text{-}2)$$

Once again, the inverse of triggering time can be obtained through the use of a look-up table.

Fig. 5-3 shows the behavior of the system with no reflected light (a), a small reflected light intensity due to a nearby hand (b), a large reflected light intensity due to a very close hand (c). It is interesting to note the diminution in ambient light intensity when the hand is brought close to the detection system.

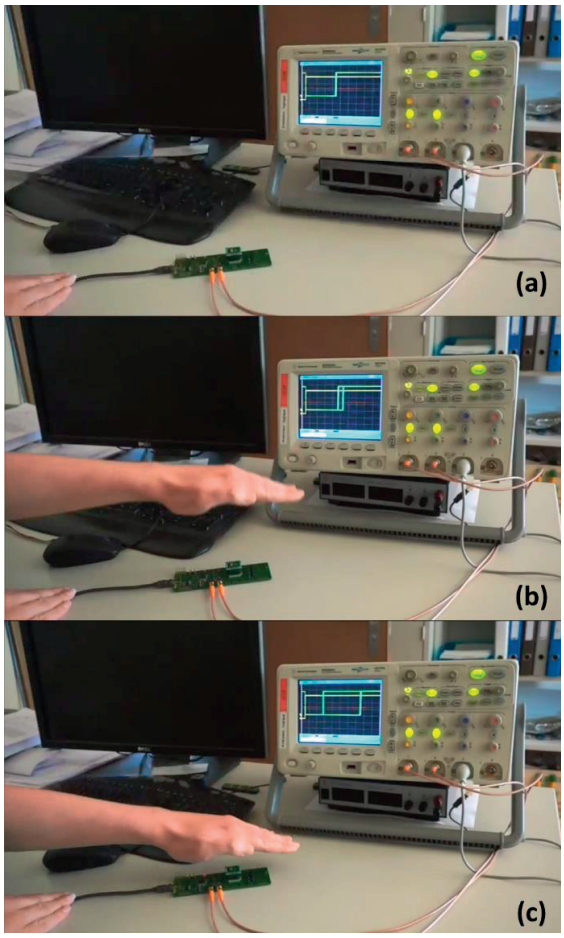

Fig. 5-3: Behavior of the proximity detection system under different reflective conditions

Fig. 5-4 presents the same experiment, but with a very absorptive object (black box). It is interesting to see that, as expected, the intensity of reflected light is way smaller for a given distance than with the hand.

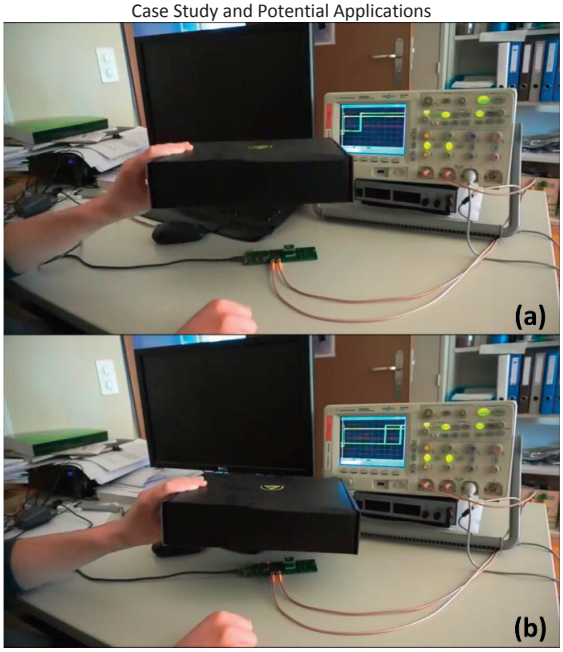

Fig. 5-4: Behavior of the proximity detection system with a very absorptive surface

Fig. 5-5 shows that the proximity detection system is still able to work when flooded with ambient light. Of course, in this case, the triggering time is way shorter and the detection system must be able to discriminate between very short times. In this figure, the time base of the oscilloscope was magnified with respect to the previous tests.

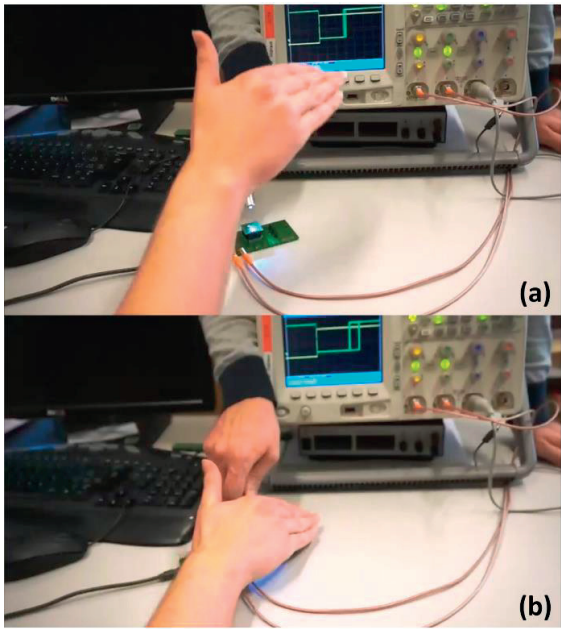

Fig. 5-5: Behavior of the proximity detection system with very strong ambient light

Overall performances can be improved by the use of a long-pass infrared filter. Such a filter cancels about 95% of ambient light. As a consequence, triggering time increases drastically and specifications of the detection system are easier to achieve, for example in terms of dynamic range which is typically in the order of 16 bits [90].

5.1.2 Light Barrier

Another demonstrated application is the light barrier. It refers to a system which detects when the path between a light emitter or reflector and a receiver is crossed by an object or a person. This type of system is extremely widely used in industrial applications, security, etc. There are multiple ways to implement it, but they can be classified in two categories.

In the first category are the synchronous systems (Fig. 5-6). It includes systems with the emitter and the receiver on the same side of the barrier, with a passive component (reflector) on the other side. It also refers to systems in which a synchronization signal is exchanged between the receiver and the emitter situated on the other side of the barrier [91]. The transmission of the synchronization signal can be either electrical or optical. When implemented with the device of interest, the operation of such systems is similar to the one of the proximity sensor.

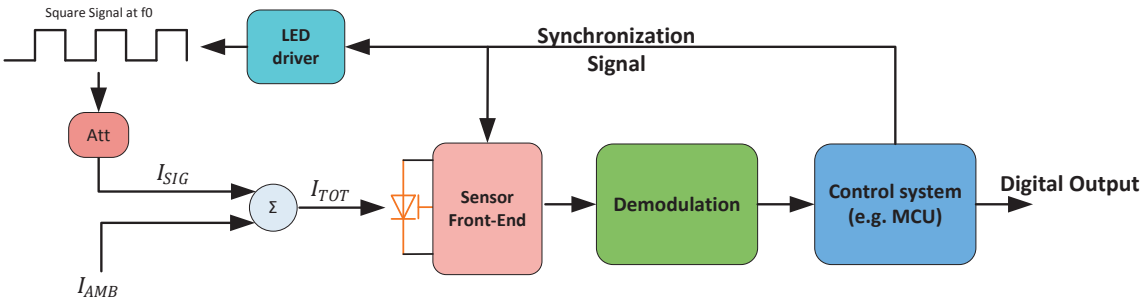

Fig. 5-6: Concept of a synchronous light barrier system using the Hybrid MOS-PN photodetector

In the second category are the asynchronous systems (Fig. 5-7), i.e. systems in which the emitter and receiver are independent (i.e. do not exchange synchronization signals). In such systems, the emitted light is usually amplitude modulated at a pre-determined frequency (usually 38 kHz [77]). The receiver amplifies the detected signal and feeds it to a bandpass filter tuned at the pre-determined frequency in order to reject ambient light as well as high frequency parasites. Those implementation are often simpler and less expensive than the synchronous ones, at the price of reduced performances. Such a system cannot be implemented in that way with the Hybrid MOS-PN device due to the nature of the output signal of the detector. As presented in section 2.2, there are two main operating modes of the device that can be used to detect a signal, PFM and PWM.

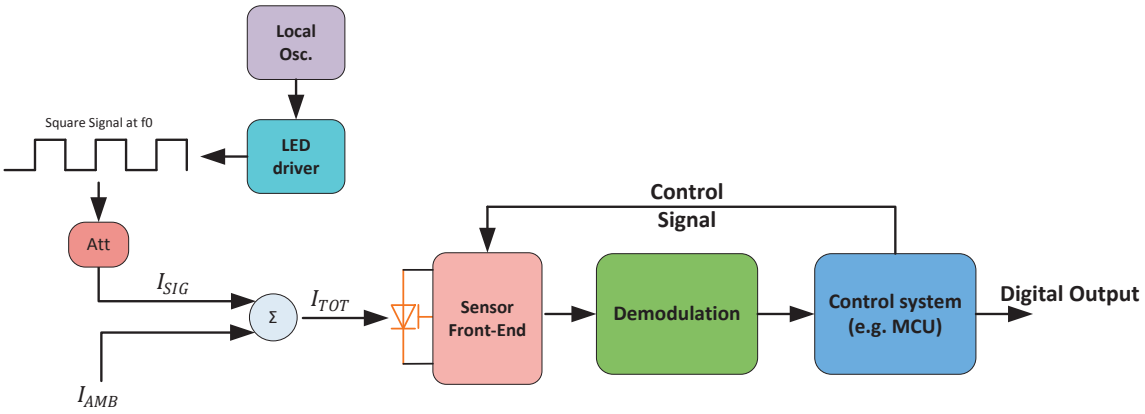

Fig. 5-7: Concept of an asynchronous light barrier system using the Hybrid MOS-PN photodetector

With a PFM detection scheme, the ON-OFF modulated light from the emitting LED translates into a two level frequency shift keying (FSK) modulation at the output of the detector. Therefore, there are two frequencies, first f_{low} that is determined by ambient light, and f_{high} which is the same but with the added intensity from the LED. Unfortunately, both frequencies depend on ambient light and their difference is proportional on the LED output power and the square of its distance to the detector.

There are several ways to implement a demodulation system using the Hybrid MOS-PN device. One of the simplest is to use a correlator, which can be understood as a digital version of the FM quadrature demodulator [92]. It works by multiplying the frequency-modulated signal by a delayed version of itself.

$$\sin(2\pi f t) \cdot \sin(2\pi f(t+\tau)) = \frac{1}{2}[\cos(2\pi f(-\tau)) - \cos(2\pi f(2t+\tau))] \tag{5-3}$$

Equation 5.3 shows that the effect of the multiplication is a component whose amplitude depends on the frequency (f) and the delay (τ), which is the demodulated signal, as well as a component oscillating at twice de frequency, which can be easily filtered out. It is easily seen that the delay must be tuned according to the actual frequency of the signal in order to ensure a successful demodulation. Unfortunately, the frequency of the signal is not known a priori. A control loop acting on the value of the delay for a demodulation of maximal amplitude is thus needed. The multiplication operation can be implemented as a simple XOR gate, and the variable delay generator can be implemented as a variable size shift register, or a variable RC delay in case of an analog implementation. Fig. 5-8 presents a conceptual schematic of the correlator-based demodulation system.

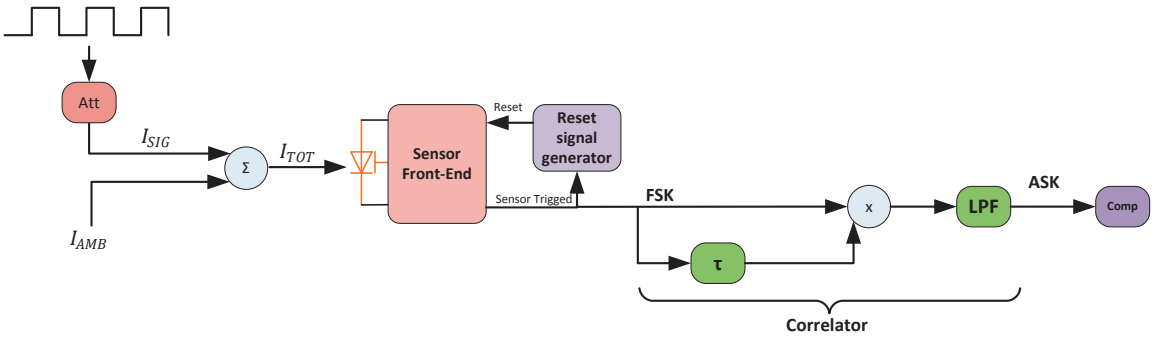

Fig. 5-8: Correlator-based FSK demodulation

Another possible solution to demodulate the FM signal is the PLL based FM demodulator. The advantage of such a system is that it is self-regulating and that the frequency of the modulated signal doesn't need to be know a priori, at the price of implementing a VCO with a high-enough dynamic range so that it is able to handle the variation in ambient light. In such a system, the demodulated signal is in fact the control signal of the VCO, as seen in Fig. 5-9.

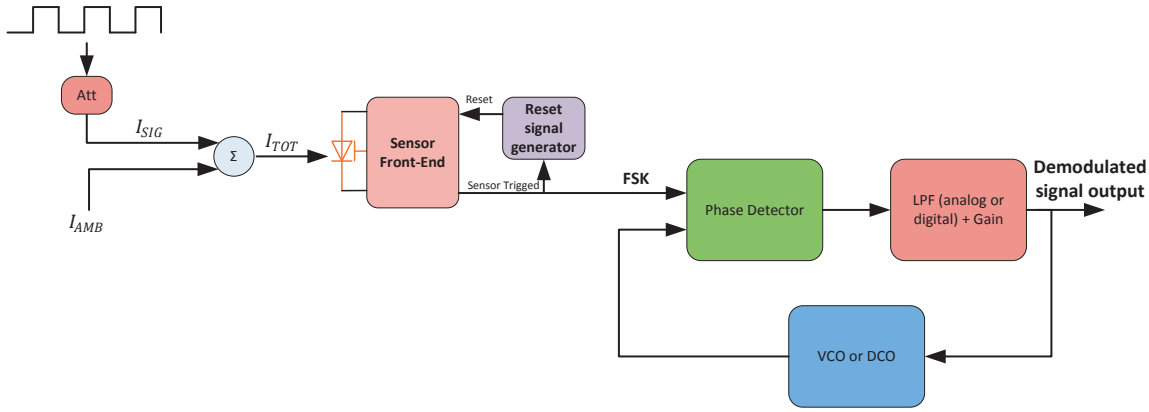

Fig. 5-9: PLL-based FSK demodulation

The demodulation method that was finally implemented as a demonstrator uses a local frequency generator that oscillates at the same frequency than the led control signal. A counter is then used to compare the value of the frequency of the modulated signal during the half-period with the LED ON with the one during the half-period with the LED OFF. If no difference is detected, it means that no light from the LED reaches the device and therefore that the barrier has been crossed.

It is of course impossible to guarantee that both oscillators (the one controlling the LED and the one on the receiver side) work at the exact same frequency. They will drift and at some point they will be in quadrature, which means that the average frequency over a period will be constant, although light from the LED is received. In order to handle that case, the local oscillator is delayed by one eight of a period when no difference in the average is detected. If this is repeated several times without any difference being measured, it means that the barrier was indeed crossed. The system is presented in Fig. 5-10.

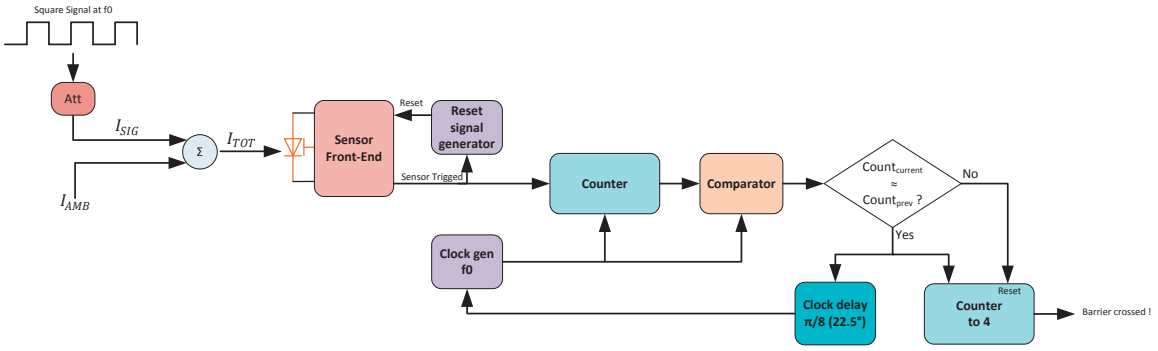

Fig. 5-10: Local-oscillator-based FSK demodulation

This detection scheme was implemented on the microcontroller of the measurement system. On the emitter side, a 950nm emitting LED with an ON-OFF modulation at a frequency of 100Hz was used. Barrier lengths up to 3 meters were demonstrated. Fig. 5-11 shows the receiver side fitted with a long-pass infrared filter used to cancel ambient light.

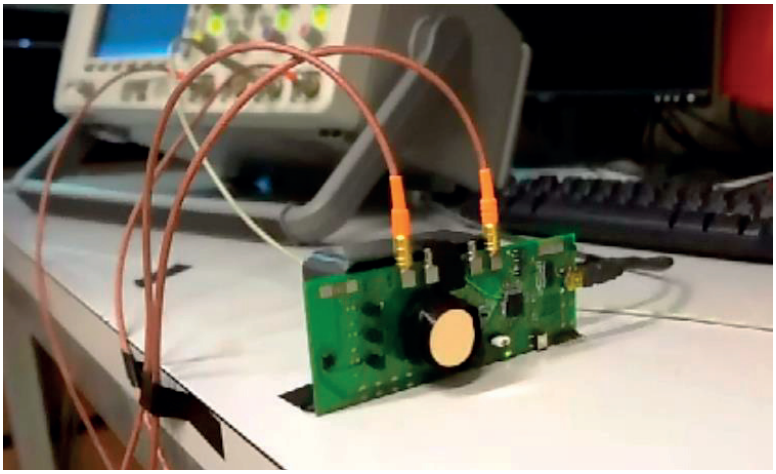

Fig. 5-11: Measurement system used as light-barrier, with IR long-pass filter.

A general limitation of PFM based systems is that the dynamic range is constrained by the duration of the reset phase (section 2.2.2). As a consequence, it is unlikely that such a system is able to meet the specifications of commercially available products, notably in terms of ambient light. The limitation in dynamic range can be avoided by using à PWM detection system.

The proposed system uses a binary counter to measure the triggering time. Those values are then accumulated in a moving average filter. By choosing the depth of the moving average as half of the LED signal period, the amplitude of the resulting signal at the output of the filter is maximized. When no difference in the average is measured over one full period of the signal, it means that the barrier has been crossed. Fig. 5-12 presents a conceptual schematic of such a detection system.

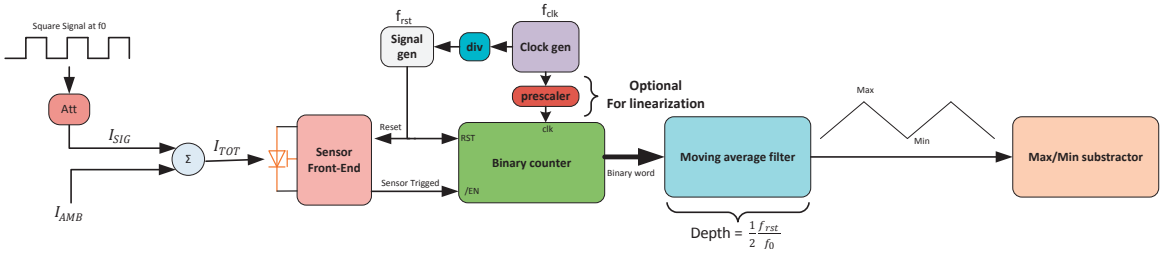

Fig. 5-12: Moving-average-based light-barrier detection system

The precision of the system is constrained by the clock frequency (f_{clk}) that drives the binary counter. A clock prescaler with a look-up table can be used to linearize the signal at the output of the filter (c.f. section 2.2.1). In case the triggering time is very short, a time-to-digital converter (TDC) can also be used to measure triggering time.

5.2 Optical Latch

Optical data links and clock distribution signals are progressively replacing electrical interconnects and voltage-based signals on shorter distances. Over the past decade, optical local-area network (LAN) became a standard and optical backplane interconnects started becoming a reality. Nevertheless, optical data transfer and clock distribution at printed-circuit board (PCB) and package level are not widespread yet. In order for those to become a reality, a power-efficient light emission technique as well as readily CMOS compatible small and power-efficient receivers are needed [93, 94].

Existing clock receiver circuits include integrating circuits [95, 96], trans-impedance amplifier-based circuits [97], and the so-called receiver-less approach, using two photodiodes connected as a "totem-pole" configuration and receiving laser-pulses alternatively. This creates a voltage swing on the middle node that can directly be directly transformed into CMOS-level signal [98].

Taking advantage of the latching properties of the Hybrid MOS-PN photodetector, a very simple all-digital clock receiver for pulsed optical clocking signals [99] can be designed. Moreover, detectors can be arranged to form a phase detector which can be used in a light-fed PLL. Such a PLL could be for example used as a local clock synthesizer, or a demodulator for optical data transmission.

Under the assumption that light intensity is sufficiently high for the triggering time to be quasi-instantaneous (i.e. in the order of the delay of a CMOS gate), the device with its front end can be modelled as a digital component with its truth table presented in Table 5-1. This corresponds to a SR-latch with reset priority, as shown in Fig. 5-13.

Light	Reset	Output
X	1	0
0	0	Hold
1	0	1

Table 5-1: Truth table of the Hybrid MOS-PN device as logical latch

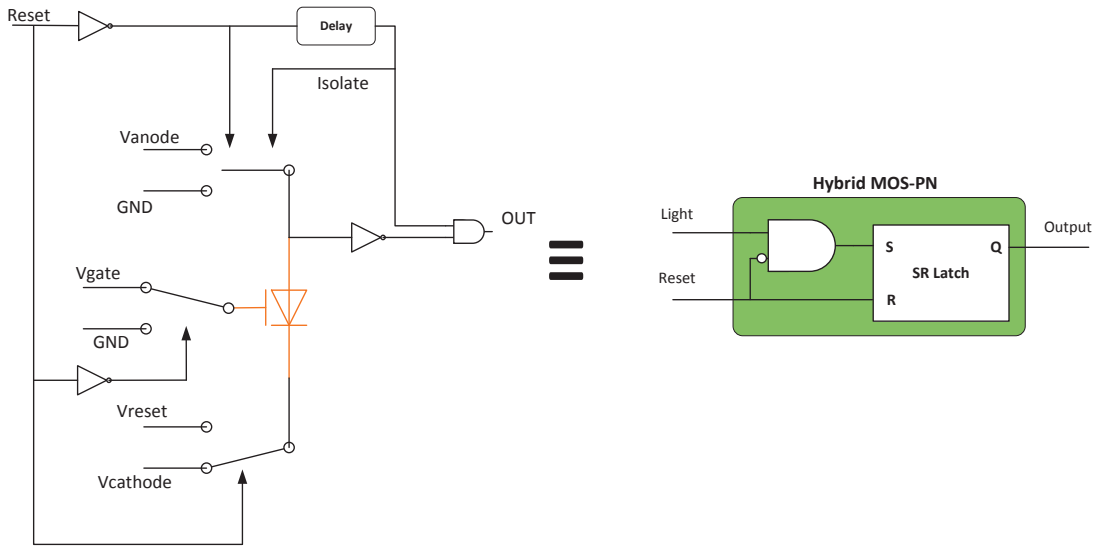

Fig. 5-13: Equivalent logic circuit of the photodetector with its front end

5.2.1 Clock Receiver

By using two adjacent cross-coupled detectors, an optical clocking signal receiver can be built. The proposed design (Fig. 5-14) features a "flip-flop like" behavior, detecting the laser pulses and recreating a 50% duty cycle clock signal at half the pulse frequency (Fig. 5-15). Such a design works under the assumption that the laser pulse width is shorter than the device triggering time and the reset signal propagation, which is not a problem considering that laser pulses can be as short as a few femto-seconds.

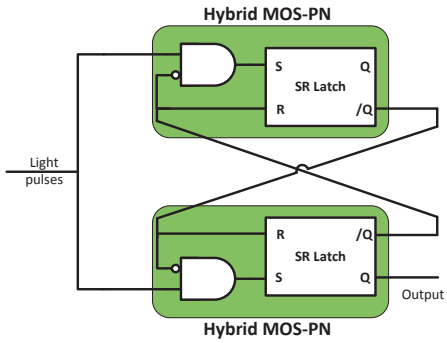

Fig. 5-14: Clock receiver with cross-coupled detectors

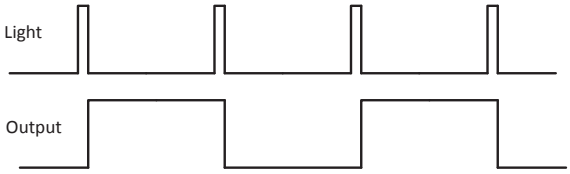

Fig. 5-15: Output waveform of the clock-receiver system

With this concept, the maximum recoverable clock frequency is constrained by the minimum acceptable reset time of the photodetector. The minimum frequency is determined by the self-triggering time due to leakage. One way to get around the frequency limitations of the device would be to locally generate a high-frequency clock out of the optically transmitted low-frequency one. In order for this to be achieved, a PLL is typically used. The next section shows that the detector itself could be used as a phase detector.

5.2.2 Phase detector for pulsed light

When driving one detector with synchronous light and reset signals, it can be seen that the duty cycle of the output signal is sensitive to phase, but only to a phase lead of the light signal with respect to the reset signal. It is interesting to note that the behavior of the detector in terms of output signal duty cycle varies depending on the nature of the light signal in the case of a phase lag. When driven by a 50% duty cycle square optical signal, the output of the detector when the phase of the optical signal lags behind the one of the reset signal has a constant duty cycle at 50% (Fig. 5-16). When driven by a pulsed optical signal of negligible width, the output for a phase lag is constant at 0 (Fig. 5-17).

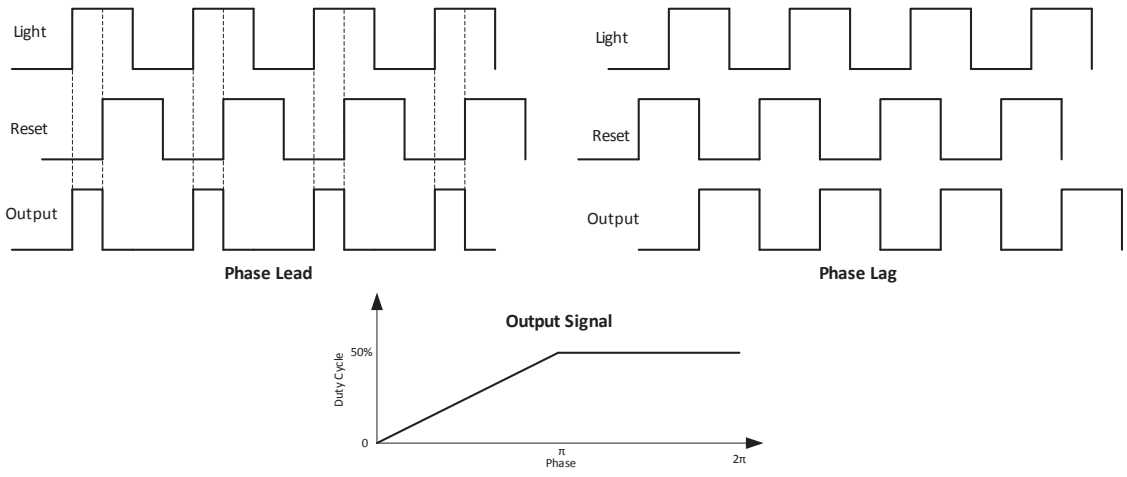

Fig. 5-16: Phase-detection behavior of the device for a 50% duty-cycle light-input signal

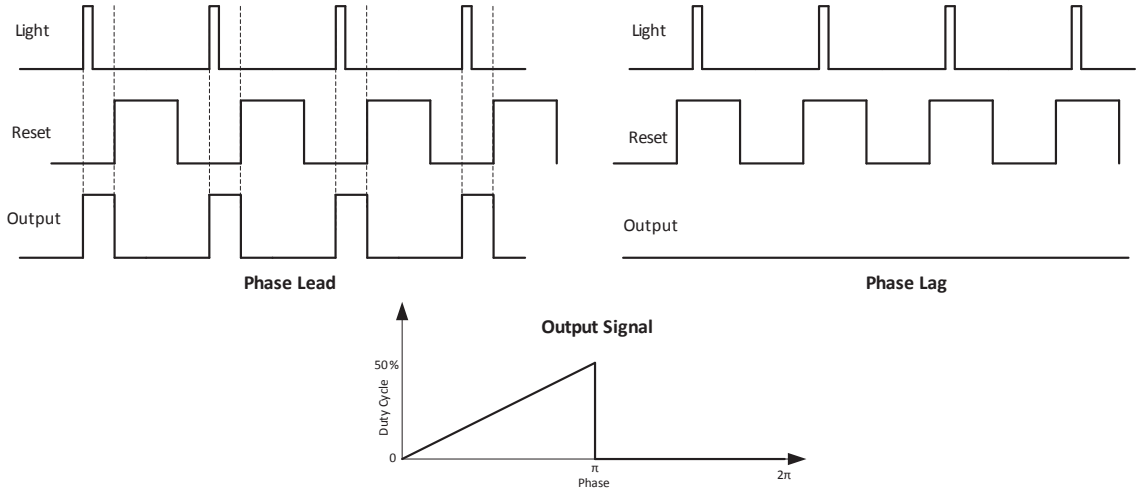

Fig. 5-17: Phase-detection behavior of the device for a pulsed light-input signal

By combining two detectors driven with complementary reset signals (Fig. 5-18), phase sensitivity can be achieved over the complete 2π range (Fig. 5-19). It is therefore possible to design a very simple phase comparator usable in a PLL that locks on a pulsed optical signal.

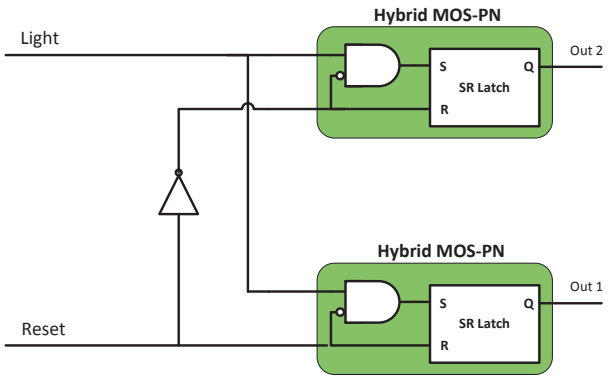

Fig. 5-18: Complementary-driven devices

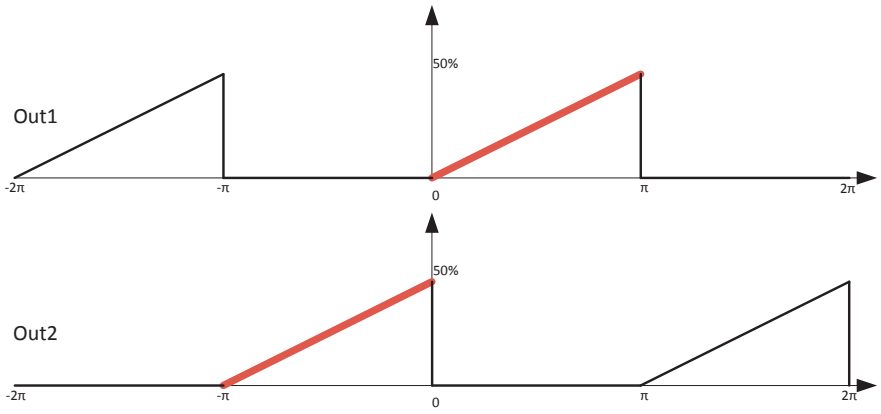

Fig. 5-19: Duty-cycle outputs of the complementary-driven devices

In order to create a usable phase comparator, it is needed to combine the two discontinuous output signal into one continuous signal over a 2π range and with a duty cycle ranging from 0 to 100%. This can be achieved by combining the Out1 and Reset signals with a logical OR in order to create an output with a duty cycle ranging from 50% to 100% in the case of a phase lead (Fig. 5-20).

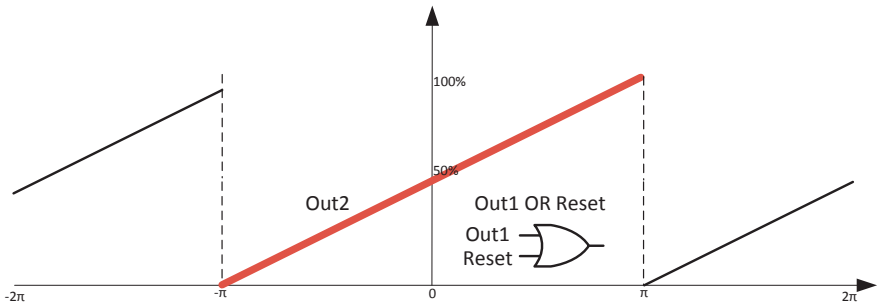

Fig. 5-20: Duty-Cycle output of the desired phase-detection signal

The outputs are then multiplexed and selected depending on whether there is a phase lead or a phase lag. Determining this condition is easy, and can be done by comparing the state or Out1 in the event of a rising edge of Reset. If a rising edge of Reset when the state of Out1 is 1, then the phase of the optical signal leads the one of the reset signal. Fig. 5-21 presents the complete phase comparator circuit. A slightly different circuit can be used to create a phase comparator working with a 50% duty cycle signal.

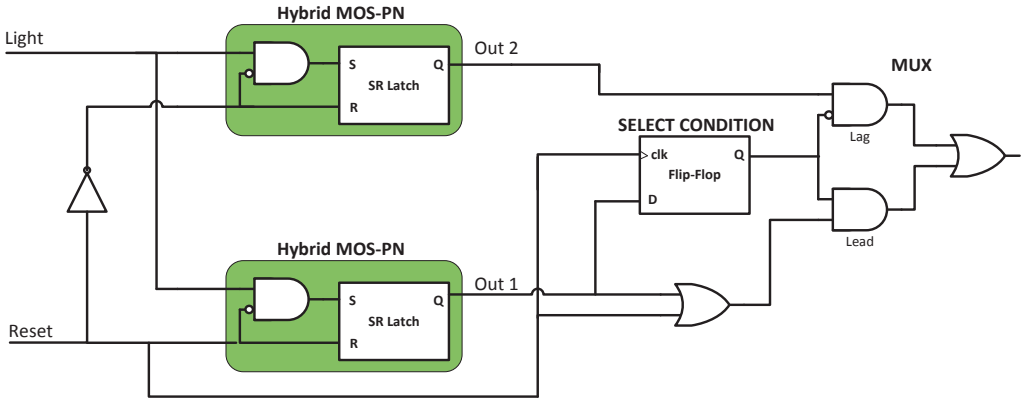

Fig. 5-21: Equivalent schematic of the phase detector using Hybrid MOS-PN devices

This complete phase comparator circuit can be directly used in a light-pulses driven PLL, e.g. for high frequency clock synthesizer, as shown in Fig. 5-22.

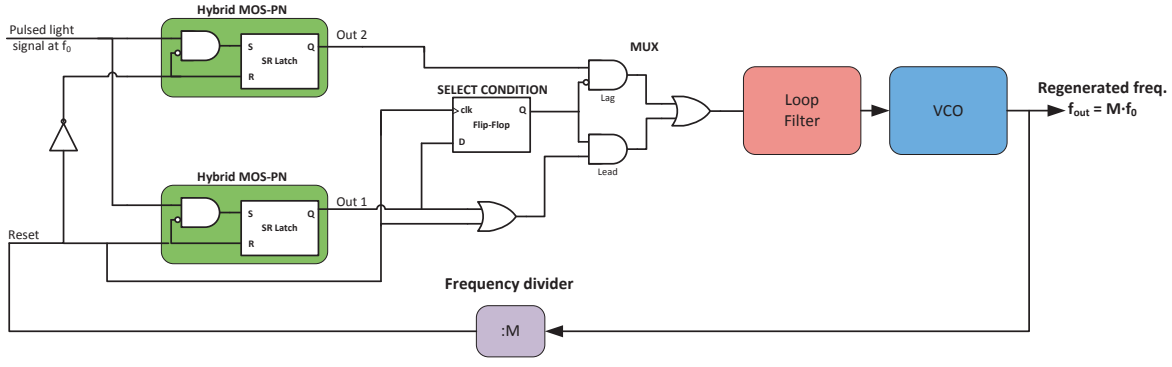

Fig. 5-22: PLL-based frequency synthesizer using the Hybrid MOS-PN detector

5.2.3 Phase detector in the general case

The previous chapter presented the phase detection properties of the Hybrid MOS-PN device in the ideal case, i.e. no ambient light and strong enough signal for the device to trigger immediately.

It can be shown that the device behaves like an imperfect XOR detector when fed with a light signal that is synchronous with the reset signal. The ambient light creates an offset, and the gain of the phase detector depends on the signal strength (Fig. 5-23).

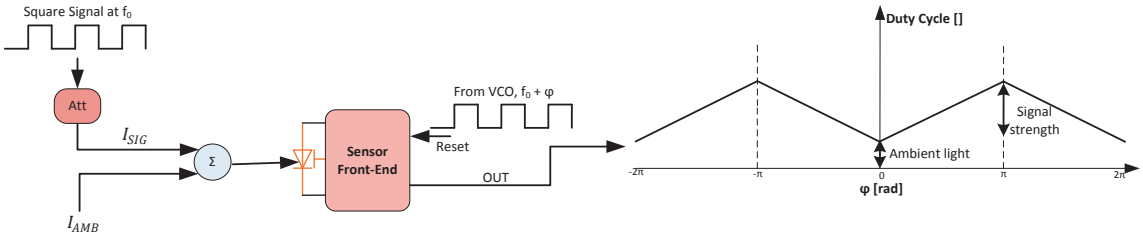

Fig. 5-23: Phase-detection characteristics of the photodetector in the general case

If it is possible to lock à PLL on the signal of such a « bad » detector, this property of the device could be used for example in a tone detector circuit that would operate like an « optical » LM 567 [100] (Fig. 5-24).

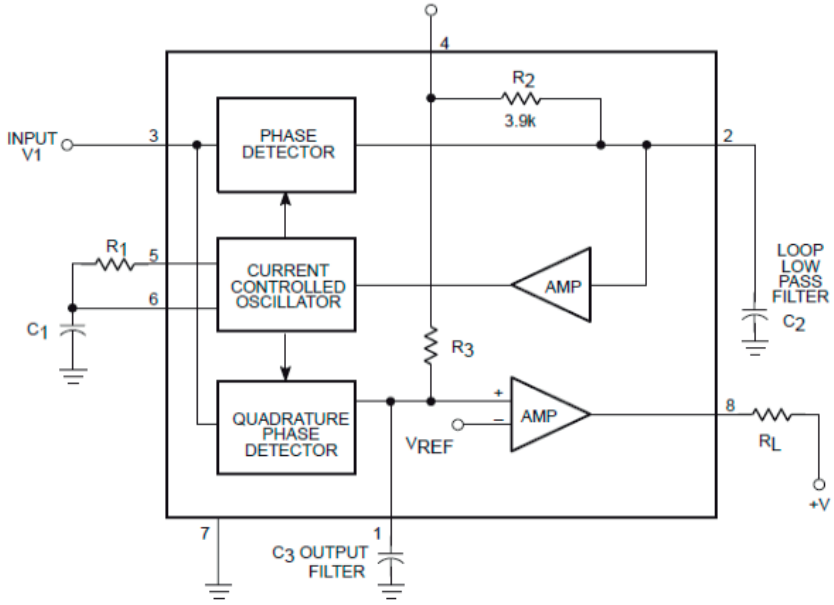

Fig. 5-24: Simplified schematic of the LM567 tone detector [101]

The challenge here would be to design a loop filter that would be able to cancel the « DC » part due to ambient light but still allowing the PLL to lock. If this is possible, the principle of the LM567 can be reused (Fig. 5-25).

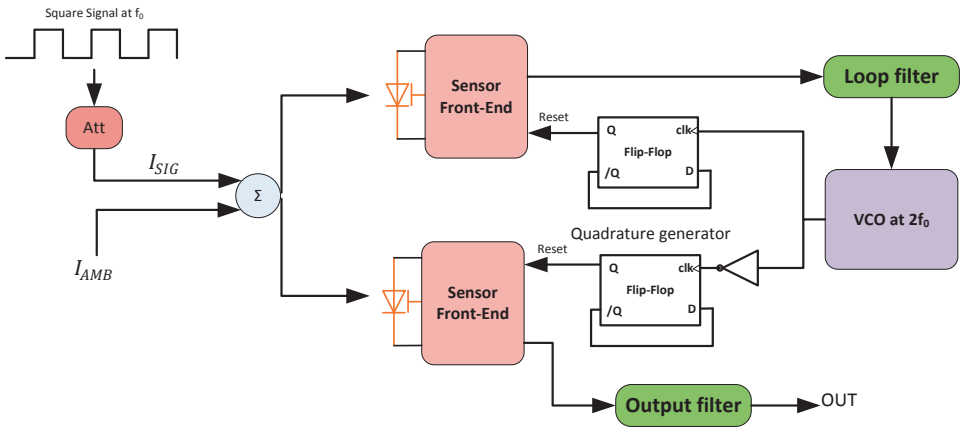

Fig. 5-25: Hypothetical tone-detector using the Hybrid-MOS-PN device as phase comparator.

5.3 Photoplethysmography (PPG)

Photoplethysmography (PPG) refers to the optical volumetric measurement of an organ. This technique is often used to measure the blood flow and the oxygen level by illuminating skin and measuring the change in light absorption of some parts of the body (typically the finger). The system performing such a measurement is called a pulse oximeter and is widespread in medical and leisure applications [102]. The standard way of implementing such a system is to measure the transmitted (or reflected) light from an emitting led through the skin with a photodiode. The photocurrent is then amplified with a transimpedance amplifier, filtered, and finally converted to digital [37, 103, 104]. Some non-uniform sampling-based approaches have also been proposed [105]. Fig. 5-26 presents the front end of a commercial product from Texas Instruments, the AFE 4403.

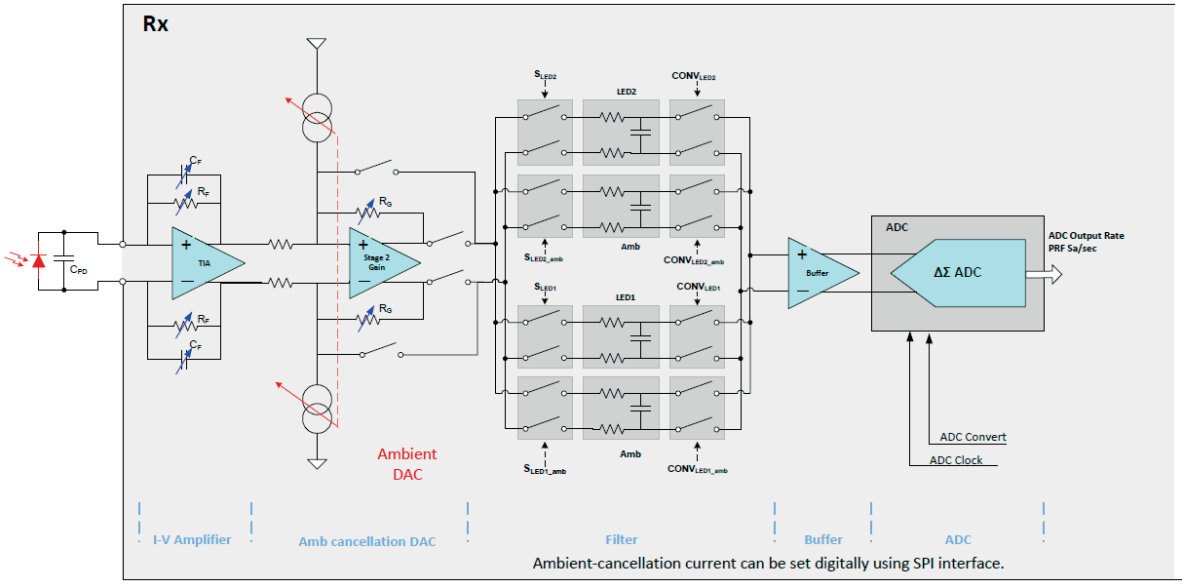

Fig. 5-26: Front end circuit of the Texas Instruments AFE4403 PPG circuit [78]

The market for portable and leisure oriented PPG system is growing rapidly due to the apparition of smart watches and dedicated sports-gear, for which minimizing the cost of the system as well as its power consumption are top priorities. By using the Hybrid MOS-PN device as detector and thus avoiding analog amplification and filtering of the photocurrent, silicon area and power consumption can be saved. In terms of silicon area, recent publications show that the area occupied by the analog signal processing chain (amplification and filtering) in PPG applications is between 0.2 mm^2 [37] and 0.6 mm^2 [36], with a current consumption of over 300 µA. Most of the area of the front ends is occupied by filtering components. However, at system level, the largest part of power consumption comes from the emitting LED, whose power has to be minimized.

In order to address those two points, a PLL-based PPG system using the hybrid MOS-PN device as photodetector is proposed. In this system, the chain comprised of the emitting led with its driver, the transmission channel (the skin of the subject) and the detector working in PFM mode forms a digitally controlled oscillator (DCO) with frequency modulation due to absorbance and/or reflectance variations in the transmission channel (Fig. 5-27).

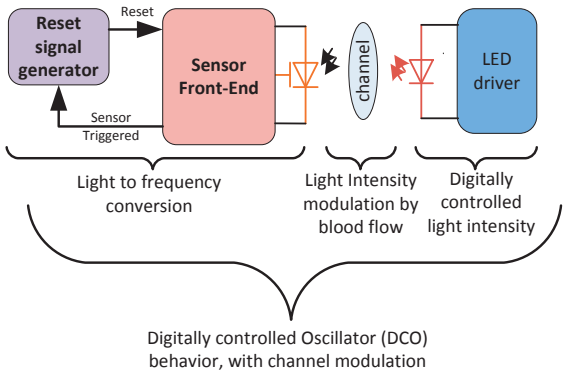

Fig. 5-27: Modelling of the optical chain with detector as a DCO

The goal of the detection system is therefore to efficiently demodulate the FM signal created by the channel. For this, a PLL is used. The goal is to lock the phase of the detector output frequency on the one of a reference frequency. Once the system is locked, the variations of the channel giving rise to variations of the detector output frequency are perfectly compensated by the control loop by acting on the LED output power, and the control signal of the LED driver is the demodulated (Fig. 5-28).

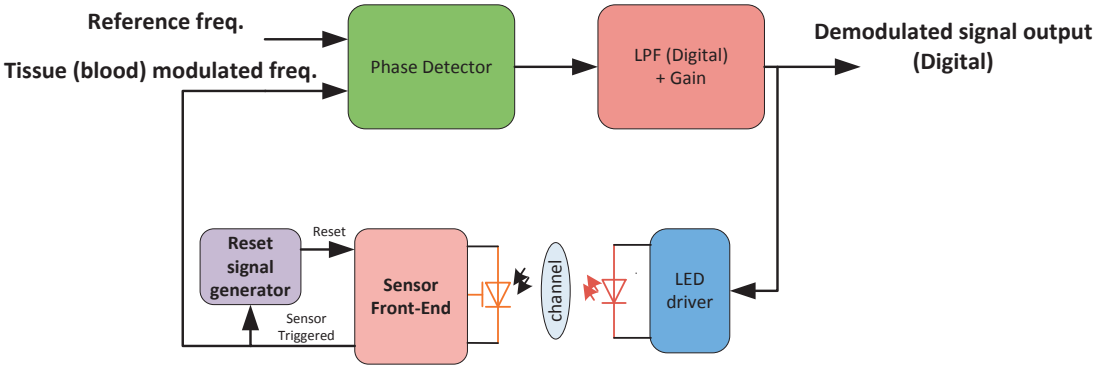

Fig. 5-28: PLL-based demodulator for PPG detection system

The Reference frequency of the control loop has to be chosen according to the “free-running frequency” of the oscillator. In this case, it means the frequency due to ambient light only. For this, a second control loop is added to the system (Fig. 5-29). When it is activated, the LED driver is inhibited and a DCO is locked on the ambient light frequency. The DCO frequency is then fixed and the inner loop is re-activated. In order for it to be able to lock, the new reference frequency should be set a little bit higher than the “true” one only due to ambient light so that the LED has to provide some light, i.e. the loop is actually closed.

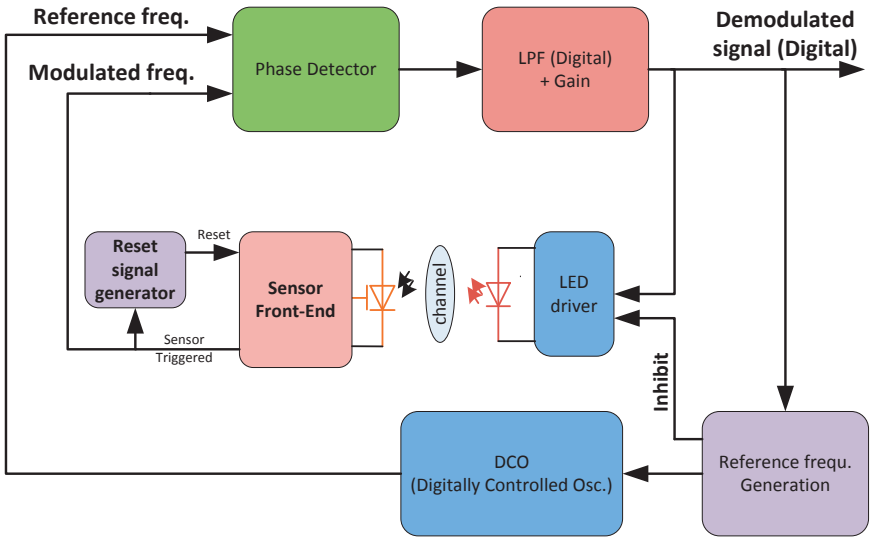

Fig. 5-29: PLL based system with second loop for reference-frequency tuning

The goal of the system is to minimize power consumption. The LED is therefore driven at the minimum possible intensity, i.e. just adding very little intensity over ambient light. However, this might not be enough to demodulate a signal with an acceptable SNR. It is therefore needed to have a control system that controls f_{ref} with a condition on the quality of the signal. A bad or inexistent signal would trigger an increase in f_{ref}, which entails an increase in LED power output due to the control loop, which finally increases the amplitude of the signal and thus its SNR. This is conceptually similar to an automatic gain control (AGC). The behavior of the system can be analyzed using the PLL formalism, as described in Fig. 5-30.

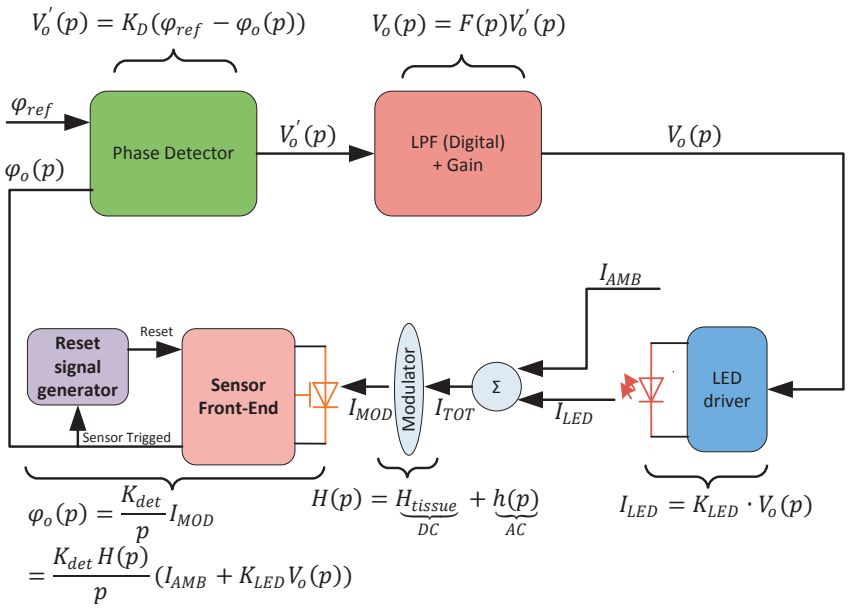

Fig. 5-30: Parameters of the PLL-based system

This analysis uses the assumption that all the light crosses the “channel” before arriving on the detector, i.e. there is no “leakage” of light onto the detector. An abstracted view of the system in terms of inputs and outputs is presented in Fig. 5-31.

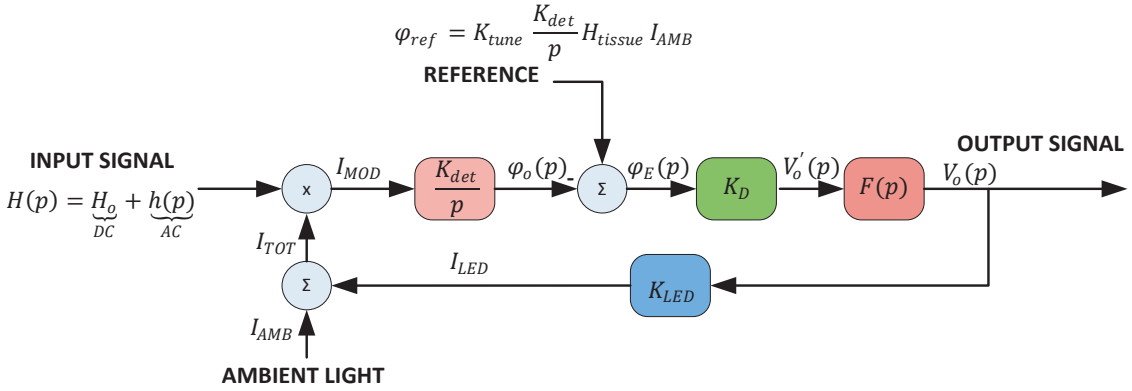

Fig. 5-31: Modelling of the system with the PLL-formalism

It is possible to derive the expression of $V_0(p)$.

$$V_o(p) = F(p)K_D\left(\varphi_{ref} - \frac{K_{det}}{p}H(p)\left(I_{AMB} + K_{LED}V_o(p)\right)\right) \tag{5-4}$$

$$\Leftrightarrow V_o(p) = \frac{F(p)K_D\left(\varphi_{ref} - \frac{K_{det}}{p}H(p)I_{AMB}\right)}{1+F(p)K_D\frac{K_{det}}{p}H(t)K_{LED}} \tag{5-5}$$

The action of the second loop (reference frequency tuner) is modelled by a dependence on I_{AMB} through H_{tissue} (no modulation) with a parameter K_{tune} which can be considered a little bit >1. It corresponds to the little higher frequency needed for the loop to be able to lock, as explained previously. The gain of the measurement chain $K_{chain} = F(p)K_D\frac{K_{det}}{p}$ is also introduces in order to lighten the notation.

$$V_o(p) = \frac{K_{chain}I_{AMB}((K_{tune}-1)H_{tissue}-h(p))}{1+K_{chain}K_{LED}H_{tissue}+K_{chain}h(p)} = I_{AMB}\frac{(K_{tune}-1)H_{tissue}-h(p)}{1/K_{chain}+K_{LED}(H_{tissue}+h(p))} \tag{5-6}$$

Equation 5-6 shows that the output level is proportional to I_{AMB}, which is expected. It also depends on the difference of the reference frequency with respect to the "ambient frequency" (K_{tune}-1).

In order to see how the output varies with respect to the modulation h(p), the derivative is calculated.

$$\frac{dV_o(p)}{dh(p)} = -I_{AMB}\frac{(1/K_{chain}+K_{tune}H_{tissue}K_{LED})}{\left(1/K_{chain}+K_{LED}H_{tissue}+K_{LED}h(p)\right)^2} \tag{5-7}$$

Considering K_{chain} >> 1, i.e. the gain of the detection chain is way bigger than all the rest.

$$\frac{dV_o(p)}{dh(p)} = \frac{-I_{AMB}K_{tune}}{K_{LED}}\frac{1}{H_{tissue}+2h(p)+\frac{1}{H_{tissue}}h(p)^2} \tag{5-8}$$

The derivative is maximized for a given modulation when ambient light I_{AMB} is strong, or the K_{tune} parameter is large, or the gain of the LED driver K_{LED} is small. This result is expected and logical. The more light, the stronger the signal, and the smaller K_{LED}, the larger the variations in V_o for a given intensity variation.

As a conclusion, it's first interesting to observe that ambient light, as long as it doesn't reach the sensor directly, is beneficial to the detection. Hence, power can the spared by designing a system taking advantage of it. Second, K_{LED} must be kept small for a better demodulation. However, keeping it small adversely affects the lock range of the PLL. One can imagine a variable gain system: high when capturing and small when locked. The PPG signal being of very small bandwidth (a few tens of Hz), the system doesn't have to be fast and the loop filter can be designed accordingly in order to minimize the noise on V_o. By using a TDC instead of the standard phase-frequency comparator, the whole treatment can be performed digitally. This is especially interesting for the filter, which would then be digital, i.e. scalable with technology and independent of physical parameters. It is also important to note that the performances of the system rely on a precisely tunable LED current. However, most efficient LED drivers are of the switching type and only provide an ON-OFF modulation of the current. Nevertheless, due to the really low bandwidth of the physiological signal to be detected, the driver can be easily controlled by a high frequency PWM or ΔΣ signal and a good precision can be guaranteed.

A MATLAB-Simulink model (Fig. 5-32) of the loop using detector parameters extracted from measurement was created. It demonstrates the feasibility of the PLL based detection system and the ambient light tracking loop. The system was able to switch back and forth between the two control loops and the PLL locked in each case (Fig. 5-33)

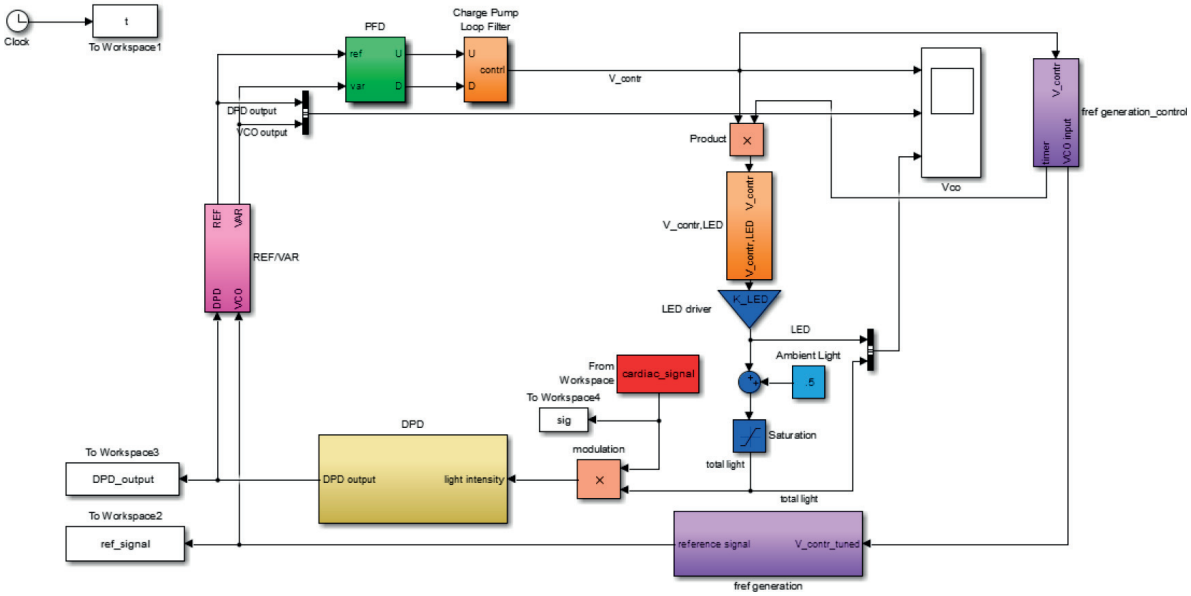

Fig. 5-32: Simulink model of the detection loop [76]

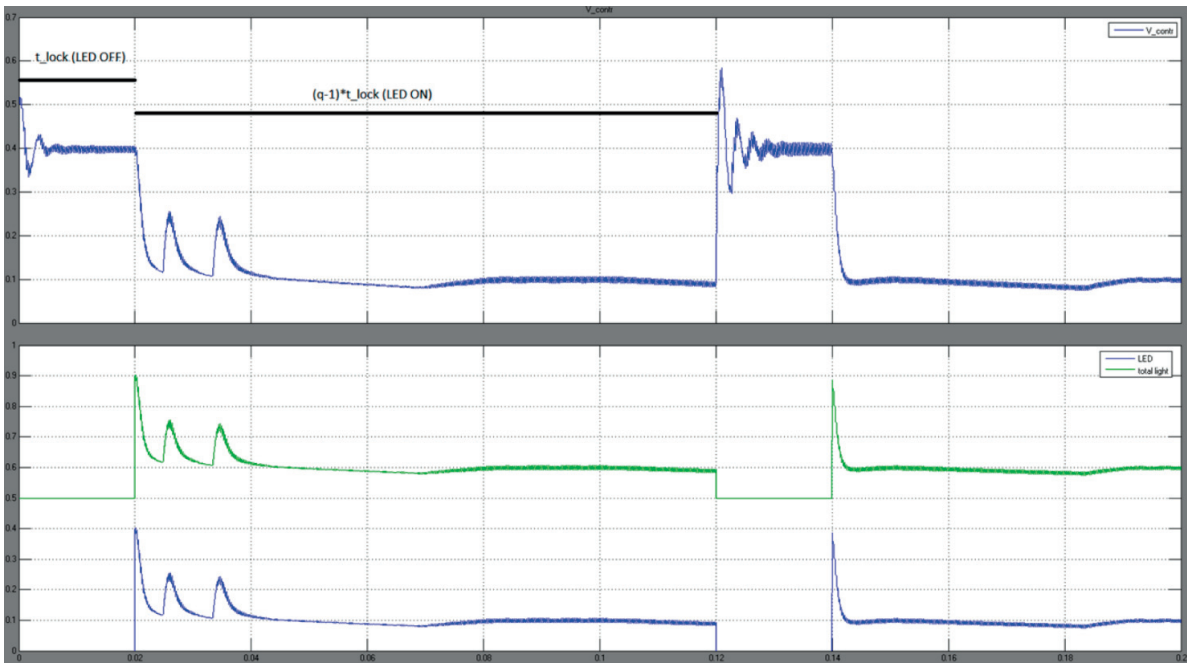

Fig. 5-33: Switch between the two control loops and locking of the PLL [76]

It is worth noting that the principle of the PLL-based detection system is independent from the Hybrid MOS-PN device and can be used with any photodetector capable of generating a PFM signal. In particular, the system can be built with a standard photodiode or a phototransistor as a detector. The concept of the PLL based detector with a phototransistor was demonstrated by building it on a Hirschman plate in the lab (Fig. 5-34).

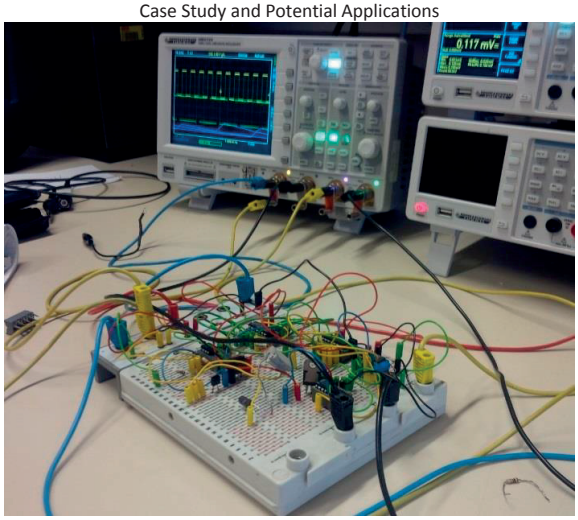

Fig. 5-34: Proof of concept of the PLL based detection system built on a Hirschman board

5.4 Array

Under the assumption that crosstalk interference between devices is not problematic, the Hybrid MOS-PN photodetector can be used to create arrays for imaging purposes. There are several ways to arrange the device of interest into arrays, depending on the amount of intelligence embedded at pixel level and the desired characteristics of the sensor in terms of dynamic range, fill factor, and size.

The time-domain operation of the detector makes it very suitable for a use in digital pixel sensors (DPS). In such an implementation, each pixel operates independently and performs analog-to-digital conversion at pixel level with its own memory and reset circuit. This increases the dynamic range of the array and avoids the rolling shutter effect that is present in standard CMOS image sensors (CIS). Those pixels are either based on PFM or PWM modulation schemes. Conceptually, both approaches have advantages and drawbacks, but chapters 2 and 3 showed that, due to the long reset time, PFM with the hybrid MOS-PN device is quite inefficient in terms of dynamic range and linearity. PWM, also called time to first spike, is thus the modulation of choice for this device.

Fig. 5-35 presents a digital pixel with embedded memory and asynchronous reset scheme using the Hybrid MOS-PN device. The asynchronous reset puts the detector in reset mode as soon as it triggers and thus avoids the large current spikes that would appears if the whole imager was resetted at once. In order to linearize the output, the pixel-level counter is driven by a variable frequency clock. The variable frequency is generated by a look-up table, as presented in section 2.2.1.

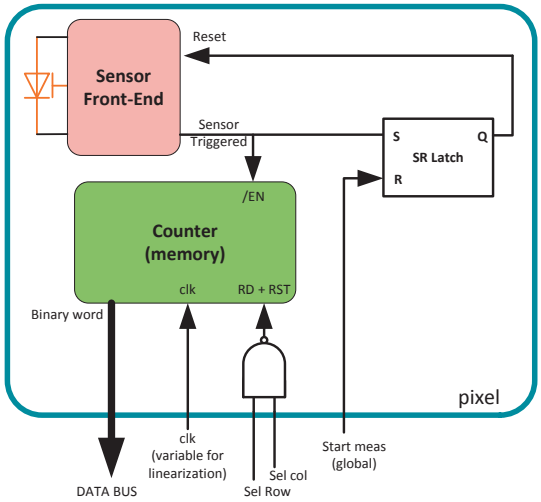

Fig. 5-35: Structure of a digital pixel using the Hybrid MOS-PN photodetector

The drawback of such an approach is the limited practical size of the memory that is reasonably implementable at pixel-level while keeping an acceptable fill-factor. Examples in literature limit the memory size to around 8 bits [58], and takes more than half of the pixel areas. In addition, even though the image is created at once, the read-out of each pixel is performed sequentially afterwards, which limits the achievable frame rate.

One way to increase the fill factor and speed-up the read-out while keeping the advantages the DPS is to avoid having one memory per pixel. Instead, each pixel generates an event when it triggers and a time-value associated with each pixel address is stored in a central memory. The complexity of such a system resides in the bus arbitration scheme that must handle priority when several pixels fire simultaneously. Bus arbitration also introduces imprecisions due to the fact that some pixels must “wait” to get a corresponding time-value attributed. This translates into a higher fixed pattern noise (FPN). The worst case scenario in precision appears for a uniformly illuminated or featureless scene where all the pixels trigger almost simultaneously.

A simpler approach that would keep the dynamic range advantage of the DPS but that would not need a bus arbitration circuit and thus have better precision and fill factor at the cost of image acquisition speed is to arrange the detectors in a “CMOS sensor” way, with the conversion taking place at the bottom of each column. In that scheme, detection and read-out is performed sequentially, one row after the other. Fig. 5-36 presents the principle of such a system. The drawback of such a system is slower acquisition time for a complete frame, which can become very large in low-illumination conditions.

A technological solution to greatly increase the fill factor of an array is to fabricate the detector and the circuit on two different silicon dies that are connected with through-silicon vias (TSV). In that case, each part of the system can be built independently and receive its own optimizations, e.g. optical coatings and low doping for the detectors and advanced CMOS process for the digital control and read-out circuits. A system design solution to increase the fill factor is to have a common driving circuit for each row, with only the detection transistors at pixel-level.

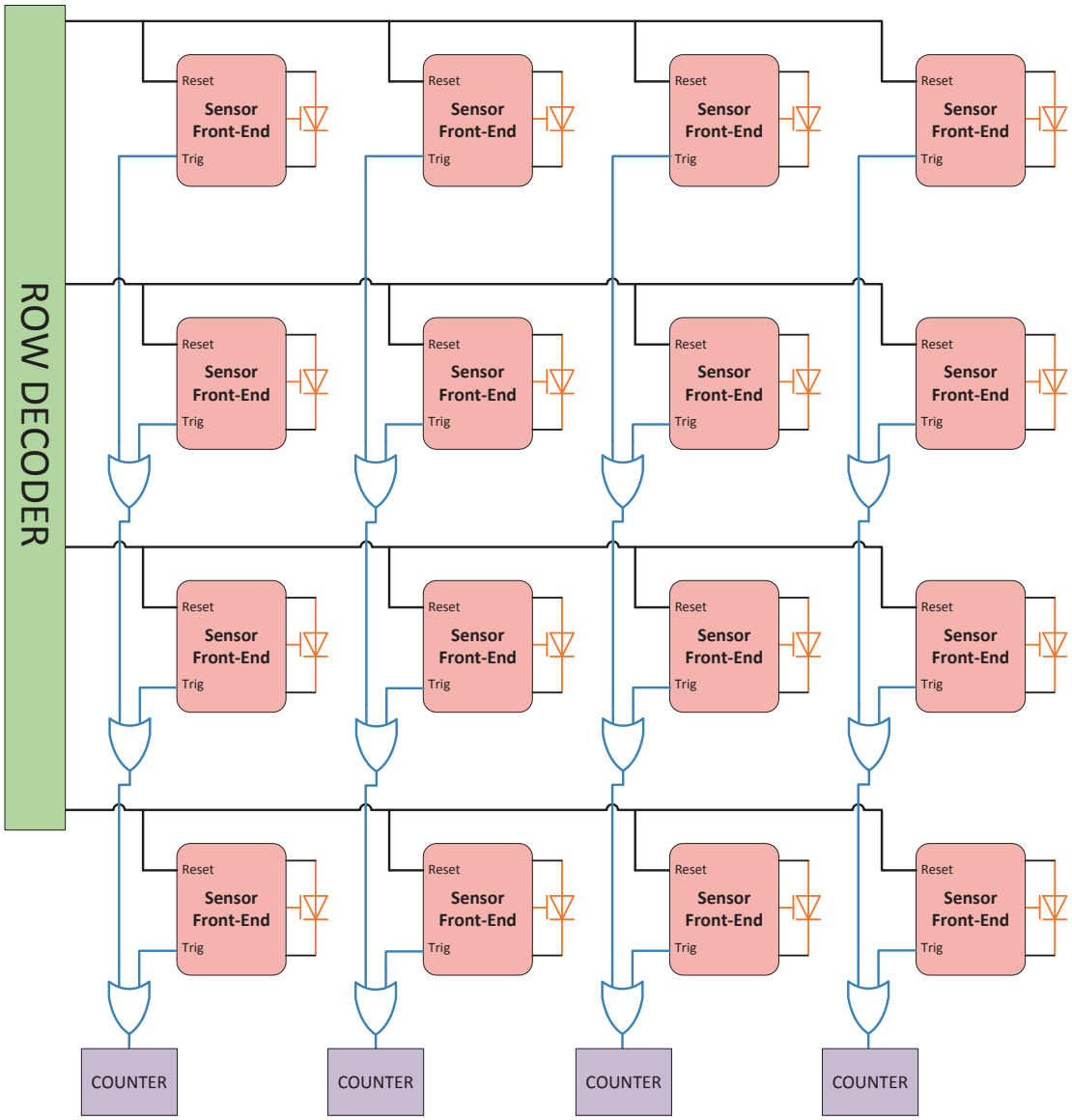

Fig. 5-36: Structure of a high fill-factor imager using the Hybrid MOS-PN photodetector.

5.5 Summary

In this chapter two working application demonstrators using the Hybrid MOS-PN device were first presented; a proximity detector system and an asynchronous light-barrier system.

It was then showed that the device can be modelled as an optical latch and therefore used as a logic element. Examples in clock recovery and phase comparison are given.

A system level approach using a PLL-based PPG detection system that can be used with the Hybrid MOS-PN device was then presented along with its proof of concept and MATLAB-Simulink model.

Finally, a discussion about the use of the device of interest in different types of arrays and their respective advantages and drawbacks was proposed.

Chapter 6 Conclusion

6.1 Achieved results

The main achievement of this thesis is the development of a new family of photodetectors displaying intrinsic light-to-time conversion and requiring almost no analog processing of their output signal. Their structure, based on a Hybrid MOS-PN combination, is fully compatible with standard CMOS processes. The concept was validated and optimized through TCAD simulations, and a prototype, including a readout circuit, was fabricated and measured.

In chapter 2, TCAD simulations performed to confirm the hypotheses about the physical behavior of the device at semiconductor level were presented. They allowed a refined understanding of the relations between the different parameters of the photodetector and its performances. The relations determining the sensitivity, signal-to-noise ratio, and dynamic range of the photodetector were proposed, as well a technique decreasing significantly dark current using voltage pulses instead of a DC bias.

The photodetector driver and front end circuits were designed and co-integrated with the sensor in a standard CMOS process, as shown in chapter 3. Those ASICS were used in a custom measurement system including a microcontroller and a USB connection to a computer. The measurement system was used to carry out a complete characterization of the photodetector, analyzing the influence of the different bias voltages and timings on light sensitivity and dark current. It was notably shown that the sensitivity of the device can be tuned by changing the gate voltage. The impact of the different bias conditions on noise was presented. The measurement system was also used to demonstrate the performance improvement when pulsed operation of the device is used.

In chapter 4 some technological solutions that could increase the performance and/or change the behavior of the device were presented. Notably, the effect of a silicon-on-insulator implementation on the performances of the proposed photodetector were studied using TCAD and its strong advantages in terms of dark current, linearity, and cross-talk analyzed. The optical properties of the SOI stack introduce a filtering phenomenon that could be interesting for some narrow light-spectrum applications, such as bioluminescence or fluorescence detection.

Potential applications of the device were presented in chapter 5. Demonstrators for proximity sensing and light curtain applications were realized. Digital applications taking advantage of the latching behavior of the detector were presented, such as clock recovery or phase detection. The use of the device in an optical heart-rate measurement system is also proposed and a PLL-based control loop aimed at reducing power consumption is proposed. Finally, concepts allowing to use the device in an array for imaging are presented.

In summary, it was shown that the Hybrid MOS-PN device has a strong potential in several application domains. Its time domain operation allows low light detection without the use of complicated electronics and its dynamic range is not limited by power supply voltage, allowing for low voltage high performance detection systems or low cost industrial applications. Its switching behavior makes it easy to interface with digital CMOS circuits, which makes it a good candidate device as optical clock receiver, for example. The simple driver and read-out circuit potentially makes it ideal to use in a Digital-Pixel-Sensor array, as well as other types of image sensors.

6.2 Future development

However, this thesis only scratched the surface in almost all aspects of device analysis and technological integration. Future work on the topic include

- Compact modelling of the device behavior with respect to technological parameters and bias conditions
- Complete noise analysis and modelling. Is shot noise the only intrinsic noise source? Is flicker noise present? How does the noise on the bias voltages translate into detection noise?
- Implementation of the proposed technological solutions, with a priority on fabrication of the device on SOI.
- Modelling of the device behavior on SOI
- Characterization of the crosstalk between devices, simulation and fabrication of an array.
- Analysis of scaling. How do the performances of the device scale with smaller technology nodes?

On the circuit and system side, a lot is to be done as well.

- Optimization of the front end circuit according to a reliable model of the device
- Characterization of the charge-equivalent noise of the front end
- Design of a very compact circuit optimized for pixel-level operation in arrays
- Exploration of techniques aimed at reducing the duration of the reset sequence
- Exploration of the feasibility of time-domain correlated double sampling with the device.
- Exploration of several types of control loops for dark and ambient current compensation, temperature compensation, dynamic range improvement, etc.
- Exploration of the operation of the device with new types of modulation, such as ΔΣ, that could be made possible with a modification of the device structure.
- Exploration of the use of the device as a digital component, design of optimized driver and front end circuits for this purpose.

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Curriculum Vitae

Denis Sallin
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STUDIES AND DIPLOMAS

2012-2015	**PhD in microelectronics** *École polytechnique fédérale de Lausanne (EPFL), Electronics Laboratory* Development and characterization of a new type of silicon photodetector and CMOS front end co-integration, in partnership with **ActLight S.A.** Author or co-author of more than 10 scientific publications
2006–2011	**BSc & MSc in Electrical Engineering** *École Polytechnique fédérale de Lausanne (EPFL)* Specialization: Electronics and Microelectronics
2003–2006	**High School Degree (Gymnasium)** *Gymnase de Nyon.* Option: Physics and applied mathematics

PROFESSIONAL EXPERIENCE

2012-2013	Partnership with **EM Microelectronic-Marin S.A**. in parallel with the PhD thesis. Design of an automated semiconductor measurement bench and transistor level characterization in order to improve a non-volatile memory process (EEPROM). Work performed in a cross-disciplinary team including process developers and circuit designers.
2011	Scientific Collaborator at the **Electronics Laboratory** (Elab) of EPFL High speed mixed-signal circuit design and complex multilayer printed circuit boards (PCB) design and fabrication in order to create a mixed-signal power network emulator. Part of a small design team that managed to successfully deliver a working system under tight time constraints and challenging fabrication process (400+ chips per board).
2004-2007	Summer jobs at **Novartis Consumer Health S.A.** Digitalization and classification of clinical trials related documents into a database. Inventory of scientific and legal archives.

COMPETENCES

Analog microelectronics and semiconductor physics

- Design of **CMOS** integrated circuits (180nm). Use of **Cadence Virtuoso** for design, simulation, and circuit layout.
- Knowledge of **photodetection** and of the different types of detectors. Photosensor and Front end circuit **co-integration** into a CMOS process. Device Level physics simulation using **Synopsys Sentaurus**.
- Application of the **ekv** transistor model to analog design.

Design, fabrication, and testing of mixed-signal electronics systems

- Mixed-Signal printed-circuit board (**PCB**) design up to 8 layers using Altium Designer.
- Analog structures (amplifiers, filtering, …) as well as complex blocks (PLL, demodulation, …)
- Microcontroller (**MCU**) programming (AVR, PIC, MSP430, ARM) in assembly and C language
- **FPGA** programming (Altera) in VHDL
- Analog-to-Digital and Digital-to-Analog converters (**ADC and DAC**) and digital communication protocols (**SPI, I2C, RS232, …**)
- Sensors and sub-systems interfacing (Wi-Fi modules, GSM modules)

Measurement, characterization, and semiconductor parameter analysis

- Design and use of automated measurement benches
- **Wafer probing**, use of parameter analyzers and switch matrices. Bench control using **LabVIEW**, communication via **GPIB** bus and SCPI commands
- Device-level electrical **Characterization** (MOSFET, parasitic BJT, diode)
- Results treatment and analysis using software such as **MATLAB**

LIST OF PUBLICATIONS

- D. Sallin, A. Koukab, and M. Kayal, "Optimized operation and temperature dependence of a direct light-to-time converter," in *New Circuits and Systems Conference (NEWCAS), 2015 IEEE 13th International*, 2015, pp. 1-4.
- D. Sallin, A. Koukab, and M. Kayal, "Toward direct light-to-digital conversion using a pulse-driven hybrid MOS-PN photodetector," *Optics letters,* vol. 40, pp. 669-672, 2015.
- D. Sallin, N. Abdo, A. Koukab, M. Estribeau, P. Magnan, and M. Kayal, "Silicon-on-insulator technology for bioluminescence imaging and application to a switching photodetector," in *Mixed Design of Integrated Circuits & Systems (MIXDES), 2015 22nd International Conference*, 2015, pp. 511-514.
- S. Okhonin, M. Gureev, D. Sallin, J. Appel, A. Koukab, A. Kvasov*, et al.*, "A dynamic operation of a PIN photodiode," *Applied Physics Letters,* vol. 106, p. 031115, 2015.
- N. Abdo, M. Estribeau, P. Magnan, D. Sallin, A. Koukab, and M. Kayal, "Optical effect considerations for bulk to SOI retargeting of hybrid MOS-PN dynamic photo-sensor," in *Advances in Sensors and Interfaces (IWASI), 2015 6th IEEE International Workshop on*, 2015, pp. 163-167.
- D. Sallin, A. Koukab, and M. Kayal, "Hybrid MOS-PN photodiode with positive feedback for pulse-modulation imaging," *Optics express,* vol. 22, pp. 14441-14449, 2014.
- D. Sallin, A. Koukab, and M. Kayal, "MOS-PN Hybrid Device With Minimum Dark Current for Sensitive Digital Photodetection," *Photonics Technology Letters, IEEE,* vol. 26, pp. 2062-2065, 2014.
- D. Sallin, A. Koukab, and M. Kayal, "Design of a direct light to time converter and its noise analysis," in *Electronics, Circuits and Systems (ICECS), 2014 21st IEEE International Conference on*, 2014, pp. 546-549.
- G. Lanz, L. Fabre, G. Lilis, T. Kyriakidis, D. Sallin, R. Cherkaoui*, et al.*, "Calibration of a mixed-signal power network transient stability analysis emulator," *International Journal of Microelectronics and Computer Science,* vol. 4, pp. 142-147, 2013.
- G. Lanz, L. Fabre, G. Lilis, T. Kyriakidis, D. Sallin, R. Cherkaoui*, et al.*, "Power network transient stability electronics emulator using mixed-signal calibration," in *Mixed Design of Integrated Circuits and Systems (MIXDES), 2013 Proceedings of the 20th International Conference*, 2013, pp. 369-373.
- T. Kyriakidis, G. Lanz, D. Sallin, G. Lilis, L. Fabre, R. Cherkaoui*, et al.*, "A mixed-platform framework for Dynamic Stability Assessment," in *Power and Energy Society General Meeting (PES), 2013 IEEE*, 2013, pp. 1-5.
- L. Fabre, D. Sallin, G. Lanz, T. Kyriakidis, I. Nagel, R. Cherkaoui*, et al.*, "A 3D architecture platform dedicated to high-speed computation for power system," in *PowerTech (POWERTECH), 2013 IEEE Grenoble*, 2013, pp. 1-6.
- L. Fabre, G. Lanz, T. Kyriakidis, D. Sallin, I. Nagel, R. Cherkaoui*, et al.*, "An ultra-high speed emulator dedicated to power system dynamics computation based on a mixed-signal hardware platform," *Power Systems, IEEE Transactions on,* vol. 28, pp. 4228-4236, 2013.

PRIZES AND AWARDS

- IEEE NewCAS 2015 conference **Best Student paper Award** (3rd rank)
- IEEE MIXDES 2015 conference **Outstanding Paper Award**
- Finalist of the **Texas Instruments European Analog Design Contest** 2013 (4th rank)
- **Excellence Award** of the *Gymnase de Nyon* (Best high-school final result)

LANGUAGES

French	English	German
Mother tongue	Full professional proficiency	Limited professional proficiency

EXTRA-PROFESSIONAL ACTIVITIES

- Students society (Verbindung, Fraternity) Valdésia: Secretary, former president
- Classical Guitar: Conservatoire, non-Professional certificate
- Military Service: technical sergeant-major

PERSONAL SITUATION

- Single
- Swiss nationality