Energy-Efficient Inexact Speculative Adder with High Performance and Accuracy Control

Vincent Camus, Jeremy Schlachter, Christian Enz

Ecole Polytechnique Fédérale de Lausanne (EPFL) - Integrated Circuits Laboratory (ICLAB)

vincent.camus@epfl.ch

Introduction

Approximate circuit design is a promising approach to improve performances and energy efficiency beyond the boundaries of conventional digital circuits. Such strategy is suitable for error-tolerant applications involving perceptive or statistical outputs. This work presents a novel architecture of an Inexact Speculative Adder [1,2] **for high-performance applications** with **optimized hardware and advanced error compensation technique**. This adder allows **precise tuning of accuracy** to match design specifications while optimizing performances and energy efficiency. It demonstrates power savings up to 26% and energy-delay-area reductions up to 60% compared to the state-of-the-art.

Inexact Speculative Adder (ISA)

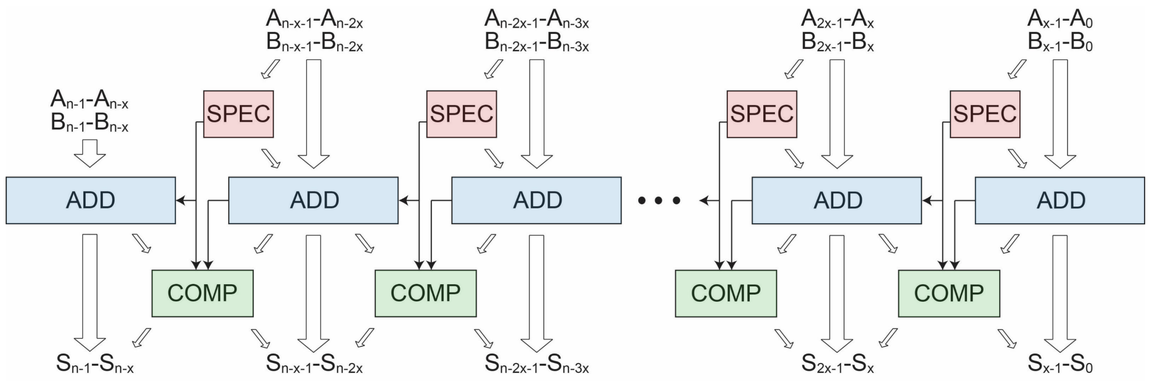

Fig. 1 *Block diagram of the Inexact Speculative Adder (ISA)*

- The ISA splits the adder in **multiple paths executed concurrently**.
- SPEC – The speculator generates a **carry signal from a limited number of input bits** in a carry look-ahead approach. When a propagate chain is longer than the SPEC size, exact carry cannot be guessed in a deterministic way.
- ADD – The sub-adder calculates partial sum from the speculated carry.
- COMP – Without compensation, internal overflows due to wrong speculations could lead to massive errors. Thus, the **COMP detects speculation faults and compensates faulty sums** either by attempting to correct local ADD sum or by reducing error magnitude on the prior ADD by a balancing technique [3].

Dual-Direction Compensation

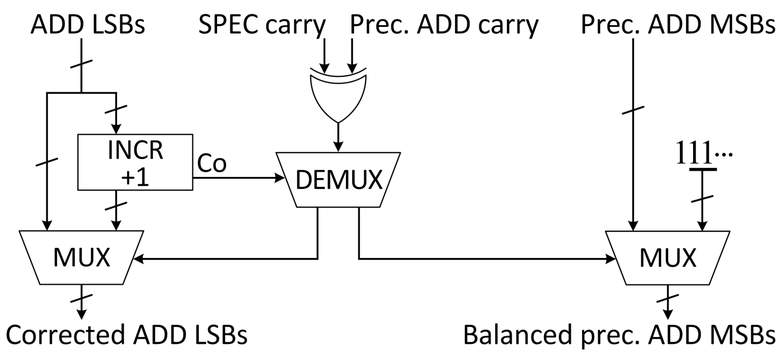

Fig. 2 *Example of COMP implementation.*

- Despite it is more complex to implement than the balancing, **the COMP corrective hardware (correction and compensation choice) is out of the critical path**, as it is precomputed in parallel with ADD.

- **The sign of the error remains the same as the one of the SPEC carry** (i.e. speculations at 0 instead of 1 induce *too low* sums and conversely). **Correction consists in an unsigned increment/decrement** in that direction.

- On the **fixed and short bit-width of the COMP, correction is possible only if it does not cause any overflow** (e.g. with a correction operating on 3 bits, incrementing 111_2 and decrementing 000_2 are irrelevant). Detecting this overflow allows to choose the right compensation technique to apply.

Design and Characterization

- In this work, **32-bit** adders with **uniformly sized blocks** (i.e. parallel paths of 2x16, 4x8, 8x4 and 16x2 bits) have been synthesized in **65 nm technology**.

- Inexact adders have been characterized with metrics based on the **relative error (*RE*)** of an inexact sum compared to the exact one. **RMS of *RE* (mean accuracy)** and **maximum of *RE* (worst-case accuracy)** are considered.

- Adders have been characterized through simulations of two sets of five million unsigned random inputs:
  - A uniform distribution to estimate the mean accuracy RE_{RMS}
  - A logarithmically uniform distribution to observe the worst-case RE_{MAX}

Addition Arithmetic and Errors

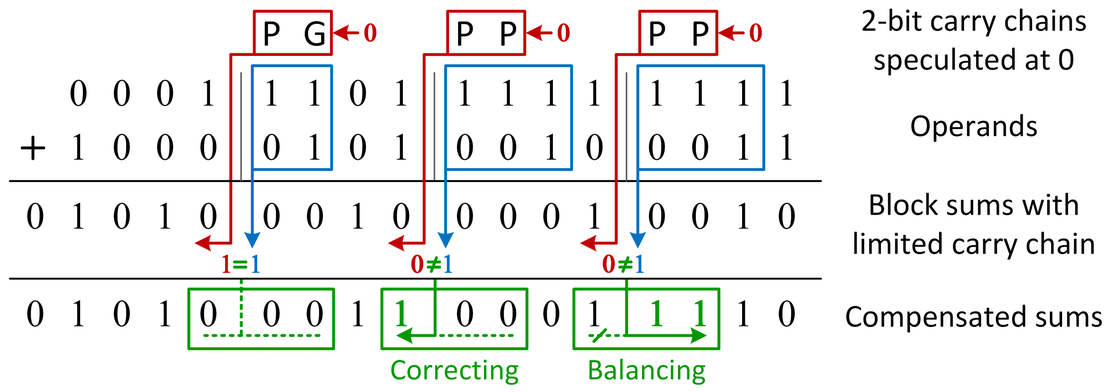

Fig. 3 *Example of ISA addition arithmetic with 2-bit SPEC, 1-bit correction and 2-bit balancing. Faults only occur in the two right-hand paths. The 1st LSB of the central path can be corrected. The 1st LSB of the right path cannot, so the first two MSBs of the preceding sum are flipped.*

- Comparison of speculated carry-in and prior sub-adder carry-out allows to detect faulty speculation. In this case, **correction is attempted on LSBs of the local sum**. If correction is not possible, **MSBs of the preceding sum are balanced** to reduce the error magnitude.

- Each element sizing impacts on the overall error characteristics:
  - SPEC → error rate and mean relative error
  - COMP balancing, longer than SPEC → mean relative error
  - COMP balancing, shorter than SPEC → mean and max relative error
  - COMP correction → error rate, mean and max relative error

Results I – High Efficiency and Tunability

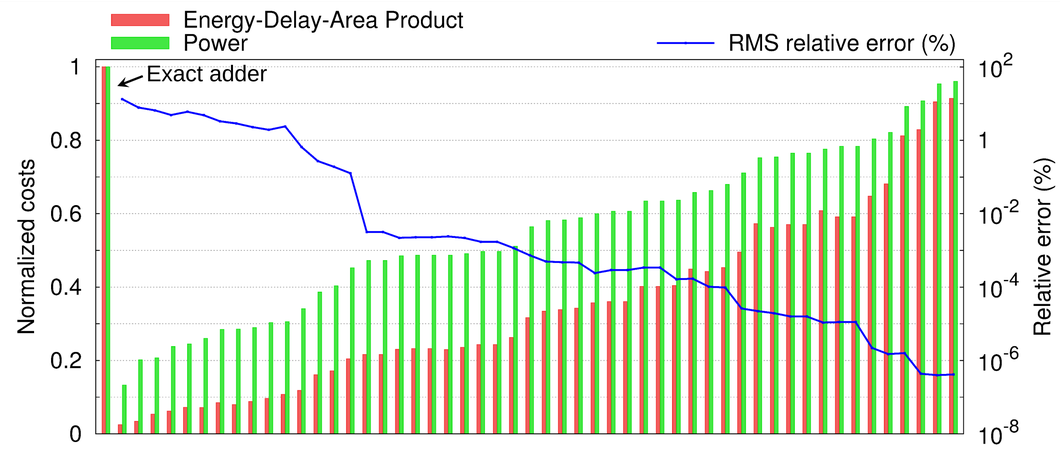

Fig. 5 *Normalized costs and accuracy of various uniform-block-sized 32-bit ISA at 3.3 GHz.*

- Results demonstrate **large savings** and **wide accuracy control range**.
  - 65% power reduction and 88% EDAP savings for 1% error RMS
  - 50% power reduction and 73% EDAP savings for 0.001% error RMS

Results II – Comparative Study

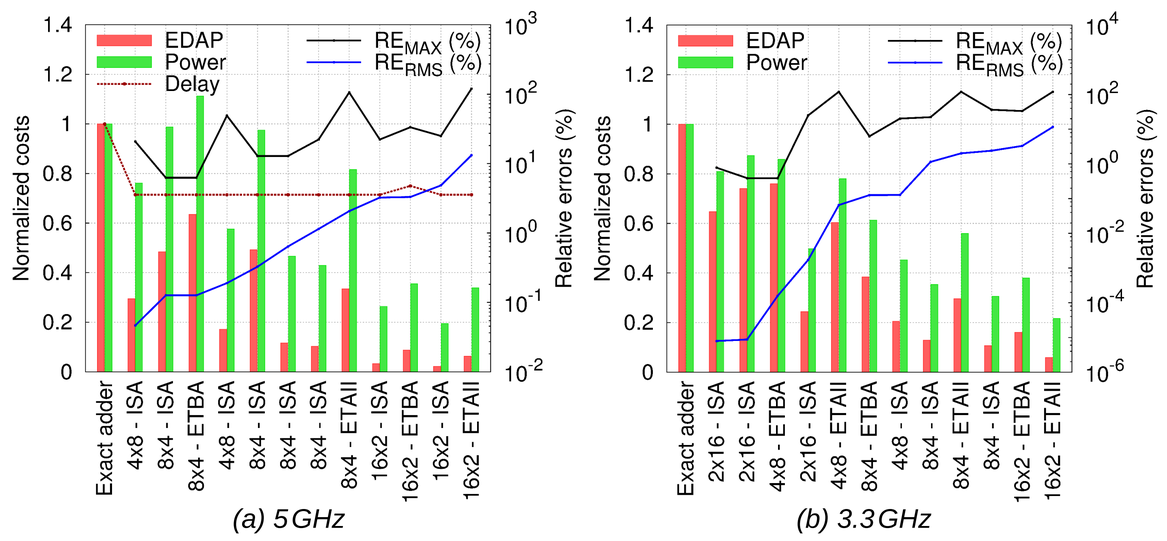

Fig. 6 *Design costs and accuracy of 32-bit speculative adders (ISA [1], ETAII [4] and ETBA [3]) synthesized at 5 GHz (a) and 3.3 GHz (b). Delay is shown in (a) as the exact adder cannot fit the 5 GHz constraint and 16x2 ETBA suffers from a drop of efficiency exactly at synthesized speed, so it is replaced with a slightly slower version for fair comparison.*

Conclusion

The Inexact Speculative Adder (ISA) offers a general topology of speculative compensated addition inclusive of the state-of-the-art and that allows notable improvements in circuit performances and accuracy tunability. It can easily be designed through a delay-accuracy trade-off approach and could simply be modeled and built in characterized libraries of approximate components.

Sponsors

FNSNF nano-tera.ch

References

[1] V. Camus *et al.*, "Energy-efficient inexact speculative adder with high performance and accuracy control," *ISCAS*, 2015
[2] V. Camus *et al.*, "Energy-efficient digital design through inexact and approximate arithmetic circuits," *NEWCAS*, 2015
[3] M. Weber *et al.*, "Balancing adder for error tolerant applications," *ISCAS*, 2013.
[4] N. Zhu *et al.*, "An enhanced low-power high-speed adder for error-tolerant application," *ISIC*, 2009.

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

iclab.epfl.ch/inexact