# Full Swing 20 GHz Frequency Divider with 1 V Supply Voltage in FD-SOI 28 nm Technology

Hasene Gulperi Ozsema, Duygu Kostak, Tugba Demirci, Yusuf Leblebici
Microelectronic Systems Laboratory (LSM)
Ecole Polytechnique Federale de Lausanne (EPFL)
Lausanne, 1015, Switzerland
Email: hasene.ozsema@epfl.ch, duygu.kostak@epfl.ch, tugba.demirci@epfl.ch, yusuf.leblebici@epfl.ch

***Abstract*—In this paper we present the design of a programmable frequency divider in 28 nm FD-SOI CMOS technology. It consists of the cascade of a divide-by-2 cell and divide-by-2/3 blocks. The final circuit is capable of dividing by even numbers between 128 and 254. The forward-body-bias property of the process and the differential-cascode voltage-switch-logic (DCVSL) family are used to achieve high operation speed. The proposed circuit achieves a maximum operating frequency of 20 GHz at 1 V supply voltage. And the area and the power consumption of the programmable divider are 1815 $\mu m^2$ and 4.35 mW, respectively.**

## I. Introduction

High-speed frequency divider design is crucial for frequency synthesizers, clock generators, clock and data recovery circuits and satellite communication systems. In the 1980s and 1990s, designers preferred to use high-$f_T$ technologies like GaAs and BiCMOS in order to divide signals at tens of GHz frequency [1]–[3]. Afterwards, as the technology nodes went below 1 $\mu$m, it was possible to design multi-gigahertz speed frequency dividers in CMOS. The architectures of these CMOS dividers were commonly based on limited-output-swing current-mode-logic (CML) or LC injection-lock topologies [4]–[7].

Today, the $f_T$ performance has dramatically increased with the availability of sub-100nm technologies. And, the potential of these new technologies for high-speed applications has been demonstrated. These technologies, however, suffer from the reduced supply voltage. On account of the drop in supply voltage, it is very hard to use cascode architectures and the circuits consume more power to keep the signal integrity at an acceptable level. Fully-Depleted Silicon-on-Insulator (FD-SOI) CMOS technology is a solution that can operate faster than bulk CMOS at the same supply voltage as it benefits from the body-bias techniques [8]. This body-bias property of FD-SOI technology has been exploited in various applications such as memories, arithmetic logic units and voltage controlled oscillators [9]–[11].

In this paper, we will present a programmable frequency divider in 28 nm FD-SOI technology. Its topology consists of the cascade of divide-by-2 and divide-by-2/3 dividers. It can divide by the even numbers between 128 and 254. The speed of the design has been increased by using the forward-body-bias technique available in FD-SOI technology. The resulting circuit achieves a maximum operating frequency of 20 GHz at 1 V supply voltage without resorting to CML or LC injection-lock topologies.

978-1-4673-6576-5/15/$31.00 ©2015 IEEE

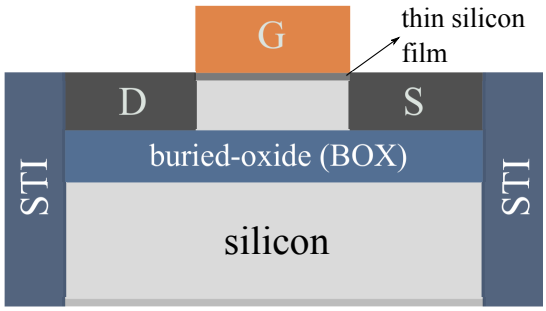


Fig. 1. Cross-sectional view of the FD-SOI device

In Section II the features of the FD-SOI technology are explained. Section III discusses the properties of the state-of-the-art high-speed frequency dividers. Section IV is about the details of the proposed programmable frequency divider. In Section V, the simulation results are presented. Finally, concluding remarks will be given in Section VI.

## II. Features of SOI Technology

From the invention of the integrated circuit (IC), year 1958, to date, the trend in IC design has been to scale down the minimum feature size. However, recent studies of *'International Technology Roadmap for Semiconductors' (ITRS)* shows that the pace of scaling is slowing down [12]. The main reason of this slowdown is the inferior transistor performance in nanometer regime. The transistor has degraded device mobility and increased leakage in these scaled technologies. Also, the reduction of the threshold voltage and the supply voltage has reached a limit. All these facts lead to flattening of the CMOS performance. FD-SOI is a planar technology that is a candidate to solve the problems of bulk silicon starting at the 28 nm node and scalable down to 14 nm [13].

Figure 1 illustrates the cross-sectional view of the FD-SOI device. The structure is composed of a thin body and a layer of oxide below the surface that is called the buried oxide (BOX). FD-SOI structure has many advantages over their bulk silicon counterpart among which the most important ones are: negligible drain-to-substrate capacitance, immunity to latch up, simple device isolation, reduced short channel effects, mitigated floating body effects and availability of body biasing [14].

In this work, we will take advantage of the body biasing feature which enables the adjustment of the threshold voltage.

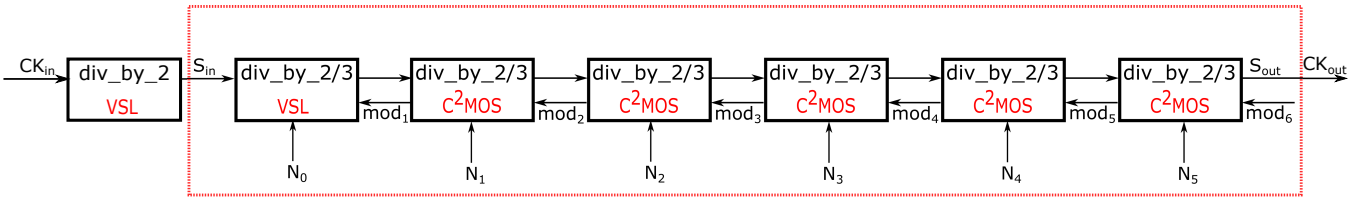


Fig. 2. Overall structure of the programmable frequency divider

Also, we will show that it is possible to control the speed of the circuit via body biasing.

## III. State of the Art

The most important specifications of a frequency divider are speed, power consumption, area (number of transistors) and flexibility. Recently, inductorless divider designs employed the CML family or True-Single-Phase-Clock (TSPC) logic family to increase the speed. Several design examples can be found in the literature [15]–[19].

Although CML circuits can achieve a very high operation frequency, they suffer from static power consumption. Also, their small output signal swing makes the approach sensitive to process and environmental variations. Moreover, usually a calibration block is necessary to avoid the variations in the output swing. And, when the dividers implemented with CML topology are used in the applications, they require an interface circuit to convert their output signal to CMOS levels. On the other hand, successful rail-to-rail high speed dividers utilizing TSPC architectures exist. Nevertheless, problems arose when the reset operation is in function. In high speed and programmable structures, it is hard to reset all internal nodes to proper voltage levels if TSPC logic is preferred. Due to these mentioned problems, a different approach is necessary for the construction of rail-to-rail high speed frequency divider design in modern technologies.

## IV. Divider Design

The proposed programmable divider is presented in Figure 2. It has a modular design, and it is comprised of a divide-by-2 cell and six cascaded divide-by-2/3 blocks. The final design can divide by any even number in the range between 128 and 254. The divide-by-2 circuit and the cascade of divide-by-2/3 dividers will be analysed in detail in the following subsections.

### A. Divide-by-2 Stage

In general, a divide-by-2 circuit can be realised by only one D flip-flop (DFF) configured as in Figure 3a. This topology is chosen for the divide-by-2 block designed in this work as well. Since the aim is to achieve very high operation speed, conventional DFF architectures are not eligible. Differential-cascode voltage-switch-logic (DCVSL) family is suitable to be used in high frequency designs. It offers the advantages of low transistor count, small switching capacitance and small input capacitance [20]. On account of these advantages, DCVSL logic is preferred to construct the DFF of divide-by-2 divider. The schematic of the DCVSL latch can be seen in Figure 3b. This structure is also named as saturated-type latch since the outputs can swing from rail to rail. The proposed architecture includes a pair of

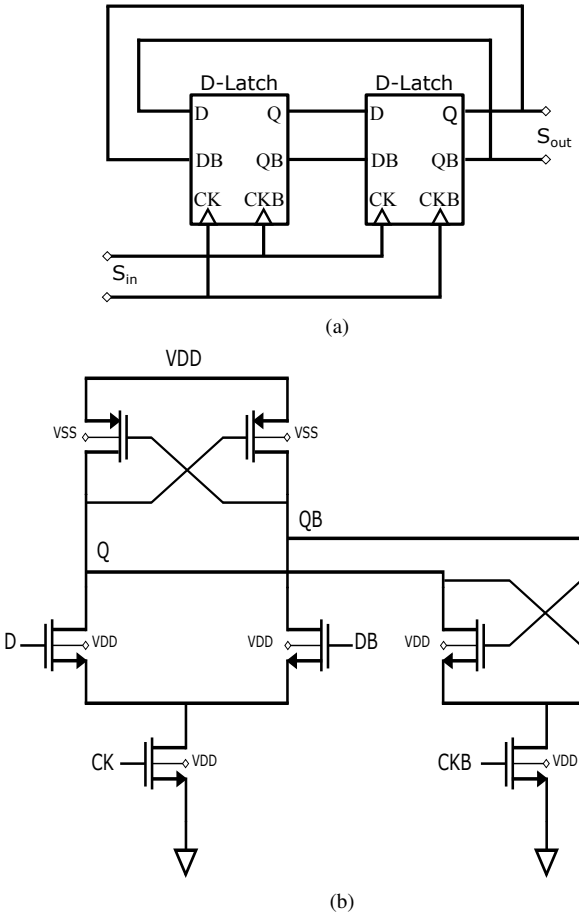


Fig. 3. (a) Divide-by-2 architecture (b) Schematic of the DCVSL latch

cross-coupled PMOS transistors providing positive feedback, which is helpful to sharpen the transition edges of the output signal and to increase the speed of the gate. Also, the topology can produce inverting and non-inverting outputs. Here, the first two branches act as clocked inverters and the cross-coupled NMOS pair is used to hold the data. When the clock signal is high, the inverter operation is in function whereas the latch enters the hold mode when the clock signal goes low. Another point is that the forward body biasing (FBB) feature of the FD-SOI technology is utilized to achieve the lowest possible threshold voltage and to increase the speed. In the given configuration the body voltage of the NMOS transistors is set to the supply while the body voltage of the PMOS transistors is set to the ground to apply the FBB.

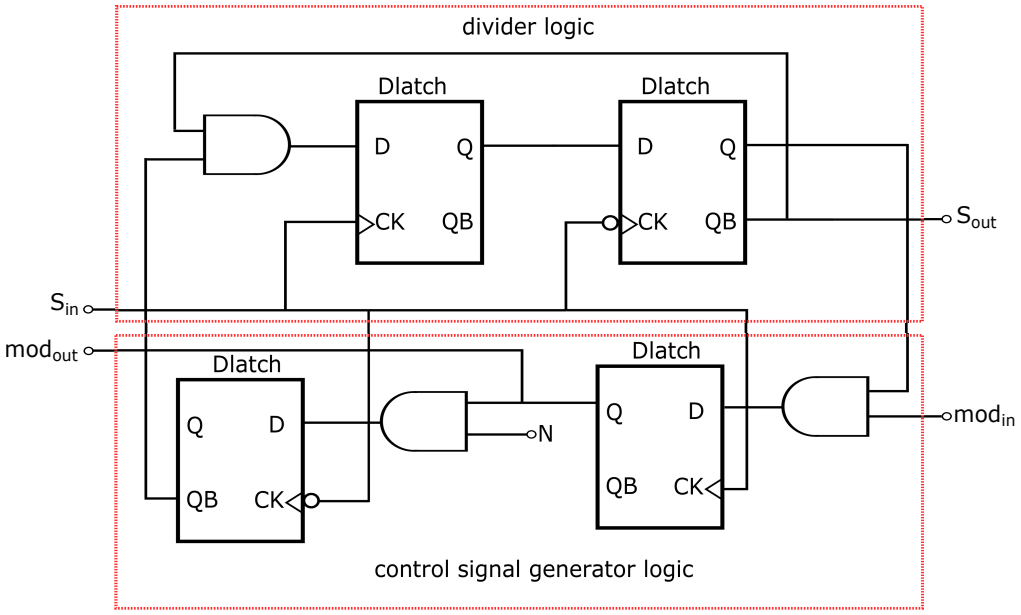


Fig. 4. Structure of the 2/3 divider

### B. Cascade of Divide-by-2/3 Dividers

The chain of six cascaded divide-by-2/3 units illustrated in Figure 2 is capable of dividing their input signal by any number from 64 to 127. It is important to set the outputs of these cells to proper voltage levels at the start up to avoid cycle skipping. Therefore, all cells are resettable. The 6-bit $N_{5:0}$ signal represents the integer divide ratio and each $N_i$ determines whether the individual cells will divide by 2 or 3. The frequency is divided by 2 when *N* is low, and it is divided by 3 when *N* is high. The $mod_{in}$ signal is a feedback input coming from the next stage in the cascaded chain and it determines when to check the *N* signal to decide division by 2 or 3. Division by 3 is achieved by swallowing one extra period of the input signal. The $mod_{in}$ is reclocked and sent out through $mod_{out}$ at the end of the division cycle. The structure is modular, and this eases the layout work and shortens the design time. Moreover, there are only local feedbacks between the adjacent cells, so long delay loops do not exist.

There can be several interpretations of divide-by-2/3 dividers, but the modular divide-by-2/3 architecture proposed in [21] has been used in our divider. The gate level schematic is shown in Figure 4. Here, $S_{in}$ is the input to be divided. *N* and $mod_{in}$ are the control signals that decide the division ratio and $S_{out}$ is the divided output signal. The overall architecture is composed of 4 D-latches and 3 AND gates. The speed is determined by the D-latch as there is a feedback loop which includes all of the latches.

The first cell of the chain is designed with DCVSL topology while the remaining cells are designed with $C^2MOS$ logic based on the work in [22]. The reason of this choice is to save area and power at the consequent stages as they are not expected to operate at very high frequencies. The FBB is applied to these cells as well to establish the uniformity of the design.

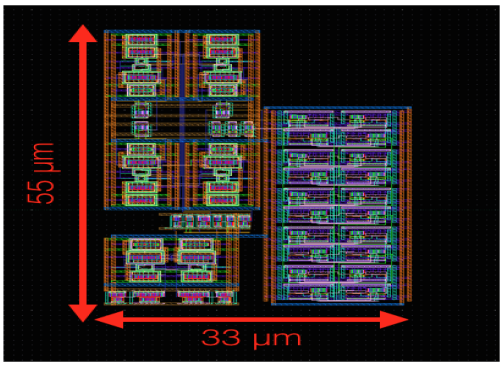


Fig. 5. Layout of the programmable divider

## V. Simulation Results

The programmable frequency divider is designed in 28 nm FD-SOI CMOS technology. The photo of the layout is shown in Figure 5. The dimensions of the layout are 33 $\mu$m x 55 $\mu$m.

The functionality of the divider is tested at the typical corner with a temperature of 120 $^oC$ and a supply voltage of 1 V . It divides correctly up to 20 GHz for all possible divide ratios (from 128 to 254). An example input-output waveform with the output signals of all divide stages can be seen in Figure 6. Here, the division ratio for the output frequency ($CK_{OUT}$) is 254. The extra swallowed period required by divide by 3 operation is clearly visible at all outputs.

The performance of the designed circuit according to the post layout simulation is summarised in Table I. When the performance is compared with the recent works, it is seen that CML topology tend to operate faster owing to its small output signal swing. However, our rail-to-rail divider has comparable speed with CML implementations. Furthermore, it offers programmability with reasonable power consumption and area occupancy.

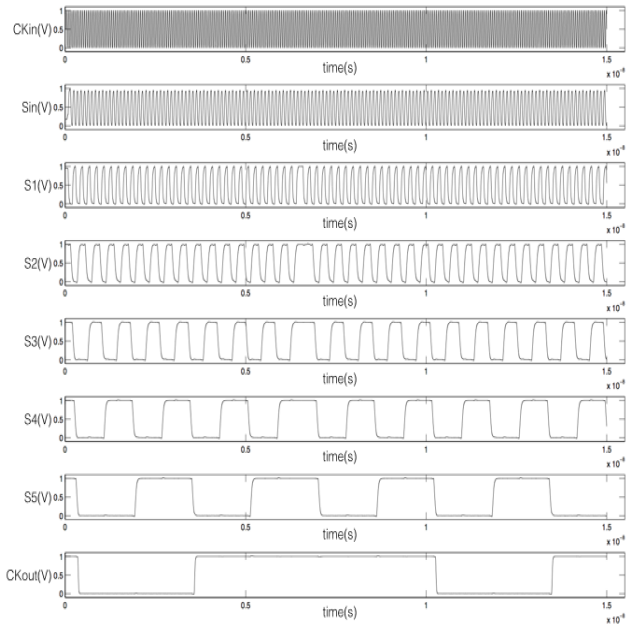


Fig. 6. Divider performance at 120 $^oC$ for an input frequency of 20 GHz

TABLE I. COMPARISON OF THE PERFORMANCES OF THE FREQUENCY DIVIDERS

| | [16] | [17] | [19] | This Work |
|---|---|---|---|---|
| **Technology** | 28nm CMOS | 90nm CMOS | 65nm CMOS | 28nm FD-SOI |
| **Topology** | CML | CML | TSPC | DCVSL |
| **Max. Frequency** | 26 GHz | 24 GHz | 17 GHz | 20 GHz |
| **Output Swing** | **Limited** | **Limited** | **Rail-to-Rail** | **Rail-to-rail** |
| **Power supply** | 1 V | 1.5 V | 1V | 1 V |
| **Programmability** | No | Yes | Yes | Yes |
| **Power Consumption** | 5.6 mW | 2.25 mW | 2 mW | 4.35 mW |
| **Area** | 490 $\mu m^2$ | 1428 $\mu m^2$ | 1250 $\mu m^2$ | 1815 $\mu m^2$ |

## VI. CONCLUSION

This paper presented a modular and programmable frequency divider. These features are achieved by employing the cascade of division cells. The high frequency blocks are designed with DCVSL family. And the remaining blocks are formed with $C^2MOS$ logic. Also, the FBB property of the FD-SOI technology is used to further increase the speed. Owing to these techniques, the divider can achieve a very high operation speed of 20 GHz at 120 $^oC$. The supply is 1 V and the outputs can swing from rail to rail. Simulation results show that the whole circuit consumes 4.35 mW. Based on this data, our design is suitable to be used as a divider in high speed frequency synthesisers, clock generators and data recovery circuits.

## REFERENCES


[1] K. Wang, P. M. Asbeck, M. Chang, G. Sullivan, and D. Miller, "A 20-ghz frequency divider implemented with heterojunction bipolar transistors," *IEEE electron device letters*, vol. 8, no. 9, pp. 383–385, 1987.

[2] Y. Amamiya, T. Niwa, N. Nagano, M. Mamada, Y. Suzuki, and H. Shimawaki, "40-ghz frequency dividers with reduced power dissipation fabricated using high-speed small-emitter-area algaas/ingaas hbts," in *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1998. Technical Digest 1998., 20th Annual*. IEEE, 1998, pp. 121–124.

[3] P. Weger, A. Felder, M. Kerber, and H. Klose, "Versatile divider circuits up to 9 ghz input-frequency realised in high-speed bicmos," *Electronics Letters*, vol. 26, no. 23, pp. 1942–1944, 1990.

[4] M. Usama, T. Kwasniewski *et al.*, "A 40 ghz quadrature lc vco and frequency divider in 90-nm cmos technology," in *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*. IEEE, 2007, pp. 3047–3050.

[5] C. Cao *et al.*, "A power efficient 26-ghz 32: 1 static frequency divider in 130-nm bulk cmos," *Microwave and Wireless Components Letters, IEEE*, vol. 15, no. 11, pp. 721–723, 2005.

[6] B. De Muer and M. Steyaert, "A 12 ghz/128 frequency divider in 0.25 $\mu$m cmos," in *Solid-State Circuits Conference, 2000. ESSCIRC'00. Proceedings of the 26rd European*. IEEE, 2000, pp. 248–251.

[7] Q. Gu, Z. Xu, D. Huang, T. LaRocca, N.-Y. Wang, W. Hant, and M.-C. F. Chang, "A low power v-band cmos frequency divider with wide locking range and accurate quadrature output phases," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 4, pp. 991–998, 2008.

[8] K. Bernstein and N. J. Rohrer, *SOI circuit design concepts*. Springer Science & Business Media, 2007.

[9] V. Asthana, M. Kar, J. Jimenez, J.-P. Noel, S. Haendler, and P. Galy, "Circuit optimization of 4t, 6t, 8t, 10t sram bitcells in 28nm utbb fd-soi technology using back-gate bias control," in *ESSCIRC (ESSCIRC), 2013 Proceedings of the*. IEEE, 2013, pp. 415–418.

[10] T. Fuse, Y. Oowaki, T. Yamada, M. Kamoshida, A. Ohta, T. Shino, S. Kawanaka, M. Terauchi, T. Yoshida, G. Matsubara *et al.*, "A 0.5 v 200 mhz 1-stage 32 b alu using a body bias controlled soi pass-gate logic," in *Solid-State Circuits Conference, 1997. Digest of Technical Papers. 43rd ISSCC., 1997 IEEE International*. IEEE, 1997, pp. 286–287.

[11] A. Fonseca, G. Jacquemod, Y. Leduc, E. De Foucauld, and P. Lorenzini, "Vco design in soi technologies," in *New Circuits and Systems Conference (NEWCAS), 2014 IEEE 12th International*. IEEE, 2014, pp. 420–423.

[12] International roadmap for semiconductors (itrs) 2010 update. [Online]. Available: http://www.itrs.net

[13] P. Flatresse, G. Cesana, and X. Cauchy. Planar fully depleted silicon technology to design competitive soc at 28nm and beyond. [Online]. Available: http://www.soitec.com

[14] T. Sakurai, A. Matsuzawa, and T. Douseki, *Fully-depleted SOI CMOS circuits and technology*. Springer, 2006.

[15] A. Ghilioni, U. Decanis, E. Monaco, A. Mazzanti, and F. Svelto, "A 6.5 mw inductorless cmos frequency divider-by-4 operating up to 70ghz," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*. IEEE, 2011, pp. 282–284.

[16] L. Szilagyi, G. Belfiore, R. Henker, and F. Ellinger, "Low power inductor-less cml latch and frequency divider for full-rate 20 gbps in 28-nm cmos," in *Microelectronics and Electronics (PRIME), 2014 10th Conference on Ph. D. Research in*. IEEE, 2014, pp. 1–4.

[17] A. Axholt and H. Sjöland, "A 2.25 mw inductor-less 24 ghz cml frequency divider in 90nm cmos," in *Circuit Theory and Design (ECCTD), 2011 20th European Conference on*. IEEE, 2011, pp. 77–80.

[18] W. Zhu, H. Yang, T. Gao, F. Liu, T. Yin, D. Zhang, and H. Zhang, "A 5.8-ghz wideband tspc divide-by-16/17 dual modulus prescaler," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 23, no. 1, pp. 194–197, 2015.

[19] M. V. Krishna, A. Jain, N. Abdul Quadir, P. D. Townsend, and P. Ossieur, "A 1v 2mw 17ghz multi-modulus frequency divider based on tspc logic using 65nm cmos," in *European Solid State Circuits Conference (ESSCIRC), ESSCIRC 2014-40th*. IEEE, 2014, pp. 431–434.

[20] D. Z. Turker, S. P. Khatri, and E. Sánchez-Sinencio, "A dcvsl delay cell for fast low power frequency synthesis applications," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 58, no. 6, pp. 1225–1238, 2011.

[21] C. S. Voucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli, and Z. Wang, "A family of low-power-truly modular programmable dividers in standard 0.35 um cmos technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1039–1045, 2000.

[22] S.-M. Kang and Y. Leblebici, *CMOS digital integrated circuits*. Tata McGraw-Hill Education, 2003.