CRYOGENIC SINGLE CHIP ELECTRON SPIN RESONANCE DETECTORS

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A Denise...

Abstract

Methods based on the electron spin resonance (ESR) phenomenon are used to study paramagnetic systems at temperatures that ranges from 1000 to below 1 K. Commercially available spectrometers achieve spin sensitivities in the order of 10^{10} spins/$\sqrt{\text{Hz}}$ at room temperature on sample with volumes in the order of few μl. This results can be improved by cooling the system at cryogenic temperatures, where the larger magnetization of paramagnetic samples cause the detected signal to increase. In systems where the noise is mainly due to thermal fluctuations, operation at low temperatures cause a lowering in the noise floor. Furthermore operation at high field (frequency) turns as well in an improved spin sensitivity. For what it concern the spin sensitivity operation at cryogenic temperature and high frequency are thus beneficial. In 2008 the group of Dr. G. Boero proposed a novel detection method based on the integration of all the element responsible for the sensitivity on a single silicon chip. The methodology allowed to study sample with nanoliter scale volume with spin sensitivity that were at least two orders of magnitude better than the best commercial spectrometer. The proposed method has performance that are comparable with the one obtained on similar scales with micro-resonator based spectroscopy tool and was proved to work for frequency up to 28 GHz and temperature down to 77 K. The detection principle can be summarized as follow. An ESR sensitive sample is placed at the center of an integrated LC oscillator operating at microwave frequency. The resonance phenomenon cause a variation in the sample magnetization that hence translate into an inductance variation. The resonance is thus detected through oscillator frequency variations. During this thesis I have investigated the possibility of extending the use of this detection method up to 200 GHz and down to 4 K. In this frame several domains were touched. First of all the design of CMOS silicon oscillators operating at frequency which are closed to the most modern technology frequency limit. The lack of model valid for the target frequencies and the needs of limiting the power consumption for matching the limited cooling power of cryogenic systems, made the subject a challenging and interesting research topic itself. The study produces a remarkable result of a system operating at about 170 GHz with a power consumption of about 3 mW at room temperature and about 1.5 mW at 4 K. With the realized devices the first measurements of integrated silicon CMOS LC oscillators at temperature below 77 K were performed. From this measurements we could confirm the presence of expected effect, such as minimum power consumption reduction and oscillator frequency increase. In addition to that, by measuring the frequency-bias characteristic, it's been noticed a succession of smooth region and sharp transitions. This jumps are tentatively attributed to the random telegraph signal (RTS) effect that is supposed to be the

main responsible for the flicker noise in sub-micrometer MOS devices. Since the impact of RTS on the performance of highly scaled transistor is expected to grow with the technology scale down, measurement methods based on LC oscillator, that shows better sensitivity if compared with nowadays employed methods, might allow to better understand the mechanism governing the effect and to develop technological strategy for lowering the impact on the future CMOS technology node. The realized devices have sensitive volumes that range from the 250 pl for the 21 GHz system to the 10 pl for the 170 GHz one. They have demonstrated ESR performances that are comparable with the most recent publication done with miniaturized resonators on mass-limited samples. The measured sensitivity are of about 10^7 spins/$\sqrt{\mathrm{Hz}}$ at 50 GHz and 300 K and of about 10^6 spins/$\sqrt{\mathrm{Hz}}$ at 28 GHz and 4 K with DPPH samples, at least 3 orders of magnitude better then commercially available state of the art devices. Finally preliminary sensitivity computation based on the electronic characterization of the realized device, predict a spin sensitivity of about 10^6 spins/$\sqrt{\mathrm{Hz}}$ at 170 GHz and room temperature and 10^4 spins/$\sqrt{\mathrm{Hz}}$ at 50 GHz and 4 K.

Key words: Electron spin resonance, ESR, ESR spectroscopy, LC oscillator, CMOS, microwave, cryogenic, random telegraph signal, RTS.

Riassunto

I metodi basati sul fenomeno della risonanza di spin elettronico sono utilizzati per studiare sistemi paramagnetici a temperature che vanno da 1000 a meno di 1 K. Gli spettrometri disponibili in commercio raggiungono una sensibilità di spin dell'ordine di 10^{10} spins/$\sqrt{\text{Hz}}$ a temperatura ambiente su campioni di volume dell'ordine di pochi μl. Questi risultati possono essere migliorati attraverso un raffreddamento del sistema a temperature criogeniche, dove la più grande magnetizzazione dei campioni paramagnetici causa un aumento del segnale detettato. In sistemi dove il rumore è principalmente dovuto a fluttuazioni termiche, operazioni a bassa temperatura causano un abbassamento dello stesso. Inoltre, le operazioni ad alto campo (frequenza) causano anch'esse un miglioramento della sensibilità di spin. Per quanto riguarda la sensibilità di spin, le operazioni a temperature criogeniche e ad alta frequenza sono dunque vantaggiose. Nel 2008, il gruppo del Dr. G. Boero ha proposto un nuovo metodo di detezione basato sull'integrazione di tutti gli elementi responsabili della sensibilità su un singolo chip di silicio. Il metodo, che presenta una sensibilità di spin di almeno due ordini di grandezza migliore rispetto agli spettrometri presenti in commercio, ha permesso di studiare dei campioni con volumi nell'ordine del nanolitro. Il metodo proposto mostra prestazioni paragonabili a quelle ottenute su una simil scala da spettrometri basati su micro risonatori e è stato provato funzionare per frequenze fino a 28 GHz e temperature fino a 77 K. Il principio di detezione può essere riassunto come segue. Un campione sensibile all'ESR viene posto al centro di un oscillatore integrato che funziona a frequenza microonde. Il fenomeno di risonanza causa una variazione della magnetizzazione del campione, la quale si traduce in una variazione di induttanza. La risonanza è quindi detettata attraverso delle variazioni della frequenza di oscillazione. Durante questa tesi, ho investigato la possibilità di estendere l'uso di questo metodo fino a 200 GHz e fino a 4 K. Per raggiungere questo obiettivo, è stato necessario toccare differenti ambiti. Prima di tutto la progettazione di oscillatori CMOS in silicio funzionanti a frequenze prossime a quelle limite delle più moderne tecnologie. L'assenza di modelli validi per le frequenze di interesse e la necessità di limitare il consumo di potenza per adattarsi alle limitate potenze di raffreddamento dei sistemi criogenici, fa della materia un interessante argomento di ricerca. Lo studio ha prodotto il notevole risultato di un sistema operativo a 170 GHz con un consumo pari a 3 mW, a temperature ambiente, e circa 1.5 mW a 4 K. Con i dispositivi realizzati sono state effettuate le prime misure di oscillatori LC integrati in silicio a temperature al di sotto dei 77 K. Con esse è stato possibile confermare la presenza di alcuni effetti attesi, come la riduzione del consumo di potenza e l'aumento della frequenza di oscillazione. Inoltre, misurando la caratteristica frequenza-

alimentazione, è stata notata una successione di regioni lisce e di transizioni nette. Questi salti sono stati attribuiti all'effetto chiamato random telegraph signal (RTS) che è supposto essere il principale responsabile del rumore fliker in dispositivi MOS sub-micrometrici. Siccome l'impatto dell'RTS sulle prestazioni di transistor molto scalati è supposto aumentare con il rimpicciolimento delle tecnologie, i metodi di misura basati su oscillatori LC, che hanno una migliore sensibilità se confrontati con i metodi correntemente utilizzati, potrebbero permettere una migliore comprensione dei meccanismi che governano l'effetto e lo sviluppo di strategie tecnologiche atte a diminuirne l'impatto sui futuri nodi tecnologici CMOS. I dispositivi realizzati hanno volumi sensibili che vanno da 250 pl per il sistema a 21 GHz ai 10 pl per quello a 170 GHz. Hanno inoltre mostrato prestazioni ESR paragonabili alle più recenti pubblicazioni effettuate con risonatori miniaturizzati su campioni limitati in massa. Le sensibilità misurate sono di circa 10^7 spins/$\sqrt{\text{Hz}}$ a 50 GHz e 300 K e di circa 10^6 spins/$\sqrt{\text{Hz}}$ a 28 GHz e 4 K con campioni di DPPH, almeno 3 ordini di grandezza migliore rispetto ai dispositivi all'avanguardia disponibili in commercio. Infine i risultati preliminari sulla sensibilità basati sulla caratterizzazione elettronica dei dispositivi, predicono una sensibilità di spin di circa 10^6 spins/$\sqrt{\text{Hz}}$ a 170 GHz e temperatura ambiente e di 10^4 spins/$\sqrt{\text{Hz}}$ a 50 GHz e 4K.

Parole chiave: Risonanza di spin elettronico, ESR, spettroscopia ESR, oscillatori LC, CMOS, micro onde, criogenia, random telegraph noise, RTS.

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1 Introduction

1.1 Introduction

Electron spin resonance (ESR) is a powerful and widely applied spectroscopic tool used in physics, chemistry, biology, medicine, and materials science to determine the structure and dynamics of compounds with transition metal ions, free radicals, triplet states, and defect centers [1–37]. It is the method of choice, for example, to determine distances between paramagnetic centers in enzymes, to unravel the details of the dynamics of proteins, to study in vivo pathological conditions caused by the presence of free-radicals, to measure non-invasively the oxygen concentration in living tissues, and to evaluate the amount of radiation absorbed by a given material. ESR methods provide detailed local structure information of ordered systems (such as single crystals) as well as in disordered systems (such as glasses, ceramics, and polymers), which lack long-range order on length scales that are not easily accessible by other techniques.

1.2 State of the art

Many scientifically and industrially relevant systems (e.g., small agglomerates of biological cells with spin-labeled macromolecules, microelectronics devices, solar cells, and catalysts) have typical dimensions and/or spatial variations of their properties of interest in the range between 10 nm and 100 μm, with spin concentrations on the order of 1 mM and lower. Due to the broad range of potential applications, the improvement of conventional inductive techniques and the development of new detection methods for high spin sensitivity and high spatial resolution ESR spectroscopy and imaging is, nowadays, a scientific and technological hot topic. Conventional inductive ESR detection methods make use of coils (up to about 1 GHz), and of loop-gap, cavity or quasi-optical resonators combined with diodes detectors or bolometers (from 1 GHz to about 500 GHz). Present ESR spectrometers are optimized for samples having a volume between $(1\ \text{mm})^3$ and $(1\ \text{cm})^3$, and achieve spin sensitivities of about 10^{10} spins/$\sqrt{\text{Hz}}$ at 300 K. Due to their relatively poor spin sensitivity, the investigation of samples of volumes

smaller than (100 μm)^3 with low spin concentrations is often extremely time consuming or impossible. The insertion of dielectric or ferroelectric structures in standard cavities [38–43], the use of small solenoidal coils [44–47], planar microcoils or microwires [48–50], and cavities with narrow slits for local measurements outside the cavity [51], allows one to perform optimized inductively detected ESR experiments on samples having volumes of the order of (100 μm)^3, with spin sensitivities down to about 10^9 spins/$\sqrt{\text{Hz}}$ at 300 K. Recently, Blank and co-workers [52–59] have extensively investigated the use of dielectric resonator structures with miniaturized features for high sensitivity spectroscopy and imaging. In these remarkable works they reported, e.g., a spin sensitivity of 3x10^8 spins/$\sqrt{\text{Hz}}$ for the E_0 centers in SiO_2 at 300 K and of about 7000 spins/$\sqrt{\text{Hz}}$ for phosphorus doped ^{28}Si at 10 K. Superconducting microresonators have been also investigated [60, 61]. Best spatial resolutions reported up to now [58, 60–62] are of about (400 nm)^3. Approximated sensitivity calculations have recently shown that nanometer scale spatial resolution (and, eventually, single spin sensitivity) with the inductive detection should be achievable at low temperature and high frequency [52, 62, 63]. To perform experiments with significantly better spin sensitivity and spatial resolution, several non-inductive methods have been proposed, such as the mechanical (MRFM)[64–66], optical (ODESR)[67, 68], scanning tunnelling microscope (ESR-STM)[69, 70], Hall [71], superconducting quantum interference (SQUID)[72–75], electrical[76–80], and diamond nitrogen-vacancy centers[81–87] detection methods. These innovative approaches have already achieved or can potentially achieve single spin sensitivity, and might represent the key element for important future applications (e.g., imaging of individual biomolecules with atomic-scale resolution [66], and magnetic resonance based quantum computers [88–90]). However, they generally suffer from a lower versatility and, in many situations, they might not represent a valid alternative to the more conventional, although less sensitive, inductive approach [62].

1.2.1 Continuous wave ESR spectrometer

The standard continuous wave (CW) ESR spectrometer is schematized in figure 1.1. An ESR sensitive sample is placed inside a micro wave resonator. This can be modelled as a solenoid wrapped around the sample, matched and tuned by a capacitive network in order to avoid reflection at the resonance frequency. The resonator is connected through a directional coupler to a microwave source that excite the sample at a frequency usually kept fixed during the experiment. This typically range from 1 to 500 GHz. When the spin are off-resonance, since the system is matched, there is no power reflected back, and hence no power arrive to the detector. Sweeping the magnetic field, when the electron spin become resonant with the irradiated microwave field the sample will absorb additional microwave power causing the resonator impedance to change. Since the resonator will exit the matching condition there will be power reflected toward the detector. By measuring the magnitude of the reflected power is possible to detect the resonance phenomena.

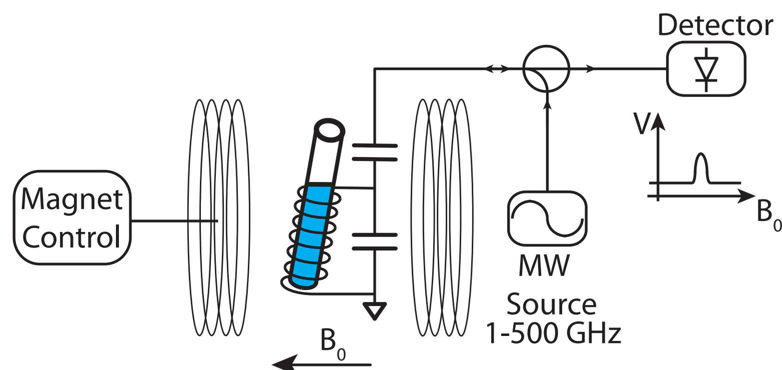

Figure 1.1 – Block diagram of a typical CW ESR detector.

1.2.2 Single chip ESR detectors

In 2008, the group of G. Boero has demonstrated that it is possible to integrate on a single silicon chip the entire part of the ESR detection system which influences the overall sensitivity of a spectrometer [91]. In this fully integrated approach, the frequency variation of the integrated oscillator due to the electron spin resonance of the sample as a function of the applied static magnetic field is measured. Two microwave oscillators, a mixer, and a frequency division module were integrated in a single silicon chip of about 1x1x0.5 mm^3. Based on this first result, we started the exploration of the potential of this unconventional, inductive detection scheme. The main motivations to further investigate the single-chip approach are:

- Despite the significantly lower Q-factor, the spin sensitivity achieved with the single-chip method is similar if not better with respect to approaches based on miniaturized resonators [52–54]. In the single-chip approach all elements which influence the spin sensitivity are located within a radius of 100 μm with respect to the detection coil, reducing signal losses to a minimum. This is particularly important for operation at high frequencies where connectivity losses are significantly larger.
- Modern deep submicrometer integrated circuit technologies allows for the design of integrated oscillators exceeding 300 GHz [92], with possible extension to the THz region in the near future [93]. This means that our approach is well suited for ESR spectroscopy up to the largest magnetic field available. At frequencies exceeding 100 GHz conventional approaches requires expensive and relatively less efficient quasi-optical technologies.
- Despite freeze-out problems in silicon, CMOS-based integrated circuit are potentially well suited for the design of integrated electronic circuits operating in a very broad temperature range, from room temperature down to 4 K at least. In this aspect, the approaches based on miniaturized resonators [58] are equally powerful.
- The small size of each chip and the on-chip direct encoding of the ESR signal into a robust frequency signal open the possibility to create dense arrays of independent

detectors that can be placed in the same magnet for simultaneous measurements on several samples ("parallel spectroscopy").

- The local and efficient conversion of DC power into a near-field non-radiating microwave magnetic field realized by the integrated oscillator (or an array of them) is potentially interesting as low cost, highly efficient local source of microwaves for dynamic nuclear polarization (DNP) experiments. For example, an array of single-chip microwave oscillators injection locked to the same frequency operating at 197 GHz or 263 GHz could be a convenient alternative to the expensive gyrotron based microwave sources [94] for 300 MHz (7.05 T) or 400 MHz (9.4 T) DNP-NMR experiments on small samples.

- The small size of the detector and, more importantly, the fact that no microwave input/output connections are required might allow for the use of the single-chip EPR detector into human or animal cavities. This is due to the fact that the microwave excitation is produced on chip and, thanks to the use of mixing and frequency division stages on the same chip, the signal output is an RF (or even AF) frequency encoded signal, which can be easily transmitted without significant signal-to-noise degradation using small diameter ordinary cables. A possible application of this approach would be local EPR-based oxymetry measurements in human or animal cavities.

1.3 Spin sensitivity

The aim of this thesis is to study, design, characterize, and use the most sensitive inductive ESR detector ever realized. Here we briefly report some approximated simple calculations to show that the proposed single-chip approach is indeed reasonably capable to achieve spin sensitivities which are well beyond state-of-the-art conventional inductive methods. Assuming a spin system with (S=1/2, g=2, T_1=T_2), the spin sensitivity for an inductive ESR detector based on the use of microcoils can be approximately written as [48, 91]

$$N_{min} = \alpha \frac{T^{3/2}}{B_0^2} \frac{\sqrt{R}}{B_u}, \tag{1.1}$$

where T is the temperature of the sample and microcoil, R is the microcoil resistance, B_u is the magnetic field produced by a unitary current in the microcoil, $\alpha \approx 20$ m^{-1}kg$^{-5/2}$s^{-4}K$^{-3/2}$A^{-3}, and B_0 is the applied static magnetic field (the resonance frequency is f_0=$\gamma/2\pi)B_0$, where ($\gamma/2\pi \approx 28$ GHz/T). For single turn microcoils we have $B_u \approx \mu_0/d$, where d is the diameter of the microcoil. For $w \geq t$ and $\delta \leq t$, the resistance can be approximately written as $R \approx \rho\pi d/2w\delta$, where $\delta = \sqrt{\rho/\mu_0\pi f_0}$ is the skin depth at frequency f_0, ρ is the resistivity of the coil metal, w is the coil wire width, and t is the coil wire thickness. For Cu, $\rho_{300K} \approx 2x10^{-8}\Omega m$. At 4.2 K the resistivity of Cu is limited by the impurities: assuming a residual resistivity ratio (RRR) $\rho_{300K}/\rho_{4.2K} \approx 10$, $\rho_{4.2} = 0.2x10^{-8}\Omega m$. State-of-the-art deep submicron CMOS technologies have top metal layers as thick as 5 μm (i.e., well above the skin depth value even at 9 GHz).

Table 1.1 shows some examples of achievable spin sensitivities based on equation 1.1. The different parameters have been varied taking into consideration the following criteria:

- The coil diameter is varied between 100 μm (approximately the largest possible diameter for an inductor which is not self-resonating due to parasitic capacitances at frequency in the order of 100 GHz) and 10 μm (reasonably the smallest effective microcoil dimension taking into consideration the integrated connectivity to the tuning capacitors and to the transistors that forms the positive feedback network).
- The operating frequency is varied between 9 GHz (value of the first single chip ESR detector [91]) and about 300 GHz (value for the highest frequency of current integrated microwave oscillator realized with CMOS technologies [92], with the THz range possibly achievable in the near future [95–102]).
- The operating temperature is varied between 300 K and 4.2 K (value at which, despite of impurity freeze-out problems, several CMOS integrated circuits have shown to be still operative [103–113]).

Table 1.1 – Examples of spin sensitivity (N_{min}) computed from Equation 1.1. See others notations in the text.

T (K)	B_0 (T)	f_0 (GHz)	d (μm)	w (μm)	t (μm)	N_{min} (spins/$\sqrt{\text{Hz}}$)
300	0.3	9	100	20	5	$4\ 10^7$
300	9.4	263	100	20	5	$1\ 10^5$
300	0.3	9	10	2	2	$4\ 10^6$
300	9.4	263	10	2	2	$1\ 10^4$
4.2	0.3	9	100	20	5	$4\ 10^4$
4.2	9.4	263	100	20	5	160
4.2	0.3	9	10	2	2	4000
4.2	9.4	263	10	2	2	16

Table 1.1, obtained assuming that the sample relaxation times doesn't change while cooling, clearly states that:

- At 300 K the proposed approach can potentially achieve spin sensitivities which are, at least, two orders of magnitude better than state-of-the-art conventional system (i.e., about 10^9 spins/$\sqrt{\text{Hz}}$).
- At 4 K the proposed approach can potentially achieve a spin sensitivity down to about 100 spins/$\sqrt{\text{Hz}}$. Single electron spin sensitivity might be possible in some hours of averaging. This confirm recent spin sensitivity calculations based on different but substantially equivalent arguments by other authors [62], where single spin sensitivity by inductive means at low temperatures and high frequencies seems also to be difficult

but not impossible. Our calculations show also that for spin concentrations down to 1 mM, sample volumes with linear dimensions below 100 nm should be measurable in a short measuring time (and down to 10 nm with some hours of averaging).

The computed spin sensitivities obtained from equation 1.1, and shown in Table 1.1, should be considered as realistic values. Nevertheless, several important experimental investigations are needed to confirm these predictions. Here a list of possible issues:

- In the calculation reported above we have considered that the overall noise of the detector is dominated by thermal noise of the microcoil. Substrate losses as well as non-thermal phase noise of the oscillator might have a significant impact on the overall noise. As demonstrated in [63, 91] the effect of non-thermal phase noise can be significantly reduced by field modulations techniques as in ordinary ESR spectrometers. However, it is still to be demonstrated that it can be reduced to a negligible level with respect to the microcoil thermal noise.

- In ordinary ESR experiments, an external microwave source is used in combination with a microwave resonator. In this configuration the amplitude of the microwave field B_1 in the resonator has no lower limit. On the contrary, in our approach where the microwave source and the microwave resonator are "nested" together forming a microwave oscillator, the amplitude of the microwave field B_1 is linked to the minimum microwave current required to assure stable oscillations. This is a relevant problem for samples easy to saturate (i.e., for sample having large values of the product $T_1 T_2$, such that $\gamma^2 B_1^2 T_1 T_2 \geq 1$). The most versatile solution would be to find an oscillator topology which requires less current for the start-up.

- In equation 1.1 we assumed $(T_1/T_2) \approx 1$. For samples with T_1 significantly longer than T_2, the spin sensitivity become worse approximately by a factor $(T_1/T_2)^{1/2}$.

1.4 Goal of this work

The single-chip approach has been investigated by the Dr. G. Boero group from 9 to 28 GHz and from 300 K down to 77 K [63, 91]. The aim of this thesis is to investigate the single chip approach up to 200 GHz and down to 4.2 K. As discussed in the previous section this will potentially allow us to achieve spins sensitivities well beyond current state of the art.

1.5 Thesis organization

The thesis is organized as follow. In chapter two, an introduction regarding the state of the art of integrated LC oscillators is provided. In the same chapter the description of a simple model capable of describing the oscillation amplitude and frequency versus bias characteristic is also presented. In chapter three is shown the electronic characterization of an integrated LC oscillator operating at temperature down to 4 K and in chapter four are shown

ESR measurements performed at cryogenic temperature with the same chip. In chapter five design strategy and performance of integrated detector operating at frequency above 100 GHz are described. Finally in chapter 6 are presented the conclusions and an outlook of this thesis.

2 LC oscillators

2.1 Introduction

As explained in chapter 1 the aim of this thesis is the demonstration of integrated oscillator as high sensitivity detector for ESR spectroscopy at cryogenic temperatures. In order to achieve this target an oscillator with high operation frequency, low noise and low power consumption is required. The continuous demanding for higher data-rate wireless communication, together with the possibility to approach terahertz operation with relatively low-cost solid state devices is pushing further every year the frequency limit of integrated solid state oscillators. Exploiting this technology trend, high sensitivity spectroscopy tool can be now realized by means of integrated technology, possibly opening the way for a capillary diffusion of magnetic resonance based spectroscopy tool which are now mainly limited to expensive laboratory equipment. For reaching the maximum oscillator frequency different solid state technology and circuit topology have been proposed. Silicon germanium heterojunction bipolar transistor (SiGe HBT) [114–116], special III-V technology (i.e. GaAs or InP)[117–119], or silicon MOSFET devices can achieve frequency in the THz range [92, 120]. InP devices are usually realized with expensive difficult to access processes, whereas SiGe BiCMOS and silicon MOSFET technologies are available from semiconductor foundries. Usually microwave oscillators built with bipolar devices show lower noise, mainly in the $1/f^3$ phase noise region, but higher power consumption for a given target frequency [115], limiting the possibility of operating at cryogenic temperatures, where the system cooling power is limited. In addition to that Silicon BiCMOS technology can't operates below the carrier freeze-out temperature, whereas for SiGe a full-customized engineering of the device can overcome this problem [121]. However this requires additional technology steps that are still not available for standard devices. For these reasons in my thesis I made the decision of using silicon MOSFET devices. Not only different technologies are capable of reaching operation at millimiter wave but also different topology can achieve the goal. Digital ring oscillator can reach frequency in the order of several GHz [122]. However they usually suffer of poor noise performances since they lack of a frequency selective network and hence they don't fit the noise constrain of a sensor. Distributed oscillator, based on the distributed amplification concept [123], don't suffer from the same problem. They

show the advantage of absorbing the parasitic element of the devices needed for sustaining the oscillation in the line delay, allowing, in theory, operation at full speed. However they need transmission lines where, in case of an ESR detector, the sensitive region (i.e. the volume where the structure generate a not negligible radio frequency magnetic field) is limited to the area in close proximity of the metal lines. LC resonator based oscillators can achieve high frequencies with structures much smaller than the wavelength and with reasonable noise performance. This makes them the usual choice for integrated oscillator in application where a good trade-off between noise and area is required. Furthermore, in this case, the sensitive region is not limited at the close proximity of the metal lines constituting the coil. Their performance is limited by the poor quality factor of integrated inductor devices [124]. As explained in chapter 1 operation at cryogenic temperature is a method for improving the device limit spin sensitivity and for studying sample that cannot be investigate at room temperature. Among others, integrated CMOS silicon LC oscillators combine together reasonable noise performance and excellent consumption characteristic, making them, probably, the best choice for the aim of this thesis. Their behaviour and characteristics will be carefully detailed in the following.

2.2 Integrated LC oscillators

CMOS integrated LC oscillators operating at frequencies ranging from 1 to about 300 GHz or above are nowadays feasible and already demonstrated [92, 120]. In almost all the cases variation of two different topologies are used. The Colpitts oscillator, shown in its differential implementation in Fig. 2.1b and the crosscoupled oscillator shown in Fig 2.1a. Colpitts oscillators usually require higher gain for reliable start up [125] and hence require higher power consumption for sustaining the oscillation. However they have slightly better close to the carrier noise performance, but this advantage rapidly degrades and, at large enough frequency offset from the carrier the two implementations shows approximately the same behaviour [126].

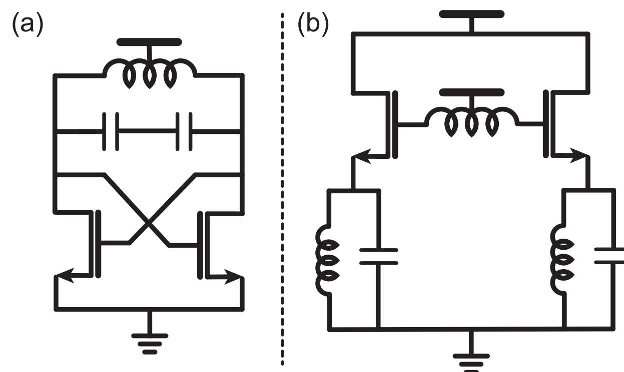

Figure 2.1 – Schematic of a) Cross-coupled LC oscillator and b) Colpitts differential oscillator.

2.2.1 Phase noise

Since our goal is to perform ESR spectroscopy by using integrated LC oscillators, oscillator noise play a key role in the definition of the detector performances. As pointed out in [127, 128] the phase noise performances of an LC oscillator depends on three elements. The resonator open-loop linewidth, which set the noise rejection properties of the overall system, the moment in the oscillation period when the noise is injected by each of the devices that form the oscillator loop and the output voltage swing level. A linear analyses of the system, as reported in [127] leads to the well known Leeson's equation:

$$L(\Delta f) = 10log\left[\frac{2k_B T R_S}{V_0^2}\left(\frac{f_0}{2Q\Delta f}\right)^2\right], \tag{2.1}$$

where k_B is the Boltzmann constant, T is the absolute temperature, V_0 is the oscillator voltage swing, R_S is the resonator series resistance and Δf is the offset frequency from the carrier. This equation doesn't take into account the effect of the flicker noise, and the noise coming from the active devices. The only useful information contained in the equation for oscillators designers is that better resonators and higher powers are needed for lower noise oscillators. A more detailed description of phase noise has been shown in [129], where the noise contribution arising from all the elements in a cross-coupled LC oscillators are taken into account, together with the flicker noise and its up-conversion mechanism. Also in this case there is not a clear circuit design oriented solution for the phase-noise that could give a deeper insight to the designer. Even if it's a problem studied deeply since many years, phase noise in oscillator is still an hot-topic involving many research groups. The difficulties in studying the problem comes from the non-linear behaviour of the oscillator which makes the study of the system too complicated for being analysed with the usual techniques employed in electronics.

2.2.2 LC oscillators for ESR spectroscopy

In the following I want to give a characteristics overview of the state of the art integrated LC oscillators highlighting the relevant aspects for ESR spectroscopy. As explained in chapter 1, the most important parameter that describe our oscillators and any oscillator possibly used as ESR detector, is the achievable spin sensitivity. This is the best figure of merit for comparing different oscillators present in literature. However some of the information needed for a good comparison are often hidden and it's then hard to calculate the hypothetical spin sensitivity for all the published oscillators. For overcoming this problem, and for comparing different oscillator present in litterature, a dedicated figure of merit (FOM) for ESR has been used in the following analyses. Observing equation 1.1 that define the system spin sensitivity, a useful

comparison can be done using the following FOM:

$$FOM_{\Delta f} = \frac{FN_{\Delta f} d_{coil}}{f_{osc}^2}, \quad (2.2)$$

where f_{osc} is the oscillation frequency, FN_{100K} is the frequency noise at a frequency offset of Δf from the carrier expressed in Hz/$\sqrt{\text{Hz}}$, and d_{coil} is the coil diameter. From the definition of equation 2.2, smaller values of the FOM corresponds to better spin sensitivities. In electronic oscillators the noise is usually expressed as phase noise, in dBc/Hz, rather than frequency noise. The relation between the two quantities is [130]:

$$FN_{@\Delta f} = 10^{\frac{PN_{@\Delta f}}{20}} \Delta f. \quad (2.3)$$

For oscillators operating in the tens of GHz range or above, phase frequency noise data are typically available for frequency offset of 1 MHz. In our FOM we consider a lower frequency offset of 100 kHz, since for ESR spectroscopy a modulation frequency of 1 MHz is sometimes too rapid if compared with the spin relaxation times. Fig. 2.2 shows a comparison of different integrated LC oscillators operating at or above K-band present in literature [92, 97, 98, 102, 120, 131–146], by mean of equation 2.2. Only oscillators where all the needed data were available are here compared.

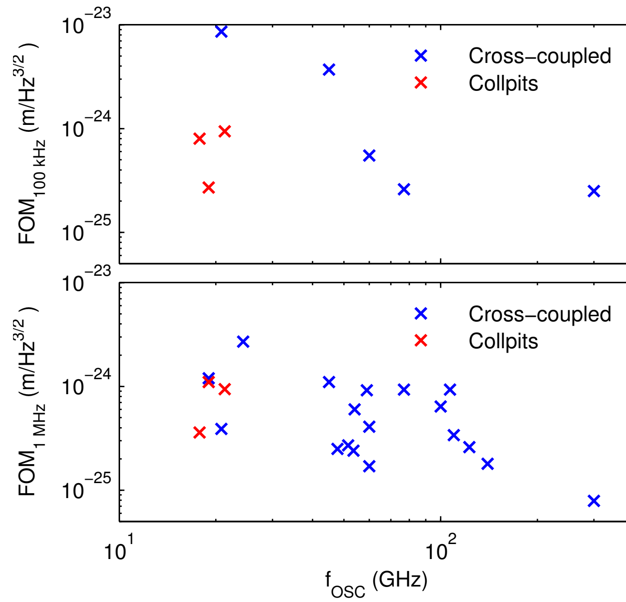

Figure 2.2 – ESR FOM for different published integrated LC oscillators at 100 kHz and 1 MHz offset from the carrier.

The results are summarized in the following table:

Table 2.1 – Comparison of literature oscillators. Notation: topology: cross-coupled (CC), colpitts (C); f_0 oscillator frequency; d coil external diameter; $PN_{100\,\mathrm{kHz}}$ phase noise at 100 kHz offset; $PN_{1\,\mathrm{MHz}}$ phase noise at 1 MHz offset; $PN_{10\,\mathrm{MHz}}$ phase noise at 10 MHz offset; $FN_{100\,\mathrm{kHz}}$ frequency noise at 100 kHz offset; $FN_{1\,\mathrm{MHz}}$ frequency noise at 1 MHz offset; $FN_{10\,\mathrm{MHz}}$ frequency noise at 10 MHz offset; $\mathrm{FOM}_{100\,\mathrm{kHz}}$ figure of merit at 100 kHz offset; $\mathrm{FOM}_{1\,\mathrm{MHz}}$ figure of merit at 1 MHz offset. [1] simulation results. [2] measured at 2 MHz offset. [3] 3 turns coil.

Ref.	Process	Topol. CC/C	f_0 GHz	d μm	$PN_{100\,\mathrm{kHz}}$ dBc/Hz	$PN_{1\,\mathrm{MHz}}$ dBc/Hz	$PN_{10\,\mathrm{MHz}}$ dBc/Hz	$\mathrm{FN}_{100\,\mathrm{kHz}}$ Hz/$\sqrt{\mathrm{Hz}}$	$\mathrm{FN}_{1\,\mathrm{MHz}}$ Hz/$\sqrt{\mathrm{Hz}}$	$\mathrm{FN}_{10\,\mathrm{MHz}}$ Hz/$\sqrt{\mathrm{Hz}}$	$\mathrm{FOM}_{100\,\mathrm{kHz}}$ m/Hz$^{3/2}$	$\mathrm{FOM}_{1\,\mathrm{MHz}}$ m/Hz$^{3/2}$
[92]	TSMC65nm	CC	300	40	[1]-45	[1]-75	[1]-100	[1]562	[1]177	[1]100	[1]$2.5\ 10^{-25}$	[1]$7.9\ 10^{-26}$
[97]	UMC90nm	CC	110	53	-	[2]-88.2	-105.2	-	[2]77.8	55	-	[2]$3.4\ 10^{-25}$
			123	41	-	[2]-86.4	-100.2	-	[2]95.7	97.7	-	[2]$2.6\ 10^{-25}$
			140	32	-	[2]-85.1	-93	-	[2]111.2	224	-	[2]$1.8\ 10^{-25}$
[98]	UMC130nm	CC	59	90	-	-89	-108	-	35.5	39.8	-	$9.2\ 10^{-25}$
			100	57	-	-	-103	-	-	70.8	-	-
[120]	IBM32nm	C	240	30	-	-	-92	-	-	251.2	-	-
			272	30	-	-	-	-	-	-	-	-
[131]	180nm	CC	19	140	-	-110	-	-	3.2	-	-	$1.2\ 10^{-24}$
[133]	65nm	CC	53.6	65	-	-99.4	-	-	10.7	-	-	$2.4\ 10^{-25}$
[134]	STM65nm	CC	54	70	-	-92	-116	-	25.2	15.8	-	$6\ 10^{-25}$
[135]	90nm	CC	60	50	-68	-90.5	-	39.8	29.9	-	$5.5\ 10^{-25}$	$4.1\ 10^{-25}$
[136]	TSMC130nm	CC	47.8	100	-	-105	-	-	5.6	-	-	$2.5\ 10^{-25}$
[132]	TSMC180nm	CC	45	190	-68	-98.9	-110	39.8	11.3	31.6	$3.7\ 10^{-24}$	$1.1\ 10^{-24}$
[138]	180nm	C	21.3	85	-86	-106	-130	5	5	3.2	$9.4\ 10^{-25}$	$9.4\ 10^{-25}$
[139]	180nm	CC	24.3	160	-62	-100	-120	79.4	10	10	$2.2\ 10^{-23}$	$2.7\ 10^{-24}$
[140]	180nm	C	19	120	-102	-110	-125	0.8	3.6	5.6	$2.7\ 10^{-25}$	$1.1\ 10^{-24}$
[141]	IBM90nm	CC	60	30	-	-94	-	-	20	-	-	$1.7\ 10^{-25}$
[142]	120nm	CC	51.6	[3]40	-	-85	-	-	56.2	-	-	$2.7\ 10^{-25}$
[143]	90nm	C	17.8	150	-75	-102	-	17.8	7.9	-	$8\ 10^{-25}$	$3.6\ 10^{-25}$

[144]	STM65nm	CC	100	49	-	-77.6	-104.5	-	131.8	59.5	-	$6.4\ 10^{-25}$
[145]	TI90nm	CC	107	85	-	-78	-101.6	-	125.9	83.2	-	$9.3\ 10^{-25}$
[146]	65nm	CC	77	45	-69.3	-89.3	-105.9	34.2	125.9	83.2	$2.6\ 10^{-25}$	$9.3\ 10^{-25}$
[147]	TSMC90nm	CC	20.8	94	-68	-115	-130	39.8	1.8	3.2	$8.6\ 10^{-24}$	$3.9\ 10^{-25}$

Figure 2.2 clearly states that, for our interest in the detection of a small as possible number of spins, a higher frequency of operation is not only supported by the theory presented in chapter 1, but also by literature results. As shown in Figure 2.2 cross-coupled oscillators shown similar performance if compared to the Colpitts counterpart at 1 MHz offset. At 100 kHz the analysed Colpitts devices have better performance as supported by theory [125, 126]. However, Colpitts implementation at higher frequencies gets critical, since the resonance frequency depends on the ratio of two capacitances and one of those, for the impossibility of adding external component due to the low capacitance value needed, is the gate source capacitance. MOS capacitance are responsible for a part of the flicker noise up-conversion mechanism [129] and hence their weight in the resonance frequency must be limited. In cross-coupled device the MOS parasitics contribute as well to the definition of the resonance frequency, but their effect is first halve by parallel interconnection of two devices and then further mitigated by the parallel coil capacitance. Furthermore Colpitts implementation, as already mentioned, shows higher power consumption, making them probably not the best choice for our application. Considering all these points in the following I will give only a description of the cross-coupled oscillator, that is the device topology used in the devices realized in this thesis.

2.3 Cross coupled LC oscillators

Cross coupled oscillators (see fig. 2.1) are usually described as negative resistance oscillators. In the easiest analysis, the device is considered as the parallel connection of two networks. An active network, that has the purpose of restoring the losses of a passive frequency selective circuit. If the parallel impedance (admittance) resulting from the parallel connection of the two networks is real negative for some frequency, the system satisfy the Barkausen criteria and hence oscillations are possible. The oscillation will then settle at an amplitude for which the impedence of the active network is in magnitude equal to the one of the resonator, meaning that the energy provided by the active device equal the one dissipated during each period. In the easiest implementation the roles of the two nets are accomplished by a parallel LC network and by a cross coupled transistors pair as energy restoring net (Fig 2.3). In this configuration, a small signal analyses even if in principle inadequate for an oscillator (that is not a linear device) can give a useful insight about the system start-up. The condition needed for sustaining the oscillation [127] is given by:

$$g_{tank} < \frac{g_m}{2}, \tag{2.4}$$

where g_m is the transistor transconductance and $g_{tank} = g_{LC} + \frac{g_{ds}}{2}$ represent the overall losses of the system. g_{LC} is the equivalent parallel admittance of the resonator at resonance, usually expressed as $Q^2 R_s$, where Q is the resonator quality factor and R_s is the inductance series resistance in the approximation that losses of the LC network are dominated by the inductor. g_{ds} is the drain source conductance, representing the transistor losses. As previously described

the oscillation frequency is set by means of an LC parallel circuit. The oscillation frequency can, in first approximation, be written as:

$$f_{osc} = \frac{1}{2\pi L_s C_{tank}}. \tag{2.5}$$

2.4 Analytical model

As explained in the previous paragraph, the validity of the small signal model is limited to the description of the start-up condition. For example it is not capable of predicting important characteristics such as the oscillation amplitude and the oscillation frequency variation linked to the supply voltage. To predict the values of these quantities I've developed a simple large signal model. As shown in figure 2.3 the model is made of two parts. The first describe the non linear real impedance behaviour (g_{mos}), the second takes into account the parasitic capacitance variation in the MOS devices (C_{mos}).

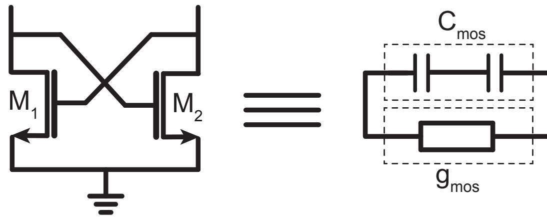

Figure 2.3 – Cross-coupled scheme and target model

2.4.1 Active model

The first assumption made in my analytical model is that the bias voltage (V_A) is higher than the transistor threshold voltage (V_{th}) for considering operation at the start-up in strong inversion. Next I assumed sinusoidal oscillation at frequency f_0 and amplitude A at gates (and drains) of the cross-coupled pair, which is a reasonable assumption since eventual higher harmonics will be filtered out by the tank. In this condition voltage at transistor nodes can be written as:

$$V_1(t) = V_A + A\,cos(2\pi f_0 t) \qquad V_2(t) = V_A - A\,cos(2\pi f_0 t) \tag{2.6}$$

Knowing the instantaneous voltages it's possible to calculate the corresponding currents. Furthermore for defining the output admittance it's necessary to define differential output voltage and current which are:

$$V_{out}(t) = V_1 - V_2 = 2A\,cos(2\pi f_0 t) \qquad I_{out}(t) = I_1 - I_2 \tag{2.7}$$

At the start-up the oscillation amplitude is small, if compared to the bias voltage, and hence the transistor never exit from the saturation region (Fig. 2.5). We are in the start-up situation that is possible to describe with the small signal analysis. Here the transistor capability are fully exploited and the losses only come, in first approximation, from the channel length modulation in the MOS devices and from the resonator. After the start-up the oscillation

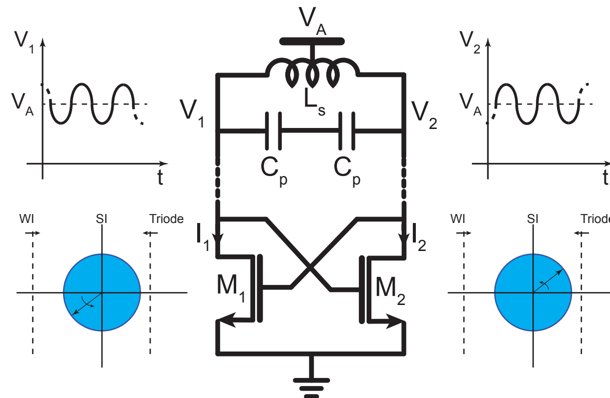

Figure 2.4 – Oscillator behaviour for small oscillation amplitudes

amplitude will continuously increase until the negative admittance generated by the cross-coupled pair will equal the value of g_{tank}. In fact increasing the amplitude of the oscillation lower the transistor efficiency, making a part of the energy dissipated through mechanism that will be detailed in the following. This indeed cause the lowering of the negative admittance seen at the cross-coupled terminals. If the equilibrium condition is not matched the oscillation amplitude will adjust in order to reach it. After starting up, if the equivalent impedance is still negative, the amplitude will increase. Increasing the amplitude the transistor will start to enter the triode region, increasing the losses toward ground, and hence lowering the resulting negative admittance. In an intuitive view when the gate voltage exceed the bias voltage of a value A, the drain voltage is below the bias voltage of the same value A. This push the device in the triode region when the condition $V_{OV} > V_{DS}$ is met, where V_{OV} is the overdrive voltage defined as $V_{OV} = V_g - V_{th}$. In the cross-coupled system, if the oscillation is operative, this condition is met when

$$cos(2\pi f_0 t) < \frac{V_{th}}{2A}. \tag{2.8}$$

The phasor interpretation of this condition is given in Figure 2.5. When the amplitude is increasing the limit between triode and saturation condition is pushed toward the cosine circle. When $(V_{th}/2A) < 1$ the transistor enters in the triode region, increasing the overall losses of the system and thus lowering the overall negative admittance. This is a well known problem in this kind of oscillators, and source filtering technique are proposed to obtain a high impedance path to ground even in this condition [148]. In any case an oscillator in triode might be not enough for reaching the admittance balance. If this is the case, the amplitude further increase and the device is pushed to work first in moderate, then in weak inversion and

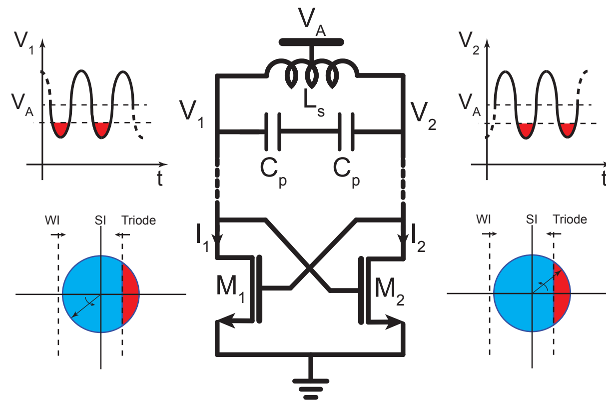

Figure 2.5 – Oscillator behaviour for medium amplitudes

then it is finally turned off. This, together with the larger effect during the period of the triode region, further decrease the network negative admittance. The condition for weak inversion is $V_{OV} < 2nV_T$ [149]. Then the cross-coupled system enter the weak inversion region when the following condition is matched:

$$cos(2\pi f_0 t) < \frac{2nV_T + V_{th} - V_A}{A} \tag{2.9}$$

The situation is illustrated in Figure 2.6. If the positive negative admittance is small (i.e. the resistive losses in the resonator are small) the amplitude can further increase. The physical limit is reached when the energy provided from the cross-coupled pair is dissipated by the cross-coupled pair itself. At that point the negative admittance reach the value of zero, meaning that the active network is not capable of providing energy and hence oscillation are possible only with an ideally non dissipating resonator.

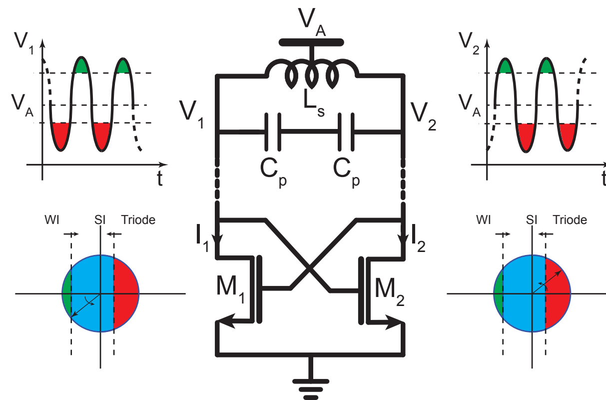

Figure 2.6 – Oscillator behaviour for large amplitudes

For evaluating the negative admittance provided by the resonator the instantaneous current for a given amplitude has to be known. In order to do that the one-piece current equation

provided in [150] is certainly convenient when compared to the normal piece-wise approach for standard MOS transistor. The single piece drain current can be written as:

$$I_D = I_Z \left[ln^2 \left(1 + e^{\frac{V_{OV}}{2nV_T}} \right) - ln^2 \left(1 + e^{\frac{V_{OV} - nV_D}{2nV_T}} \right) \right] \left(1 + \frac{V_D}{V_E} \right), \tag{2.10}$$

where

$$I_Z = 2\mu C_{OX} \frac{W}{L} n V_T^2 = 4\beta n V_T^2, \tag{2.11}$$

$\beta = \mu C_{OX} W/(2L)$ is the MOSFET beta factor, V_{OV} defined as $V_G - V_{th}$ is the MOSFET overdrive voltage, V_G and V_D are the MOSFET gain and drain voltages respectively, and V_E is the Early voltage describing the channel length modulation effect. By means of equations 2.11 and 2.6 it's possible to compute the instantaneous current during the period. A comparison between the current simulated with our model and Spectre (circuit simulator under Cadence environment) for a voltage amplitude equal to $0.9V_A$ is presented in figure 2.7. The simulation results plotted in 2.7 shows drain and gate voltages together with drain current for one of the two transistors in the cross-coupled pair. The two simulations give very similar results. Furthermore it is possible to notice all the different operation regions. At t=0 the device has low gate and high drain voltage and hence it's off. After that the gate voltage rise-up and the device enter first at weak and then in strong inversion. While the gate voltage raise-up the drain voltage decrease and, at t=0.3 s, the device enter in triode region. Later the gate voltage reach its maximum, the transistor symmetrically go through the same operation region, and this explain the current profile symmetry.

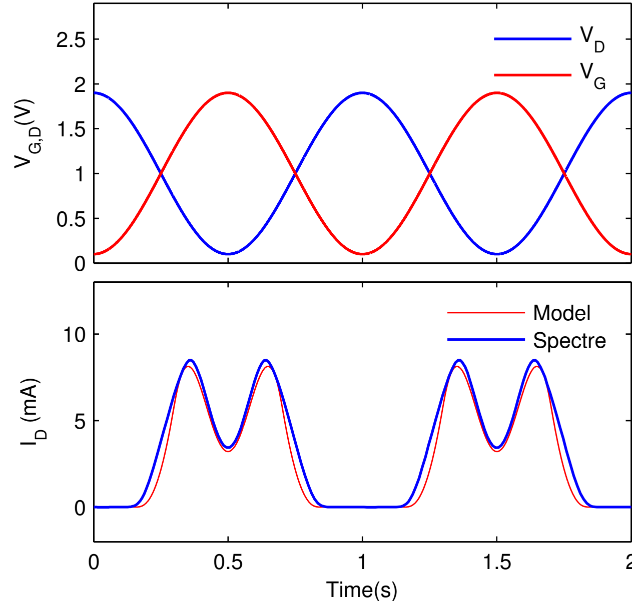

Figure 2.7 – Analytical and Spectre drain current comparison. Simulation and Cadence Spectre simulation parameter V_A=1V, β=12.5 mA/V^2, V_{th}=0.545 V, V_E=-6 V, V_T=26 mV.

Equation 2.11 is not considered as accurate for short channel devices [150] but, can give us enough insight about the behaviour of the integrated oscillator. The output admittance can be calculated as the average admittance over a period

$$g_{MOS}(A) = \frac{1}{T}\int_0^T \frac{I_{out}(A,t)V_{out}(A,t)}{V_{rms}^2}dt. \tag{2.12}$$

Numerical solution of equation 2.12 are shown in figure 2.8. It can be noticed that the minimum admittance value is equal to $g_m/2$, as predicted by the small signal model and represented by green line in figure 2.8. The small discrepancy present between the numerically solved (blue line) and ideal line (dotted green line) is due to the channel length modulation effect that degrades the performance of the system already at the start-up. When the amplitude cross the threshold $V_{th}/2A$ the device enter the triode region dissipating more energy. This can be modelled with a line that asymptomatically reach a slope equal to $6\beta/4$ (dotted red line in figure 2.8). The slope is obtained considering the asymptotic behaviour when the two transistors are pushed in the off and in deep triode region respectively. From the graph is possible to notice that a maximum amplitude of about 1.2 V_A is expected in the ideal case, when a lossless resonator is used.

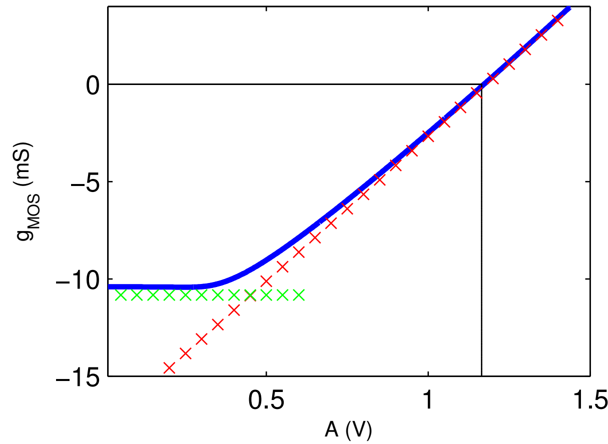

Figure 2.8 – Negative admittance as a function of the oscillator amplitude. The blue line is the numerically solved admittance. The dotted green line represent the ideal behaviour for small amplitudes, the dotted red line represent the asymptotic behaviour for large amplitudes. Simulation parameter: β=12.5 mA/V^2, V_{th}=0.545 V, V_E=-6 V, V_T=26 mV.

When a real resonator is used the amplitude is expected to set at a value for which the negative admittance provided by the cross-coupled pair exactly match the positive admittance of the frequency selective tank. This is shown in figure 2.9.

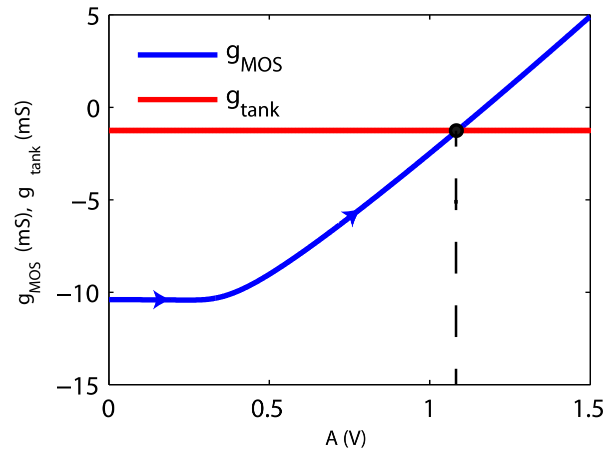

Figure 2.9 – Oscillator Amplitude determination. The Amplitude set at the value where $g_{MOS}+g_{tank}=0$.

2.4.2 Parasitic capacitance

In the design of microwave LC oscillators it is not possible to neglect the effect due to the MOS capacitance on the operating frequency since it is not possible to use a large enough tank capacitance for making the MOS capacitance negligible. Since MOS capacitances are voltage dependent, this cause the equivalent capacitance seen at the cross-coupled terminals to change with the oscillation amplitude. For gaining an insight about the capacitance behaviour, and hence regarding the frequency dependence with the biases, we'll go through an analyses similar to the one we performed for the active devices. Also in this case an enough accurate but simple large signal equation is found by means of the combination proposed in [151], which describe the intrinsic MOS capacitances behaviour in triode and strong inversion regions and its inherent repartition between source and drain as a function of the applied voltages. The equation proposed doesn't describe the behaviour of the MOS capacitance in weak or moderate inversion, since it propose the repartition of a constant total gate capacitance between the two terminal of source and drain. In our case, since we are dealing with a large signal, the equation is not enough accurate for catching the behaviour during the all period. As previously explained, the oscillation push the transistor in deep weak inversion and even in the off region. In these operation regions assuming the capacitance as a mere repartition of the parallel plate approximation between drain and source leads to large errors. This because the processes of charge redistribution that take place below threshold strongly impact the gate capacitance profile [152]. These effects are, in first approximation, caught by considering an intrinsic gate capacitance which is a function of the applied gate voltage [153] as:

$$
\begin{aligned}
C_{GS} &= \tfrac{2}{3} C_{ch} \tfrac{1+2\eta}{(1+\eta)^2} \\
C_{GD} &= \tfrac{2}{3} C_{ch} \tfrac{\eta^2+2\eta}{(1+\eta)^2} \\
C_{ch} &= C_i \left[1+2e^{-\frac{V_{OV}}{V_{th}}}\right]^{-1},
\end{aligned}
\tag{2.13}
$$

where $C_i = C_{ox}WL$ is the intrinsic gate capacitance, C_{ox} is the gate capacitance per unit area, W and L are the transistor channel width and length, C_{GS} is the gate-source capacitance, C_{GD} is the gate-drain capacitance, V_{OV} is the overdrive voltage and V_{th} is the threshold voltage. η is a piecewise function that describe the "level of triode" of the device. It is equal to 0 when the device is in the saturation region (i.e. $V_{OV} < V_{ds}$) and equal to $1 - V_{ds}/V_{OV}$ when it is in the triode region [151]. The instantaneous capacitance is calculated for voltages given by equation 2.7. As for the drain current the results are in good agreement with the Spectre simulation as reported in figure 2.10. However slightly different simulation parameters has to be used for better fitting the Spectre simulation. The large difference on the gate drain capacitance in the saturation region is due to the fact the model doesn't take into account the extrinsic MOS capacitance [151] that set the minimum possible value for any capacitance in the system, that in the technology is about 10 fF. The differential capacitance seen at the terminal of the cross-coupled pair can be written as follow [154]:

$$
C_{MOS} = \frac{C_{GS} + 4C_{GD}}{2}. \tag{2.14}
$$

From equation 2.14 it is possible to notice that the effect of the gate-drain capacitance is bigger than the gate-source one in a cross-coupled pair. At the start-up, when we can consider the device as operating in saturation region, the parasitic capacitance seen at the cross-coupled terminal will be due to the gate-source capacitance (the gate-drain is at its minimum in this condition) and hence we have the maximum frequency of oscillation. When the amplitude increases the device enters in the triode region and hence the contribution of the gate-drain capacitance is no longer negligible causing a lowering of the operating frequency. With the growth of the oscillation amplitude the device will also start to be pushed in weak and then in the off region. In this regions the capacitance seen at the gate terminal is lowered due to the carrier depletion on the silicon side [151]. This reduces the C_{GS} capacitance and mitigate the effect of the larger triode capacitance. Operation region are well visible in the graph of figure 2.11.

In analogy with the transistor admittance it is possible to calculate the average parasitic capacitance during a period as shown in equation 2.15. Numerical solutions are then computed and, together with the value for inductance and capacitance used in the design reported in appendix A.1, used for computing the oscillation frequency. In figure 2.12 it is possible to notice the good agreement between measurement done on the device detailed in appendix

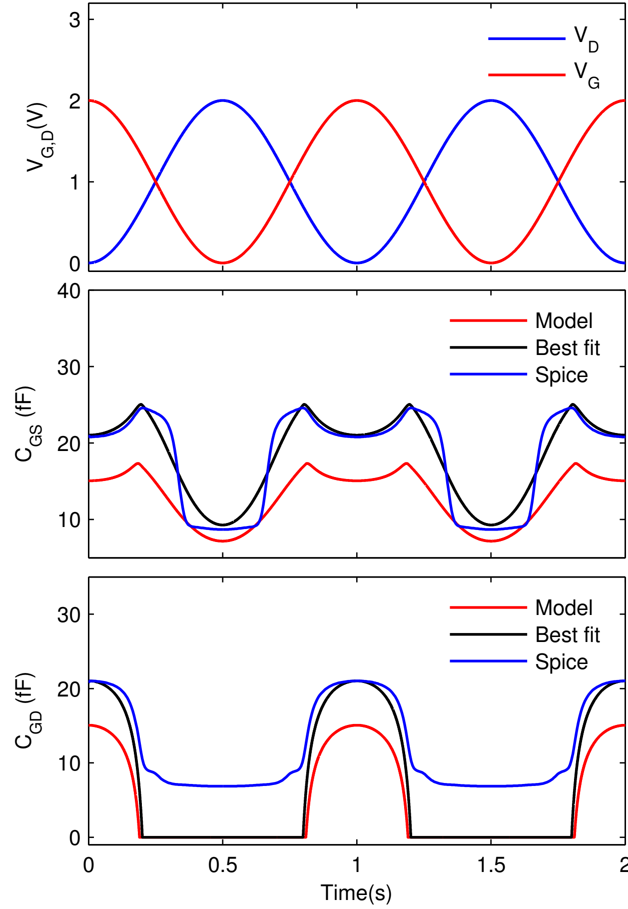

Figure 2.10 – Analytical and Spectre capacitance comparison. Model simulation and Cadence Spectre simulation parameters: V_A=1V, C_i=34 fF, V_{th}=0.545 V. Best fit simulation parameter: V_A=1V, C_i=44 fF, V_{th}=0.4 V.

A.1 and our model. Furthermore results obtained by simulating the oscillator with Spectre and our model are shown. Our model shows a better agreement with the measurement curve. The simulation is done considering an oscillation amplitude equal to 1.1 V_A, computed set amplitude for an oscillator with an equivalent parallel impedance of 800 Ω and cross-coupled transistor with characteristic equal to the one detailed in the caption of figure 2.8.

$$C_{avg} = \frac{1}{T}\int_0^T C_{MOS}(A,t)\,dt. \tag{2.15}$$

Since the use of a piecewise equation for parasitic capacitance is often unpractical I've searched for a one piece capacitance equation describing the behaviour over the entire period. The results are reported in equation 2.16 and figure 2.13 where a slightly worse agreement

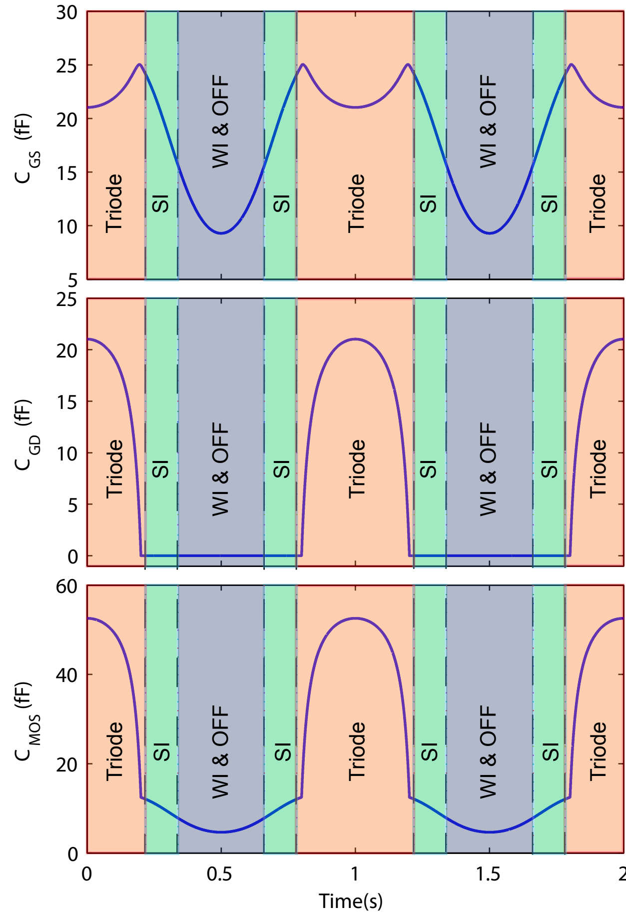

Figure 2.11 – Capacitance behaviour in all operation regions.

between Spectre and the model simulation is shown with respect to figure 2.10.

$$\begin{aligned} C_{GS} &= C_{ch}\left(\frac{1}{3e^{\frac{-3V_{DS}}{|V_{OV}|}}} + \frac{1}{3}\right) \\ C_{GD} &= C_{ch}\left(1 - \frac{1}{3e^{\frac{-3V_{DS}}{|V_{OV}|}}}\right). \end{aligned} \tag{2.16}$$

In order of being capable of solving the oscillator equations with a differential equation solver the value of the differential admittance and capacitance for every voltage value applied to the system are computed. The voltage at the transistor node can be written as:

$$V_1 = V_A + A \qquad\qquad V_2 = V_A - A \tag{2.17}$$

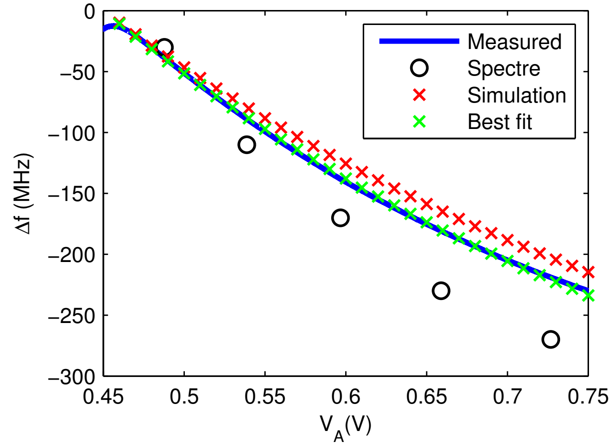

Figure 2.12 – Simulated Vs. measured frequency curve. Spectre and model simulation parameters: C_i=24 fF, V_{th}=0.350 V, L= 300 pH, C=125 fF. Best fit parameters: C_i=44 fF, V_{th}=0.285 V, L= 300 pH, C=161 fF.

Using this voltages the differential admittance can be approximated as follow:

$$Y = -2\beta(V_A - \mid A \mid) \tag{2.18}$$

The capacitive element can be written as follow:

$$C_{MOS} = \frac{1}{2} WLC_{ox} \frac{1}{1+e^{-\frac{V_A-A-V_{th}}{V_{th}}}} \left(\frac{4}{3} - \frac{2}{3} \frac{1}{1+e^{-\frac{3(V_A+A)}{|V_A-A-V_{th}|}}} \right) \tag{2.19}$$

Combining the last two elements it's possible to solve the following differential equations:

$$\begin{cases} -\frac{1}{L_s}\left(\frac{YA}{C_{MOS}+C_0} + \frac{I}{C_{MOS}+C_0} + R\frac{dI}{dt}\right), \\ V = RI + L\frac{dI}{dt}, \end{cases} \tag{2.20}$$

where I is the current flowing in the coil, V is the voltage at the crosscoupled terminal, C_0 is the fixed resonator capacitance, R is the coil resistance, W and L are transistor width and length. Solving the system with a differential equation solver it's been possible to validate the model.

2.5 Injection locking

As mentioned in the previous paragraphs one of the goal of this thesis is the study of microwave oscillators operating at cryogenic temperature. Operation at temperatures below 4 K is done by means of cryostats where liquid helium is pumped. Temperatures down to 1.5 K can be reached by pumping ^4He and down to 0.3 K with ^3He. The cooling power of these systems at these

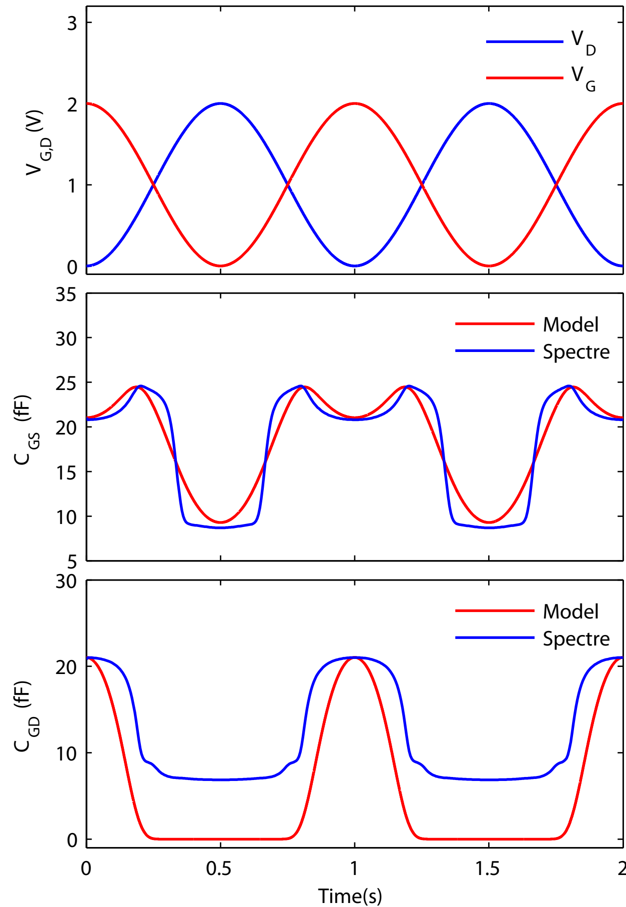

Figure 2.13 – "One piece" capacitance model. Simulation parameter: V_A=1V, C_i=44 fF, V_{th}=0.4 V. Cadence Spectre simulation parameter: V_A=1V, C_i=34 fF, V_{th}=0.545 V

temperatures is limited and hence, for avoiding local heating created by the device, the power dissipated by the integrated oscillator must be limited. Additionally it is practically impossible to drive the output bonding pad with a microwave signal since a high frequency buffer would consume to large power. A down-conversion scheme has to be implemented. In the first implementation of the detector realized in Boero's group and operating at 9 GHz [91], the down conversion was done by mixing of two signals coming from oscillators operative at a similar frequency. To avoid injection locking, the two oscillators have to operate at a frequency offset of about 1 GHz. A frequency division module was added for further lower the frequency. In a second implementation of the concept, operative at 28 GHz, a direct division of the microwave carrier was implemented [63]. This, due to the high power consumption of the frequency divider operating at high frequency, is not an optimum solution for cryogenic operation. The device presented in [155] operative at 21 GHz adopts a down-conversion solution analogous to the one in [91]. The second oscillator is operative at 17 GHz and a frequency division modulus by 16 further lower the output frequency. This device was demonstrated operating at temperature down to 4.2 K. The frequency offset between oscillators has been chosen by the

experience of the previous design where an offset of 1 GHz was necessary for avoiding locking of the oscillators operating at 9 GHz. For further reducing the power consumption, the two oscillators might be designed to be at a frequency offset as small as possible, avoiding then further down-conversion. A study of injection locking for oscillator placed in close proximity realized with planar technology has been done. As explained in [156], injection locking is a well known phenomena that effect oscillators. This is mainly due to the fact oscillators working at close frequencies and capable of exchanging energy, tend to minimize the amount of energy transferred between them working at the same frequency at a given phase offset. In our electronic system we can state that the two oscillators are capable of exchanging energy through an electric coupling, that take place in the region of the mixer through the parasitic capacitances, and magnetically, through inductive coupling of the two coils. If the former is generally well modelled in the standard post layout simulation, the latter is usually not, unless a more complicated electro-magnetic simulation is carried out after system layout. The analyses carried out in [157] provide a useful tool that allow the computation of the mutual inductances of two coplanar coils (Eqn. 2.21).

$$M_{12} = M_{21} = M = \frac{\mu_0 \pi r^2}{4z}\left[P_{-1/2}^{-1}\sqrt{1-\left(\frac{z}{2r}\right)^2}\right]^2, \tag{2.21}$$

where r is the coils radius, z is the center-center distance and P is the associated Legendre function of order -1. Following the concepts described in [156] it is possible to write the minimum offset frequency to avoid injection locking as a function of the distance between the coil as

$$\omega_L = \frac{\omega_0}{2Q}\frac{M}{L}, \tag{2.22}$$

where Q is the resonator quality factor, ω_0 is the oscillator center frequency and L is the resonator inductance. The value listed in table 2.2 are the one for the chip reported in chapter 5 considering a quality factor equal to 20 for all the different systems and assuming the same current in both the oscillators. The results show that an inductive coupling is practically impossible because nominally identically designed oscillators (i.e. identical layout) will never be operative at the same frequency (within less then 10 MHz, i.e., less than 0.1 % apart) because of process mismatches and different loading of the oscillators due to the mixer topology. In case injection locking is produced by means of the electric coupling, the bias voltage frequency dependence can be exploited in order to unlock the two oscillators.

2.6 Conclusions

In this chapter a simple yet sufficiently accurate model describing a cross-coupled pair oscillator has been presented. The model is capable of predicting the amplitude of oscillation. In addition to that a model describing the parasitic capacitance behaviour as a function of the oscillation amplitude and bias voltage is also described. The two analytical models have been

Table 2.2 – Computed locking frequency for chapter 5 design. z is the coil-coil center distance, r is the coil radius and Δf_{min} is the expected minimum offset frequency for preventing the locking of the two oscillators

f_0(GHz)	z (μm)	r(μm)	Δf_{min}(MHz)
28	320	95	6
28	340	90	5
56	240	60	9
112	180	36	12
200	160	22	13

compared with Spectre simulations showing a good agreement. The two models combined together offer an intuitive description of the oscillator and they can possibly be use in future in all the applications where an intuitive yet exhaustive oscillator description is needed.

3 CMOS LC oscillators at cryogenic temperatures

3.1 Introduction

As explained in chapter 1, ESR detectors working at cryogenic temperature can be useful, for example, for studying sample with limited number of spins or impossible to study at room temperature due to short relaxation times. At the beginning of this thesis the operation of CMOS devices and circuits at temperatures down to 4 K and below was already investigated in detail [103, 106, 108, 109, 113, 158–164]. However, no characterizations of CMOS LC-oscillators at cryogenic temperatures were reported. In this thesis I investigated the behaviour of miniaturized microwave LC-oscillators based on MOSFETs down to 4 K. Macroscopic effects such as phase-frequency noise reduction, lower power operation together to different frequency to bias characteristics are observed. The main original contribution of this work is the observation of oscillation frequency jumps. We tentatively attribute the origin of the observed jumps to the capture and emission of electrons from traps located in proximity of the transistor channel which, in turns, produce a variation of the effective MOS capacitance [165, 166] and, finally, a variation of the measured oscillator frequency. Once elucidated the origin of the observed behaviour, the oscillator based experimental method proposed here might represents an additional powerful tool, complementary to current methods, for the investigation of defects in MOS (and possibly others) electronic devices. [167–169]

3.2 Macroscopic effects

The experiments on the integrated LC oscillators at 4 K were performed by inserting a printed circuit board (PCB) into a 65 l liquid helium dewar, pressurized at about 100 mbar above atmospheric pression. On the board the K2 chip (see appendix A.1)was glued and electrically connected through wire bondind and a commercial amplifier (Texas Instrument THS4304D) was used as buffer to drive the coaxial cable carrying the chip output signal at about 300 MHz. Immediately outside the dewar an amplifier (MiniCircuit ZFL-500) was added for making the signal coming from the chip sufficiently large for the voltage to frequency conversion. The

oscillator power consumption at start-up is about 0.6 mW at room temperature and 0.25 mW at 4 K. Higher transistor transconductance and lower resonator losses are responsible for the lower power consumption at low temperature. Lower resonator losses are expected, since the metal resistivity decrease with temperature due to lower scattering of the electrons by phonons [170]. As explained in [106, 171, 172] the transconductance improves while lowering the temperature, making transistor efficiency higher, and hence lowering the system power consumption. This second system improvement is mainly due to the higher silicon mobility expected at cryogenic temperature [106, 173]. For the same reasons the power consumption of the down-conversion chain pass from 19 to 5.5 mW making the total chip power consumption decreases from roughly 20 to 6 mW. In addition to that the output buffer power consumption decreases from 75 to 40 mW.

The output frequency of the chip goes from roughly 220 MHz at 300 K to 350 MHz at 4 K. This is caused by the oscillation frequency of the two integrated oscillators that increase by about 2 GHz going from 300 K to 4 K (i.e., the oscillation frequencies are about 23 GHz and 19 GHz at 4 K). Frequency increases in linear way between room temperature and about 77 K. Below liquid nitrogen temperature the frequency rapidly set at the 4 K value. The absolute frequency variation are in the order of 200 MHz between room temperature and liquid nitrogen, and 3 GHz between 77 and 30 K. This behaviour can be explained partially with a lower gate

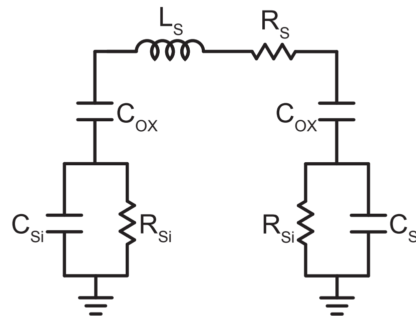

Figure 3.1 – Integrated coil lumped model

capacitance [172], and with a lower coil to substrate parasitic capacitance. The resonator coil can be in first approximation modeled as the lumped scheme shown in figure 3.1. The model take into account the parasitic element that are between the metallic top metallic top metal coil and the silicon substrate. At room temperature the substrate is modelled as a resistance (R_{Si}) with value that are in the order of few kΩ, and a parallel capacitance (C_{Si}) that has value in the order of 1 fF. At the operative frequency (i.e. 20 GHz) the substrate net can be reasonably approximated as purely resistive, and thus the parasitic capacitance seen from the coil terminal can be approximate by the oxide capacitance (C_{OX}) that has value in the order of 30 fF. At lower temperature, where the carrier freeze-out effect is not longer negligible, the substrate resistance increases. At the limit where the substrate resistance tend to infinite the capacitance net look as the series of two capacitors, where the smallest one is the substrate capacitance. This makes the equivalent coil capacitance approximately equal to the substrate

one, boosting the operating frequency. Since the substrate losses are lowered, the quality factor further increase, again contributing to the lower power operation. Additionally, the oscillation frequency depends on the oscillator bias current but it is independent on the applied static magnetic field (up to at least 1.5 T).

Figure 3.2 shows the phase and frequency noise spectral density (i.e. in dBc/Hz and Hz/$\sqrt{\text{Hz}}$) referred to the integrated LC oscillator output. The measurement are taken connecting the previously described set-up to an Agilent E5052A Signal Source Analyzer.

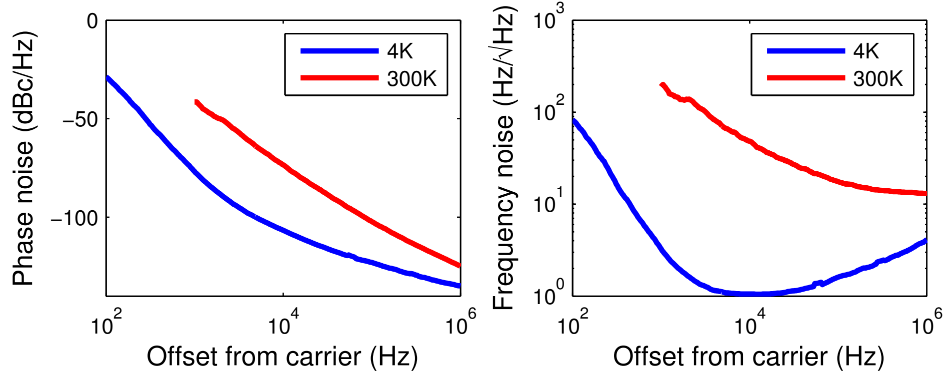

Figure 3.2 – Phase and frequency noise spectral density of the integrated LC-oscillators at 300 K and at 4.2 K. Oscillator bias current 3 mA at 300 K and 1.2 mA at 4 K

At 300 K, the noise at 100 kHz offset from the carrier is about 20 Hz/$\sqrt{\text{Hz}}$. At 4.2 K, a minimum noise of about 1 Hz/$\sqrt{\text{Hz}}$ is measured at 10 kHz offset from the carrier. Assuming R_{300K}=2 Ω, $V_{A,300K}$=1 V, R_{4K}=0.2Ω, $V_{0,4.2K}$=1V the frequency noise spectral density due to the coil series resistance, which is given by $S_V = kTR\omega^2/(2\pi)^2V_A^2$, are 2 Hz/$\sqrt{\text{Hz}}$ at 300 K and 0.1 Hz/$\sqrt{\text{Hz}}$ at 4.2 K, respectively. Consequently, the measured frequency noise is about an order of magnitude larger than the coil thermal noise limit at both temperatures, probably due to the noise contribution from the cross-coupled transistor pair. We observed that the measured frequency noise at low temperatures is highly dependent on the bias voltage V_A due the frequency jumps effect discussed in the next section.

3.3 Frequency jumps

In electronic circuits based on MOSFETs the major noise sources are the thermal noise due to the channel resistance and the 1/f noise, which is usually attributed to fluctuations in the number or mobility of the charge carriers in the channel [174–178]. The microscopic origin of the 1/f noise in MOSFETs devices has been thoroughly investigated [167, 174, 176, 179, 180]. These efforts are justified by the impact of the 1/f noise on key-performance of electronic circuits. The 1/f noise has, for example, a direct influence on signal-to-noise ratio deterioration in operational amplifiers [181] as well as on the phase noise of radio-frequency and microwave oscillators [128]. In small devices, some of the physical phenomena

responsible for the low frequency noise can be observed in the time domain as random telegraph signals (RTS) (also called random telegraph noise or burst noise). The superposition of RTS is considered as the major source (but not the only one) of the 1/f noise in small devices [177, 178, 182, 183]. The RTS phenomenon has been observed in many solid state devices, including point contact diodes [184], p-n junctions [185, 186] and MOSFETs [182, 187]. In MOSFETs it is usually observed as jumps between two (or more) drain-source current levels at fixed gate and drain-source voltages [167, 182, 187, 188]. These jumps are attributed to capture-emission of charge carriers by traps located in proximity of the conductive channel [167, 178, 183, 189].Nowadays, the interest in the investigation of the RTS (and of related phenomena such as the bias temperature instability [179]) is justified by its growing impact on the behaviour of many electronic devices as their size is downscaled [179]. For example, the performance of image sensors [190, 191] and memories [192, 193] are highly influenced by these phenomena.

Figure 3.3c shows some details of the experimental set-up where A and B are the DC bias of the oscillators, VDD is the DC supply for mixer and frequency-divider (1.5 V) and OUTp and OUTn are the differential output signal (at about 300 MHz). The frequency at the output of the chip is measured by an home made delay line discriminator (Figure 3.3d) [194].

Figure 3.4 shows the frequency difference between the two integrated oscillators as a function of the oscillator bias B at fixed bias A. Since the bias of the oscillator at the lower frequency is fixed, the decrease of the frequency difference corresponds to a decrease of the frequency of the oscillator operating at the higher frequency. This behaviour is due to the larger effective gate-source capacitance at higher bias [153, 195] as explained in chapter 2. At 300 K as well as at 77 K, the oscillation frequency is a continuous function of the oscillator bias voltage. For a bias sufficiently far from the oscillator start-up the curves at 300 and 4.2 K show similar slopes (about 1 GHz/V) but an otherwise different behaviour. At 4.2 K, the oscillator frequency show sharp transitions as a function of the oscillator bias current, with relatively flat regions between the sharp transitions. At 4 K, frequency jumps as large as 30 MHz (i.e., about 0.1% of the oscillation frequency) are experimentally observed.

Figure 3.5 shows variations of the frequency of the oscillator B as a function of the oscillator B bias voltage at 4 K taken with with an acquisition rate of 1.2 kHz and a bandwidth of 200 Hz. Figure 3.5a shows the oscillation frequency variation obtained in two consecutive upward sweeps of the oscillator bias voltage taken at a distance of 10 s. The position and amplitude of the frequency jumps is approximately the same in the two sweeps. Figure 3.5b shows the oscillation frequency variation obtained in two consecutive sweeps in opposite directions, each sweep lasting 5 s. The position of some frequency jumps shows an hysteresis, with shifts of the jumps to lower bias voltages for the downward sweep up to 50 mV. Figure 3.5c shows the oscillation frequency variation obtained in two non-consecutive sweeps in the upward direction separated by 10 hours. The position and amplitude of the jumps is significantly changed, indicating that after 10 hours the system has, at least partially, lost the memory of its initial state.

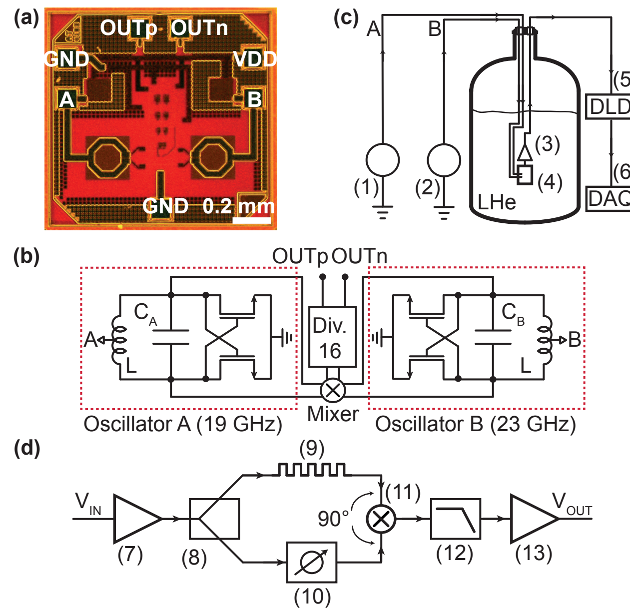

Figure 3.3 – (a) Photomicrograph and (b) block-diagram of the integrated circuit. A and B: DC bias of the oscillators, VDD: DC supply for mixer and frequency-divider (1.5 V). OUTp and OUTn: Differential output signal (at about 200 MHz). The transistor width/length is 20 μm/0.12 μm. L=300 pH, C_A=230 fF, C_B=160 fF. (c) Experimental set-up: (1) and (2) DC I/V sources (Keitley 2400), (3) buffer (TI THS4304D), (4) integrated circuit, (5) delay line discriminator, (6) data acquisition card (NI PCI-6259). (d) Block-diagram of the delay line discriminator: (7) RF amplifier (Minicircuits GVA-62 RF), (8) power splitter (Minicircuits SBTC-2-10LX), (9) 10 m long coaxial cable (Huber+Suhner RG58), (10) phase shifter (ATM P-1102), (11) mixer (Minicircuits JMS-5MH), (12) low pass filter, (13) amplifier (TI OPA1611).

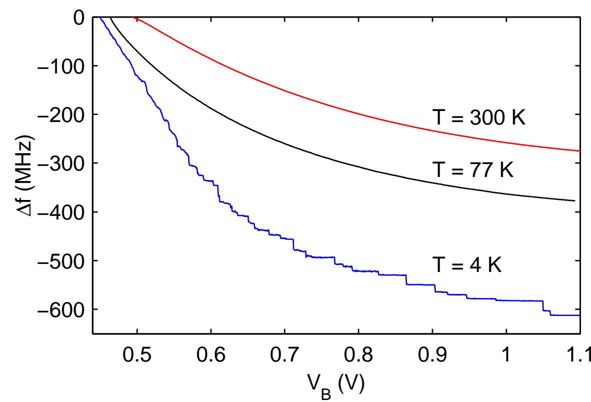

Figure 3.4 – Variation of the frequency of the oscillator B as a function of the oscillator B bias voltage at 300 K, 77 K, and 4 K. The frequency of oscillator B at the start-up of the oscillations (i.e., at a bias voltage of about 0.5 V, slightly dependent on temperature) are 21 GHz at 300 K and 77 K, and 23 GHz at 4 K. The frequency of the oscillator A, biased with a fixed current of 2 mA, are 17 GHz at 300 K and 77 K, and 19 GHz at 4 K. The frequency is measured with an effective bandwidth of 2.5 Hz. The sweep time is 20 minutes.

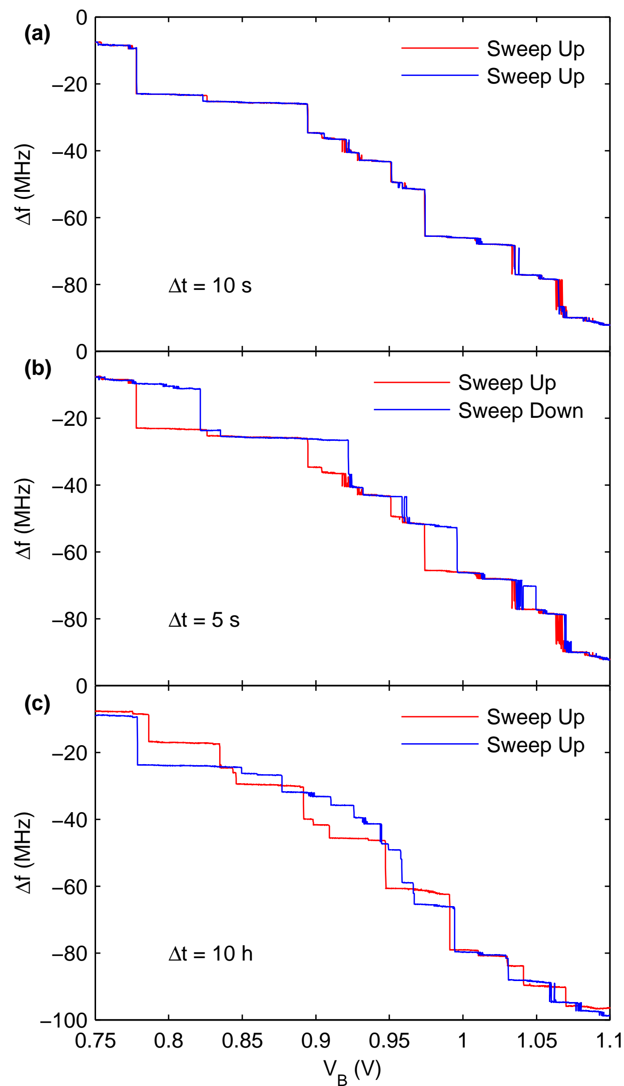

Figure 3.5 – Variation of the frequency of the oscillator B as a function of the oscillator B bias voltage at 4 K. (a) Two sweeps in the upward direction taken at a distance of 10 s, each lasting 5 s. (b) Two consecutive sweeps in opposite directions, each lasting 5 s. (c) Two sweeps in the upward direction, each lasting 5 s, measured at a distance of 10 hours. Oscillator A is biased with a fixed current of 3 mA. The frequency is measured with an acquisition rate of 1.2 kHz and a bandwidth of 200 Hz.

Figure 3.6 reports a more detailed analysis of the time dependence of the positions and amplitudes of the frequency jumps. It is an intensity graph representing the density of measured points in a series of consecutive upward sweeps of the oscillator B bias voltage, each lasting 5 s and separated by 10 s, measured at 4 K; the vertical bin is 200 kHz and horizontal bin is 57 μV. The acquisition rate is 1.2 kHz and the bandwidth is 200 Hz. In particular, Fig. 3.6 shows an intensity chart representing the density of measured points. Figure 3.6a (obtained in a measuring time of 0.8 h ,300 sweeps) is obtained in 300 consecutive upward sweeps of the bias voltage, resulting in a total measurement time of 0.8 hours. Figure 3.6b is obtained in 3600 consecutive upward sweeps, resulting in a total measurement time of 10 hours. This representation of the measured data indicates that after 10 hours a significant correlation in the obtained results is still present. In particular, the presence of well separated horizontal lines of higher density indicates that the frequency jumps are relatively constant in amplitude, giving rise to "forbidden" frequencies gaps. Figures 3.6c and 3.6d show zoom-in views of parts of the intensity charts to better visualize this behavior. Figure 3.6b shows that, on a time scale of several hours, more than one frequency value is observed at the same bias voltage.

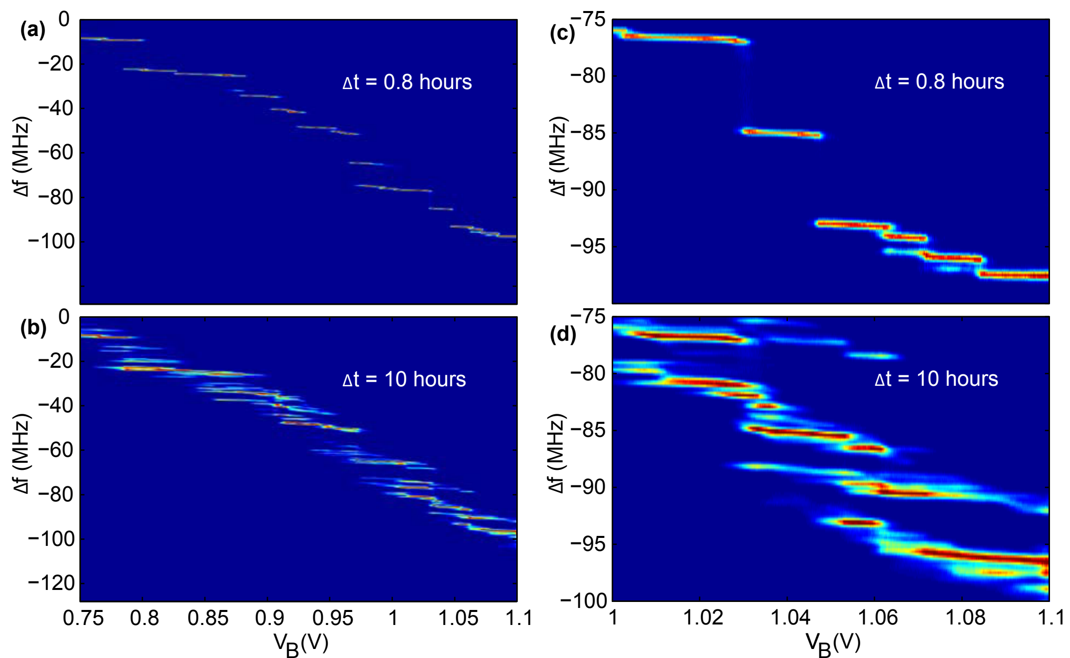

Figure 3.6 – Intensity graph representing the density of measured points in a series of consecutive upward sweeps of the oscillator B bias voltage, each lasting 5 s and separated by 10 s, measured at 4 K (vertical bin: 200 kHz, horizontal bin: 57 μV). Intensity graphs obtained in a measuring time of (a) 0.8 hours (300 sweeps) and (b) 10 hours (3600 sweeps), (c) and (d) zoom-in view of the previous graphs. The acquisition rate is 1.2 kHz and the bandwidth is 200 Hz.

This is confirmed also by measurements of the oscillator frequency at fixed oscillator bias voltage for several hours shown in figure 3.7. For a bias voltage approximately in the middle between two frequency jumps, the oscillator frequency is stable for a typical time of about

an hour. After this period of time it shows RTS like behavior between two or more levels for a typical time of some hours, eventually becoming again stable for an hour, assuming a value corresponding to one of the previous levels. We believe that this behavior is mainly due to an intrinsic instability at the transistor level and not to instrumental instabilities (such as noise on the oscillator bias voltage).

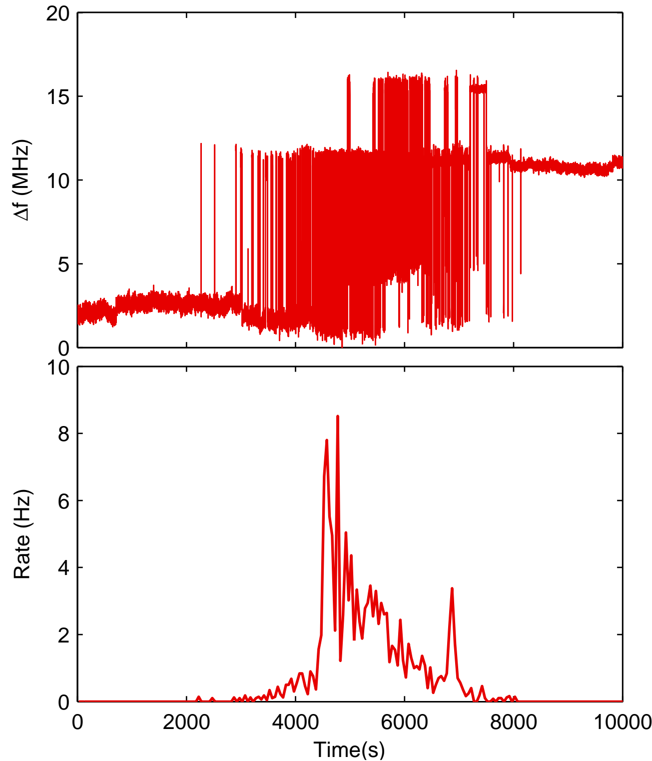

Figure 3.7 – Oscillator frequency at fixed bias voltage for several hours and related frequency jumps rate. The bias current of the oscillator A and B is 3 and 2.1 mA. The acquisition rate is 12 kHz and the bandwidth is 5 kHz.

Figure 3.8a shows the results of measurements performed at nearby oscillator B bias currents at 4K. The bias current of the oscillator A is 3 mA. The acquisition rate is 12 kHz and the bandwidth is 5 kHz. Changing the bias current from 1.935 to 1.953 mA (i.e., by 18 μA in total, corresponding to a variation of the bias voltage by 2 mV from 0.636 V to 0.638 V), the oscillation frequency changes by about 6 MHz. The fluctuations of the oscillator frequency not clearly associable to jumps are in the order of 40 kHz rms. At the lowest current the oscillator frequency shows no jumps. At intermediate currents it shows jumps of 6 MHz with a predominance of the higher or the lower level depending on the bias current. No jumps are observed at the largest bias current value. As shown in Fig. 3.8b, the ratio between the time spent in the upper frequency level τ_{up} and that spent in the lower frequency level τ_{down} is an exponential function of the bias current. This behaviour is very similar to the RTS observed by measuring the drain current as a function of time for different values of the gate voltage

[178, 180, 187, 188, 196].

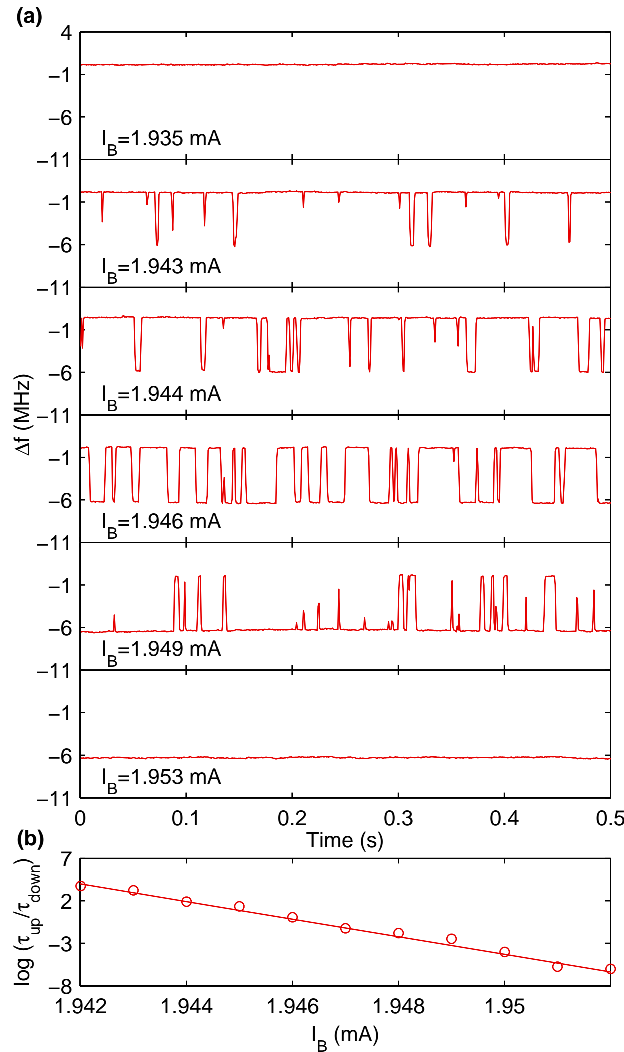

Figure 3.8 – (a) Variation of the frequency of the oscillator B as a function of time at slightly different oscillator B bias currents measured at 4 K. The bias current of the oscillator A is 3 mA. The acquisition rate is 12 kHz and the bandwidth is 5 kHz. (b) Ratio between the time at the higher frequency level and that at the lower level as a function of the oscillator B bias current (the red line is the exponential fit of the measured data).

Figure 3.9 shows a selection of measured signals at fixed oscillator B bias current for a measuring time of 1 s with acquisition rate of 5 kHz and bandwidth of 5 kHz. Depending on the bias current, multiple jumps between three to five different levels are possible, with jump amplitudes from 0.5 to 11 MHz.

The oscillator frequency variation versus oscillator bias voltage for sweeps in the same direction are identical for consecutive sweeps lasting 100 ms to 10 s, indicating that in this time

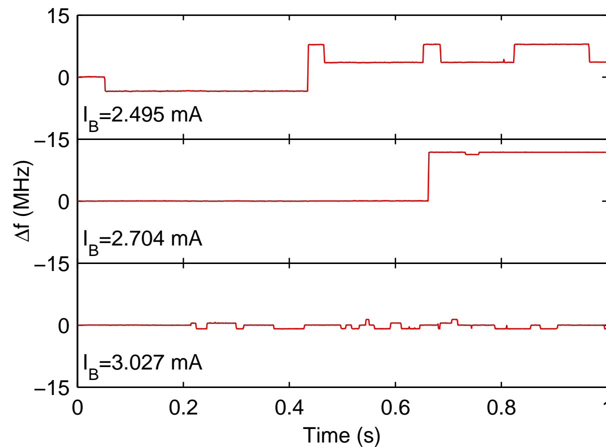

Figure 3.9 – Variation of the frequency of the oscillator B as a function of time at different oscillator bias voltages measured at 4 K. The bias current of the oscillator A is 3 mA. The acquisition rate is 12 kHz and the bandwidth is 5 kHz.

scale no relaxation nor drift processes are measurable. Some of the frequency jumps are "infinitely" sharp up to a resolution in the bias voltage of 0.3 mV and a time resolution of 0.2 ms, showing no RTS like behavior. At fixed oscillator bias current, the oscillator "bias" voltage shows synchronized jumps with the jumps in the oscillation frequency (Fig. 3.10). However, the ratio between voltage and frequency jumps is not the same for all transitions and it can be either positive or negative. A typical ratio is about ±1 mV/MHz but values as low as ±0.05 mV/MHz are also measured. The largest jumps of the oscillator bias voltage are of about ±6 mV. In some measurements, the voltage jump is not measurable because it is below the noise level (about 0.5 mV rms). The non-linear relationship between the frequency jumps and the bias voltage jumps indicates a certain degree of complementarity between the conventional RTS voltage or current observation and the oscillator frequency measurements reported in this work.

Finally, we have also observed that nominally identical oscillators (i.e., same technology and identical layout) as well as oscillators having identical topology (i.e., LC-oscillator made with cross-coupled MOSFETs) but realized with different CMOS technologies (STMicroelectronics 130 nm, TSMC 180 nm and TSMC 40 nm) show similar frequency versus bias characteristics, all characterized by frequency jumps at 4 K.

3.4 Conclusions

In conclusion we demonstrated the feasibility of integrated LC oscillator based on MOSFETs at 4 K. The oscillators frequency is about 10% higher with respect to room temperature probably due to lower gate and coil parasitic capacitance. The power consumption is reduced, due to lower coil resistivity and higher transistor transconductance for given current. The larger oscillator frequency variation as a function of the oscillator bias voltage observed at

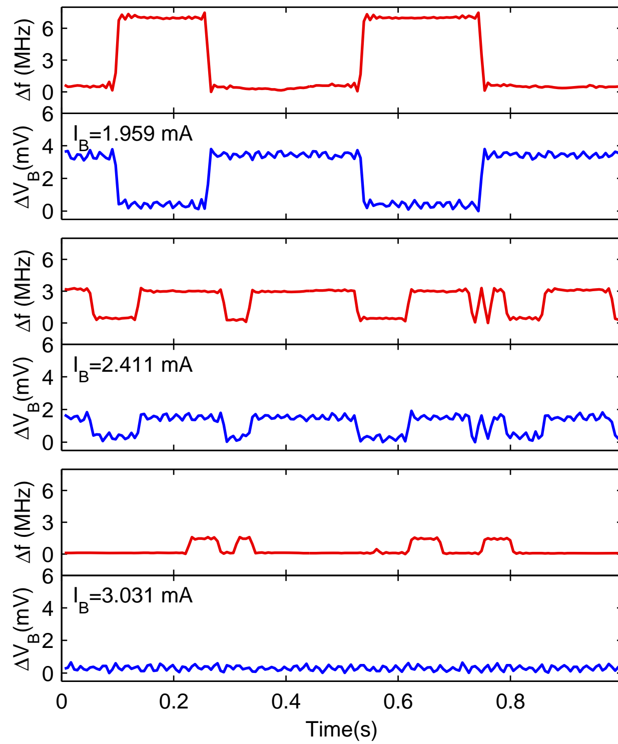

Figure 3.10 – Variation of the frequency of the oscillator B and its bias voltage as a function of time at 4 K. The bias current of the oscillator A is 3 mA. The acquisition rate is 12 kHz and the bandwidth is 5 kHz.

4 K with respect to 300 K (Fig. 3.4) might be due to the reduced impurity ionization at low temperature [197]. The observed oscillator frequency jumps can be tentatively attributed to two distinct phenomena: single boron atom ionization and capture/emission of single charges by defects. At 4 K, the boron atoms are weakly ionized in absence of an electrical field (i.e., at zero bias voltage) and, hence, the MOS capacitance due to the depletion region is very small. Increasing the bias voltage, boron atoms are progressively ionized by the electric field [197]. The ionization determines the formation of a depletion region and, consequently, the increase of the depletion capacitance and the decrease of the oscillation frequency. Although in our experiments the transistors voltages and currents are oscillating at several GHz and with large amplitudes (about 1 V and a few mA, respectively), the physical origin of some measured frequency jumps might be the same as the one generating the RTS with static and low-frequency biasing at low voltage and current levels. RTS in MOSFETs at low temperature [187, 196, 198] are usually attributed to capture/emission of charge carriers by defects at or near the Si/SiO2 interface.

In summary, in this work we show that, at low temperature, integrated LC oscillators based on MOSFETs present sharp frequency jumps as a function of the oscillator biasing and as a function of time. The observed phenomena might have a significant impact as additional tool for the investigation of present and future deep submicrometer integrated circuit technologies.

As outlook, in order to elucidate the physical origin and to obtain a quantitative model of the observed frequency jumps, it is certainly interesting to perform measurements at variable temperature and magnetic field. These experiments might allow to clarify the importance of tunneling and thermally activated processes [198] in the observed frequency jumps. Experiments at variable magnetic field [80, 179, 199], particularly in electron spin resonance conditions, might be useful to identify the defects responsible for the observed frequency jumps.

In addition to that it would be certainly interesting to study the behaviour of the oscillator at a temperature below the superconducting transition temperature of the miniaturized coil. Due to the low critical magnetic field of Al [200], the possibility to replace the aluminium integrated coils with a post-processing integration of coils made of materials having a larger critical field, such as thin films of Nb [61, 201, 202] might be considered.

Additionally, operation at temperatures below 1 K with a frequency above 100 GHz will allow to investigate the behaviour of the oscillator in the condition $kT < \hbar\omega_{LC}$. This condition combined with the dependence of the MOSFET gate-source capacitance on the oscillation amplitude, which determines the frequency Vs bias voltage characteristic shown in figure 3.4 and consequently introduces an anharmonicity in the oscillator behaviour, might allow us to observe a non-trivial quantum behaviour of the LC-oscillator.

4 ESR spectroscopy at cryogenic temperatures

4.1 Introduction

Methods based on the electron spin resonance (ESR) phenomenon are used to investigate samples in a wide temperature range, ranging from above 1000 K [203–206] to below 1 K [207, 208]. Low temperature measurements are usually performed in large microwave cavities as well as with miniaturized conductive [52, 209] or superconducting [60, 61] resonators. Miniaturized resonators are typically used to maximize the signal-to-noise ratio in experiments with mass-limited samples [48–50, 52, 54, 56, 91]. In Refs. [63, 91, 210] the group of Dr. G. Boero has presented single-chip integrated inductive ESR detectors, fabricated using complementary metal oxide semiconductor (CMOS) technologies, operating between 8 GHz and 28 GHz. The ESR phenomenon was detected as a variation of the frequency of an integrated LC-oscillator due to an effective variation of its coil impedance caused by the resonant complex susceptibility of the sample. Operation in the temperature range from 300 K to 77 K was demonstrated in Refs. [63, 210]. Depending on the specific sample (and, in particular on the dependence of its relaxation times on temperature), the possibility to operate down to 4 K might represent a significant advantage in terms of spin sensitivity (larger polarization, lower thermal noise) as well as in terms of information richness. In this thesis I have investigated the use of single chip LC oscillators as ESR detectors at temperatures down to 4 K.

4.2 Performance of the single-chip detector

The single chip detector used in the following experiments is the "K2 chip" which cryogenic behaviour is detailed in chapter 3 and appendix A.1. The value of B_1 generated by our single-chip detector is estimated by measuring the voltage at the oscillator bias node V_B. In condition of stable oscillation the oscillation amplitude $V_0 \approx V_B$ [211]. Hence, $B_1 \approx (1/2)B_u(V_B/\omega_{LC}L)$, where $B_u \approx \mu_0/d$, d is the coil diameter, and L is the coil inductance. This B_1 estimation is in agreement with saturation experiments with samples of known relaxation times. Figure 4.1 shows an illustration of the set-up used to characterize the performance of the single-chip

ESR detector. The chip is glued onto a printed circuit board and electrically connected by wire bonding. On the same printed circuit board a commercial amplifier is used as buffer to drive the coaxial cable carrying the chip output signal at about 300 MHz. The system operates properly in the range from 300 K down to at least 4 K (no measurements below 4 K have been performed yet). The printed circuit board is inserted in a dynamic continuous flow cryostat where the temperature is controlled by means of a temperature controller unit working with a thin film resistance temperature sensor. The signal at the output of the buffer is mixed, at room temperature, with a local oscillator signal having a frequency about 10 MHz higher. The signal at the output of the mixer (with a carrier frequency of about 10 MHz) is fed into a phase-locked loop (PLL). In most of the experiments, a magnetic field modulation at kHz frequencies is added to the static magnetic field to improve the signal-to-noise ratio as in ordinary ESR spectrometers. The signal at the output of the frequency-to-voltage converter is demodulated by a lock-in amplifier. The lock-in internal reference signal is amplified and applied to the field modulation coils. Some experiments are performed without field modulation. In order to use the spectrometer lock-in also in these measurements, the signal at the output of the frequency-to-voltage converter is chopped using a switch controlled by the 100 kHz reference signal of the lock-in amplifier, as shown schematically in Fig.4.1.

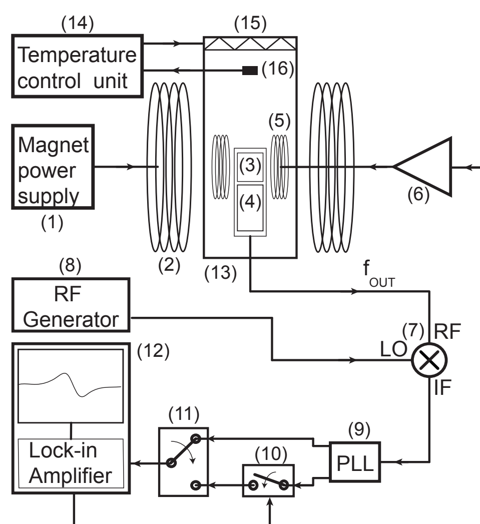

Figure 4.1 – Block diagram of the experimental set-up: (1) Electromagnet power supply (Bruker), (2) electromagnet (Bruker, 0 to 1.5 T), (3) single chip ESR detector, (4) buffer (Texas Instruments THS4304D), (5) magnetic field modulation coils, (6) power amplifier (Rohrer PA508), (7) mixer (Mini-Circuits ZAD-3), (8) signal generator (Rohde-Schwarz SMR-20), (9) phase locked loop (PLL) circuitry (see Ref. [63]), (10) RF Switch (Mini-Circuits ZYSW-2-50DR), (11) selection mode switch, (12) lock-in of the EPR spectrometer (Bruker Elexsys-II E500), (13) cryostat (Oxford Instruments CF935), (14) temperature controller (Oxford Instruments ITC503), (15) heater, (16) temperature sensor (Lake Shore Cernox CX1050).

As reported in Chapter 3 , at 300 K, the noise at 100 kHz offset from the carrier is about 20 Hz/$\sqrt{\text{Hz}}$. At 4.2 K, a minimum noise of about 1 Hz/$\sqrt{\text{Hz}}$ is measured at 10 kHz offset from the

carrier. The measured frequency noise at low temperatures is highly dependent on the parameters used in the temperature control loop and on the He pump settings, going from a minimum value of 1 to a maximum value of 100 Hz/$\sqrt{\text{Hz}}$. This is due to the influence of temperature instabilities on the oscillator phase noise and to the frequency jumps phenomenon discussed in chapter 3. Unfortunately, we are not yet able to find a strategy to reproducibly achieve the minimum frequency noise of 1 Hz/$\sqrt{\text{Hz}}$ in all measurements. However, this minimum frequency noise is reproducibly obtained when the chip is immersed in liquid helium.

4.3 Experimental results

To investigate the behaviour of the integrated LC-oscillator as electron spin resonance detectors we performed experiments with several different samples over the entire temperature range from 300 K to 4 K. In order to demonstrate the versatility of the realized single-chip ESR detector, we performed measurements with samples having significantly different characteristics: an exchange narrowed standard system (DPPH) , two hyperfine splitted systems having 100% and 1% concentrations (Cu^{2+} in TPP and in $Ni(mnt)_2$), a zero field splitted system (Cr^{3+} in Al_2O_3), and a very broad line Fe^{3+} system. Figure 4.2 shows measurements performed with two different samples placed on the coils of the two integrated oscillators. A spherical crystal of Cr^{3+}:Al_2O_3 (Ruby G10, Saphirwerk Industrieprodukt AG, Switzerland) having a concentration of 1% of Cr3+ is placed in the center of the 17 GHz oscillator coil. A single crystal of DPPH (1,1-diphenyl-2-picryl-hydrazyl) having a volume of about (4 μm)^3 is placed at the center of the 21 GHz oscillator coil. The DPPH sample is obtained by slow evaporation of a solution of DPPH powder (Aldrich D9132) in diethyl ether at room temperature in air (0.13% in volume of DPPH), as previously reported in Ref. [212]. As extensively investigate in Refs. [137, 213], the ruby spectrum consists of six lines, with intensity and position strongly dependent on the orientation of the crystal with respect to the applied static magnetic field. In the inset of Fig 4.2a, a background signal at $B_0 \approx 0.63$ T, which corresponds to g≈2 for the 17 GHz oscillator, is clearly visible (its amplitude is 5 kHz and its linewidth is 2.3 mT). The origin of the background signal, which is no more visible at low temperatures, is unclear. Figure 4.2 shows that the resonances are shifted towards higher magnetic fields at lower temperatures. This is due to the shift towards higher frequencies of the oscillators at lower temperatures discussed in chapter 3.

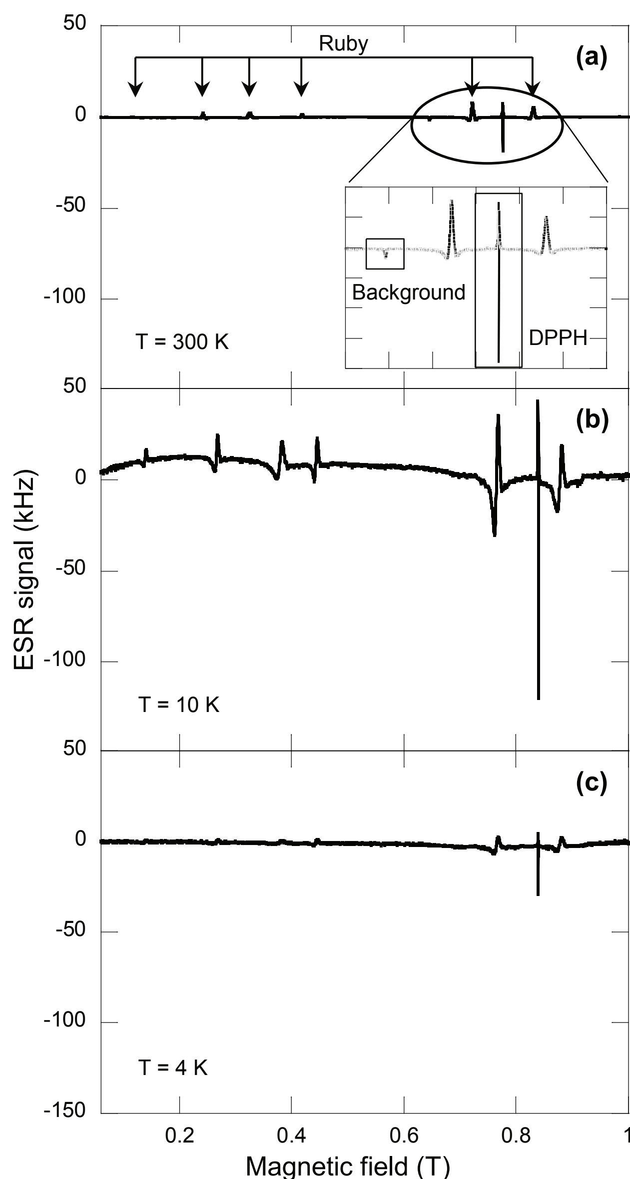

Figure 4.2 – ESR spectra. The experimental ESR signal shown here (in kHz) is the amplitude of the component at the field modulation frequency of the LC-oscillator frequency. Experimental conditions notations: T is the sample temperature, B_1 is the amplitude of the microwave magnetic field, B_m is the amplitude of the modulation magnetic field, ν_m is the frequency of the magnetic field modulation, t_s is the time interval of the magnetic field sweep, Δf is the equivalent noise bandwidth of the lock-in, ω_{LC} is the oscillator frequency far from the resonant magnetic field. ESR spectra of a spherical crystal of ruby sample (Cr^{3+}:Al_2O_3 sample with 1% Cr^{3+} content) having a diameter of 122 μm placed on the 17 GHz oscillator coil and a DPPH sample having size of about $(4\mu\ \mathrm{m})^3$ placed on the 21 GHz oscillator coil at different temperatures. Experimental conditions: ν_m=100 kHz, t_s= 335 s, $\Delta f \approx 3$ Hz,(a) $B_1 \approx 0.09$ mT, $B_m \approx 0.25$ mT.(b) $B_1 \approx 0.11$ mT, $B_m \approx 0.25$ mT.(c) $B_1 \approx 0.11$ mT, $B_m \approx 0.25$ mT.

Due to the temperature dependence of the oscillators frequencies mentioned above, in Fig. 4.3 (as well as in 4.4 and 4.5) the obtained spectra are plotted as a function of magnetic field offset with respect to the resonance condition. Figure 4.3 reports spectra of the DPPH sample obtained with narrow field sweeps about the resonance field at different temperatures. The spectra in Fig.4.2 are taken with a larger field modulation amplitude, optimized for the ruby sample (0.25 mT instead of 0.06 mT), and a faster sweep rate (30 G/s instead of 0.7 G/s) with respect to those in Fig.4.3 Combined with the fact that the two spectra are taken with the same lock-in time constant (about 80 ms), the DPPH spectra in Fig.4.2 are distorted whereas those in Fig. 4.3 are not.

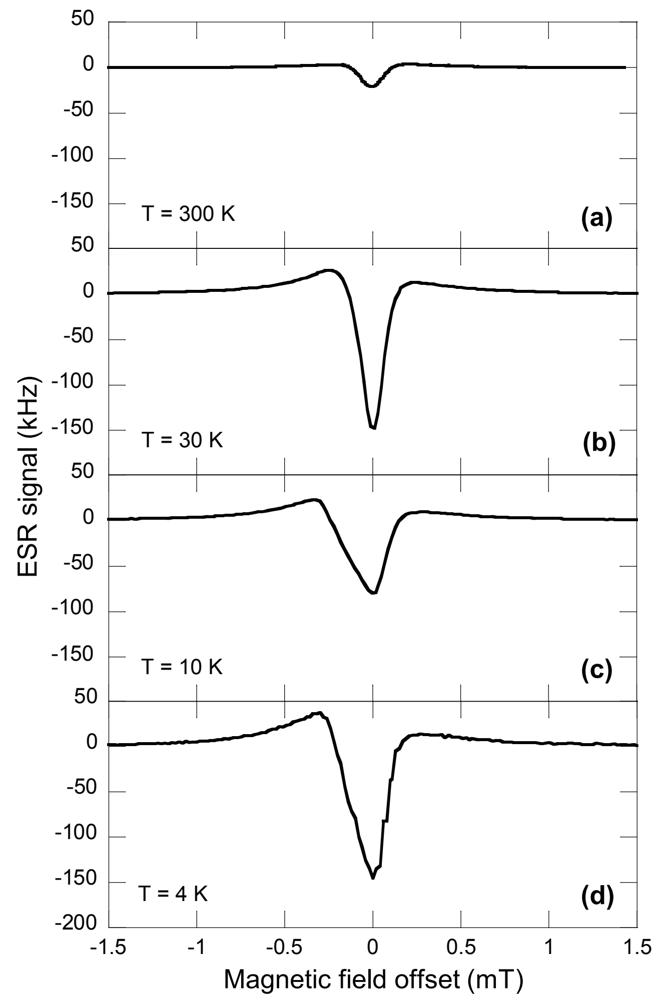

Figure 4.3 – ESR spectra of a DPPH sample having size of about $(4\mu\text{m})^3$ placed on the 21 GHz oscillator coil at different temperatures. Experimental conditions: $B_m \approx 0.25$ mT, ν_m=100 kHz, t_s= 42 s , $\Delta f \approx 3$ Hz, (a) $B_1 \approx 0.11$ mT, $B_m \approx 0.25$mT. (b-d) $B_1 \approx 0.11$ mT, $B_m \approx 0.06$mT. See notations in Fig. 4.2.

The narrow sweeps in Figs.4.3 are reported to show that the obtained signal shape corresponds, although only approximately, to the derivative of a dispersion signal as expected from field

modulation. These line-shape variations can be either due to an effective deviation from a perect Lorentian dispersion of the sample itself or to the oscillator behaviour that mixes the dispersion with the absorption. The opposite sign of the ruby and DPPH signals is due to the fact that the two samples are placed on two different oscillators and that the measured quantity is the difference between the two oscillators frequencies. An increase of the frequency of the oscillator operating at higher frequency corresponds to an increase of the frequency difference, whereas an increase of the frequency of the oscillator operating at the lower frequency corresponds to a decrease of the frequency difference.

Since DPPH has a spin concentration of about 2x10^{27} spins/m^3, the (4 μm)^3 sample contains about 10^{11} spins. The ESR signal is about 20 kHz at 300 K and about 180 kHz at 30 K, as expected in the Curie-law approximation. The measured frequency noise spectral density is 30 Hz/$\sqrt{\text{Hz}}$ at 300 K and 20 Hz/$\sqrt{\text{Hz}}$ at 30 K. Consequently, the experimental spin sensitivities, as defined by Eq. 11 in Ref. [91], is about $N_{min} \approx 5\text{x}10^8$ spins/$\text{Hz}^{1/2}$ at 300 K and 4x10^7 spins/$\text{Hz}^{1/2}$ at 30 K. At lower temperatures the DPPH signal becomes smaller and broader. As discussed above, in the temperature range from 4 to 10 K, the frequency noise spectral density assumes values from 1 Hz/$\sqrt{\text{Hz}}$ to 100 Hz/$\sqrt{\text{Hz}}$. This corresponds to spin sensitivities in the range from $N_{min} \approx 10^6$ spins/$\text{Hz}^{1/2}$ to $N_{min} \approx 10^8$ spins/$\text{Hz}^{1/2}$. By means of Eq 11 in Ref. [91], we can compute the expected spin sensitivity of the single-chip ESR detector. Assuming an Al resistivity at 4.2 K of $10^{-9}\Omega$m,(typical values are in the range $10^{-12}\Omega$m to $10^{-9}\Omega$m [170]), an Al thickness of 7.5μm, a coil trace width of 30μm,and a coil diameter of d= 200 μm, we obtain a coil microwave resistance R≈ 0.2 Ω and a unitary field $B_u \approx (\mu_0/d) \approx 6$ mT/A. Assuming $T_1 \approx T_2$, $B_0 \approx 1$ T, and T = 4.2 K, we obtain $N_{min} \approx 10^4$ spins/$\text{Hz}^{1/2}$. The relatively large B_1 produced by the integrated oscillator saturates partially the DPPH sample, decreasing the frequency variation by approximately an order of magnitude with respect to the optimal non saturated conditions. As a consequence of the larger noise and the reduced signal amplitude, the experimentally achieved spin sensitivity is two orders of magnitude worse than the one achievable under the optimal conditions considered above (i.e., for $\gamma^2 B_1^2 T_1 T_2 < 1$ and with a frequency noise only due to the coil resistance thermal noise). Figure 4.4 shows spectra of a single crystal of non-diluted Cu(II)-tetraphenylporphine (CuTPP, Aldrich 25182) having a volume of about (80 μm)^3.

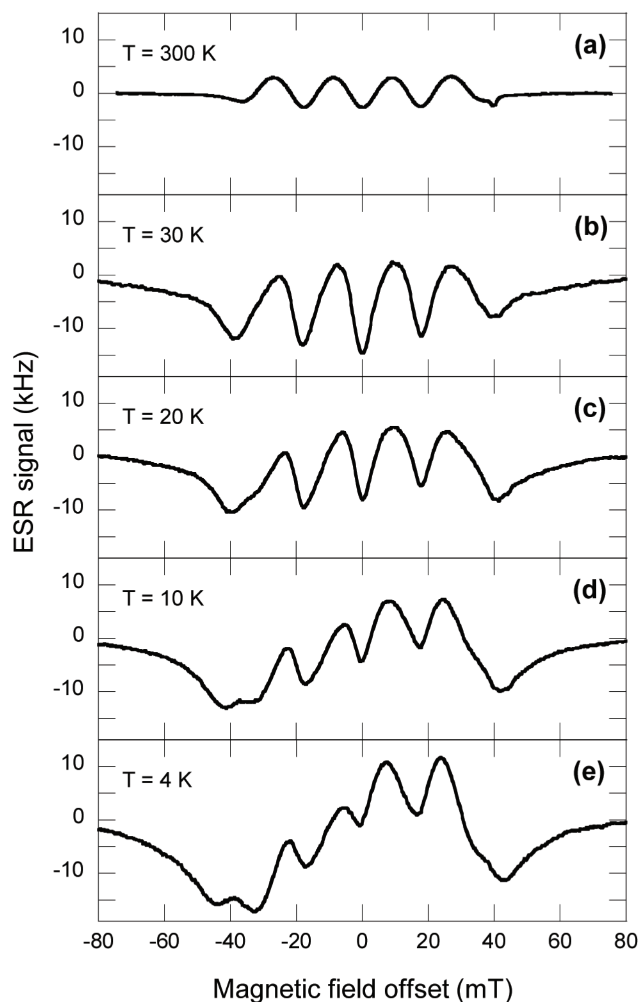

Figure 4.4 – ESR spectra of single crystal of CuTPP having a volume of about (80μm)^3 at different temperature placed on the 17 GHz oscillator coil at different temperatures. Experimental conditions: $B_m \approx 0.25$ mT, ν_m=100 kHz, t_s= 84 s , $\Delta f \approx 6$ Hz, (a) $B_1 \approx 0.09$ mT, (b-e) $B_1 \approx 0.11$ mT. See notations in Fig. 4.2.

Figure 4.5 shows spectra of a single crystal of Cu^{2+} doped tetramethylammonium bis (maleonitriledithiolato) nickel with a Cu concentration of 1% (1% $Cu(mnt)_2$) in $Ni(mnt)_2$) and a volume of about (120 μ)^3. All spectra show the hyperfine splitting produced by the Cu nuclei (^{63}Cu and ^{65}Cu), having spin I=3/2. The CuTPP spectra are similar in shape but the signal amplitude does not increase following the Curie law. The 1% $Cu(mnt)_2$ spectra have amplitudes which also do not follow the Curie law and have shapes which are highly temperature dependent. For both samples this behaviour is probably due to the temperature dependence of their relaxation times.

Figure 4.6 shows spectra of a (200 μm)^3 microcrystalline powder of synthetic β-haematin (Fe(III)-protoporphyrin-IX)$_2$, a synthetic analogue of haemozoin, a product of haemoglobin

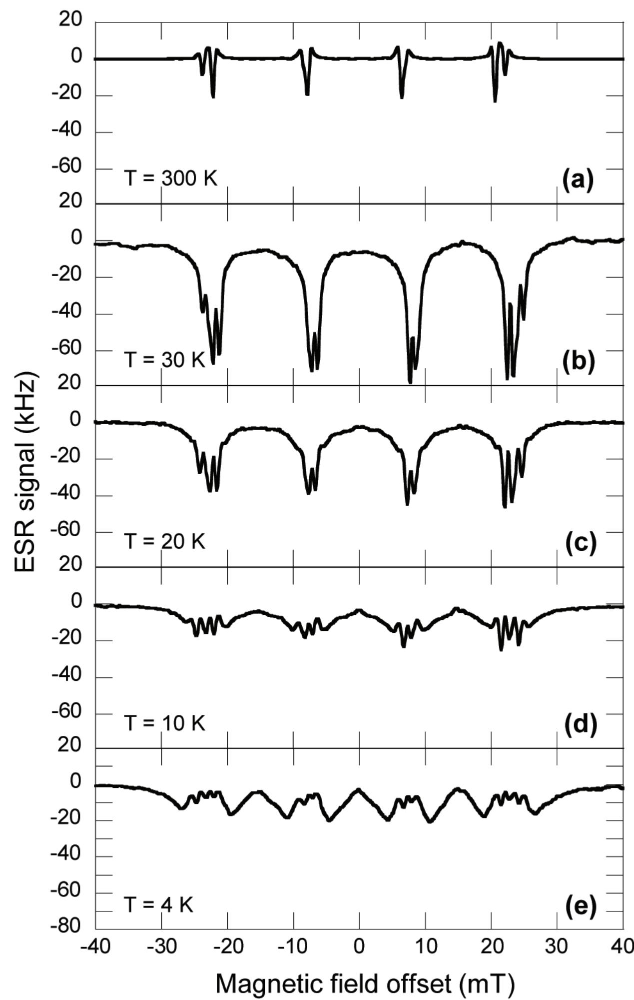

Figure 4.5 – ESR spectra of single crystal of $Cu(mnt)_2$ in $Ni(mnt)_2$ with a Cu concentration of 1% having a volume of about (120 μm)^3 at different temperature placed on the 21 GHz oscillator. Experimental conditions: $B_m \approx 0.25$ mT, ν_m=100 kHz, t_s= 84 s , $\Delta f \approx 6$ Hz, (a) $B_1 \approx$ 0.09 mT,(b-e) $B_1 \approx 0.11$ mT. See notations in Fig. 4.2.

responsible for malaria [214, 215]. Due to the very broad resonance lines (about 0.2 T) with respect to the maximum magnetic field modulation achievable with our set-up (about 1 mT), a better signal-to-noise ratio is obtained by measuring the spectra without magnetic field modulation. The sample is placed at the center of the 17 GHz oscillator. Figure 4.6 shows measurements performed at different temperatures. No signal is measurable at room temperature. As reported in Ref.[216] the ESR spectra of β-haematin consist of a strong signal at $g_{eff} \approx 4$, and a weaker signal at $g_{eff} \approx 2$. These measurements are taken by chopping the signal at the frequency-to-voltage converter output (see Fig.4.1 and discussion above). The inset of Fig.4.6d shows the component after four averages. These measurements on synthetic β-haematin show that our single-chip ESR detector has a relatively weak low frequency noise (about 300 Hz rms with a bandwidth of 13 Hz and a sweep lasting 80 s) which allows for

measurements without field modulation, a desirable feature for measuring resonance lines much broader than the maximum achievable magnetic field modulation amplitude.

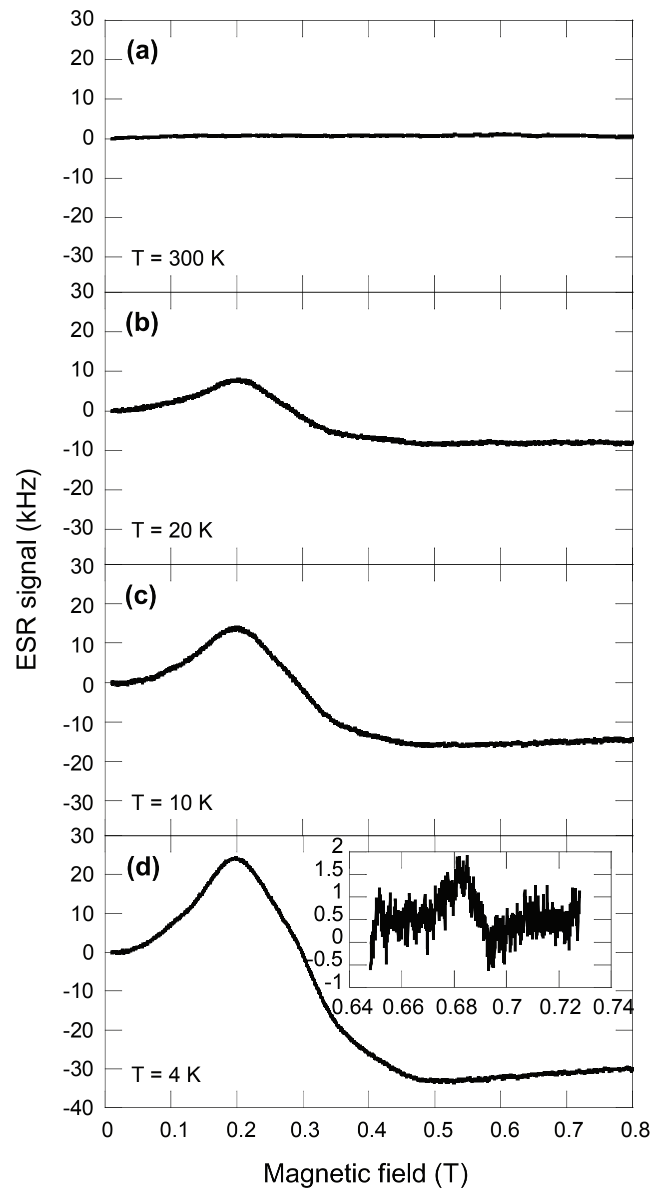

Figure 4.6 – ESR spectra acquired at different temperatures for a microcrystalline powder of synthetic β-hematin having a volume of about $(200\mu\text{m})^3$ at different temperature placed on the 17 GHz oscillator. Inset: blowup of the $g \approx 2$ region of the ESR spectrum. Experimental conditions: t_s= 84 s, $\Delta f \approx 13$ Hz, (a) $B_1 \approx 0.09$ mT,(b-d) $B_1 \approx 0.07$ mT. See notations in Fig. 4.2.

4.4 Conclusions and outlook

In this work we have experimentally demonstrated that CMOS single-chip microwave LC-oscillators are a valid alternative to miniaturized resonators [52, 52, 209] for high spin sensitivity ESR spectroscopy on mass limited samples in the entire temperature range from 300 K down to at least 4 K. The spin sensitivity measured with a sample of DPPH is 10^8 spins/ $Hz^{1/2}$ at 300 K and down to 10^6 spins/ $Hz^{1/2}$ at 4 K. These values are more than an order of magnitude better that recent results obtained with a sample of DPPH using a miniaturized resonator [209], and similar to those obtained with a sample of *E* centers in SiO_2 at 300 K and with a sample of phosphorous doped silicon (^{28}Si:P) at 10 K also measured with a miniaturized resonator [54]. Due to the dependence of the spin sensitivity on the relaxation times, the comparison with the remarkable results reported in [54] obtained with different samples is only indicative. In the following, I describe the main advantages and disadvantages of single-chip microwave oscillators with respect to miniaturized resonators. The small size of each chip and the on-chip downconversion of the ESR signal into a robust frequency-encoded signal might allow one to create dense arrays of independent detectors that can be placed in the same magnet for simultaneous measurements of different samples. The integration of all components responsible for the spin sensitivity within a distance of 100 μm from the detection coil reduce the signal losses to a minimum. This might be particularly important at frequencies exceeding 100 GHz where conventional approaches requires expensive technologies to limit the losses and the degradation of the signal-to-noise ratio. CMOS LC-oscillators operating up to 300 GHz have been already reported [92, 120] and operation at THz frequencies might be possible in the near future [217]. This means that the single-chip microwave oscillator approach is suitable up to the largest magnetic fields currently available. The local conversion of DC power into a near-field in a non-radiating microwave magnetic field obtained with the single-chip microwave oscillator might be interesting also as a local source of microwaves for dynamic nuclear polarization (DNP) experiments. The main disadvantage of our single-chip approach is the difficulty in producing low B_1 fields. This problem is particularly relevant for samples easily saturated (i.e., having a large relaxation times product T_1T_2). Currently, with a coil having a diameter of the order of 100 μm, we can hardly produce B_1 fields significantly smaller than 0.1 mT. As explained in chapter 2, this is due to the fact that the microwave current in the integrated coil cannot be made arbitrarily small: a minimum value is required to sustain stable oscillations. A possible solution might be the use of non steady-state techniques to our detection approach, such as the rapid scan of the magnetic field [218] or the oscillator frequency [219]. A rapid frequency scan can be easily implemented by means of a voltage controlled capacitor placed in parallel to the integrated oscillator coil or by means of the frequency jumps phenomenon. As previously discussed, temperature instabilities in the cryostat affect significantly the oscillator frequency noise. These problems are caused by the fact that, contrary to conventional approaches, the microwave source is located in the cryostat and it is nested in the detector itself. Although we believe that the temperature instability problem can be solved by a careful optimization of the temperature control system or by a less temperature sensitive oscillator design, the effectiveness of these solutions is not demonstrated yet. As

shown in chapter 3 there are oscillator bias condition in which the frequency jumps are rare events on the time scale of an ESR magnetic field scan and hence their effect is negligible on ESR experiments. In the future investigation of the possibility to operate the CMOS single-chip detectors below 4 K will be performed.

5 Single chip ESR detectors from 28 to 170 GHz

5.1 Introduction

In Chapter 1 we stated that integrated ESR detector can possibly achieve, if operative at frequency in the order of 100 GHz or above, sensitivity which are possibly five orders of magnitude better if compared with state of the art commercial inductive detector and can possibly approach single spin detection if operative at cryogenic temperature. Furthermore spectroscopy at high field can be an effective tool for studying spectra which are not completely resolved at lower fields [220–223] and the integrated source could be possibly used as microwave source for DNP-NMR spectroscopy [224, 225]. In order to make a relevant step ahead a chip operative at about 200 GHz (i.e. 7 T) has been designed. Even if operation at frequency in the range of 300 GHz or above has been already demonstrated with standard CMOS technology [92, 120] the design of a device operating at about 200 GHz is not straight forward due to the lack of models valid in the range of interest. In order to be conservative, to test the available technology, and to completely exploit the available area I decided to design on the same chip several systems operative at about 28, 55, 110 and 200 GHz. The design methodology for the higher frequency systems (i.e. above 100 GHz), together with the measurements of the fabricated chip are presented in the following.

5.2 Design of the ESR detector

In order to design an oscillator with a maximum operative frequency of 200 GHz a technology with a maximum operative frequency (i.e. f_t) larger than 200 GHz is necessary. In this case I've chosen the 40 nm bulk CMOS technology provided by TSMC which has a maximum f_t in the order of 400 GHz. The lower frequency system (28-50 GHz) are designed with the methodology proposed in [154]. Usually oscillator operative at millimeter wave are designed by using only NMOS, due to the higher speed of NMOS devices if compared to PMOS [127]. Since the technology allow operation of PMOS at high frequency, two versions of the 28 GHz system are implemented, one using both N and PMOS (CMOS oscillator) and one using a more classical

NMOS approach. Since they operate at a frequency well below the maximum one, in a region where foundry models are still valid, they can be designed using standard design procedures. Even if, in theory, operation at higher frequencies is possible, the models provided by the foundry are not valid for frequency above 90 GHz. In fact, sophisticated electromagnetic simulations performed with Keysight Momentum (a 3D planar electro-magnetic simulator initially intended to be used for the design) shows unsatisfactory result already at frequencies around 90 GHz, making simulation based on the design kit useless for our purpose. In order to overcome this problem, a simpler model capable of predicting the start-up of the oscillator and its operating frequency has been developed. Using the technology data provided by the foundry (i.e. list of materials, metals and oxides thickness) a simple model of the integrated micro-coil has been developed based on the equations found in [226, 227]. The model is analogous to the one presented in chapter 3 and reproduced in figure 5.1 for completeness. Even if some important effects such as substrate coupling and proximity effects are not considered in the model, the model describe the system with sufficient accuracy. Furthermore even if we expect to operate at frequencies above 100 GHz, we can still use the lumped model approximation since the wave-length on silicon is much longer than the largest interconnection metal (i.e. $\lambda \approx 800\ \mu$m at 100 GHz). In equation 5.1 the equation describing the element of the model are presented.

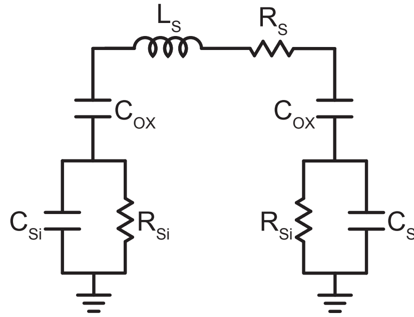

Figure 5.1 – Integrated coil lumped model

$$
\begin{aligned}
L_S &= K_1 \mu_0 \frac{d_{avg}}{1+K_2\eta} \\
R_S &= \frac{\rho l}{w\delta(1-e^{-t/\delta})} \\
C_{OX} &= \frac{1}{2} l w \frac{\epsilon_{OX}}{t_{OX}} \\
C_{Si} &= \frac{1}{2} l w C_{Sub} \\
R_{Si} &= \frac{2}{l w G_{Sub}},
\end{aligned}
\tag{5.1}
$$

where K_1= 2.25 and K_2= 3.55 are the coefficient for the modified Wheeler equation for octagonal coil [226], d_{avg} is the average coil diameter, η is the coil fill ratio defined as $2w/2d_{avg}$,

w, t and l are the coil metal width, thickness and length respectively, ρ is the metal resistivity at DC, δ is the skin depth at the oscillating frequency, ϵ_{OX} and t_{OX} are the oxide dielectric constant and thickness, C_{Sub} and G_{Sub} are the silicon substrate capacitance and conductance for unit area [227]. Information regarding the silicon capacitance and conductance, unless directly measured on chip, are usually hardly accessible. For this reason and since their effect on the oscillation frequency, at least at room temperature, is marginal they are neglected in the following description. After this consideration the self resonance frequency (i.e. the maximum frequency at which the coil can operates) can be written as:

$$f_{sr} = \frac{1}{2\pi\sqrt{\frac{L_S C_{OX}}{2}}}. \tag{5.2}$$

The self resonance is the starting element for our optimization approach, allowing us to immediately discard all the coil that can't operate at the target frequency. As explained in chapter 2 the active device will further load the resonator with its parasitic capacitance. For each possible coil the additional capacitance required for operation at the target frequency it's then computed. Since for operation at frequencies above 100 GHz the required capacitance for coil with reasonable performance (i.e. quality factor higher than 10 and self resonance above the target frequency) is in the same order of magnitude of the MOS capacitance, no extra capacitor are added to the resonator. From the additional capacitance required for operation at the target frequency an extra load for the down conversion chain and metal interconnection it is deduced. This is estimated in about 10 fF. The remaining capacitance it is allocated to the cross-coupled network and, knowing the gate capacitance per unit area, define the maximum gate width (since the length for operation at high speed is set to minimum) for a given coil. At the last step, the start-up condition has to be checked. The total capacitance is C_{tot}=C_{DC}+C_{MOS}+C_0 where C_{DC} is ≈ 10 fF, C_{MOS} is the MOS cross-coupled capacitance and C_0 is the added capacitance in parallel with the inductor. The transistor transconductance it's extracted by means of Spectre simulation, and the related negative admittance it's computed. Since the oscillator operates at a frequency closed to f_t the performance of the transistor are lowered by it's own parasitics, that drain the output current toward ground. For accounting this effect, and taking some design margin, the MOS transconductance is lowered by an order of magnitude. The taken margin has been considered as reasonable considering that the transistor gain gets equal to 1 at a frequency that is just double of the target one. As explained in chapter 2 the parallel admittance of the overall network is computed and, if the resulting admittance is negative, meaning that the oscillator will start-up, the system is a possible solution for our problem. Since, as explained in chapter 3, low power operation at cryogenic temperature it is also crucial, the system operative with the minimum power consumption has been chosen and then implemented. The layout of the cross-coupled pair is designed by means of the layout strategy explained in [98] and the transistors are placed as closed as possible to the resonator. Block diagram and schematic of the realized system and oscillator

are shown in figure 5.2 and all the element sizes are summarized in table 5.1.

Table 5.1 – Integrated system detail: f_0 oscillator frequency; d_{coil} coil external diameter; w_{coil} coil width; L coil inductance; C_{tot} resonator capacitance (in parenthesis the value of C_0 if present), W_n NMOS transistor width, W_p PMOS transistor width. The transistor length is 40 nm for all the designs

System	f_0 (GHz)	d_{coil} (μm)	w_{coil} (μm)	L (pH)	C (fF)	W_n (μm)	W_p (μm)
28 CMOS	28	180	15	274	118 (100)	9.6	24
28 NMOS	28	190	15	260	125 (100)	12	-
55 NMOS	55	120	15	117	71 (50)	13	-
105 NMOS	105	70	10	65	35 (15)	13	-
200 NMOS	200	45	5	53	12	9.6	-

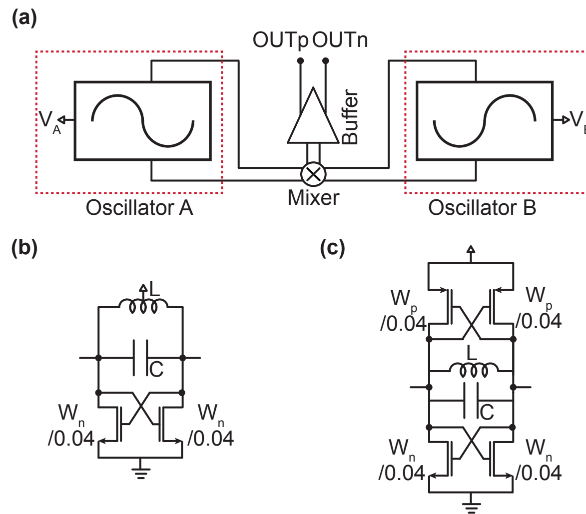

Figure 5.2 – (a) Block-diagram of the integrated circuit. V_A and V_B: DC bias of the oscillators. OUTp and OUTn: Differential output signal. Transistor level schematic of the integrated detector: (b) NMOS oscillators, (c) CMOS oscillator.

5.2.1 Down-conversion chain design

As explained in chapter 2 it is unpractical to drive with reasonable amplitude the bonding pad with low power consumption and high speed. A possible solution has been found by frequency mixing of two oscillators operating at a frequency offset as small as possible. As explained in chapter 2 the frequency offset must be above a certain level in order to avoid injection locking between the two systems. This limit the minimum frequency offset. Two identically designed oscillator are placed on the same chip. This is possible since I estimated that the frequency offset arising from device mismatch and unavoidable interconnection layout difference is enough for avoiding injection locking of the two systems (for the 200 GHz devices an offset of 1 GHz is estimated). Assuming the two oscillators operating at a frequency offset in the order

of 1 GHz (reasonably the largest frequency offset between two identically designed oscillator placed in closed proximity), a frequency mixer based on the double-balance Gilbert cell it is designed. The mixer, as shown in figure 5.3a, it is biased with a resistance since simulations of the 28 and 55 GHz systems shows that it is the best way for avoiding mixer flicker noise up-conversion into oscillator phase noise. In this way the mixer power consumption can be controlled by the oscillator amplitude and when oscillator low power operation is required, for example for operation at cryogenic temperature, the mixer will also operates at its minimum current. For limiting the capacitive load mismatch for the two oscillators (i.e. difference of few fF for operation at 100 GHz or above translate in frequency mismatch in the order of few GHz) the mixer is designed with the two lower switches with size that are double if compared with the four upper one. In this way the only load mismatch is coming from the different metal interconnection required for the oscillators-mixer interconnections. For driving the bonding pad required for electrical connection an output buffer it is designed. For allowing better control of the power consumption the bias current it is provided by either an external component (i.e. a resistor placed on the PCB) or by means of an external current source. To further reduce the power consumption the output buffer is designed as class AB output stage. The simulated down-conversion chain can drive a capacitive load of 1 pF at 1 GHz with an amplitude of 10 mV and a power consumption of 800 μW (considering a mixer driven by two oscillators working at 200 and 199 GHz respectively and with 1 V amplitude)

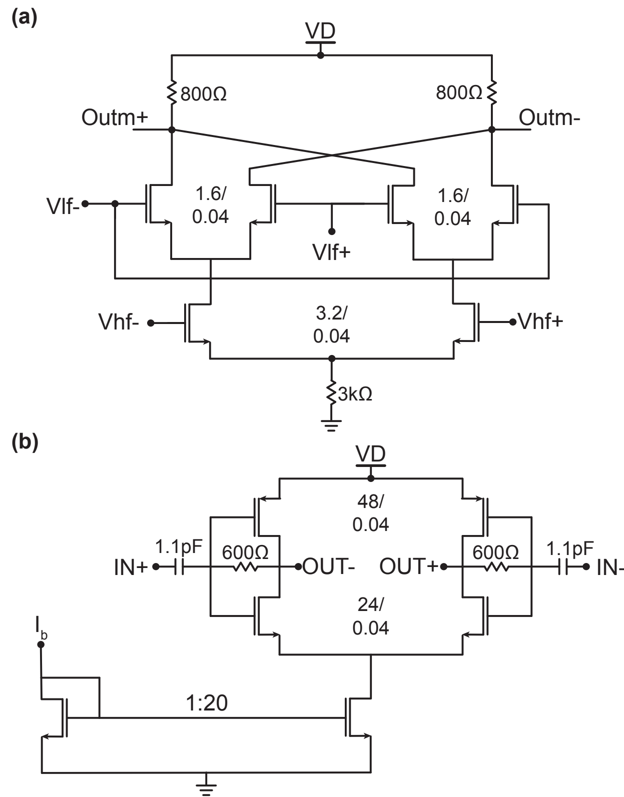

Figure 5.3 – Transistor level schematic of the integrated detector down conversion chain: (a) Schematics of the frequency mixer. (b) Block diagram of the class AB output buffer. $V_D \approx 1.1$ V, $I_B \approx$ 1-10 μA)

5.3 Performance of the realized devices

The realized device is shown in figure 5.4. It is designed with the 40 nm bulk CMOS technology provided by TSMC. This technology is accessible for universities through the Europractice Miniasic shuttle program. In this way it is possible to purchase a single block of 1.85 x 1.85 mm^2. Since our larger systems have sizes below 500 μm, for optimizing the area filling, multiple systems can be placed in the chip area. For this reason, and with the aim of comparing the performance of similar oscillators working at different frequencies, oscillators operating at nominal frequencies of 28, 55, 110 and 200 GHz are designed. In Figure 5.4 the details of the interconnection are also shown. They are identical for all the systems with the exception of the 28 GHz CMOS.

Since the system does not allow to have direct access to the oscillator frequency, this is measured by means of ESR spectroscopy. The set-up used for the measurement it is shown in figure 5.5. A sample of BDPA (Sigma 35585-94-5) is placed at the center of each oscillator and the field at resonance is measured with an NMR magnetometer. In this way it is possible to

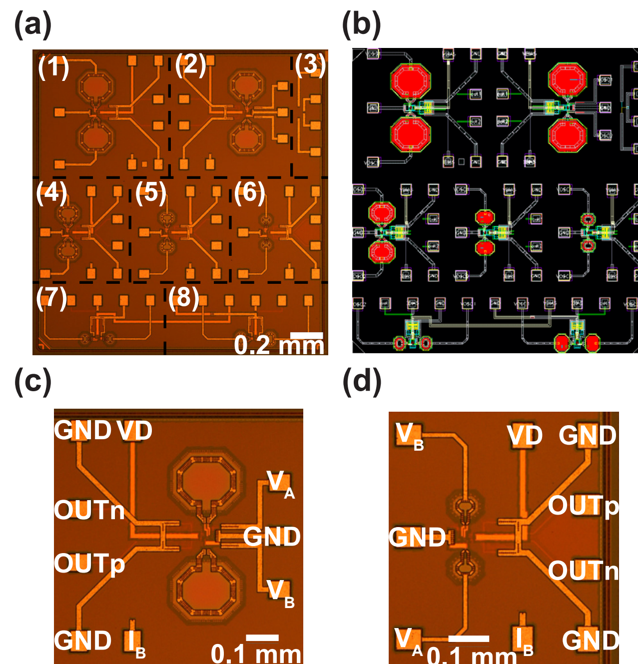

Figure 5.4 – (a) Optical microscope image of the realized chip. 1) 28 GHz detector, 2) 28 GHz CMOS detector, 3) Cross-coupled pair test structure, 4) 55 GHz detector, 5, 8) 110 GHz detector, 6, 7) 200 GHz detector. (b) layout, (c, d) detailed interconnection for the 28 GHz CMOS and 200 GHz device. V_A and V_B: DC power supply of the two oscillators (0.5 to 1.1 V). VD: DC power supply for the mixer and output buffer (1.1-1.5 V). I_B: DC power supply for the output buffer (1-10 μA). OUTp and OUTn: differential output signal ($\approx$ 1 GHz).

characterize the system operating at 28 and 50 GHz. Since in our laboratory at the moment we have no access to a variable field magnet above 2 T, it is not possible to characterize a system operating at a frequency above 56 GHz with the same method. In order to measure the oscillation frequency of the nominally 105 and 200 GHz oscillators, the chip are assembled over a probe suitable for being inserted inside a 7.05 T NMR fixed field magnet (Bruker 300). As close as possible to the chip a Hall sensor magnetometer (Asahi HZ302C) it is mounted for measuring the field at resonance. The resonance is revealed by monitoring the DC output of the delay line discriminator (figure 5.5). Exploiting the fringing field of the 7 T magnet, by slow insertion of the probe it is possible to recognize the ESR resonance. Once there's evidence of the resonance we measure the magnetic field with the previously calibrated Hall sensor. In this is way an effective oscillation frequency of 105 and 170 GHz is measured for the 110 and 200 GHz systems respectively.

A Spectrum obtained with the set-up of figure 5.5 and the oscillator operating at 170 GHz is presented in figure 5.6. The spectrum is obtained with a sample of $CuSO_4$ and it is distorted by the strong gradient of the magnetic field. A field at resonance of about 6.1 T is measured which coresponds to an oscillation frequency of about 170 GHz.

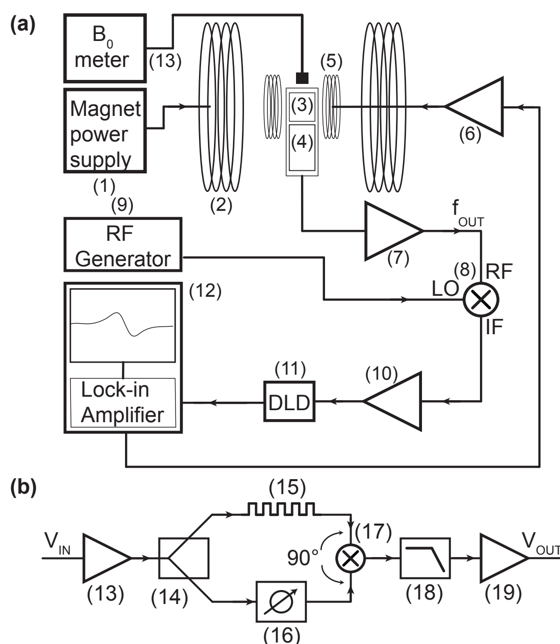

Figure 5.5 – Block diagram of the experimental set-up: (1) Electromagnet power supply (Bruker), (2) electromagnet (Bruker, 0 to 2 T), (3) multi-band ESR detector, (4) buffer (Texas Instruments THS4304D), (5) magnetic field modulation coils, (6) power amplifier (Rohrer PA508), (7, 10) low noise amplifier (Mini-Circuits ZFL-1000LN),(8) mixer (Mini-Circuits ZFM-2000), (9) signal generator (Rohde-Schwarz SMR-20), (11) Delay line discriminator, (12) lock-in amplifier (EG&G 7265), (13) NMR Tesla-meter (Metrolab PT2025). (b) Block-diagram of the delay line discriminator: (13) RF amplifier (Minicircuits GVA-62 RF), (14) power splitter (Minicircuits SBTC-2-10LX), (15) 10 m long coaxial cable (Huber+Suhner RG58), (16) phase shifter (ATM P-1102), (17) mixer (Minicircuits JMS-5MH), (18) low pass filter, (19) amplifier (TI OPA1611).

Even if designed and layouted with the aim of reducing the load mismatch between the two oscillators, the oscillator operating at 105 and 170 GHz, show a measured frequency offset larger then expected (an offset below 2 GHz was expected for the 170 GHz device). The measured frequency offset, at equal bias for the two oscillators are 1.8 and 4 GHz for the 105 and 170 GHz system respectively. The offset is about 350 MHz for the 50 GHz system and 100 MHz for the 28 GHz CMOS. For the higher frequency devices the frequency offset can be reduced down to 300 and 800 MHz by changing the bias point of the two oscillators. A reduction of the frequency offset has been observed also when the oscillators are cooled down at 77 K. In this case the offset when both the oscillator are biased at the same point goes down to 1 and 2 GHz for the 105 and 170 GHz device respectively. When biased at room temperature the oscillators, in the 170 and 105 systems, start-up for a bias current of about 1.6 mA. The voltage measured at the bias point is of 0.6 V making the power consumption at start up of about 1 mW. The down-conversion chain drain 1 mA current from a 1.1 V supply voltage, consuming 1.1 mW. The system overall power consumption at room temperature is about 3 mW. When the oscillator is cooled down at 77 K, due to higher transistor efficiency and lower losses in the resonator, the start-up current reduce to about 1 mA with a voltage measured

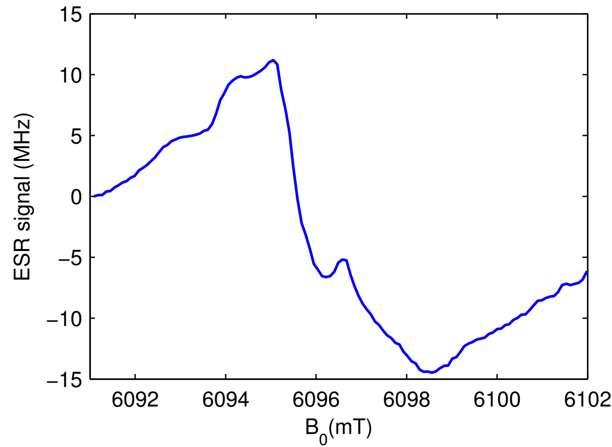

Figure 5.6 – ESR spectra of a $CuSO_4$ crystal having size of about $(20\mu m)^3$ placed on the 170 GHz coil. Experimental conditions: T=300, $f_0 \approx$ 170 GHz, t_s= 30 s, See notations in Fig. 5.11.

at bias point of 0.6 V. This lower the power consumption of the integrated oscillators to 0.6 mW and of the integrated microsystem to 2.2 mW. Last electronic check concern the phase noise coming from the system. This is been measured by means of the home made delay line discriminator detailed in figure 5.5. The results are summarized in table 5.2 .

Table 5.2 – Integrated system detail at 300 K: f_0 oscillator frequency; $PN_{100\,kHz}$ phase noise at 100 kHz offset; $PN_{1\,MHz}$ phase noise at 1 MHz offset; $FN_{100\,kHz}$ frequency noise at 100 kHz offset; $FN_{1\,MHz}$ frequency noise at 1 MHz offset.

f_0 GHz	$PN_{100\,kHz}$ dBc/Hz	$PN_{1\,MHz}$ dBc/Hz	$FN_{100\,kHz}$ Hz/$\sqrt{Hz}$	$FN_{1\,MHz}$ Hz/$\sqrt{Hz}$
28 CMOS	-60	-88	100	40
28 NMOS	-	-	-	-
50 NMOS	-64.5	-92	60	25
105 NMOS	-52	-82	250	80
170 NMOS	-48	-80	390	105

5.3.1 Cryogenic characterization

Measurements of the realized device operating at 50, 105 and 170 GHz at 4 K are presented in the following. The measurements are carried out by inserting the microsystem in a liquid helium bath with a set-up analogous to the one presented in chapter 3. All the cryogenic effects reported in chapter 3 for the 20 GHz oscillator in the 130 nm IBM technology are present in this design too. In particular the minimum power consumption of the oscillators it is reduced. This is equal to 125 μW (0.28 mA, 0.45 V) for the 50 GHz system; to 450 μW (0.9 mA, 0.5 V) for the oscillator at 105 GHz; to 730 μW (1.3 mA, 0.56V) for 170 GHz system. The minimum observed

down conversion chain consumption (minimum power for reasonable amplitude at minimum oscillation power) is, for the 105 GHz system of 330 μW (0.3 mA, 1.1 V). The minimum total power consumption are thus about 600 μW, 1.2 mW and 1.8 mW for the 50, 105 and 170 GHz devices respectively. The offset between the two oscillators when biased with the same voltage further reduce if compared with room temperature. The offset goes down to about 180 MHz, 800 MHz and 1.8 GHz for the three devices respectively. Unfortunately, at the moment, we don't have access to a cryo-system allowing us to measure the system absolute frequency through ESR experiments at 4 K. Based on the previous experience reported in chapter 3 the system is expected to be faster with respect of the room temperature behaviour. In figures 5.7, 5.8, 5.9 the frequency bias characteristics for the devices are shown. Since on the devices a frequency division module is not integrated, the absolute frequency variation is directly accessible from the output. Assuming to measure the frequency variation while keeping one of the two oscillator at fixed bias this will cause the system output signal to reach the limit of our acquisition set-up (i.e. about 1 GHz). For overcoming this problem the measurements range is divided in more scan. At the end of each scan the oscillator A bias (that is not swept) is moved toward the other in order to cancel the too high frequency difference. The obtained curve are then joined and shown in figures 5.7, 5.8, 5.9.

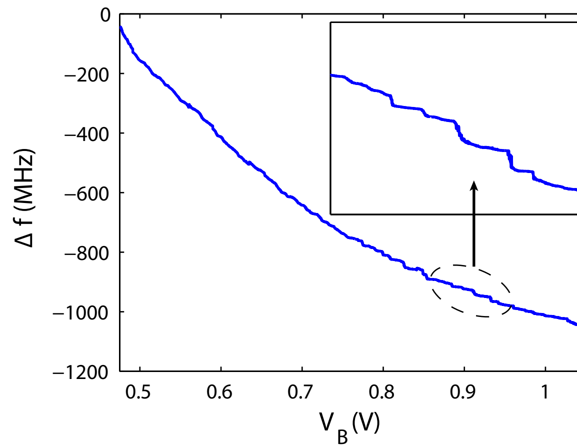

Figure 5.7 – Variation of the frequency of the 50 GHz oscillator B as a function of the oscillator B bias voltage at 4 K. The frequency is measured with an effective bandwidth of 2.5 Hz. The sweep time is 20 minutes.

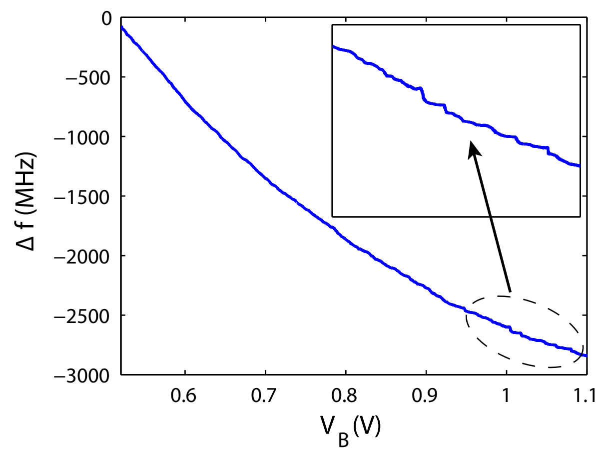

Figure 5.8 – Variation of the frequency of the 100 GHz oscillator B as a function of the oscillator B bias voltage at 4 K. The frequency is measured with an effective bandwidth of 2.5 Hz. The sweep time is 20 minutes.

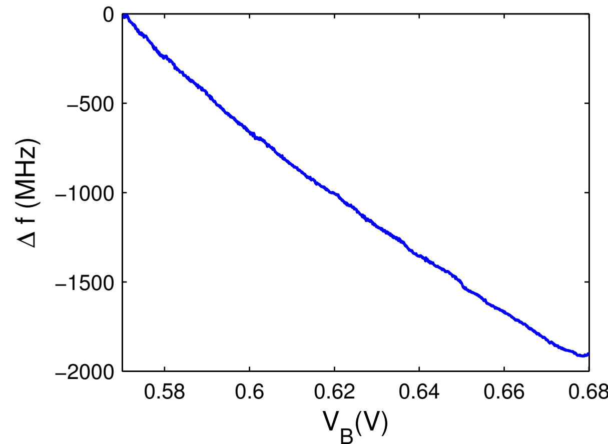

Figure 5.9 – Variation of the frequency of the 170 GHz oscillator B as a function of the oscillator B bias voltage at 4 K. The frequency is measured with an effective bandwidth of 2.5 Hz. The sweep time is 10 minutes.

The curve in figure 5.9 is obtained after a partial sweep, since the bias voltage of transistor A required for bringing the frequency offset at a level low enough for being detected by our set-up would exceed the gate break-down voltage. In figures 5.7 and 5.8 frequency jumps similar to the one shown in chapter 3 are shown. This jumps are more evident at high bias level. Since it's not been possible to measure the characteristic at high bias this jump are less evident for the 170 GHz oscillator. It's been anyway proven their presence by measurement taken at fixed bias for long time that shown the appearance of frequency jumps of about 60 MHz. The measured phase noise with all the system characteristics are summarized in table 5.3. Cooling the oscillator from 300 K to 4 K the phase noise clearly improve for the 50 GHz system, it remains almost the same for the 100 GHz and it get worse for the 170 GHz system. The cause of this behaviour are attributed to the absence of zones without jumps that are observed for the faster systems.

Table 5.3 – Integrated system detail at 4 K: f_0 oscillator frequency; P_{Osc} oscillator minimum power consumption; P_{Sys} system minimum power consumption; $PN_{100\,\mathrm{kHz}}$ phase noise at 100 kHz offset; $PN_{1\,\mathrm{MHz}}$ phase noise at 1 MHz offset; $FN_{100\,\mathrm{kHz}}$ frequency noise at 100 kHz offset; $FN_{1\,\mathrm{MHz}}$ frequency noise at 1 MHz offset.

f_0 GHz	P_{Osc} mW	P_{Sys} mW	$PN_{100\,\mathrm{kHz}}$ dBc/Hz	$PN_{1\,\mathrm{MHz}}$ dBc/Hz	$FN_{100\,\mathrm{kHz}}$ Hz/$\sqrt{\mathrm{Hz}}$	$FN_{1\,\mathrm{MHz}}$ Hz/$\sqrt{\mathrm{Hz}}$
50 NMOS	0.125	0.6	-92	-107	10	4
105 NMOS	0.45	1.2	-54	-82	200	80
170 NMOS	0.73	1.8	-43	-72	700	250

In figure 5.10 rapid frequency acquisition of the 100 GHz system are performed for slightly different bias voltages. The observed phenomenon is similar to the one observed in chapter

3. By slightly changing the oscillator bias it is possible to observe different transition rates as expected from the RTS theory.

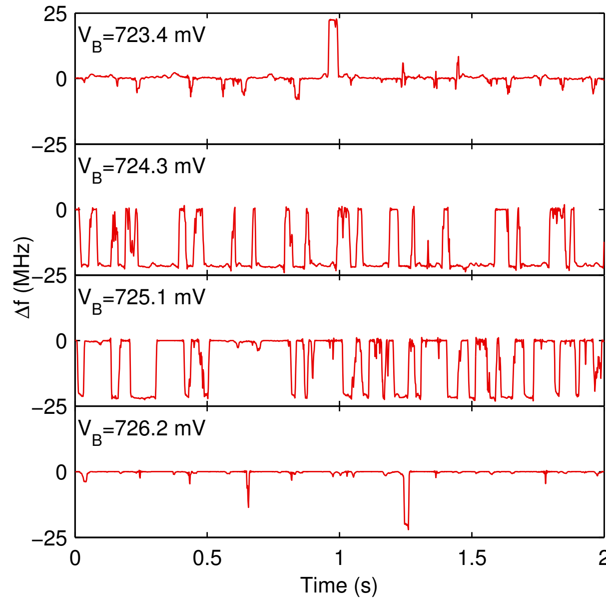

Figure 5.10 – Variation of the frequency of the 100 GHz oscillator B as a function of time at slightly different oscillator B bias voltages measured at 4 K. The bias voltage of the oscillator A is 1 V. The acquisition rate is 12 kHz and the bandwidth is 5 kHz.

5.3.2 ESR measurements

In the following preliminary ESR measurements performed with the 50 and 100 GHz systems are briefly discussed. The measurements are taken with the set-up detailed in figure 5.5. In figure 5.11 are shown measurement of a single crystal of BDPA (α ,γ-Bisdiphenylene-β-phenylallyl) having a volume of about (2 μm)^3 placed at the center of the 50 GHz oscillator coil. Through line-width resonance measurements at different B_1, this is estimated in a range that goes from 0.05 mT at low bias level (i.e. 700 μA and 0.55 V) to 1.5 mT at high bias level (i.e. 15 mA and 1.1 V). Since BDPA has a spin concentration of about 1.5x10^{27} spins/m^3, the (2 μm)^3 sample contains about 10^{10} spins. The ESR signal is about 30 kHz and the measured frequency noise spectral density is 60 Hz/$\sqrt{\text{Hz}}$. Consequently, the experimental spin sensitivities, as defined by Eq. 11 in Ref. [91], is about N$_{min} \approx$ 7x10^7 spins/Hz$^{1/2}$.

In Fig 5.12, a background signal (i.e. measured without sample on the oscillation coil) at B$_0$ $\approx$1.76 T, which corresponds to g$\approx$2 for the 50 GHz oscillator, is clearly visible (its amplitude is 10 kHz and its linewidth is 1 mT). The signal is the superposition of the background arising from the two oscillators that are operating at a frequency offset of about 500 MHz (about 18 mT). If compared with the background signal presented in chapter 4 and [63] the main signal is about two times narrower and additional features are visible. The origin of the background signal, is unknown. In oscillator designed with a different older technology provided by the

same foundry (TSMC180nm) the observed background is not present. This might indicate that the background signal might be originated by technological steps that are introduced in deep-submicrometer MOS technology, making ESR of background signals a potentially interesting tool for IC technology investigations. Figure 5.13 shows measurements performed with a crystal of Cr^{3+}:Al_2O_3 having size of about $(60\mu m)^3$ and a concentration of 1% of Cr3+ placed in the center of the 50 GHz oscillator coil. As extensively investigated in Refs. [137, 213], the ruby spectrum consists of six lines, with intensity and position strongly dependent on the orientation of the crystal with respect to the applied static magnetic field. The background signal detailed in Fig 5.12 is clearly visible.

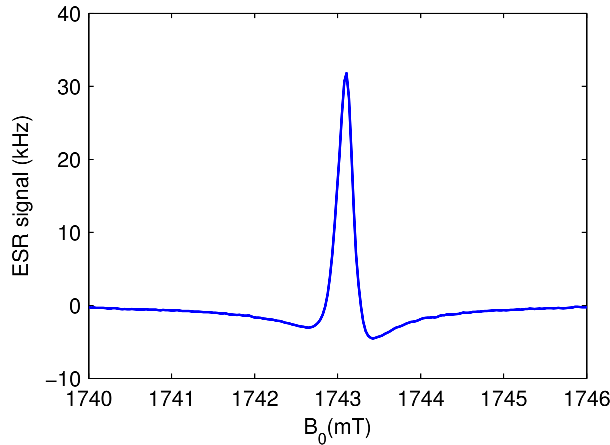

Figure 5.11 – ESR spectra. The experimental ESR signal shown here (in kHz) is the amplitude of the component at the field modulation frequency of the LC-oscillator frequency. Experimental conditions notations: T is the sample temperature,f_0 is the oscillation frequency, B_1 is the amplitude of the microwave magnetic field, B_m is the amplitude of the modulation magnetic field,ν_m is the frequency of the magnetic field modulation, t_s is the time interval of the magnetic field sweep,Δf is the equivalent noise bandwidth of the lock-in. ESR spectra of a BDPA sample having size of about $(2\mu m)^3$ placed on the 50 GHz coil. Experimental conditions:T=300 K, $f_0 \approx 50$ GHz, ν_m=100 kHz, t_s= 50 s, $\Delta f \approx 2.5$ Hz, $B_1 \approx 0.09$ mT, $B_m \approx 0.1$mT.

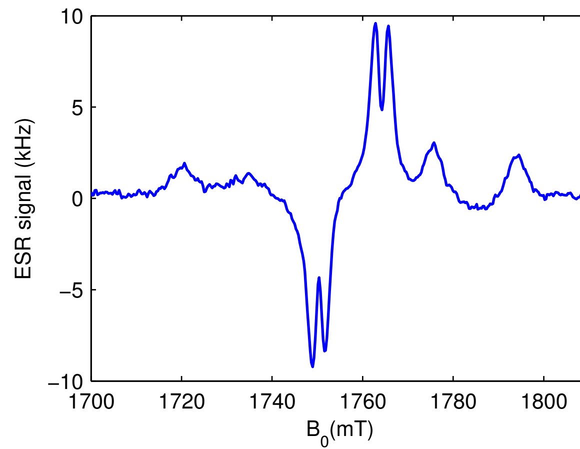

Figure 5.12 – Background ESR spectra. Experimental conditions: T=300 K, $f_0 \approx$ 50 GHz, ν_m=100 kHz, t_s= 50 s, $\Delta f \approx$ 2.5 Hz, $B_1 \approx$ 0.15 mT, $B_m \approx$ 1 mT. See notations in Fig. 5.11.

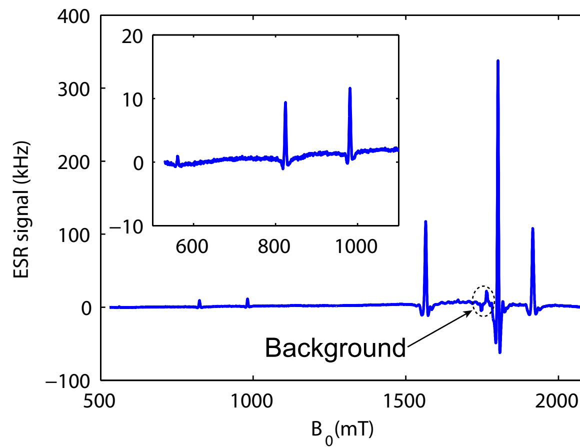

Figure 5.13 – ESR spectra of a Ruby crystal having size of about (60μm)^3 placed on the 50 GHz coil. Experimental conditions: T=300 K, $f_0 \approx$ 50 GHz, ν_m=100 kHz, t_s= 300 s, $\Delta f \approx$ 2.5 Hz,$B_1 \approx$ 0.15 mT, $B_m \approx$ 1 mT. See notations in Fig. 5.11.

In order to test the systems operating at 100 GHz preliminary measurement of a ruby crystal having size of about $(70\mu m)^3$ are shown in figure 5.14. Unfortunaltely, since the maximum available field is of about 2 T, the only measurable signal is the one related to the resonance appearing at the lowest field.

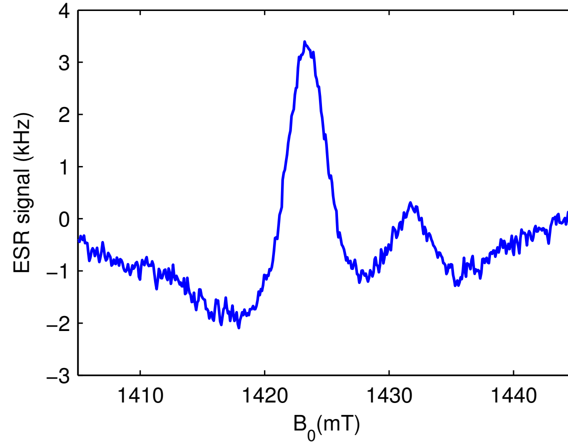

Figure 5.14 – ESR spectra of a Ruby crystal having size of about $(70\mu m)^3$ placed on the 105 GHz coil. Experimental conditions: T=300 K, $f_0 \approx$ 105 GHz, ν_m=100 kHz, t_s= 30 s, $\Delta f \approx$ 2.5 Hz, $B_m \approx$ 1 mT. See notations in Fig. 5.11.

Since they are operating at higher frequency and with smaller coil, the oscillator at 105 and 170 GHz are expected to have better spin sensitivity if compared to the 50 GHz system. However the stronger phase noise at 100 kHz offset partially cancel the benefit arising from the higher operation frequency. This is due to the fact that at higher frequency, the effect of the up-conversion of the transistor flicker noise on the phase frequency noise get dominant at small offset from the carrier. This makes the noise contribution arising from the coil resistance negligible and hence reduce the expected sensitivity improvement. Nevertheless an improvement of a factor three in sensitivity moving from 50 to 170 GHz is expected. The sensitivity of the 50 GHz device can be improved by a factor of two by modulating the signal at 1 MHz frequency. In the case of 1 MHz modulation the improvement expected in the sensitivity by moving to 170 GHz is about five.

5.4 Conclusions

In this chapter a design methodology for high frequency low power cross-coupled LC oscillators has been introduced. The methodology has been validated through design and measurements of systems operating at frequency ranging from 28 to 170 GHz. Operation at 4 K of the devices has been also demonstrated. As a best result a system operative at 170 GHz with about 3 mW power consumption at room temperature and 1.5 mW at 4 K has been measured. When operative at 4 K the realized devices show behaviour that are similar to the one presented in chapter 3. In addition to that on the higher frequency devices, bias zones

free of frequency jumps are not observed. With the realized devices a spin sensitivity of about 10^7 spins/$\sqrt{\text{Hz}}$ (i.e. at least 3 order of magnitude better than commercial devices has been proven. The higher frequency devices operates in a regime where the condition $kT < \hbar\omega_{LC}$ is met. This condition combined with the dependence of the MOSFET gate-source capacitance on the oscillation amplitude, which introduces an anharmonicity in the oscillator behaviour, might allow to observe a non-trivial quantum behaviour of the LC-oscillator. Furthermore the chip capability of locally convert DC power into a non radiating microwave magnetic field can be exploit as a local, inexpensive source of microwaves for dynamic nuclear polarization (DNP) experiments at high field.

6 Conclusions and outlook

6.1 Summary

During this work several integrated micro systems for ESR spectroscopy were developed. We demonstrated the possibility of using integrated LC oscillators operating in a frequency range from 20 GHz to 170 GHz as detectors for ESR. Operation at cryogenic temperature of integrated LC oscillators has also been demonstrated and a first study of cryogenic effects has been carried out. Furthermore the possibility of using our approach for performing ESR spectroscopy at temperature down to 4 K has been demonstrated.

6.2 Conclusions

We have demonstrated the operability of integrated LC oscillators based on silicon MOSFET at frequencies up to 170 GHz and temperatures down to 4 K. Several effects are observed when operating in these conditions. Oscillator power consumption at start-up reduces mainly due to the lower losses arising from the coil and for the higher transistor efficiency. The oscillator frequency increase, probably due to the lower coil parasitic capacitance. The frequency-bias characteristic shows larger variation if compared with the room temperature curve, probably due to the reduced impurity ionization at low temperature. Furthermore the curve profile at 4 K shows a succession of smooth zones and sharp transitions. The observed frequency jumps are tentatively attributed to the same mechanism responsible for the RTS with static and low-frequency biasing at low voltage and current levels. In conclusion LC oscillators based on MOSFET might be a useful tool for studying the impact of RTS like phenomena on the new sub-micrometer technology.

We have also demonstrated the possibility of using CMOS single-chip microwave LC-oscillators for high spin sensitivity ESR spectroscopy on mass limited sample at temperature from 300 K down to at least 4 K. The measured spin sensitivity with DPPH sample is 10^8 spins/$\sqrt{\text{Hz}}$ at 300 K and down to 10^6 spins/$\sqrt{\text{Hz}}$ at 4 K with the 20 GHz system. The measured spin sensitivity with BDPA sample at 50 GHz is about 10^7 spins/$\sqrt{\text{Hz}}$ at 300 K. The sensitive volume of the

realized devices ranges from about 250 to 10 pl. The developed technique can reach spin sensitivity comparable with the one of miniaturized resonators [52–59] but with several potential advantages. First of all the implementation of all the electronics needed for the spectroscopy experiment in the single chip allow one to create a dense arrays of independents detectors that can be placed in the same magnet for parallel measurements on different samples. Furthermore the integration of all the component responsible to the spin sensitivity within a distance of 100 μm from the detection coil reduce the signal losses to a minimum. The main disadvantage of the proposed technique is the difficulty in producing B_1 lower then 0.1 mT. This is due to the fact that a minimum current is needed for reliable start-up of the oscillator. This is a problem for sample that shows long relaxation time and hence easily saturates. In addition to that, since the microwave source in the cryogenic experiment is placed in the cryostat, the device noise is strongly related to the stability of the environment. This make a more accurate design of the cryo-system required, if compared with the standard approach where the microwave source is placed outside the cryostat. Furthermore, the difficulties in pulsing the oscillation frequency in the time scale required by pulsed ESR experiment limit the use of the technique to CW experiments. The realized device are compared with the state of the art oscillators by means of the FOM defined in chapter 2. The computed FOM are summarized in table 6.1 and the comparison with state of the art oscillators is shown in figure 6.1. As is it possible to notice our oscillator behaves slightly worse then the best reported in literature. This can be partially attributed to the fact that our output signal is the mixing of two oscillators with comparable noise performance, increasing the overall system phase noise by 3 dB. Even if this approach is not the optimum concerning the noise, it allow us to limit the system power consumption to few mW, crucial aspect for operation at cryogenic temperatures. Furthermore the measurement method employed measure double side band instead of single side band noise. The combination of this two effects together contribute to lower the phase noise performance by a factor of two. For our oscillators the FOM improve by moving toward higher frequency. This confirm the conclusion of the literature study performed in chapter 2. This means that the larger noise related of the higher frequency systems does not cancel the increased signal strength. This translates in the fact that the best FOM, and hence the best spin sensitivity, can be achieved with the highest frequency system.

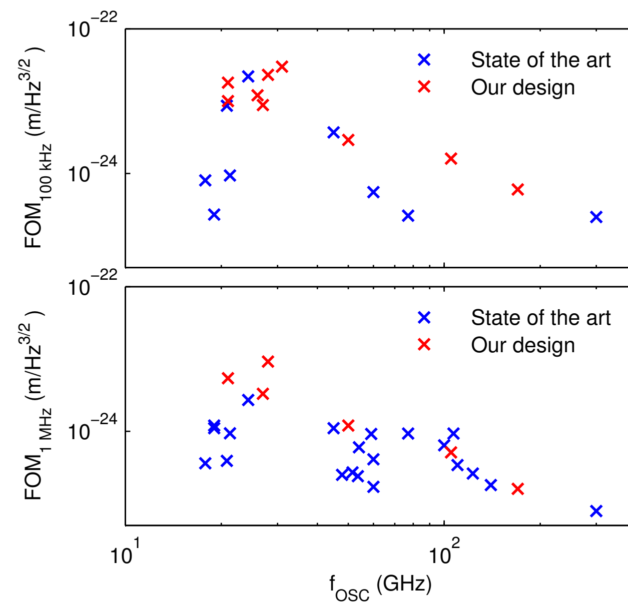

Figure 6.1 – ESR FOM for different published integrated LC oscillators at 100 kHz and 1 MHz offset from the carrier.

Table 6.1 – Comparison of literature and designed oscillators. Notation: f_0 oscillator frequency; d coil external diameter; $PN_{100\,\text{kHz}}$ phase noise at 100 kHz offset; $PN_{1\,\text{MHz}}$ phase noise at 1 MHz offset; $PN_{10\,\text{MHz}}$ phase noise at 10 MHz offset; $FN_{100\,\text{kHz}}$ frequency noise at 100 kHz offset; $FN_{1\,\text{MHz}}$ frequency noise at 1 MHz offset; $FN_{10\,\text{MHz}}$ frequency noise at 10 MHz offset; $\text{FOM}_{100\,\text{kHz}}$ figure of merit at 100 kHz offset; $\text{FOM}_{1\,\text{MHz}}$ figure of merit at 1 MHz offset. [1] simulation results. [2] measured at 2 MHz offset. [3] 3 turns coil. * Voltage controlled oscillator (VCO).

Ref.	Process	f_0 GHz	d μm	$PN_{100\,\text{kHz}}$ dBc/Hz	$PN_{1\,\text{MHz}}$ dBc/Hz	$PN_{10\,\text{MHz}}$ dBc/Hz	$\text{FN}_{100\,\text{kHz}}$ $\text{Hz}/\sqrt{\text{Hz}}$	$\text{FN}_{1\,\text{MHz}}$ $\text{Hz}/\sqrt{\text{Hz}}$	$\text{FN}_{10\,\text{MHz}}$ $\text{Hz}/\sqrt{\text{Hz}}$	$\text{FOM}_{100\,\text{kHz}}$ $\text{m/Hz}^{3/2}$	$\text{FOM}_{1\,\text{MHz}}$ $\text{m/Hz}^{3/2}$
[92]	TSMC65nm	300	40	[1]-45	[1]-75	[1]-100	[1]562	[1]177	[1]100	[1]$2.5\ 10^{-25}$	[1]$7.9\ 10^{-26}$
[97]	UMC90nm	110	53	-	[2]-88.2	-105.2	-	[2]77.8	55	-	[2]$3.4\ 10^{-25}$
		123	41	-	[2]-86.4	-100.2	-	[2]95.7	97.7	-	[2]$2.6\ 10^{-25}$
		140	32	-	[2]-85.1	-93	-	[2]111.2	224	-	[2]$1.8\ 10^{-25}$
[98]	UMC130nm	59	90	-	-89	-108	-	35.5	39.8	-	$9.2\ 10^{-25}$
		100	57	-	-	-103	-	-	70.8	-	-
[120]	IBM32nm	240	30	-	-	-92	-	-	251.2	-	-
		272	30	-	-	-	-	-	-	-	-
[131]	180nm	19	140	-	-110	-	-	3.2	-	-	$1.2\ 10^{-24}$
[133]	65nm	53.6	65	-	-99.4	-	-	10.7	-	-	$2.4\ 10^{-25}$
[134]	STM65nm	54	70	-	-92	-116	-	25.2	15.8	-	$6\ 10^{-25}$
[135]	90nm	60	50	-68	-90.5	-	39.8	29.9	-	$5.5\ 10^{-25}$	$4.1\ 10^{-25}$
[136]	TSMC130nm	47.8	100	-	-105	-	-	5.6	-	-	$2.5\ 10^{-25}$
[132]	TSMC180nm	45	190	-68	-98.9	-110	39.8	11.3	31.6	$3.7\ 10^{-24}$	$1.1\ 10^{-24}$
[138]	180nm	21.3	85	-86	-106	-130	5	5	3.2	$9.4\ 10^{-25}$	$9.4\ 10^{-25}$
[139]	180nm	24.3	160	-62	-100	-120	79.4	10	10	$2.2\ 10^{-23}$	$2.7\ 10^{-24}$
[140]	180nm	19	120	-102	-110	-125	0.8	3.6	5.6	$2.7\ 10^{-25}$	$1.1\ 10^{-24}$
[141]	IBM90nm	60	30	-	-94	-	-	20	-	-	$1.7\ 10^{-25}$
[142]	120nm	51.6	[3]40	-	-85	-	-	56.2	-	-	$2.7\ 10^{-25}$
[143]	90nm	17.8	150	-75	-102	-	17.8	7.9	-	$8\ 10^{-25}$	$3.6\ 10^{-25}$

[144]	STM65nm	100	49	-	-77.6	-104.5	-	131.8	59.5	-	$6.4\ 10^{-25}$
[145]	TI90nm	107	85	-	-78	-101.6	-	125.9	83.2	-	$9.3\ 10^{-25}$
[146]	65nm	77	45	-69.3	-89.3	-105.9	34.2	125.9	83.2	$2.6\ 10^{-25}$	$9.3\ 10^{-25}$
[147]	TSMC90nm	20.8	94	-68	-115	-130	39.8	1.8	3.2	$8.6\ 10^{-24}$	$3.9\ 10^{-25}$
This work	IBM130nm	21	200	-72	-98	-	23	12	-	$1\ 10^{-23}$	$5.4\ 10^{-24}$
This work	STM130nm	26	145	-65	-	-	55	-	-	$1.2\ 10^{-23}$	-
This work	TSMC180nm	27	160	-65	-96	-	55	15	-	$8.8\ 10^{-24}$	$3.3\ 10^{-24}$
This work	TSMC180nm	21	160	-66	-	-	50	-	-	$1.8\ 10^{-23}$	-
This work	STM130nm	31	145	-53	-	-	200	-	-	$3\ 10^{-23}$	-
This work	TSMC40nm	28	180	-60	-88	-	100	40	-	$2.3\ 10^{-23}$	$9.2\ 10^{-24}$
This work	TSMC40nm	50	120	-64	-92	-	60	25	-	$2.9\ 10^{-24}$	$1.2\ 10^{-24}$
This work	TSMC40nm	105	70	-52	-82	-	250	80	-	$1.6\ 10^{-24}$	$5.1\ 10^{-25}$
This work	TSMC40nm	170	45	-43	-76	-	700	150	-	$6\ 10^{-25}$	$1.6\ 10^{-25}$

Finally we experimentally obtained a spin sensitivity of about 10^7 spins/$\sqrt{\text{Hz}}$ at room temperature and 10^6 spins/$\sqrt{\text{Hz}}$ at 4 K with BDPA and DPPH samples. The expected spin sensitivity for the 170 GHz device at room temperature is about 10^6 spins/$\sqrt{\text{Hz}}$. At 4 K a spin sensitivity of about 10^4 spins/$\sqrt{\text{Hz}}$ is expected with the 50 GHz device. This sensitivity extrapolation, not yet experimentally confirmed are obtained in the assumption of constant relaxation time. The sensitive volumes for the realized chips range from the 250 pl of the 21 GHz device to the 10 pl of the 170 GHz one.

The results presented in chapter 2 and 5 are unpublished. The main results reported in chapter 3 and 4 have been published in Ref. [155] and Ref. [228] respectively.

6.3 Outlook

The observed phenomena at cryogenic temperature might have a significant impact as additional tool for the investigation of present and future technology. Measurements at variable temperature and magnetic field might better clarify what are the origins of the observed phenomena and identify the defects responsible of the observed frequency jumps.

Furthermore the cooling at temperature below 1 K of the 105 and 170 GHz oscillators might allow to investigate the behaviour of the oscillator in the condition $kT < \hbar\omega_{LC}$. This condition combined with the dependence of the MOSFET gate-source capacitance on the oscillation amplitude, which introduces an anharmonicity in the oscillator behaviour, might allow to observe a non-trivial quantum behaviour of the LC-oscillator.

Concerning the ESR spectroscopy, solutions for overcoming the problem of the too strong magnetic field arising from the integrated oscillator has to be investigated. One possible solution might be the use of non steady state technique, such as rapid passage of the magnetic field or of the oscillator frequency.

The chip capability of locally convert DC power into a non radiating microwave magnetic field might be interesting as a local, inexpensive source of microwaves for dynamic nuclear polarization (DNP) experiments.

A Details of the integrated detectors

In this appendix, details of the integrated detector will be presented. The transistor level schematics will be shown for the "K2 chip" that has been used in the experiment presented in chapter 3,4. All the other detectors use similar geometry, making transistor level schematic for all of them redundant. The performances of the detectors are finally summarized in table A1.

A.1 K2 chip

Figure A.1 shows photo, layout and the block diagram of the realized chip. The chip is designed with an IBM 130 nm bulk CMOS process (IBM 8RF). It essentially consists of two LC-oscillators

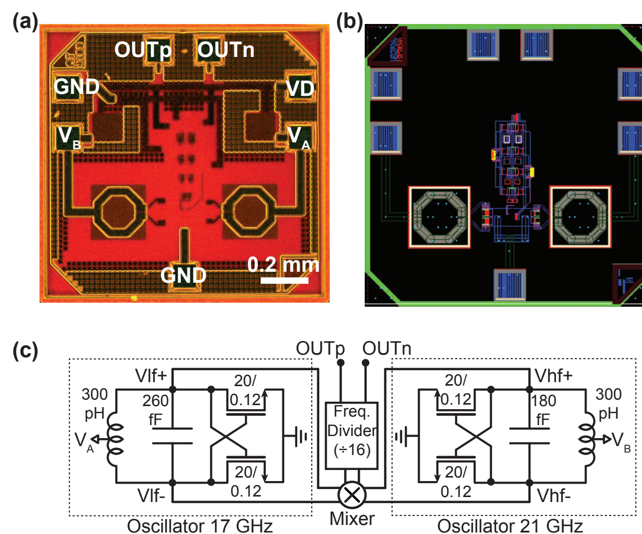

Figure A.1 – (a) Optical microscope image, (b) layout and (c) block diagram of the single-chip electron spin resonance detector. V_A and V_B: DC power supply of the two oscillators (0.5 to 3.5 V). VD: DC power supply for the mixer and frequency-division module (1.5 V). OUTp and OUTn: differential output signal ($\approx$ 220MHz).The transistor dimensions width/length are in micrometers.

operating at 20.6 GHz and 17.1 GHz, respectively. The excitation/detection octagonal coils have a diameter of 200 μm, a track width of 30 μm and an inductance of 300 pH,. The microwave magnetic field B_1 can be varied from 0.1 to 0.7 mT by changing the oscillator supply voltage from 0.5 to 3.5 V. On the same chip, a mixer and a frequency division stage are also integrated. By mixing the two oscillator output voltages a signal at about 3.5 GHz is obtained, which is subsequently divided by 16, resulting in a chip output signal at about 220 MHz. Detail regarding the connections are inserted in the capture of figure A.1. Figure A.2 shows the schematics and block diagrams of the mixer and frequency divider. The frequency mixer needed for down-conversion of the oscillation frequency is based on a double-balanced Gilbert cell topology (see pages 368 to 370 of Ref. [127]). By mixing the two oscillator output voltages a signal at about 4 GHz is obtained. The sum frequency component is filtered out by the system parasitic (i.e., a low pass filter is not necessary). The frequency divider is realized by means of current model logic (CML) D-latches with resistive load (see pages 683 to 699 of Ref.[127]). The main advantage of the topology is that doesn't require a rail to rail input for being operative but, since the locking range of the topology is limited due to the internal latch, a careful design has to be carried out. The on chip divide ratio is 16, by a cascade of four identical divide-by-two frequency dividers. The output buffer, realized as standard source follower amplifier, is capable of driving an output load of 5 pF with a voltage swing of 0.2 V at 200 MHz. The main detail and chip characteristic are summerized in table A1.

A.2 K3 chip

Figure A.3 shows photo, layout and the block diagram of the realized chip. The chip is designed with an STM 130 nm bulk CMOS process (STM HCMOS9). It essentially consists of two LC-oscillators operating at 26 GHz and 22 GHz, respectively. The excitation/detection octagonal coils have a diameter of 145 μm ,a track width of 13 μm and an inductance of 260 pH. On the same chip, a mixer and a frequency division stage are also integrated. By mixing the two oscillator output voltages a signal at about 4 GHz is obtained, which is subsequently divided by 16, resulting in a chip output signal at about 250 MHz. Details regarding the connections are inserted in the capture of figure A.3. Two test oscillators are present in the chip with the purpose of testing the technology limit. One oscillator, that share the coil with the previously described system is operative at its self oscillating frequency (the capacitance necessary from the resonance is arising from parasitic) and a second system designed for evaluating operation close to the technology limit. The main detail and chip characteristic are summerized in table A1.

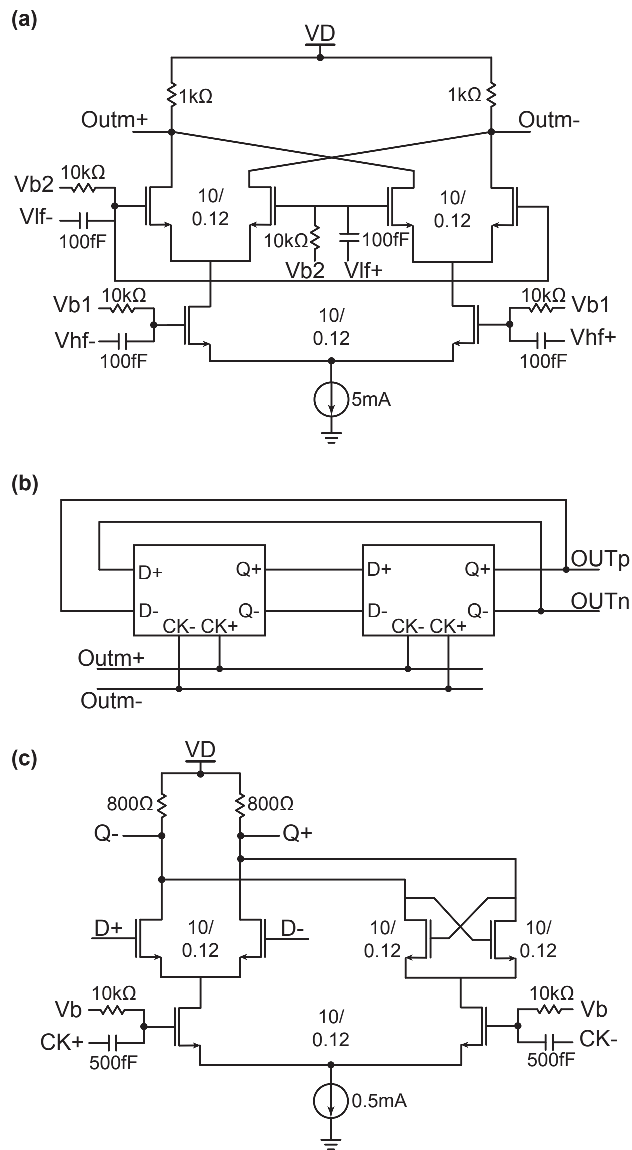

Figure A.2 – Transistor level schematic of the integrated detector: (a) Schematics of the frequency mixer ($V_{b1} \approx 0.9$ V, $V_{b1} \approx 0.6$ V). (b) Block diagram of the frequency divider based on D-latches. (c) Schematics of the D-latch ($V_b \approx 0.6$ V).

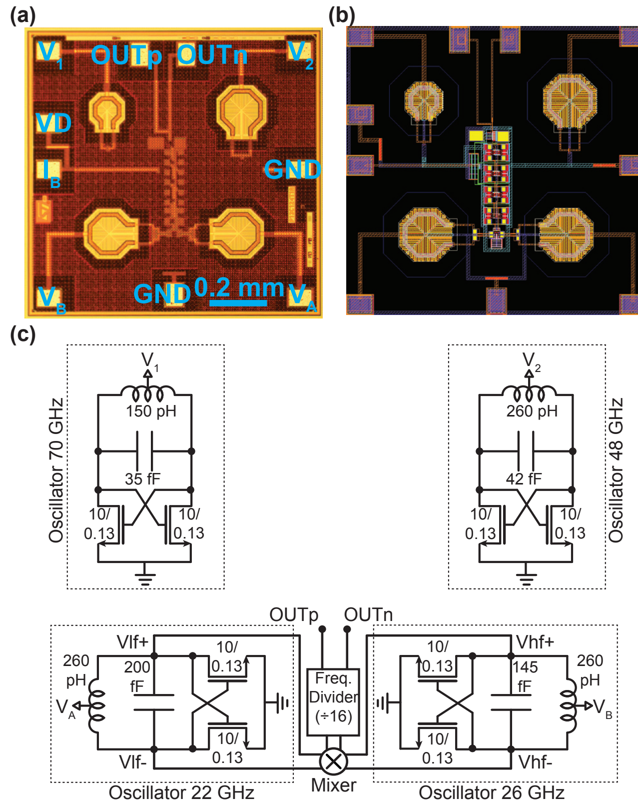

Figure A.3 – (a) Optical microscope image, (b) layout and (c) block diagram of the single-chip electron spin resonance detector. V_A and V_B: DC power supply of the two oscillators (0.5 to 3.5 V). VD: DC power supply for the mixer and frequency-division module (1.5 V). I_B: DC power supply for the mixer and frequency-division module (100 μA). OUTp and OUTn: differential output signal ($\approx$ 300MHz). V_1, V_2 test oscillator bias (0.5, 3.5V). The transistor dimensions width/length are in micrometers.

A.3 K4 chip

Figure A.4 shows photo, layout and the block diagram of the realized chip. Two systems are integrated on the same chip using a TSMC 180nm technology. The first essentially consists of two LC-oscillators operating at 27 GHz and 25 GHz, respectively. The excitation/detection octagonal coils have a diameter of 160 μm ,a track width of 30 μm and an inductance of 200 pH. On the same chip, a mixer and a frequency division stage are also integrated. By mixing the two oscillator output voltages a signal at about 2 GHz is obtained, which is subsequently divided by 4, resulting in a chip output signal at about 500 MHz. The second essentially consists of two voltage controlled LC-oscillators with center frequency of about 21 GHz and 19 GHz, respectively. The excitation/detection octagonal coils have the same size of the previously described system. On the same chip, a mixer and a frequency division stage are also integrated. By mixing the two oscillator output voltages a signal at about 2 GHz is obtained, which is subsequently divided by 4, resulting in a chip output signal at about 500 MHz. Two

additional cross-coupled system are added for further studies and tests. Details regarding the connections are inserted in the capture of figure A.4. The main detail and chip characteristic are summerized in table A1.

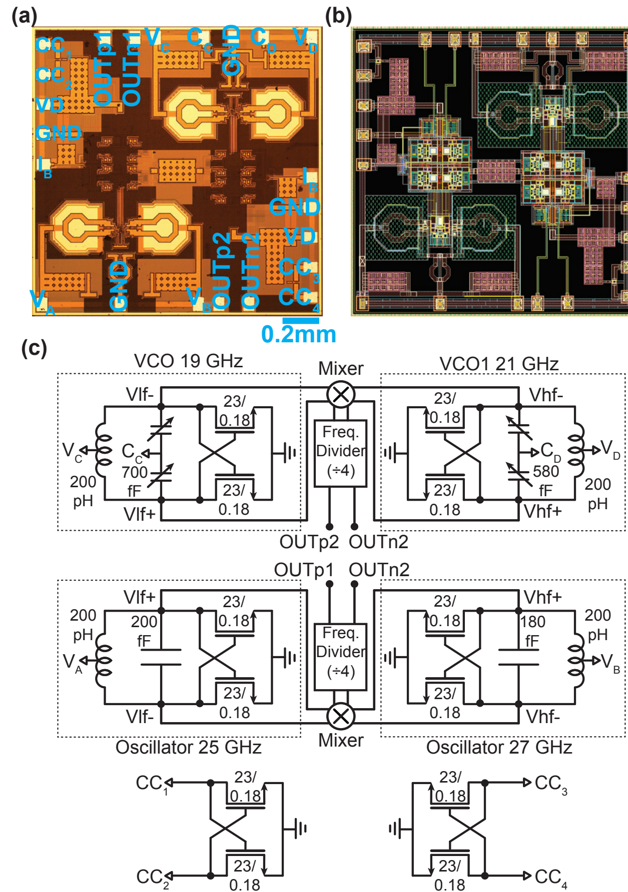

Figure A.4 – (a) Optical microscope image, (b) layout and (c) block diagram of the single-chip electron spin resonance detector. V_A and V_B: DC power supply of the two oscillators (0.5 to 3.5 V). V_C and V_D: DC power supply of the two voltage controlled oscillator (0.5 to 3.5 V).C_C and C_D: control voltage of the controlled oscillator (0.5 to 3.5 V). VD: DC power supply for the mixer and frequency-division module (1.8 V). I_B: DC power supply for the mixer and frequency-division module (100 μA). OUTp1, OUTp2, OUTn1 and OUTn2: differential output signal (≈ 300MHz). CC_1, CC_2, CC_3, CC_4 test cross-couple bias (0, 3.5V). The transistor dimensions width/length are in micrometers.

A.4 ENDOR chip

Figure A.5 shows photo, layout and the block diagram of the realized chip. Two systems are integrated on the same chip using a TSMC 180nm technology. They both essentially consists of two LC-oscillators operating at 27 GHz and 26 GHz, respectively. The excitation/detection octagonal coils have a diameter of 160 μm ,a track width of 30 μm and an inductance of

200 pH. On the same chip, a mixer is also integrated. By mixing the two oscillator output voltages a signal at about 1 GHz is obtained. On one of the two systems an integrated double turn inductance is added with the purpose of being used for NMR excitation in an ENDOR experiment. The coil is 350 μm wide and 800μm long and can generate a magnetic field of 72 G/A. The maximum current is 0.2 A. Details regarding the connections are inserted in the capture of figure A.5. The main detail and chip characteristic are summerized in table A.1.

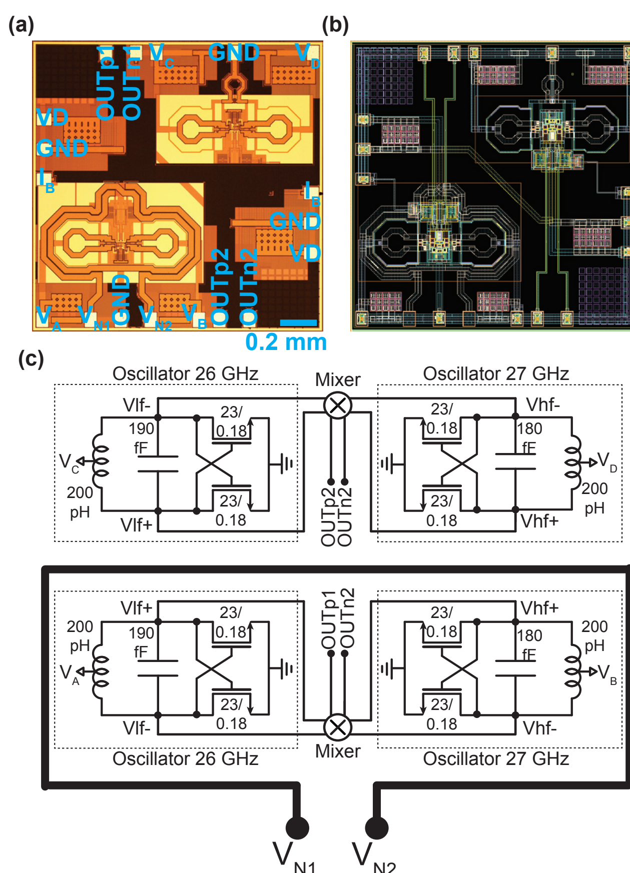

Figure A.5 – (a) Optical microscope image, (b) layout and (c) block diagram of the single-chip electron spin resonance detector. V_A, V_B, V_C and V_D: DC power supply of the two oscillators (0.5 to 3.5 V).V_{N1}, V_{N2}: NMR coil termination. VD: DC power supply for the mixer (1.8 V). I_B: DC power supply for the mixer and frequency-division module (100 μA). OUTp1, OUTp2, OUTn1 and OUTn2: differential output signal ($\approx$ 1 GHz). The transistor dimensions width/length are in micrometers.

A.5 DNP chip 1

Figure A.6 shows photo, layout and the block diagram of the realized chip. The chip is designed with an STM 130 nm bulk CMOS process (STM HCMOS9). It essentially consists of two LC-oscillators operating at 31 GHz and 30 GHz, respectively. The excitation/detection octagonal

coils have a diameter of 145 μm ,a track width of 13 μm and an inductance of 260 pH. On the same chip, a mixer and a frequency division stage are also integrated. By mixing the two oscillator output voltages a signal at about 1 GHz is obtained, which is subsequently divided by 4, resulting in a chip output signal at about 250 MHz. Details regarding the connections are inserted in the capture of figure A.6. Four injection locked oscillators analogous to the one presented in the "K3 Chip" are also designed. The injection locking is assured by means of capacitive connection between the oscillators. Additionally a two turns coil intended to be used for NMR excitation it's also present. Details regarding the connections are inserted in the capture of figure A.6. The main detail and chip characteristic are summerized in table A1.

A.6 DNP chip 2

Figure A.7 shows photo, layout and the block diagram of the realized chip. Two systems are integrated on the same chip using a TSMC 180nm technology. The first essentially consists of two LC-oscillators operating at 27 GHz and 26 GHz, respectively. The excitation/detection octagonal coils have a diameter of 160 μm ,a track width of 30 μm and an inductance of 200 pH. On the same chip, a mixer is also integrated. By mixing the two oscillator output voltages a signal at about 1 GHz is obtained. The second essentially consists of two voltage controlled LC-oscillators with center frequency of about 21 GHz and 20 GHz, respectively. The excitation/detection octagonal coils have the same size of the previously described system. On the same chip, a mixer and a frequency division stage are also integrated. By mixing the two oscillator output voltages a signal at about 1 GHz is obtained. Two additional transistors are added for further studies and tests. Details regarding the connections are inserted in the capture of figure A.7. The main detail and chip characteristic are summarized in table A1.

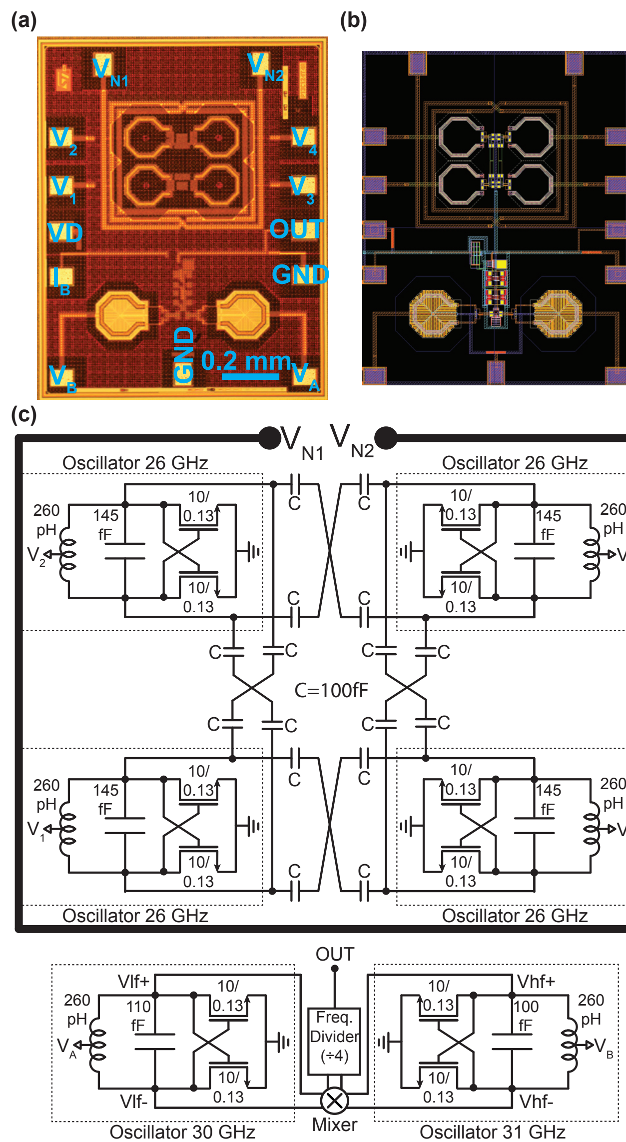

Figure A.6 – (a) Optical microscope image, (b) layout and (c) block diagram of the single-chip electron spin resonance detector. V_A and V_B: DC power supply of the two oscillators (0.5 to 3.5 V). VD: DC power supply for the mixer and frequency-division module (1.8 V). I_B: DC power supply for the mixer and frequency-division module (100 μA). OUTp and OUTn: differential output signal ($\approx$ 250MHz). $V_{1,2,3,4}$: DC power supply of the injection locked oscillators (0.5 to 3.5 V). V_{N1}, V_{N2}: NMR coil termination. The transistor dimensions width/length are in micrometers.

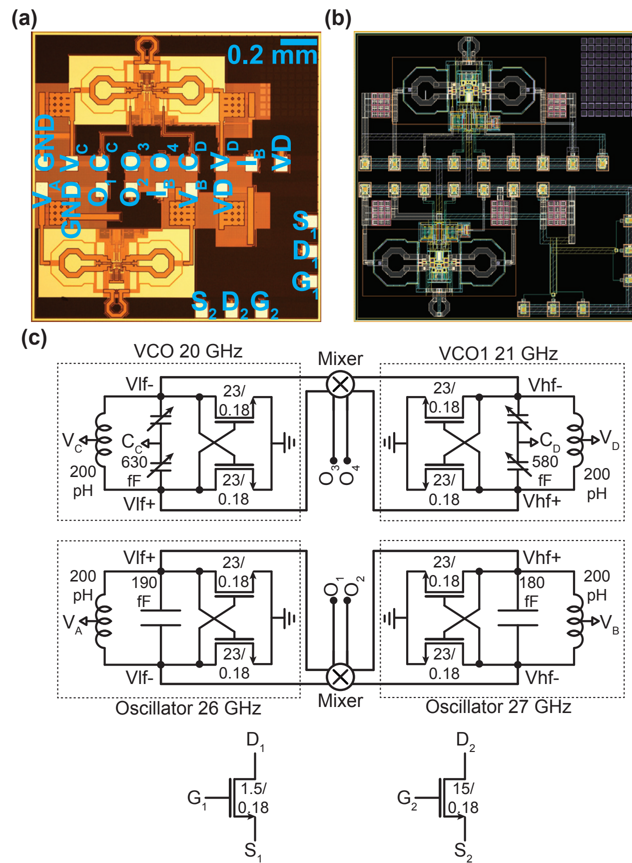

Figure A.7 – (a) Optical microscope image, (b) layout and (c) block diagram of the single-chip electron spin resonance detector. V_A and V_B: DC power supply of the two oscillators (0.5 to 3.5 V). V_C and V_D: DC power supply of the two voltage controlled oscillator (0.5 to 3.5 V).C_C and C_D: control voltage of the controlled oscillator (0.5 to 3.5 V). VD: DC power supply for the mixer and frequency-division module (1.8 V). I_B: DC power supply for the mixer and frequency-division module (100 μA). O_1, O_2, O_3 and O_4: differential output signal ($\approx$ 1 GHz). $D_{1,2}$, $G_{1,2}$, $S_{1,2}$, CC_4: drain, gate and source of test structure (0, 3.5V). The transistor dimensions width/length are in micrometers.

A.7 Summary table

Table A.1 – Summary of performance of the integrated single chip detectors: f_0 oscillator frequency; d_{coil} coil external diameter; w_{coil} coil width; t_{coil} coil thickness; $FN_{@100kHz}$ frequency noise at 100 kHz offset

Chip	f_0 (GHz)	d_{coil} (μm)	w_{coil} (μm)	t_{coil} (μm)	$FN_{@100kHz}$ Hz/$\sqrt{\text{Hz}}$
K2	20	200	30	7.5	24
K3	26	145	13	2.2	55
K4/ENDOR/DNP2	27	160	30	2.8	40
K4VCO/ENDORVCO	21	160	30	2.8	50
DNP1	31	145	13	2.2	200
HF	28	180	15	3.1	100
HF	28	190	15	3.1	-
HF	50	120	15	3.1	60
HF	105	70	10	3.1	250
HF	170	45	5	3.1	700

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