Architecture and Characterization of a Calibrator for PMUs Operating in Power Distribution Systems

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***Abstract*—In recent years, the Phasor Measurement Unit (PMU) technology is rapidly evolving towards the potential deployment also in power distribution systems (DSs). In general, this specific field of applications requires PMUs whose accuracy levels are beyond those required by the IEEE Std. C37.118. Additionally, there is the need to define the architecture of an associated calibration system capable to assess the metrological performances of these devices. In this paper, we first analyse the impact of the uncertainties (in term of phase and magnitude) introduced by arbitrary PMUs on a state estimation (SE) process performed on the IEEE 13-bus distribution test feeder. The outcomes of this analysis are used to infer the most stringent steady-state performances of PMUs for DSs monitoring and, consequently, to define the requirements and the hardware architecture of a PMU calibrator presently developed at the Author's laboratories. A preliminary metrological characterization of the proposed calibrator is presented in the paper.**

***Index Terms*—Calibration, distribution systems, Phasor Measurement Unit (PMU), IEEE Std. C37.118.**

I. Introduction

The Phasor Measurement Unit (PMU) technology represents one of the backbone systems enabling the quasi real-time monitoring of transmission networks (TNs). In recent years, PMU devices are also being extended to distribution systems (DSs). In particular, this technology might represent a solution for the monitoring of DSs characterized by a large presence of distributed generation units (DGs). In this respect, the applications that might take advantage of the PMU technology in DSs are: power flow monitoring, state estimators, protection, as well as control systems (e.g., [1]–[5]). As known, the reference that defines the performances of PMUs is the IEEE Standard for Synchrophasor Measurements for Power Systems C37.118.1-2011 [6] and its recent amendment [7]. The compliance of a PMU is expressed in terms of: Total Vector Error (TVE), Frequency Error (FE), and Rate-Of-Change-Of-Frequency (ROCOF) Error (RFE). The TVE is the main parameter that quantifies the PMU performances and takes into account both magnitude and phase error [1]. The IEEE standard defines PMU performances both for steady-state and dynamic operating conditions. Focusing on steady-state operating conditions, the mentioned IEEE standard limits the TVE to 1%, which corresponds to either a maximum phase error of 0.57 deg (with no magnitude error) or a magnitude error of 1% (with no phase error). The compliance with [6], [7] is quantified by comparing the PMU under test with a reference system (i.e., the PMU calibrator) that has a level of accuracy, at least, one order of magnitude higher. In this respect, the most advanced reference systems have, for steady-state compliance, a TVE of 0.05 [8], [9]. Nevertheless, the performances defines by [6], [7] are mainly suitable to TN applications. In fact, an uncertainty of 0.57 deg for the phase error appears inappropriate for the use of PMUs in DSs (e.g., [10]). Indeed, in general, the nodal voltage phasors of DSs are separated by angles that are comparable with the limit of the phase uncertainty imposed by [6], [7]. Therefore, for the extension of PMUs in DSs, a higher accuracy of these devices is, in general, required. Consequently, the metrological assessment of PMUs for DS applications becomes a technical challenge for the National Metrology Institutes (NMIs). For this reason, the Swiss Federal Institute of Metrology (METAS) and the Distributed Electrical Systems laboratory of the École Polytechnique Fédérale de Lausanne (DESL-EPFL) are developing a PMU calibrator able to face this technological challenge. The main contents of this paper are: (i) the analysis of the accuracy requirements of PMUs for DS steady-state applications; (ii) the definition of the hardware architecture of a high accurate PMU calibrator; (iii) the metrological characterization and the performance assessment of the proposed PMU calibrator. In Section II, we discuss the influence of the uncertainties, in terms of phase and magnitude, introduced by PMUs with a given TVE on the state estimation (SE) accuracy performed on a benchmark distribution system. This analysis is used to infer the steady-state PMU accuracy requirements for DS applications and, consequently, the ones of their calibrator. In Section III, we analyze the influence of phase and magnitude error on the TVE assessment and we illustrate the hardware architecture of a novel PMU calibration system. In Section IV, we illustrate the preliminary characterizations of the hardware components and the on-line assessment of the magnitude error of the system. In the final Section V, we discus the preliminary

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[1]It is worth reminding that the PMU phase error is a combination of the time-synchronization error and the accuracy of the synchrophasor estimation process implemented in the device.

results and the future steps of this research.

II. PMU Accuracy Requirements with Respect to the State Estimation of Distribution Systems

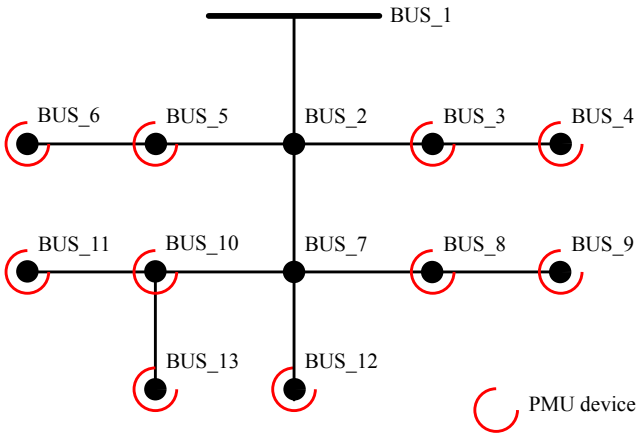

Fig. 1. The simulated IEEE 13-bus distribution test feeder with the assumed PMU locations.

In order to define the accuracy requirements of PMUs for steady-state DS applications, and the consequent ones of the associated calibration system, we here make reference to a steady-state functionality that might be fed by PMU data, namely the SE. In this section, we report a SE study made on the IEEE 13-bus distribution test feeder [11][2] using the discrete Kalman filter state estimation (DKF-SE) process described in [12]. It was assumed that nodal phasors (voltages and currents) were measured by PMUs having known TVEs. The PMUs locations are given in Fig. 1 and they have been chosen by means of an a-posteriori analysis to achieve a good SE accuracy both for estimated voltages and current phasors. The procedure adopted to perform the SE is the following:

1) For each time-step, a load flow is computed in order to determine the true quantities X^T (nodal voltages and nodal currents) of the network;
2) The simulated PMU measurements (X^M) are created by perturbing the real and the imaginary part of the X^T inferred from step 1) with a randomly-generated Gaussian noise (N) characterized by a null mean value (μ) and a standard deviation (σ) equal to 1/3 of the maximum error of the PMU measurements ε. As the DKF-SE is formulated in rectangular coordinates, ε is assumed to be the same for the real and the imaginary part ($\varepsilon_r = \varepsilon_i = \varepsilon$) and is relative to the amplitude of the X^T inferred in the step 1). Therefore, the X^M are derived from the X^T as:

$$X^M = X^T + N(0, \varepsilon/3) \quad (1)$$

For a given TVE the maximum error corresponds to ε=TVE/$\sqrt{2}$.
3) The state of the system is calculated using the X^M.
4) The SE errors are assessed by comparing the estimated quantities of step 3) with the X^T coming from step 1).

We can estimate the impact of the TVE on the SE accuracy by observing the estimation errors at the buses not equipped with PMUs, namely buses 2 and 7. It is worth mentioning that unlike similar works [13], [14], we did not use any pseudo-measurement or other measurement devices in the nodes not observed by PMUs.

Due to the particular features of DSs, and to the fact that the selected SE process uses nodal voltages as state variables, the quantities most affected by the PMU uncertainty are the nodal current phasors. Table I shows the influence of the PMU uncertainty, expressed in terms of TVE, on the accuracy of the voltage and current magnitude/phase estimations at bus 7. Indeed this node exhibits the worst estimation accuracy. The values shown in Table I are the means of the absolute errors with respect to a simulation of 5000 estimations. It can be seen that PMUs characterized by a TVE = 1% are inadequate to achieve sufficient SE accuracy. In particular, the error of the estimated currents is 25% for the magnitude (ΔI-m) and 1367 mrad for the phase (ΔI-φ). In order to achieve a maximum error on the estimated currents of less than 10% for the magnitude and 100 mrad for the phase, the TVE needs to be in the order of 0.3%. This brief assessment enables us to estimate the accuracy levels required for PMUs to be used in a DS context for SE analysis. Consequently, an associated PMU calibrator has to be characterized by accuracy levels that are at least, 10 times better than TVE = 0.3% (0.3% for the magnitude and 3 mrad for the phase assuming no magnitude error). The value of TVE = 0.03% is the one adopted as a reference for the design of the PMU calibrator described in what follows. It is also worth mentioning that PMU requirements are application-driven. Compared to other applications (e.g. power-flow monitoring [15]), the SE is, in general, more demanding in term of steady-state accuracy. The specific SE analysis we performed enable us to infer the most stringent steady-state accuracy requirements for PMU operating in DSs.

TABLE I
Mean values of the absolute errors of the nodal voltage and nodal current magnitude/phase estimations at bus 7, as a function of the PMU accuracy expressed in terms of TVE %.

TVE (%)	ΔV_M **(%)**	ΔV_φ **(mrad)**	ΔI_M **(%)**	ΔI_φ **(mrad)**
1	0.0015	0.025	25	1367
0.5	0.0006	0.014	24	177
0.3	0.0004	0.012	9	70

[2] Details about the grid parameters and the load profiles are given in our previous work [12].

III. Design Principles and Hardware Architecture of the PMU Calibrator

A. Design principles

The calibration is based on generating stable reference waveforms for a PMU under test [16]. The PMU calibrator is made of a forward path (waveform generation), a return path, used for the measurement of the references supplied to the PMU under test and a Coordinated Universal Time (UTC) aligned master clock. The overall accuracy of the PMU calibrator lies in the ability of the return path to recapture with a higher degree of fidelity, with respect to the forward path, the reference waveforms applied to the PMU under test. These signals, once resampled, are processed so that they can directly be compared with the data reported by the PMU under test. To achieve this, the forward and the return path should introduce a low magnitude and phase error stable over time. The phase error (Δ_φ) is influenced both by timing and synchronization uncertainties. The former is caused by the misalignment of the master clock with UTC while the latter is introduced by the various phase shift and delays in the hardware components of the PMU calibrator. The magnitude error (Δ_M) drift is primarily caused by the resistors values of the hardware components that change over time and with temperature. Each part of the hardware must be metrological characterized to ensure that the calibrator meets the required performances. The characterization encompasses the assessment of timing uncertainty, synchronization uncertainty and magnitude uncertainty. Combined, they permit to infer the required TVE error for the calibrator. Figure 2 shows the dependence of Δ_φ on the TVE for different values of Δ_M. Until Δ_φ is below 100 μrad, its influence on the TVE is marginal compared to Δ_M. While the timing uncertainty and synchronization uncertainty can be characterized at the time of design, the magnitude error can be compensated with a-posteriori assessment. The minimization of phase and magnitude error permits to obtain the required TVE error for the calibrator.

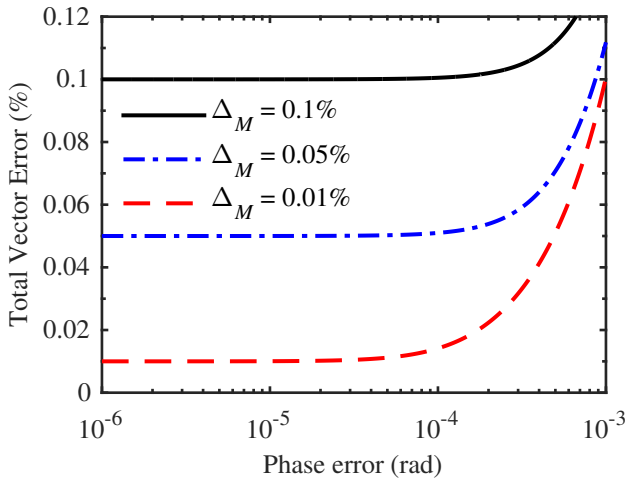

Fig. 2. Dependence of the combined timing and phase error (Δ_φ) on the TVE for different values of magnitude error (Δ_M). The phase error combines timing and synchronization uncertainties.

B. Hardware architecture

The hardware architecture of the PMU calibrator is shown in Fig. 3. It is made up of four main elements: (i) a master reference clock (clock in Fig. 3); (ii) a time synchronization board (time sync. in Fig. 3) used to time align the different hardware modules; (iii) digital-to-analogic converters (DACs in Fig. 3) to generate the signal reference waveforms; (iv) analog-to-digital converters (ADCs in Fig. 3) to re-acquire and analyze the reference waveforms. The core of the system is a National Instruments (NI) PXI (PCI eXtensions for instrumentation) 1042Q chassis in which the following modules are plugged: a NI PXI-8110 high-performance Intel Core 2 Quad Q9100-based embedded controller, a NI PXI-6682 timing and synchronization module, and a NI PXI-6289 high accuracy data acquisition board (DAQ).

The master reference clock of the proposed PMU calibrator is represented by the UTC-CH (official time in Switzerland) generated in the METAS laboratories. The PXI-6682 receives the pulse-per-second (PPS) signals of the UTC-CH and disciplines a 10 MHz clock that is distributed on the PXI backplane. All the modules connected to the PXI chassis are then synchronized with the UTC-PPS by mean of the clock generated by the PXI-6682. The PXI-6289 generates signal reference waveforms with a sampling rate of 500 kSa/s. As PMUs are characterized by maximum sampling frequencies of few tens of kHz, this sampling rate permits to limit the harmonic distortion of the reference waveforms and to avoid aliasing problems. The DACs on the PXI-6289 have a 16-bits resolution and an amplitude accuracy, declared by the manufacturer, of 1540 µV (on the ±10 V range). The reference waveforms are then applied to the PMU under test and are simultaneously re-acquired by the ADCs of the PXI-6289. The ADCs of the PXI-6289 have an 18-bits resolution and an amplitude accuracy, declared by the manufacturer, of 980 µV (±10 V range). At the moment, the references waveforms generate by the PMU calibrator are voltage signals in the range

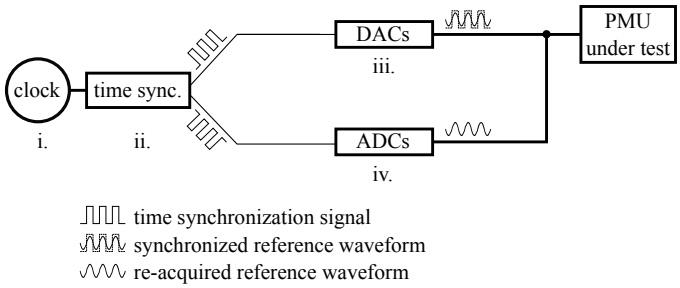

Fig. 3. Architecture of the proposed PMU calibrator hardware. The DACs and the ADCs are synchronized to the UTC-CH (clock) through the time synchronization board (time synch.).

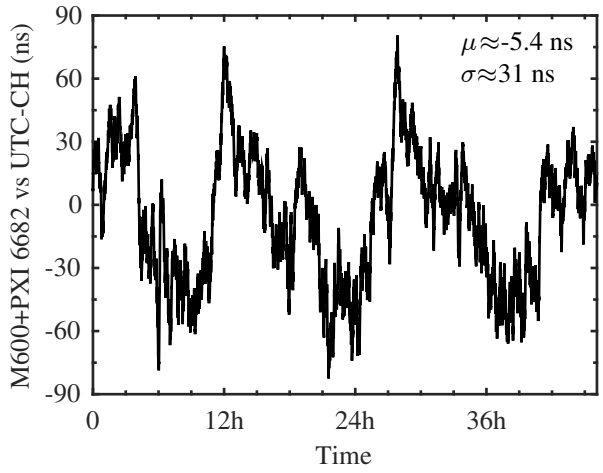

Fig. 4. Combined uncertainty of two arbitrary GPS-receivers: Meinberg LANTIME M600 (M600) and PXI-6682.

of ±10 V[3].

IV. Characterization of the Hardware Components

As already mentioned, the PMU calibrator is made of a forward path (waveform generation), a return path used for the measurement of the reference waveform supplied to the PMU under test and, in general, a UTC aligned master clock. The most advanced PMU calibrators nowadays available are time aligned to UTC via the PPS signals of the Global Position System (GPS). As a consequence, when a PMU is being characterized with a calibrator, two GPS-receivers are actually used: one on the PMU calibrator and one on the PMU itself. Even though, the two GPS-receivers are physically very close and they receive the same GPS signal, they are not synchronized between each other. The relative uncertainties of the two GPS-receivers could add up together distorting the reliability of the calibration. Figure 4 shows an example of the combined uncertainty of two arbitrary GPS-receivers (Meinberg LANTIME M600 and a PXI-6682) with respect to UTC-CH generated by METAS. The combined uncertainty of the two GPS-receivers follows a normal distribution characterized by μ≈-5 ns and σ≈30 ns. Therefore, the total timing uncertainty caused by the two GPS-receivers corresponds to circa 30 rad (±3σ). A better phase accuracy can be achieved substituting the GPS-receiver of the PMU calibrator with a more accurate master clock.

A. Timing uncertainty

In order to limit the timing uncertainty and consequently the phase error of the calibrator, we use as master clock directly the UTC-CH generated at METAS. In this section, we compare

[3]It is worth observing that the majority of modern sensors installed in DSs are characterized by low-voltage outputs (typically in the ±10 V range). Therefore, for these applications there is no need to further amplify the calibrator signals.

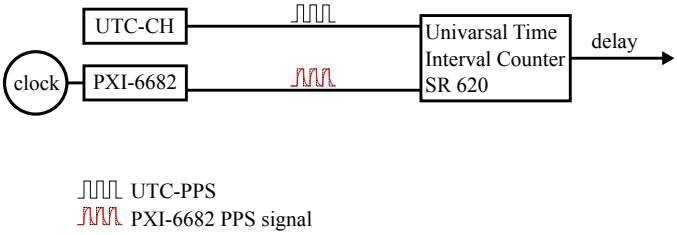

Fig. 5. Sketch of the system used to characterise the timing uncertainty of the time synchronization of the PMU calibrator. Two master clock (clock) are compared, GPS signal and UTC-CH.

the common approach where the master clock is represented by the GPS signal with the solution we adopt that implements as a master clock the UTC-CH.

In both cases, the PXI-6682 is disciplined by the master clock and generates a PPS signal. The PPS signal, routed out from the PXI-6682, is then compared against the PPS signal of the UTC-CH (UTC-PPS) through a Universal Time Interval Counter SR620 (Fig. 5). As shown in Fig. 6, the short-term accuracy of the PXI-6682 output referred to UTC-CH follows a normal distribution. When the PXI-6682 is disciplined using as a master clock the GPS signal, the short-term accuracy of the PXI-6682 is about 26 ns. Instead, when the PXI-6682 is directly disciplined by UTC-CH signal, the short-term accuracy that actively contributes to the TVE of the PMU calibrator improves of circa 100 times. The timing uncertainty introduced by the PXI-6682 when disciplined through the UTC-CH has been estimated to circa ±81 ps (this number refers to the ±3σ of the distribution shown in Fig. 6). For a 50 Hz reference signal, this uncertainty corresponds to 25 nrad.

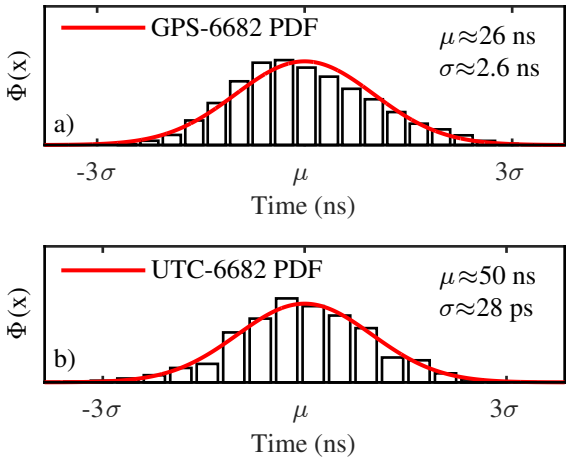

Fig. 6. Probability density function of the timing uncertainty of the PXI-6682 disciplined by GPS (a) and UTC (b). The PPS signal, routed out from the PXI-6682, is compared against the PPS signal of the UTC-CH.

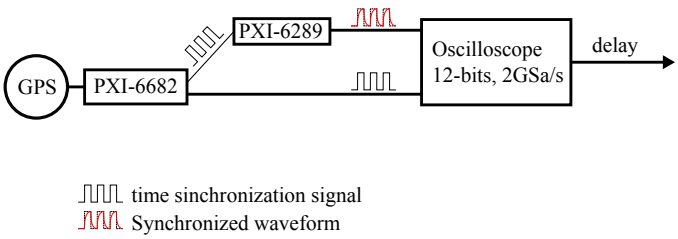

Fig. 7. Sketch of the characterization of the PXI-6289 DACs. The master reference clock is the GPS-PPS signal.

B. Synchronization uncertainty

An inaccurate synchronization of the hardware components is translated into a phase error in the reference waveforms. In order to quantify the total phase error of the system, we have characterized the DACs. In this section, we report the jitter measurements of the DACs. A sketch of the characterization method is shown in Fig. 7. Using the GPS-PPS as a master clock, we have routed out from the PXI-6682 a clock frequency of 100 kHz. Then, we have generated with the PXI-6289 a square waveform of frequency 100 kHz. The sampling rate of the PXI-6289 has been set to 1 MSa/s. Thus, we have acquired 2000 periods of the two waveforms using a high-resolution oscilloscope LeCroy Hro G4Zi (12-bits, 2 GSa/s, clock accuracy of 1.5 ppm and trigger jitter 6 ps). Figure 8 shows an example of the two acquired waveforms. As it can be observed, the output waveform of the PXI-6289 (dashed red line in Fig. Fig. 8) is smoothed due to the effect of low-pass filters on the PXI module.

The delay between the PXI-6682 and the PXI-6289 is defined as the time difference between the values reached by the two signals in correspondence of 50% the maximum amplitude. The delay between PXI-6682 and PXI-6289 follows a normal distribution characterized by $\mu \approx 221$ ns and $\sigma \approx 0.16$ ns. The PXI-6289 has a systematic delay of 221 ns, which can be easily compensated, and a random error of 0.2 ns that actively contributes to the TVE of the PMU calibrator. It is worth observing that the oscilloscope used to quantify the delay has a vertical accuracy of 0.5% referred to the full scale (±5 V in our case). In order to assess the consistency of the method, we have inferred the distribution of the delay for the different magnitude thresholds of 0.1%, 0.2% and 0.5%. The systematic delay varies accordingly whereas, considering the errors introduced by the oscilloscope, the random error is constant. The synchronization uncertainty introduced by the PXI-6289 can be estimated in $\pm 3\sigma$, circa±0.6 ns (0.2 μrad). The same results have been confirmed using the method reported in Section IV-A. The output of the PXI-6289 was compared with the PXI-6682 though the Universal Time Interval Counter SR620. The master clock was the GPS signal, the sampling rate was set to 500 kSa/s (nominal sampling rate of the calibrator) and the signal frequency was 50 Hz.

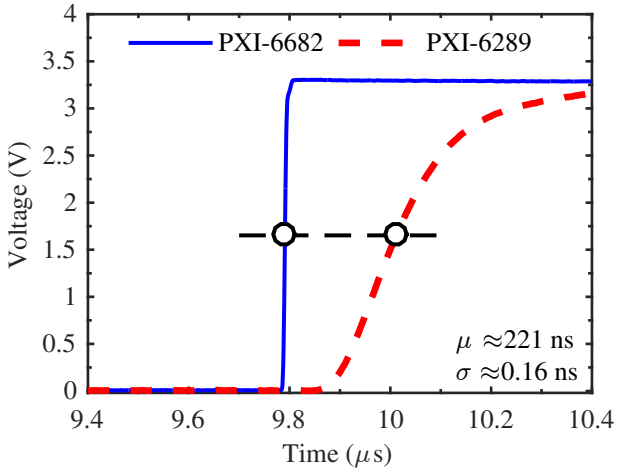

Fig. 8. Delay between the PXI-6682 and the PXI-6289 board can be quantified in the order of 221 ±0.6 ns.

C. Magnitude uncertainty

While the phase error can be characterized at the time of design, the magnitude accuracy is difficult to maintain over time and over a given temperature range with an accuracy of about 100 ppm. The magnitude accuracy drift is primarily caused by the ADCs that tend to be sensitive to the temperature. To circumvent this problem, the calibrator is recalibrated between measurements. This is achieved with the usage of a high precision digital voltmeter HP 3458A. This multimeter has a DC accuracy of up to 8.5 digits and is based on an integrating ADC. However, precision AC measurement can also be made in the DC mode [17]. This instrument is also characterized with very good 90 days stability and a low temperature coefficient. A single HP 3458A is used to calibrate all the three voltage channels between measurements on the PMU under test. Indeed, between two measurements, the calibrator continues to generate 50 Hz signal at nominal values to the PMU under test. During this time, the signal reference waveforms are alternatively applied to the HP 3458A and are measured with an accuracy of 100 ppm. The data generated by the DACs in the PMU calibrator are then adjusted based on these measurements. The all operation is repeated every 30 minutes. At the moment, the range of the calibrator is ± 10 V, considering a maximum uncertainty of 100 ppm, the ΔV_M of the calibrator correspond to 0.01 %.

V. Conclusions

The paper describes the architecture and the metrological characterization of a high-accuracy PMU calibrator presently developed by the DESL-EPFL and METAS. In the first part of the paper we report a study on the steady-state accuracy requirements for PMUs operating in DSs. Making reference to the IEEE 13-bus distribution test feeder where a given number of PMUs is installed, we perform a SE analysis varying numerically the accuracy of the PMUs deployed in the grid. For the specific case, in order to achieve a sufficient SE accuracy, the PMUs have to be characterized by a TVE =

0.3%. As a consequence, an associated PMU calibrator has to be characterize by a TVE of, at least, 0.03%.

Then, we describe the the hardware architecture of the proposed PMU calibrator. We quantify: the influence of phase and magnitude error on the TVE assessment and the importance of the accuracy of the master reference clock. The PMU calibrators nowadays available are synchronized to UTC through GPS signal. Therefore, the calibration of a generic PMU involves two GPS-receivers: one on the PMU calibrator and one on the PMU itself. We demonstrate that the combined uncertainty of the two GPS-receivers might distort the reliability of the calibration because a significant timing uncertainty is introduced. For this reasons, the proposed PMU calibrator implements as a master reference clock the UTC-CH generated at METAS laboratories. The implementation of this solution improves substantially the timing accuracy of the PMU calibrator. We quantify the timing uncertainty of the proposed PMU calibrator in ±81 ps.

Afterwards, we present the metrological characterization of the hardware component of the calibration system. In particular, we estimate the synchronization uncertainty introduced by the DACs, referred to the output of the time synchronization board, in ±0.6 ns. As the DACs and the ADCs, used for the measurement of the voltage reference waveforms, are implements on the same board (PXI-6289), we assume the same synchronization uncertainty for the DACs and the ADCs since they are implemented on the same board. This assumption results into a more conservative uncertainty than the one that can be inferred from the board datasheet (i.e., 0.1 ns).

We measure the total magnitude error of the calibrator through a high precision digital voltmeter HP 3458A that acquires the voltage reference waveforms generated by the DACs. The HP 3458A provides an accuracy of 100 ppm that in the rage of ± 10 V correspond to Δ_M = 0.01 %.

The performances of the proposed PMU calibrator are summarized in Table II. The combined timing and synchronization uncertainty of the proposed PMU calibrator is then around 1.3 ns, which means a phase error (Δ_φ) lower than 500 nrad for a 50 Hz voltage signal. As shown in Section III-A, with Δ_M=0.01 %, below 100 μrad the weight of Δ_{varphi} (500 nrad in our case), on the TVE, is negligible compared to the Δ_M. Therefore, the proposed calibrator system has an estimated TVE of $\approx$ 0.01% referred to steady-state conditions. This uncertainty is circa five times smaller than the most advanced PMU test systems.

TABLE II
FAULT CURRENT LIMITER PARAMETERS SUMMARY

	Δ_φ **(nrad)**	Δ_M **(%)**	**TVE (%)**
Time synch. board	25		
DACs	200		
ADCs	200		
PMU calibrator	< 500	0.01	≈ 0.01

At the moment, the calibration system is limited to the generation of voltage waveforms in the range of ±10 V. Moreover, the assessment of the TVE makes reference to steady-state conditions only. The future work concerns: (i) the extension of the system to current reference waveforms; (ii) the upscale of the system to enables us the calibration of PMUs with high rated voltage/current. (iii) the metrological assessment of the dynamic performance of the PMU calibration; (iv) couple the proposed calibrator with Phasor Data Concentration features in order to be able to perform all the latency assessment dictated by the IEEE standards [6], [7].

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