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Impact of Asymmetric Configurations on the Heterogate Germanium Electron–Hole Bilayer Tunnel FET Including Quantum Confinement

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***Abstract*— We investigate the effect of asymmetric configurations on the heterogate germanium electron–hole bilayer tunnel FET (TFET) and assess the improvement that they provide in terms of boosting the typically very low ON-current levels of TFET devices in the presence of field-induced quantum confinement. We show that when a very strong inversion for holes is induced at the bottom of the channel, the formation of the inversion layer for electrons is shifted to higher gate voltages, which in turn enhances the electrostatic control of the band bending at the top of the channel. As a result, the pinning of the quantized energy subbands is prevented for a wider range of gate voltages, and this allows vertical band-to-band tunneling distances to be further reduced compared with the conventional symmetric electron–hole bilayer configurations.**

***Index Terms*— Asymmetric layouts, band-to-band tunneling (BTBT), heterogate electron–hole bilayer tunnel FET (HG-EHBTFET), inversion layer, quantum confinement.**

I. Introduction

Tunnel FETs (TFETs) have been gaining growing interest in the last years as potentially compelling devices to replace the traditional MOSFETs at low V_{DD} and overcome their 60-mV/decade subthreshold swing (SS) limit at room temperature [1] imposed by the thermionic emission mechanism on which they rely. TFETs, on the contrary, operate on the physically different basis of band-to-band tunneling (BTBT) phenomena. The quantum mechanical process of tunneling between valence and conduction bands removes the aforementioned switching limitation and allows the possibility of developing steep slope devices (SS $<$ 60 mV/decade). As a result, great effort in simulation, modeling, and fabrication has been devoted to this type of transistors [2]–[8].

Manuscript received April 10, 2015; revised July 2, 2015 and July 31, 2015; accepted August 24, 2015. This work was supported in part by the Ramón Areces Foundation and in part by the Seventh Framework Programme through the E2-Switch Project under Grant 619509. The work of J. L. Padilla was supported by the Ramón Areces Foundation for a Post-Doctoral Fellowship. The review of this paper was arranged by Editor Y. Momiyama.

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Digital Object Identifier 10.1109/TED.2015.2476350

Essentially, most of the TFETs are based on asymmetrically doped gated p-i-n structures in which the efficiency of the gate to trigger and control BTBT is greatly correlated with the orientation of the gate electric field induced by it [9]. It was shown that the optimal configuration arises when both electric field and tunneling directions are aligned [10]–[13]. In this last case, the ON-current turns out to be proportional to the gate length. However, for the sake of scalability, gate lengths cannot be increased beyond certain limits and this imposes severe constraints to the current levels that may be reached in the ON-state. In addition, and to sharpen the switching behavior of this type of transistors, it was proposed to exploit BTBT between 2-D electron and hole gases to take an advantage of the impact of carrier dimensionality on tunneling [14]. As a result, the electron–hole bilayer TFET (EHBTFET) [15] was featured with very appealingly low SS values. Current levels at low operating voltages were also reported to be enhanced through direct BTBT processes in germanium EHBTFETs [16]. Unfortunately, when field-induced quantum confinement was considered in these devices [17], quantization of the formerly continuous valence and conduction bands led to reduced I_{ON} values. The appearance of harmful effects coming from confinement has also been elucidated in different TFET structures other than the EHBTFET [18]–[22].

Very recently, the combination of quantum confinement assessment along with the possibility of determining dynamically the BTBT path [23] showed—conversely to what happened in the semiclassical framework—that the EHBTFET suffered from parasitic lateral tunneling processes [24], [25]. The presence of this unwanted lateral tunneling was demonstrated to degrade the steepness of the I_{DS}–V_{GS} curves. To get rid of this deleterious contribution, a heterogate EHBTFET (HG-EHBTFET) was proposed with very abrupt switching behavior restored [24] and suitable for low operating voltages [26], [27]. Heterogate structures in planar devices with different gate materials above the same or different gate dielectrics along the channel might be accomplished through electron beam, selective/angle ion implantation, or precise lithographic alignment.

Alternative configurations to those presented in this paper might be achieved by the use of very highly doped pockets (e.g., p^+ pocket at the bottom of the overlap region combined with an undoped top-side pocket; or both p^+ and n^+ pockets

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at the bottom and top of the overlap, respectively). However, they would imply to resign the control of the inversion layer formation by gate biasing. Other configurations with symmetrically arranged gates and including lightly doped drain–source regions were also proposed in [28], but turn out to be unadvisable due to the persistence of the aforementioned parasitic lateral tunneling processes that degrade their switching behavior.

In this paper, we demonstrate how, by means of asymmetric configurations, it becomes possible to control the formation of the electron inversion layer in the germanium HG-EHBTFET for a fixed tunneling onset. The formation of this inversion layer is known to be responsible of the energy subband pinning and the subsequent BTBT distance saturation. Therefore, the delayed formation of the inversion layer due to very strong asymmetric layouts will lead to considerably enhanced ON-state currents but at the expense of sacrificing to some extent the sharp switching behavior. We show that a convenient tradeoff can be obtained by moderate asymmetric setups where steepness is preserved while I_{ON} values turn out to be still boosted.

The structure of this paper is as follows. Section II describes the device structure and outlines the simulation setup. In Section III, we assess the impact of different grades of asymmetry and find the optimal configuration for a 10-nm-thick Ge HG-EHBTFET. Section IV elucidates the effect of body thickness reduction, combined with different asymmetric layouts, on the device performance. Finally, the conclusion is drawn in Section V.

II. Device Structure and Simulation Approach

The structures shown in Fig. 1 feature a source p$^+$ region (10^{20} atoms/cm^3), an intrinsic channel region with central overlap and side underlap regions (10^{15} atoms/cm^3), and a drain n$^+$ region (10^{20} atoms/cm^3). The germanium body thickness is chosen to be 10 nm for the results and analysis of Section III, and modified to lower values in Section IV. Top- and bottom-gate dielectrics are 3-nm-thick HfO_2 layers. Drain bias will be 0.3 V throughout this paper and bottom-gate bias, V_{BG}, initially set to 0 V. The different asymmetric configurations will be induced by gradual negative values of V_{BG}. The top-gate workfunctions, $\phi_{tg,ol}$ and $\phi_{tg,ul}$, as well as the bottom-gate workfunctions, $\phi_{bg,ol}$ and $\phi_{bg,ul}$, need to be wisely chosen in order to: 1) suppress parasitic lateral tunneling between the overlap and underlap regions before the onset of vertical BTBT (two constraints); 2) avoid lateral BTBT (perpendicular to the gate electric field) from the right underlap to the drain (one constraint); and 3) tune the triggering of vertical BTBT by subband alignment to very low top-gate voltage, namely, $V_{TG,align} = 0.04$ V (one constraint). As the number of constraints equals the number of workfunctions understood as degrees of freedom, we will derive their optimized values in Section III.

The quantization direction is along the [100] crystal orientation of Ge. Along this direction, the L electron valleys are fourfold degenerate with quantization effective mass $m_y = 0.12m_0$ and transverse effective masses $m_x = 0.15m_0$ and $m_z = 0.58m_0$. For the Γ valley, the effective masses of

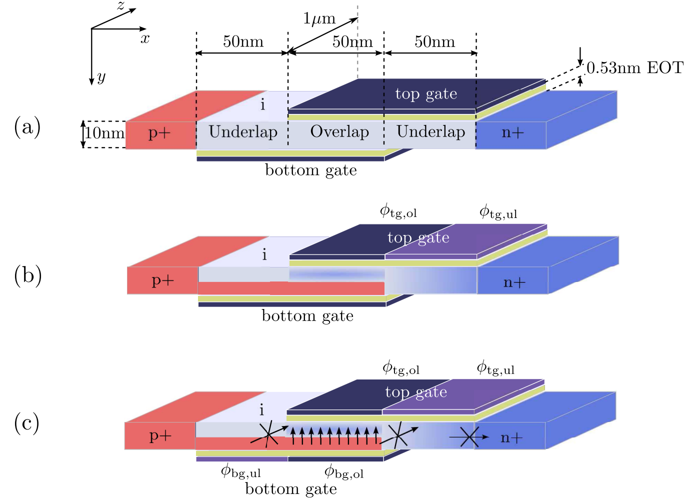

Fig. 1. (a) Schematic cross section (not to scale) of Ge EHBTFET along with the dimensions considered in this paper. (b) Originally proposed HG-EHBTFET structure with heterogate configuration at the top gate to prevent lateral tunneling between the overlap and the right underlap regions. (c) HG-EHBTFET structure considered in this paper. As a result of the vertical BTBT onset adjustment to low V_{TG}, an additional harmful lateral leakage (crossed out arrows) apart from that reported in [24] led to the necessity of similar heterogate setup at the bottom gate. Recall that, in (b) and (c), the apparent p$^+$ doping at the bottom of the channel is not such, but the result of the hole inversion layer formation is induced by opposite biasing at the gates and the utilization of different metal workfunctions.

heavy holes, light holes, and electrons are $m_{hh} = 0.33m_0$, $m_{lh} = 0.044m_0$, and $m_e = m_{lh}$, respectively [29].

The simulation approach was introduced in [24] and is based on a TCAD hybrid integration that combines the up-to-date versions of the two most widely used simulators: 1) Silvaco ATLAS (v.5.20.2.R) [30] and 2) Synopsys Sentaurus (v.2014.09) [23]. Essentially, the simulation consists of two successive steps in each of which we make use of the simulator that provides the most accurate results depending on what needs to be calculated. First, we choose ATLAS to self-consistently solve the Schrödinger and Poisson equations and obtain the electrostatics derived from the inclusion of quantum mechanical confinement. Namely, the free charge distribution is reshaped and the formerly continuous conduction and valence bands turn into a discrete set of energy subbands as repeatedly shown in [17], [18], [20], and [31]. The Schrödinger–Poisson model of ATLAS allows 1-D and 2-D treatments and is known to offer good performance in terms of convergence compared with the 1-D Schrödinger model of Sentaurus which is mostly intended for calibration purposes [23] and features frequent convergence issues [32].

Once the electrostatics is derived, BTBT is accounted as a postprocessing step by means of the dynamic nonlocal BTBT model of Sentaurus [23] which dynamically calculates the tunneling paths based on the energy band profiles. This segmented simulation scheme has been demonstrated to be well-founded as long as tunneling generation does not modify in a noticeable way the charge distribution obtained in the absence of BTBT [17], [21], [22]. Nevertheless, prior to this carrier injection, two main aspects need to be arranged in order to employ the output of the first simulation step

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TABLE I
SEMICLASSICAL AND QUANTUM CORRECTED A AND B PARAMETERS FOR Ge IN THE DYNAMIC NONLOCAL BTBT MODEL. QUANTUM CORRECTED VALUES CONSIDER ONLY THE CONTRIBUTION TO TUNNELING OF HEAVY HOLES

PARAMETER	DIRECT BTBT		INDIRECT BTBT [100]	
	SEMICLASS.	QUANTUM CORRECTED	SEMICLASS.	QUANTUM CORRECTED
A ($\mathrm{cm}^{-3}\mathrm{s}^{-1}$)	1.46×10^{20}	1.959×10^{20}	1.67×10^{15}	1.806×10^{14}
B (Vcm^{-1})	6.04×10^{6}	8.028×10^{6}	6.55×10^{6}	11.12×10^{6}

as the input of the second. First, the potential and charge distributions arising from the ATLAS Schrödinger–Poisson model are accounted for in Sentaurus through appropriate calibration of a density gradient model. Second, we modify the band profiles of the conduction and valence bands via structure editor tools to make them coincident with their first bound states, therefore, managing BTBT to occur between first subbands, and not between band edges (which now become forbidden states) as it happened semiclassically. This TCAD-based bandgap widening was originally proposed for TFETs where BTBT direction was not aligned with the gate electric field [20]; and later extended for the case of alignment, as in line TFETs with a 1-D band structure modification [22], or the HG-EHBTFET, with a more accurate 2-D bandgap adjustment [24]. Very recently, the quantization bandgap widening effects for pocketed dual-metal-gate TFETs have been assessed using very similar techniques [32].

Phonon-assisted and direct BTBT parameters have been conveniently modified compared with those presented in [29] in order to remove from them light holes contribution to tunneling. Severe quantization effects due to their low effective mass prevent alignment between their first subband (E_{lh1}) and that corresponding to electrons (E_{e1}). So far, the semiclassical tunneling parameters and quantum corrected ones for germanium are presented in Table I. Removing light holes contribution represents, on one hand, an additional difficulty that will lower I_{ON} levels; but on the other, it reinforces the necessity of optimization mechanisms in the presence of confinement such as those, hereinafter, discussed based on asymmetric setups. Gate leakage assessment [33] has not been included in this paper and remains as a pending task for future work.

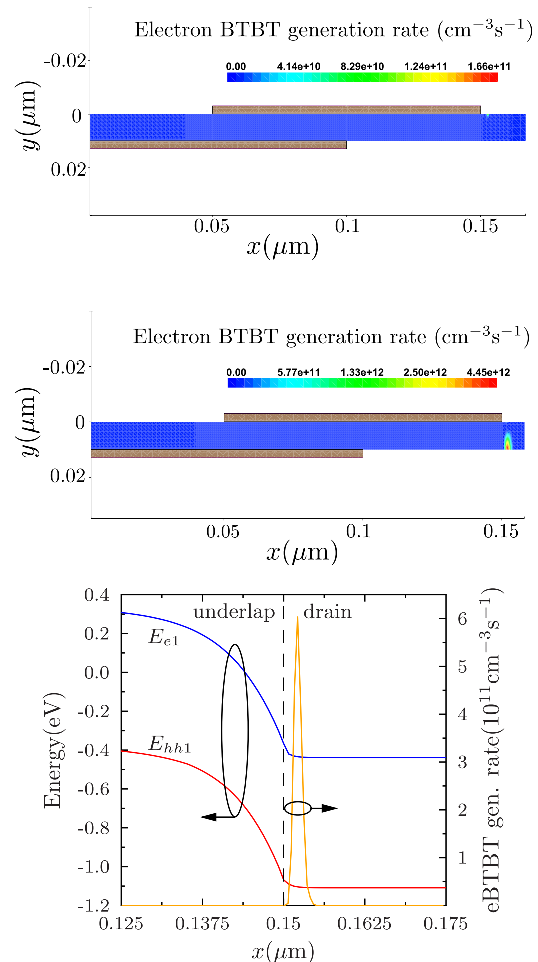

Fig. 2. Top: 2-D plot displaying the electron BTBT generation rate at $V_{\mathrm{DS}} = 0.3$ V and $V_{\mathrm{TG}} = V_{\mathrm{BG}} = 0$ V for $\phi_{\mathrm{tg,ul}} = \phi_{\mathrm{tg,ul}}^{\max} = 4.25$ eV. Observe that no lateral BTBT exists flowing to the drain. Middle: 2-D plot for electron BTBT generation rate for $\phi_{\mathrm{tg,ul}} = 4.3$ eV. In this case, a certain BTBT is triggered between the underlap and the drain. Bottom: band profile corresponding to a horizontal underlap-to-drain cut at the middle of the channel for $\phi_{\mathrm{tg,ul}} = 4.3$ eV showing the band alignment that allows incipient BTBT.

III. SIMULATION RESULTS AND DEVICE OPTIMIZATION

In this section, we consider a fixed 10-nm value for the body thickness of the HG-EHBTFET, as shown in Fig. 1(c). The first workfunction to be analyzed, $\phi_{\mathrm{tg,ul}}$, corresponds to the top-gate underlap adjacent to the drain. It was established [24] that in order to suppress the parasitic lateral leakage between the overlap and the drain underlap, $\phi_{\mathrm{tg,ul}}$ needed to be raised with respect to $\phi_{\mathrm{tg,ol}}$. However, given the doping profiles of the different regions, the desired onset of vertical BTBT at very low top-gate voltages (we choose $V_{\mathrm{TG,align}} = 0.04$ V) imposes a constraint on the maximum value allowed for $\phi_{\mathrm{tg,ul}}$. Otherwise, should this maximum value (which turns out to be $\phi_{\mathrm{tg,ul}}^{\max} = 4.25$ eV) exceed, the lateral BTBT from the right underlap to the drain would appear, thus degrading the device performance. Observe how indeed in Fig. 2, for $\phi_{\mathrm{tg,ul}} = 4.3$ eV and $V_{\mathrm{TG}} = 0$ V (OFF-state), a certain BTBT generation rate appears directly in the drain whereas a value of $\phi_{\mathrm{tg,ul}} = 4.25$ eV still prevents the appearance of this parasitic tunneling. As quantization is taken along the y-direction given the extended horizontal length of the device, the bound states retain a dependence on x, i.e., $E_i = E_i(x)$. The values of the other workfunctions do not affect this channel-to-drain tunneling and, in order to fix $\phi_{\mathrm{tg,ul}}$, they have simply been chosen to avoid other tunneling phenomena.

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TABLE II
OPTIMIZED TOP- AND BOTTOM-GATE WORKFUNCTIONS FOR DIFFERENT ASYMMETRIC CONFIGURATIONS IN THE Ge HG-EHBTFET FEATURING A BODY THICKNESS OF 10 nm WITH $V_{\mathrm{TG,align}} = 0.04$ V

$\phi_{\mathrm{tg,ol}}$(eV)	$\phi_{\mathrm{tg,ul}}$(eV)	$\phi_{\mathrm{bg,ol}}$(eV)	$\phi_{\mathrm{bg,ul}}$(eV)	V_{BG}(V)	V_{inv}(V)	$E_{e1,\mathrm{ul}} - E_{e1,\mathrm{ol}}$(eV)	$E_{hh1,\mathrm{ol}} - E_{hh1,\mathrm{ul}}$(eV)
3.258	4.25	5.25	4.60	0	0.32	0.269	0.050
3.351				-0.25	0.48	0.192	0.036
3.414				-0.5	0.56	0.145	0.041
3.472				-0.75	0.64	0.101	0.050
3.529				-1.0	0.72	0.057	0.060
3.587				-1.25	0.78	0.014	0.069

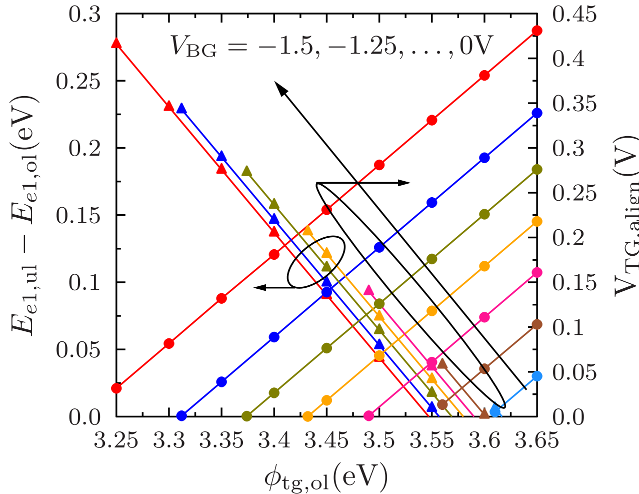


Fig. 3. Values for the vertical tunneling onset, $V_{\mathrm{TG,align}}$ (circle markers), and energy difference $E_{e1,\mathrm{ul}} - E_{e1,\mathrm{ol}}$ (triangle markers) as a function of $\phi_{\mathrm{tg,ol}}$. Appropriate values for $\phi_{\mathrm{tg,ol}}$ can be found for $V_{\mathrm{BG}} > -1.25$ V satisfying $V_{\mathrm{TG,align}} = 0.04$ V and $E_{e1,\mathrm{ul}} > E_{e1,\mathrm{ol}}$.

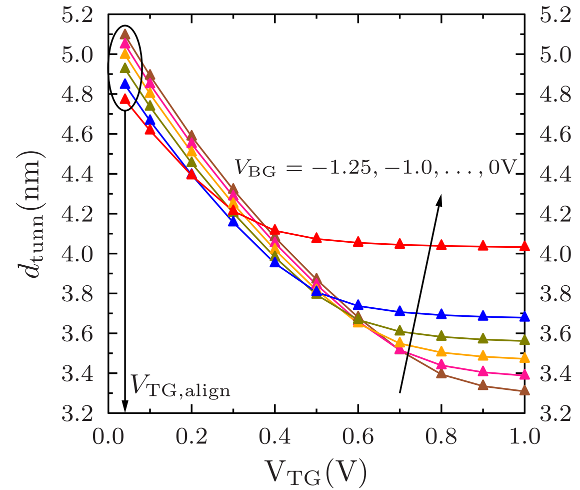


Fig. 4. Minimum vertical BTBT distances versus V_{TG} for the different asymmetric configurations at $V_{\mathrm{DS}} = 0.3$ V. The formation of the inversion layer for electrons in each case determines the gate voltage at which tunneling distances start to saturate. Notice the opposite behavior of d_{tunn} before and after V_{inv}.

Once $\phi_{\mathrm{tg,ul}}$ is fixed to 4.25 eV, we proceed to find the appropriate values for the workfunctions in the overlap region, $\phi_{\mathrm{tg,ol}}$ and $\phi_{\mathrm{bg,ol}}$. Considering that any voltage applied to the bottom gate might be absorbed by $\phi_{\mathrm{bg,ol}}$, we have a certain freedom to select its reference value at $V_{\mathrm{BG}} = 0$ V. We choose $\phi_{\mathrm{bg,ol}} = 5.25$ eV. Now, we have to fix $\phi_{\mathrm{tg,ol}}$ in order to trigger the vertical BTBT at $V_{\mathrm{TG}} = V_{\mathrm{TG,align}} = 0.04$ V and provided that $E_{e1,\mathrm{ul}} > E_{e1,\mathrm{ol}}$ to avoid the parasitic tunneling leakage [24]. $E_{e1,\mathrm{ul}}$ and $E_{e1,\mathrm{ol}}$ are extracted at the center of the drain underlap and overlap regions, respectively [26]. Fig. 3 shows the dependence of the difference $E_{e1,\mathrm{ul}} - E_{e1,\mathrm{ol}}$ and $V_{\mathrm{TG,align}}$ on the values of $\phi_{\mathrm{tg,ol}}$ for different bottom-gate biases. It can be seen how for -1.25 V $< V_{\mathrm{BG}} < 0$ V, it is possible, at least in theory, to find a suitable $\phi_{\mathrm{tg,ol}}$ fulfilling the desired requirements. From a technological point of view, binary alloys could be investigated as a way to cope with this necessary workfunction tuning. Therefore, the allowed asymmetric configurations for the HG-EHBTFET will be controlled by the applied negative V_{BG} up to -1.25 V.

Finally, we fit $\phi_{\mathrm{bg,ul}}$ in order to suppress the detrimental lateral BTBT from the source underlap to the overlap region [see Fig. 1(c)]. To do so, we force that $E_{hh1,\mathrm{ol}} > E_{hh1,\mathrm{ul}}$ at $V_{\mathrm{TG}} = V_{\mathrm{TG,align}}$. As $\phi_{\mathrm{bg,ol}}$ was previously chosen to be 5.25 eV, if we impose that $E_{hh1,\mathrm{ol}} - E_{hh1,\mathrm{ul}} \approx 0.05$ eV, we obtain $\phi_{\mathrm{bg,ul}} = 4.60$ eV.

A summary of the values obtained for the different workfunctions according to the degree of asymmetry (controlled by V_{BG}) is presented in Table II. We have also included the top-gate voltages at which the inversion layer for electrons is formed at the top of the channel, V_{inv}, obtained as described in [34].

We observe how, as the inversion for holes at the bottom becomes stronger, the formation of the electron inversion layer at the top of the channel is shifted to higher V_{TG} values. The increasing asymmetry allows the top gate to retain electrostatic control on the channel for a wider range of voltages, which means that the energy subbands remain longer unpinned. As a result, strong asymmetric setups will allow vertical BTBT distances to be further reduced in the ON-state.

Fig. 4 shows the evolution of the minimum tunneling distance at the center of the overlap region for the different bottom-gate voltages. Note that although stronger asymmetries provide lower d_{tunn} values at high V_{TG} (as a result of V_{inv} shifting), this behavior turns out to be the opposite at $V_{\mathrm{TG}} = V_{\mathrm{TG,align}}$. The reason for this lies in the fact that when we fix V_{TG} to $V_{\mathrm{TG,align}}$ and apply increasing negative biases at the bottom gate, we gradually shift holes from inversion to strong inversion, which means that the band structure at the bottom of the channel gradually diverges from

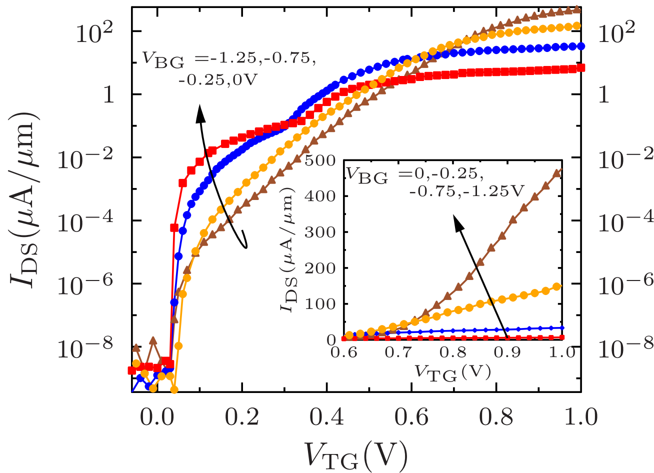


Fig. 5. I_{DS}–V_{TG} curves for different bottom-gate biases. $V_{BG} = 0$ V features the steepest switching behavior at tunneling onset, whereas the lowest ON-current at high V_{TG}. For operation voltages ~0.5 V, $V_{BG} = -0.25$ V provides a convenient tradeoff.

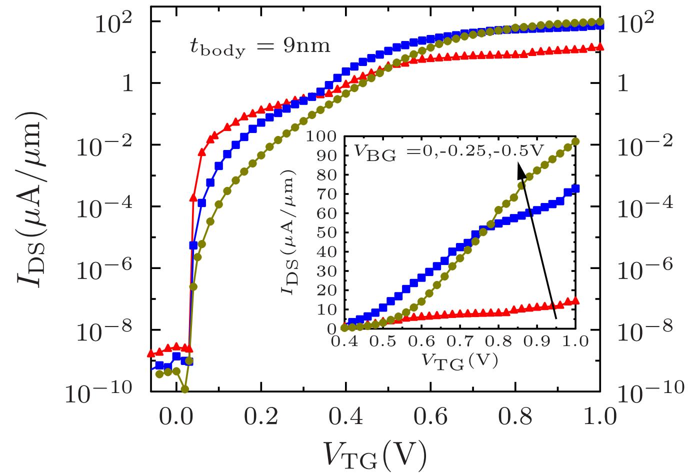
TABLE III
POINT AND AVERAGE SSs ALONG WITH ON-CURRENT LEVELS AT $V_{TG} = 0.5$ AND 1 V FOR DIFFERENT ASYMMETRIC CONFIGURATIONS IN THE 10-nm Ge HG-EHBTFET

V_{BG}(V)	SS_{pt}(mV/dec)	SS_{av}(mV/dec)	$I_{ON}^{0.5V}$(μA/μm)	I_{ON}^{1V}(μA/μm)
0	2.31	38.96	1.99	6.93
-0.25	4.80	36.56	6.00	33.25
-0.75	6.06	43.98	1.73	150.97
-1.25	5.77	43.97	0.68	476.88

a linear profile and adopts a more rounded shape with a subsequent tunneling distance increase between electron and hole subbands at the moment of alignment. Therefore, very tough asymmetric setups would feature degraded switching performance compared with the conventional EHBTFETs. Considering the tunneling reduction ratios displayed in Fig. 4 when $V_{TG} > V_{inv}$ (i.e., when tunneling distance has started to saturate), it can be seen that $V_{BG} = -0.25$ V offers an appealing tradeoff as can be indeed confirmed inspecting the transfer characteristics, as shown in Fig. 5. We observe that the steepest point SS (taken at $V_{TG} = V_{TG,align}$) corresponds to $V_{BG} = 0$ V with $SS_{pt} = 2.31$ mV/decade, but at the expense of the lowest current level at $V_{TG} = 1$ V. Table III contains the values for point SS, average SS (taken between $V_{TG,align}$ and $V_{TG,align} + V_{DS}$), and ON-current at $V_{TG} = 0.5$ and 1 V for the curves shown in Fig. 5.

IV. BODY THICKNESS VARIATION

Body thickness reduction might be considered as a possible solution in order to boost I_{ON} levels displayed in Section III given that, in principle, the lower tunneling distances could be reached this way. However, as we reduce t_{body}, the harmful effects coming from quantum confinement become stronger, which could make subband alignment more difficult to be attained. Moreover, the role of the electron inversion layer formation in such a scenario with tougher quantization would also require a careful assessment. In this context, we aim to analyze the potential benefits that a moderate asymmetric setup would provide for $t_{body} = 8$ and 9 nm and their implications on SS and I_{ON} values.



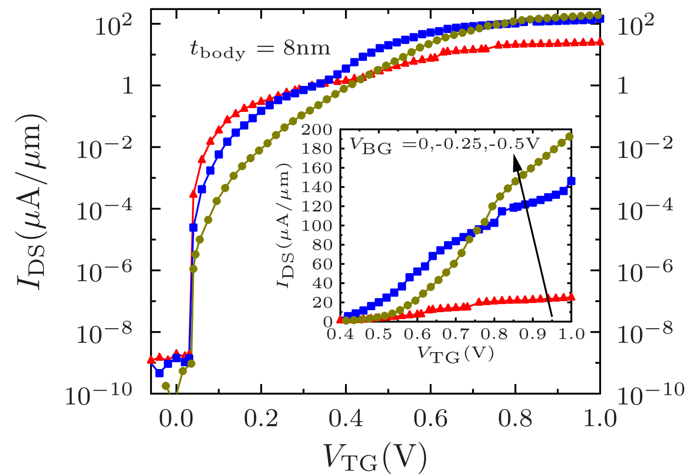


Fig. 6. Transfer characteristics for $t_{body} = 8$ and 9 nm corresponding to different asymmetric configurations $V_{BG} = 0$ V (triangle markers), $V_{BG} = -0.25$ V (square markers), and $V_{BG} = -0.5$ V (circle markers). We have adjusted the gate workfunctions in order to make $V_{inv}(V_{BG} = 0$ V) coincident with that for $t_{body} = 10$ nm. We observe that the case $V_{BG} = -0.25$ V features again the most convenient behavior.

Let us start off by adjusting the top- and bottom-gate workfunctions at $V_{BG} = 0$ V in order to fulfill the constraints exposed in Section II and to make $V_{TG,align}$ and V_{inv} coincident with those shown in the first row of Table II (i.e., 0.04 and 0.32 V, respectively). In Table IV, we present these optimized values along with the ones for a moderate asymmetric configuration corresponding to $V_{BG} = -0.25$ and -0.5 V.

Notice that the induction of asymmetric conditions by means of bottom-gate biasing has an interesting implication shifting V_{inv} to higher values of V_{TG} as we reduce t_{body}. Namely, for $t_{body} = 10$ nm, we report a displacement of V_{inv} at $V_{BG} = -0.25$ V of 50% (from $V_{inv} = 0.32$ to 0.48 V); whereas for $t_{body} = 9$ and 8 nm, this shifting turns out to be of 56% and 63%, respectively. This behavior associated with t_{body} reduction is really appealing given that as V_{inv} increases, energy subband pinning is delayed and smaller tunneling distances can be achieved as inferred from Fig. 4. Transfer characteristics for $t_{body} = 8$ and 9 nm are shown in Fig. 6. Advisable tradeoff between SS steepness and boosted

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TABLE IV
OPTIMIZED TOP- AND BOTTOM-GATE WORKFUNCTIONS FOR $V_{BG} = 0, -0.25$, AND -0.5 V AND $t_{body} = 8$ AND 9 nm WITH $V_{TG,align} = 0.04$ V IN THE Ge HG-EHBTFET

t_{body}(nm)	$\phi_{tg,ol}$(eV)	$\phi_{tg,ul}$(eV)	$\phi_{bg,ol}$(eV)	$\phi_{bg,ul}$(eV)	V_{BG}(V)	V_{inv}(V)	ΔE_{e1}(eV)	ΔE_{hh1}(eV)
9	3.150	4.25	5.33	4.60	0	0.32	0.286	0.045
	3.248				-0.25	0.50	0.204	0.033
	3.313				-0.5	0.58	0.156	0.041
8	3.013	4.25	5.45	4.60	0	0.32	0.300	0.047
	3.111				-0.25	0.52	0.217	0.032
	3.175				-0.5	0.62	0.169	0.040

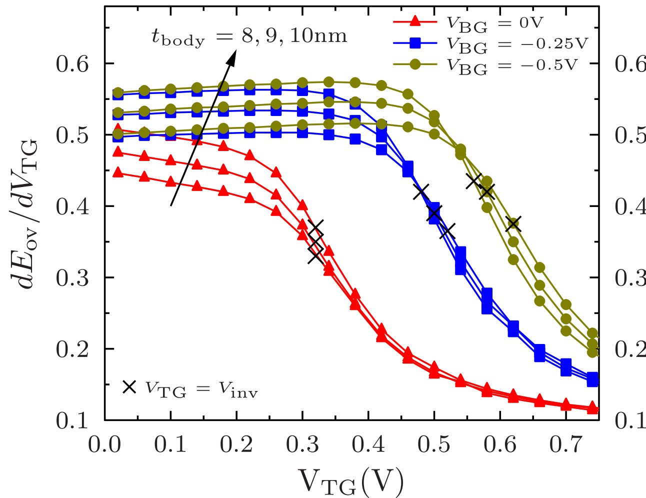

Fig. 7. Behavior of the gate-to-gate efficiencies for $t_{body} = 8, 9$, and 10 nm corresponding to the asymmetric configurations induced by bottom-gate biases of 0, -0.25, and -0.5 V. In spite of the efficiency decrease due to the stronger confinement effects when we reduce t_{body}, the induction of moderate asymmetries keeps the efficiencies over 0.5 for a wider range of V_{TG} values.

I_{ON} is obtained at $V_{BG} = -0.25$ V, similar to what happened for $t_{body} = 10$ nm.

We investigate now the effect of these asymmetric layouts on the behavior of the gate efficiency, understood as the fraction of the total gate-to-gate incremental voltage modifying the energy overlap between the first subbands [33], i.e., dE_{ov}/dV_{TG}, taken at the center of the channel. Fig. 7 shows how, for each of the different V_{BG} values considered in this section, the efficiency drops once V_{inv} is left behind. Moreover, it is very interesting to see that the decreasing trend of the efficiency observed for $V_{TG} < V_{inv}$ at $V_{BG} = 0$ V disappears when we increase the negative bias applied at the bottom gate ($V_{BG} = -0.25$ and -0.5 V). Therefore, for low operating voltages such that $V_{DD} < V_{inv}$, a moderate asymmetry guarantees sustained efficiencies ≥ 0.5 for $t_{body} \geq 8$ nm, which proves to be a noticeable result considering that the quantum confinement effects are known to constrain efficiency values well below 1 [33].

These results make us conclude that in the presence of field-induced quantum confinement, a moderate asymmetric setup for the HG-EHBTFET reveals itself as a mechanism for optimizing ON-state currents while preserving an abrupt switching behavior. Furthermore, as long as the operation voltage remains below V_{inv} (for example, $V_{TG} = 0.5$ V for $t_{body} = 8$ nm at $V_{BG} = -0.25$ V), the HG-EHBTFET should rather be considered as a pseudobilayer-based TFET featuring enhanced gate-to-gate efficiency values. Such a pseudobilayer configuration provides an additional advantage as it may alleviate the inconveniences of confining very large concentrations of opposite carriers in very reduced body thicknesses.

V. CONCLUSION

In this paper, we have optimized the structure of the heterogate germanium EHBTFET and investigated the implications that certain asymmetric configurations have on the device performance in the presence of field-induced quantum confinement. We have shown that a moderate asymmetric setup proves to be an advisable mechanism to be explored for boosting ON-state current levels while preserving very steep SSs and improving gate-to-gate efficiencies. Moreover, the pseudobilayer configurations derived from these asymmetric layouts may help to relieve the expected difficulties of keeping apart very large electron and hole concentrations in very thin structures.

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