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A sub-mW pulse-based 5-bit flash ADC with a time-domain fully-digital reference ladder

Nikola Katic*, Radisav Cojbasic, Alexandre Schmid, Yusuf Leblebici

Swiss Federal Institute of Technology (EPFL), Batiment ELD, Station 11, 1015 Lausanne, Switzerland

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ABSTRACT

The concept of time-domain reference-ladder for the implementation of fully-digital flash-ADCs is proposed in this work. The complete reference ladder is implemented using only digital circuits. Based on this concept, a flash ADC is proposed and implemented in this work using digital circuits, one comparator and a customized sample-and-ramp circuit. An unconventional time-to-digital conversion (TDC) technique is introduced which performs the complete conversion within a single clock cycle. The measurement results show that the proposed 5-bit converter achieves an 80 MHz sampling rate while consuming 900 μW of power from the 1.8 V supply voltage. The prototype ADC is developed in a 180 nm standard CMOS technology and achieves the power efficiency of 445 fJ/conversion which is comparable to many existing state-of-the-art flash ADCs. The measured performance is achieved without any design optimization or circuit calibration techniques confirming the promising benefits of the proposed topology. Thanks to the fully-digital structure, the circuit enables a robust and compact implementation which is very convenient for interleaving and beneficial for many potential applications.

1. Introduction

Digital circuits are significantly less sensitive to noise, device mismatch and integrated circuit parasitic effects than their analog counterparts. Moreover, conventional analog design techniques require signal linearity which is especially important in analog-to-digital converter (ADC) design. However, linearity has been increasingly hard to achieve in modern sub-micron CMOS processes due to low supply voltage and reduced intrinsic gain of the MOSFET devices. Digital CMOS circuits operate rail-to-rail; they are essentially non-linear, hence they do not rely on signal linearity. Accordingly, recent trend in ADC design increasingly promotes digital implementations of the converter core [1,2]. In addition, digital circuits can perform error-correction tasks very efficiently which has motivated the studies of digitally-assisted analog circuits for over a decade [3]. Nowadays, digital calibration is a necessity for efficient high and medium resolution ADCs [4–6] and is starting to emerge even in low resolution ADCs [7].

Time-to-digital conversion (TDC) represents an additional recent research focus in the field of ADC design. Thanks to the CMOS technology scaling, the CMOS gate delay has reached the pico-second range which allows a very high time-domain (ps) resolution [8–12]. TDCs process signals in time-domain and can be based on mainly digital circuits, consequently exploiting all the benefits of digital operation. Conveniently, TDCs utilize the high speed of modern CMOS technologies (high cutoff frequency f_T) and do not rely on voltage amplitudes, which allows them to operate at a low supply voltage. Nevertheless, achieving the high resolution in time-domain is not as straight-forward as it might seem. Conventional flip-flops (latches) which are needed to sample the high-speed data, suffer from relatively high setup and hold-times. Moreover, latch regeneration process can be very sensitive to input signal amplitudes and device mismatch. If not taken into consideration, these circuit non-idealities can set the limit to the achievable time resolution, therefore limiting the overall performance of the converter. Design in [8] uses time multipliers to multiply the timing residue created by the long latch regeneration process. This approach effectively eliminates the problem of long latch regeneration and creates fine-coarse converter topology (similar to folding) ADC. A similar approach is used in [9] where a different algorithm (called Redundant Remainder Number System) is used to handle the timing residues and create a folding-flash TDC architecture. In order to ensure narrow sampling window, design in [10] implements a sense-amplifier based latches. Designs presented in [11] and [12] use dynamic latches that are typically less sensitive to timing issues and uncertainties, but often consume more power than static latches. Dynamic latches with pulse-triggered sampling are used in this work because they are very

* Corresponding author.
E-mail address: katic.nik@gmail.com (N. Katic).

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robust when it comes to timing uncertainties and have very low setup and hold times. Another important difficulty of Time-to-Digital conversion is an effective conversion of the input voltage to time domain. An effective solution is used in [12], where the input voltage is sampled and compared to the dual ramp reference, generating pulse-width-modulated (PWM) digital output. Similar concept with a different implementation (sample-and-ramp) is used in this work in order to deal with the input voltage-to-time conversion.

Despite the previously mentioned trends, most state-of-the-art flash ADCs use some form of resistive reference ladder and focus on improvements and optimizations of the existing concepts [13–35]. An interesting design is presented in [13] which uses TDC technique to directly implement a flash converter, however the design still uses a resistive reference ladder at the input stage. The main contribution of this paper consists of replacing the existing concept of the flash ADC's resistive reference ladder with the time-domain reference ladder which offers a straight-forward and efficient digital implementation. This approach results in a digital flash ADC topology with only one comparator. The comparator's pre-amplifier and the sample-and-ramp circuit are the only design blocks operating in the analog-domain. Following the proposed approach, flash ADCs can become fully digital circuits and benefit from digital and time-domain operation. Such implementations are more convenient for low supply voltage operation and for the implementation in the existing advanced nano-meter CMOS technologies. This paper discusses the concept of time-domain reference ladder, the fully-digital flash ADC, and presents a prototype flash ADC design implemented in a 180 nm CMOS technology. The paper is organized as follows. The digital reference ladder concept is explained in Section 2. Section 3 discusses the top-level architecture and the main features of the proposed flash ADC. A specific output decoding scheme implemented to increase the number of available quantization levels and the reliability of the conversion is explained in Section 4. The input-voltage to time-domain converter (voltage-to-time converter, VTC) is discussed in Section 5. The measurement results are presented in Section 6 and the paper conclusion is provided in Section 7.

2. Time-domain pulse-based digital reference ladder

The core function of a conventional flash ADC can be broken down into two fundamental steps, (1) the generation of reference (quantization) voltage levels, and (2) the comparison of the input analog voltage with the generated references. In a conventional flash-topology, the first step is performed by a resistive ladder while the comparison with the generated references is performed by a set of comparators (one per reference). This concept is illustrated in Fig. 1(a). Nevertheless, the same functionality can be achieved by the digital circuit in Fig. 1(b).

A reference clock signal (CLK_{REF}) is generated as a delayed version of the input sampling clock (CLK_{SMPL}) to allow for the input sampling before the reference ladder starts its operation (this will be explained in more detail in Section 5). The reference clock is used as an input to an array of 32 inverters which creates a family of 16 clock signals delayed with respect to each other. The reference clock rising edge and the rising-edges of even inverter outputs are transformed into short pulses using pulse generators (PG – Fig. 1(b)). The pulses generated from inverter outputs symbolize a specific (reference) instance in time during a single clock cycle and provide 16 functional and equally distant time references. A voltage-to-time converter (Section 5) creates an input pulse ($V_{in,pulse}$) which is delayed in time according to the ADC's analog input voltage. The timing of the input pulse is compared to the timings of the reference pulses by a set of dynamic (precharged)

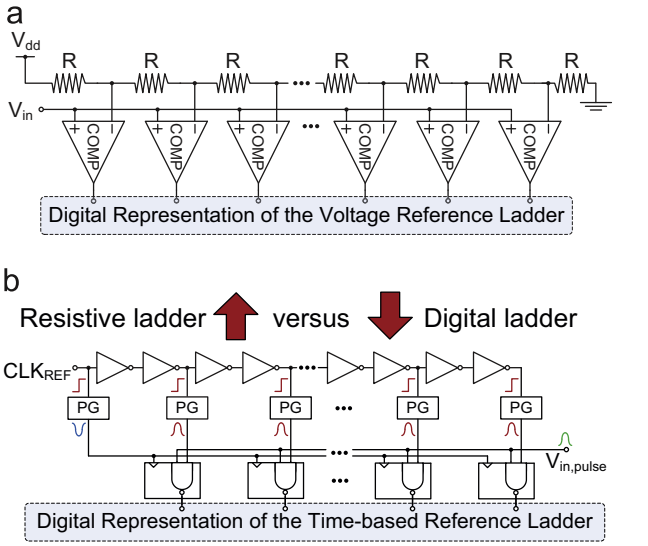

Fig. 1. Conventional (voltage-mode) reference ladder (a), and proposed digital (time-domain) reference ladder (b).

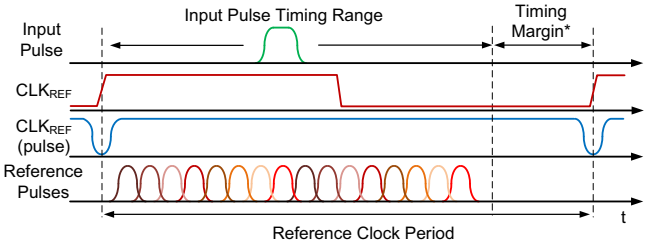

Fig. 2. Operation principle of the digital (time-domain) reference ladder ∗ timing margin is needed to account for PVT variations and to accommodate for the sampling time of the next input sample.

NAND-latches (time-domain comparators). A clock reference pulse ($CLK_{REF,pulse}$) is generated from the CLK_{REF} and used to precharge the NAND-latches. The operation principle of the new (time-domain) reference ladder is shown in Fig. 2. A set of reference pulses is generated during each reference clock period. Each of these pulses defines a different time reference and is provided to the input of a corresponding NAND-latch (Fig. 1(b)). The input pulse is provided to the remaining input of each NAND-latch. The digital signal value at the output of the latches changes depending on the timing of the input pulse compared to the reference pulses. Only the latches that receive a reference pulse which is close (in time) to the input pulse will provide a logic zero at the output. The location of zeros in the output code provides information about the input pulse position and therefore about the ADC's input analog voltage. Before the next rising edge of the reference clock, a timing margin is required (Fig. 2). This timing margin is necessary to account for the worst case PVT variations and at the same time accommodate enough time for correct input voltage settling and sampling. Because the reference delays can vary, the margin has to be large enough to deal with the worst-case delays (the PVT variations are calibrated at the converter input – see Section 5). The margin also needs to be large enough to enable sampling of the next input sample. The sampling pulse width is controlled by the delay between the input signal sampling clock (CLK_{SMPL}) and reference clock CLK_{REF} (see also Figs. 3 and 8). Because the CLK_{SMPL} rising edge comes before the CLK_{REF} rising edge, this timing delay needs to be accounted for within the CLK_{REF} cycle.

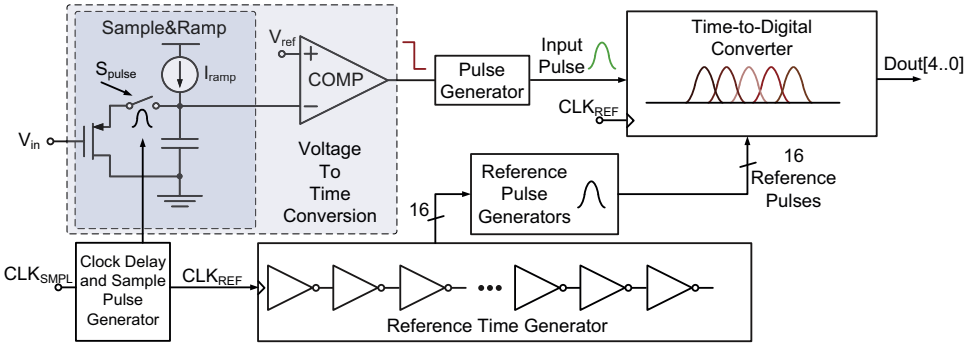

Fig. 3. Block-level diagram of the pulse-based flash ADC.

3. Pulse-based fully-digital flash ADC

The block-level diagram of the complete proposed pulse-based flash ADC is shown in Fig. 3. An analog input voltage to the ADC is converted into time-domain by a voltage-to-time converter which consists of a sample-and-ramp circuit and a comparator. A pulse generator converts the falling-edge of the comparator output into an input pulse which is provided to the time-to-digital converter (the TDC, which consists of NAND-Latches, Fig. 1(b)). The reference-time-generator (RTG) consists of an inverter chain (32 inverters – Fig. 1(b)) and is followed by the reference pulse generators which create the family of 16 reference pulses. The final digital code is delivered as the output of the time-to-digital converter.

A classical circuit implementation of a fully-digital falling-edge pulse generator is shown in Fig. 4, and the transistor level schematic of the dynamic NAND-latch is shown in Fig. 5. This type of dynamic latch is essentially a pulse-triggered latch (flip-flop). A very useful feature of pulse-triggered latches is that they have setup and hold times very close to zero. This is very important if the data needs to be latched reliably at a very high speed. Conventional flip-flops have large setup and hold times that have to be accounted for and can severely limit the obtainable time-resolution. Because the pulse-triggered latch is practically necessary for this purpose, the NAND function was simply embedded inside for a more compact design and faster implementation. The latch operates as follows. The latch is precharged when the clock pulse $CLK_{REF,pulse}$ drives the gate voltage of transistor M3 low (reference clock pulse is active at zero – Fig. 5). As a result, node X is charged to V_{dd} through M3, and node Y is discharged to ground. Consequently, transistor M6 precharges the output of the latch (V_{out}) to V_{dd} (during precharge, transistor M4 is off). After the precharge phase is finished, the $CLK_{REF,pulse}$ signal becomes equal to V_{dd}, transistor M3 turns off, transistor M4 turns on, and the latch enters the sensing phase. As inputs, each latch receives a pulse whose timing corresponds to the ADC's analog input voltage (output of voltage-to-time converter $V_{pulse,input}$) and a pulse which corresponds to one of the time-reference pulses $V_{pulse,rtg}$. The latch can only change its output state if the input pulse and the reference pulse are simultaneously delivered. In this case, node X is discharged to ground, and node Y is driven high. Finally, transistors M4 and M5 drive the latch output low (V_{out}). At the end of the clock cycle, the latches which have an output set to zero correspond to the reference levels that are closest (in time) to the actual value of the analog input voltage. A set of 16 conventional flip-flops samples the latch outputs before the latches are precharged for the next conversion cycle.

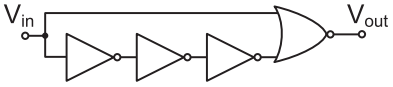

Fig. 4. Fully-digital pulse-generator.

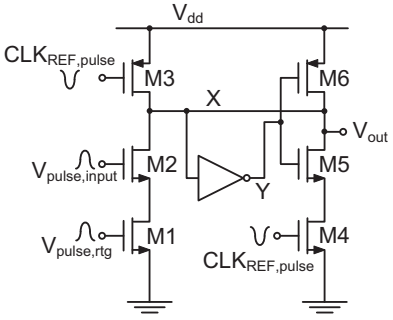

Fig. 5. Schematic of the dynamic NAND-latch (time-domain comparator).

4. Pulse-based ADC decoding scheme

A family of 16 reference pulses (reference levels or quantization levels) would result in a 4-bit resolution ADC, using traditional thermometer coding. However, in order to increase the number of quantization levels of the ADC, and the reliability of the conversion, a specific decoding scheme is proposed in this paper. The input pulse is designed to be slightly wider (in time) than the reference pulses (Fig. 2). As the result, the input pulse can have a time-domain overlap with either one or two reference pulses. A situation where the input pulse has a time overlap with only one reference pulse is depicted in Fig. 6(a). The input pulse only overlaps with the reference pulse k. Consequently, the output of the corresponding NAND-latch will be discharged to zero ($D_{out}[k]$). For instance, if $k=5$, the digital code at the output of the NAND-latches will be "1111111111011111". A situation where the input pulse has a time overlap with two of the reference pulses is shown in Fig. 6(b). In this case, the input pulse overlaps with pulses k and $k-1$. Hence, the output of two latches will have a zero value at the end of the clock cycle. Again, if $k=5$, the corresponding digital code observed at the output of the NAND-latches will be "1111111111001111". This coding scheme doubles the number of effective reference (quantization) levels. The decoding look-up table is defined in Table 1. Therefore, the example values (for $k=5$) from Fig. 6 correspond to the digital codes "01011" and "01010", or decimal values (quantization levels) 11 and 10, respectively.

In addition to increasing the effective number of quantization levels, the applied coding scheme also improves the reliability of the analog-to-digital conversion. Because the input pulse is designed to be "wider" (in time), the input pulse is guaranteed to

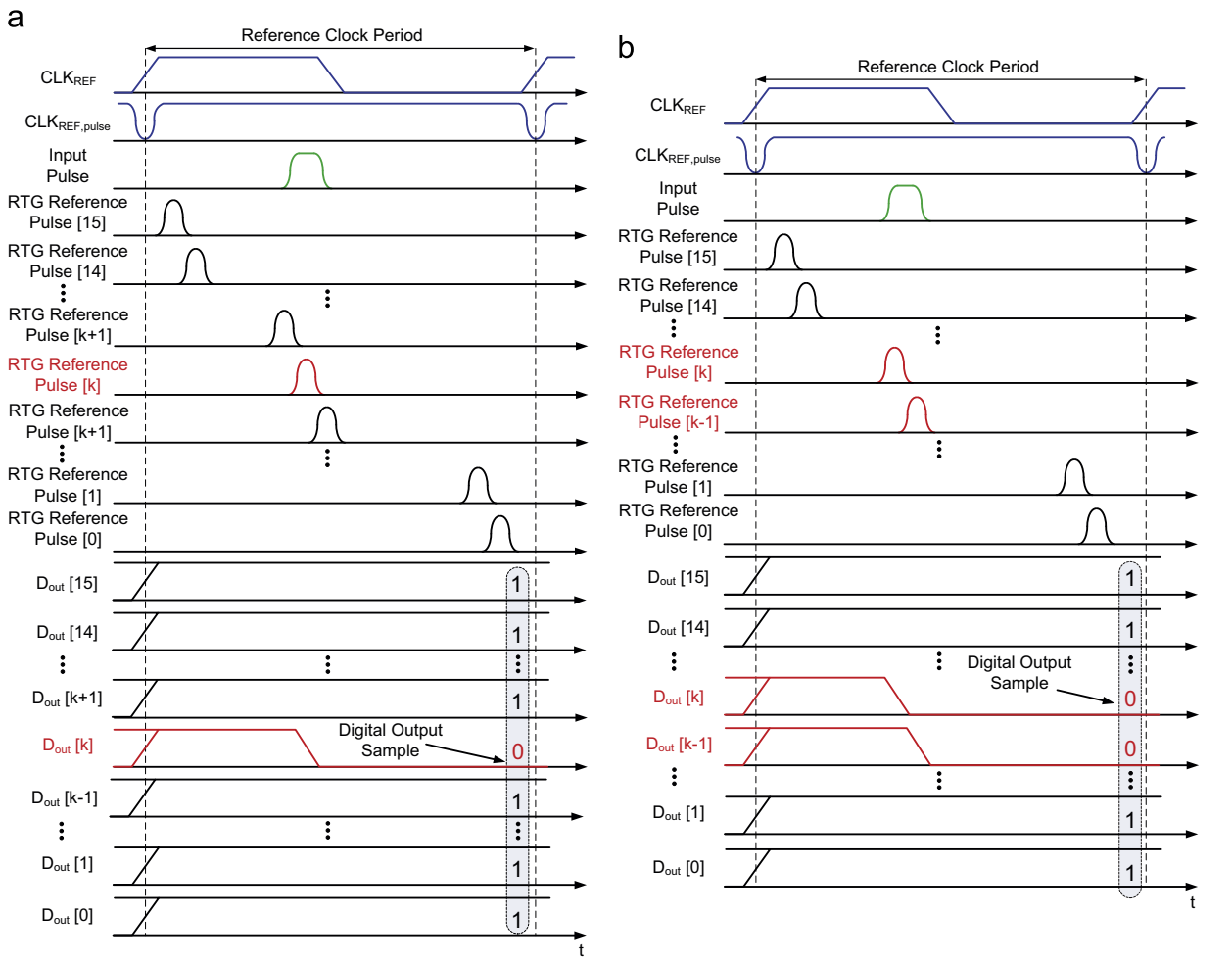

Fig. 6. Waveforms of the time-to-digital conversion when the input pulse overlaps with only one of the reference pulses (a) or the two reference pulses (b).

Table 1
Decoding scheme look-up table.

Latch output	Final digital output	Decimal value
1111111111111111	00000	0
1111111111111110	00001	1
1111111111111100	00010	2
1111111111111101	00011	3
…	…	…
1111111111001111	01010	10
1111111111011111	01011	11
…	…	…
1011111111111111	11101	29
0011111111111111	11110	30
0111111111111111	11111	31

overlap with at least one of the reference pulses. If the input pulse was designed to be more narrow in time domain, certain time intervals may exist which are without an overlap between the input pulse and the reference pulses, providing a false output of "1111111111111111" (or decimal 0). Such input pulse sizing and coding scheme would be extremely sensitive to random device mismatch due to fabrication process variations. Any undesirable scenario involving the non-existing overlap would result in a zero-output and a very large conversion error. Alternatively, using the implemented coding scheme, random device mismatch only changes the ratio between the subsequent quantization levels causing a minimal conversion error.

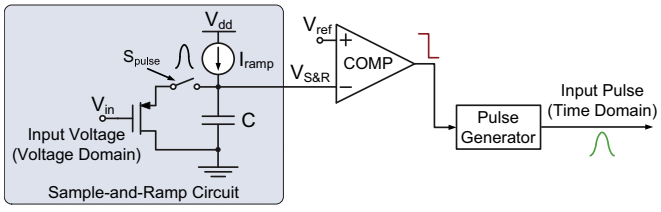

Fig. 7. Schematic of the voltage-to-time converter.

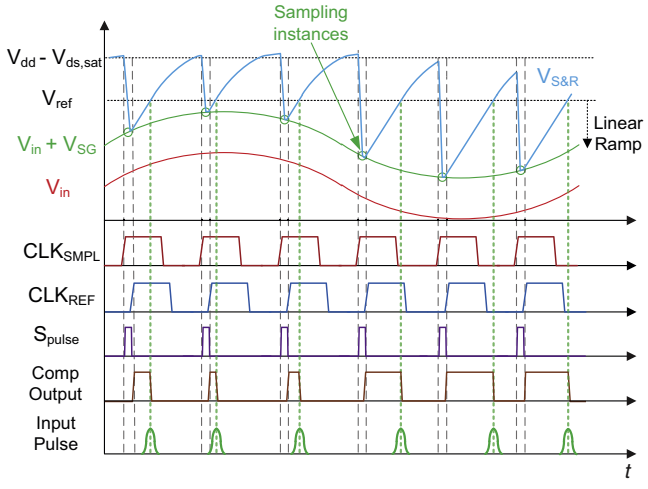

Fig. 8. Signal waveforms of the voltage-to-time converter.

5. Voltage-to-time converter

Voltage-to-time conversion is necessary at the input of the ADC in order to utilize the (digital) time-domain reference ladder. The schematic of the voltage-to-time converter is shown in Fig. 7. The analog voltage input is connected to the gate of the source-follower input transistor. The input sampling pulse (S_{pulse}) turns on the transmission gate switch (see Figs. 3 and 7). Consequently, the ramp current (I_{ramp}) flows through the source-follower, and the input voltage is sampled ($V_{S\&R}$). This is illustrated in Fig. 8. Because the source-follower transistor is instantly in saturation due to high value of I_{ramp} and the sampling switch resistance is very small, the resistance seen by the sampling capacitor (Fig. 7) is $1/g_m$ (g_m is the small-signal transconductance of the source follower). Hence, the sampling time constant is equal to C/g_m (where C is the sampling capacitance value). The value of I_{ramp} is tunable and is typically equal to 70 μA. For the sampling capacitor of 400 fF used in this work, this results in approximately $\tau = 430$ ps of settling time constant. The duration of the sampling pulse S_{pulse} was nominally set to 2 ns which provides more than 4.5τ of settling time. The sampling pulse duration can be programmed to 1.5 ns, 2 ns, 2.5 ns and 3 ns (the overall clock cycle duration is 12.5 ns or 80 MHz). The sampled voltage is equal to the input voltage augmented by the source-gate voltage of the input transistor which is a constant DC value equal to $V_{S\&R} = V_{in} + V_{SG}$ (V_{SG} was typically around 570 mV in this design). After the transmission gate (sampling) switch is turned off, the sampling capacitor voltage ($V_{S\&R}$) starts to ramp-up with a constant slope. The comparator makes a transition at the output when the ramp voltage reaches the reference voltage V_{ref} (V_{ref} can be tuned to be between 1.2 V and 1.45 V. The nominal value was set to 1.35 V). The pulse generator converts the comparator output transition into an input pulse. The time interval (t_{ramp}) required for the ramp to reach the voltage reference V_{ref} linearly changes, depending on the value of the input voltage:

$$t_{ramp} \approx \frac{C}{I_{ramp}} \cdot (V_{ref} - (V_{in} + V_{SG})) = -\frac{C}{I_{ramp}} \cdot V_{in} + constant. \quad (1)$$

Hence, the position (timing) of the input pulse within the clock period is linearly dependent on the analog input voltage V_{in} (Fig. 8). For higher V_{in} values, the input pulse is closer to the beginning of the reference clock period, while for the lower V_{in} values, the input pulse is closer to the end of the reference clock period. The values of I_{ramp} and V_{ref} are tunable to calibrate for the PVT variations in the reference ladder. PVT shifts cause offset and gain error in the converter by changing all the quantization levels by the same amount (they are changed equally, relative to each other). Therefore, offset and gain error caused by PVT can be compensated easily by adjusting only V_{ref} (offset) and I_{ramp} (gain).

The complete schematic of the comparator used for time-to-digital conversion is shown in Fig. 9. It consists of a preamplifier stage, followed by a Dynamic Threshold-Detecting Latch (DTDL). The circuit operates as follows. When the clock pulse is low (active at zero), node X is precharged to V_{dd}, while the node Y is discharged to ground setting the comparator output high (M3 is driven by the inverted clock pulse). After the clock pulse, transistors M3 and M4 remain off, while transistor M2 remains on. When the negative input voltage becomes higher than the positive input voltage (when the ramp voltage becomes higher than the reference voltage), the voltage at node X decreases, turning on transistor M1. Consequently, node Y is pulled up to V_{dd}, which results in flipping the state of the latch and discharging the comparator output to ground. Thus, the comparator output generates a falling-edge when the ramp voltage crosses the reference voltage.

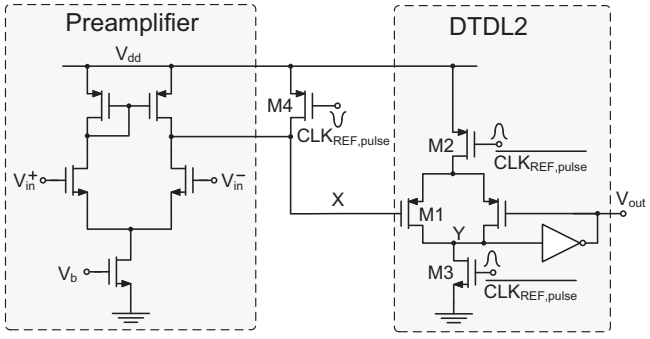

Fig. 9. Comparator for the time-to-digital conversion.

6. Measurement results

The complete die micrograph and the pulse-based flash ADC fabricated in a UMC's 180 nm standard CMOS process are shown in Fig. 10. The proposed flash ADC occupies a silicon area of only 130 μm × 73 μm, with the time-to-digital converter as the most area-demanding building block. The full-scale (FS) analog input voltage range of the ADC is 0–620 mV. The 5-bit flash converter prototype operates from a 1.8 V power supply and achieves a sampling rate of 80 MHz, while consuming 900 μW of power (without the I/O drivers). Overall, this results in an ADC's power efficiency (FoM) of approximately 445 fJ/conv, with an FoM defined as:

$$FoM = \frac{P_{ADC}}{2^{ENOB} \cdot 2 \cdot f_{BW}}, \quad (2)$$

where P_{ADC} is the ADC power consumption, $ENOB$ is the effective number of bits and f_{BW} is the ADC input bandwidth. The overall performance summary of the ADC is shown in Table 2.

Fig. 11 shows the integral nonlinearity (INL) and differential nonlinearity (DNL) measured using a slow input ramp signal (input ramp from 0 to 620 mV in 40 μs). The measured peak INL is equal to 0.52 LSB while the peak DNL is 0.22 LSB. At −0.6 dBFS (260 mV input DC with 240 mV input amplitude), the dynamic ADC measurements have shown 4.65-bit of maximum effective resolution with an SNR and SNDR equal to 31.5 dB and 29.8 dB, respectively. Fig. 12 shows the resulting 16384-point FFT output spectrum at four different input signal frequencies (2.42 MHz, 10.23 MHz, 20.54 MHz and 29.6 MHz) and the corresponding obtained SNR, SNDR and SFDR values. The observed input signal distortion is mainly caused by the voltage-to-time converter current mirror (sample-and-ramp circuit - see Fig. 7). As the ramp voltage approach V_{ref}, the current mirror is still in saturation, but starts approaching linear mode and modulating the ramp current

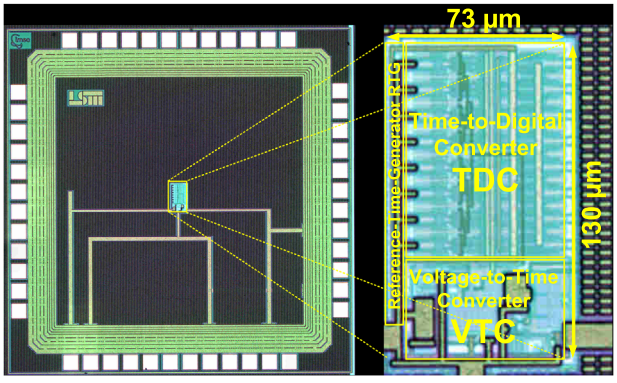

Fig. 10. Die micrograph and the complete pulse-based flash ADC (zoomed in).

(I_{ramp}). This effect can be observed in Fig. 8. The effect of the proposed decoding scheme is depicted in Fig. 13, showing the raw ADC output at a 1 MHz input frequency captured by the logic analyzer.

7. Conclusion

A concept of time-domain flash ADC reference ladder based on entirely digital circuits is presented in this paper. Based on this concept, a fully-digital pulse-based flash ADC prototype is proposed and developed. The converter requires only one comparator for the voltage-to-time conversion. The time-to-digital conversion is performed within a single clock cycle, as a fundamental difference from conventional TDCs which typically require a large number of clock cycles (counting) to perform the conversion. Measurement results show that a 5-bit converter can achieve an 80 MHz sampling rate while consuming only 900 μW of power. The prototype ADC is developed in a 180 nm standard CMOS technology and achieves a power efficiency which is comparable to many existing state-of-the-art flash ADCs. Table 3 shows the performance comparison with the existing state-of-the-art flash ADCs operating in the GHz range. Because GHz-range operation is more difficult to achieve, an overview of more comparable state-of-the-art flash ADCs which operate in the MHz-range is provided in Table 4. Finally, a performance comparison with the existing state-of-the-art TDCs is shown in Table 5. Depending on the application, TDC designs sometimes do not report effective number of bits (see Table 5). This is mainly due to high non-linearity which is not important for the specific application. The presented performance of the TDC designed in this work is obtained without applying any design optimization or circuit calibration techniques, confirming the promising benefits of the proposed topology. Many potential optimization techniques exist that can improve the performance of the existing prototype. Calibration of the reference-time-generator could improve the linearity of the converter and result in better power efficiency due to the possible reduction of the loading capacitance value. In addition, voltage-to-time conversion can be optimized in terms of sampling capacitor size, comparator performance and power consumption to achieve higher power efficiency.

Thanks to the digital-(time-)domain operation, the proposed technique is extremely scalable and would benefit from an integration in newer nanometer CMOS technology nodes. Thanks to

Table 2
Flash ADC performance summary.

Specification	Value
Input range (FS)	0–620 mV
Sampling frequency	80 MHz
Input bandwidth	40 MHz
SFDR	28.5–34.5 dB
SNDR	26.2–29.8 dB
SNR	27.5–31.5 dB
Power consumption (without I/O)	900 μW
Peak efficiency (FOM)	445 fJ/conv
Silicon area	130 μm × 73 μm
Technology	0.18 μm Std CMOS

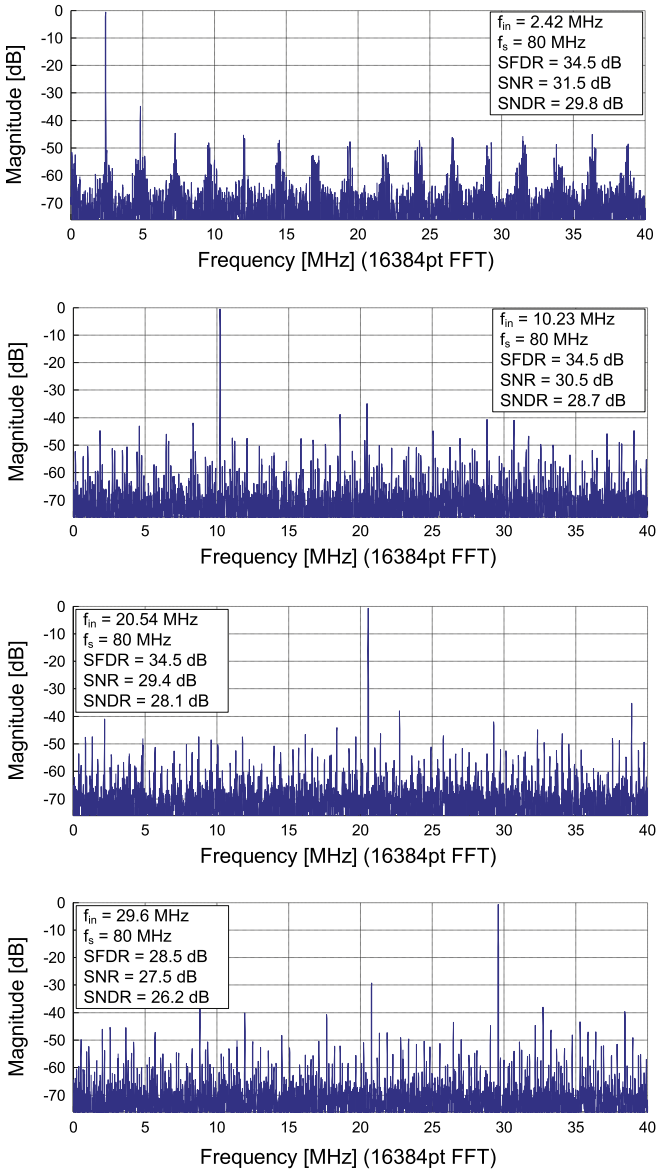

Fig. 12. Measured output signal 16384-pt FFT spectrum at different ADC-input frequencies (2.42 MHz, 10.23 MHz, 20.54 MHz and 29.6 MHz).

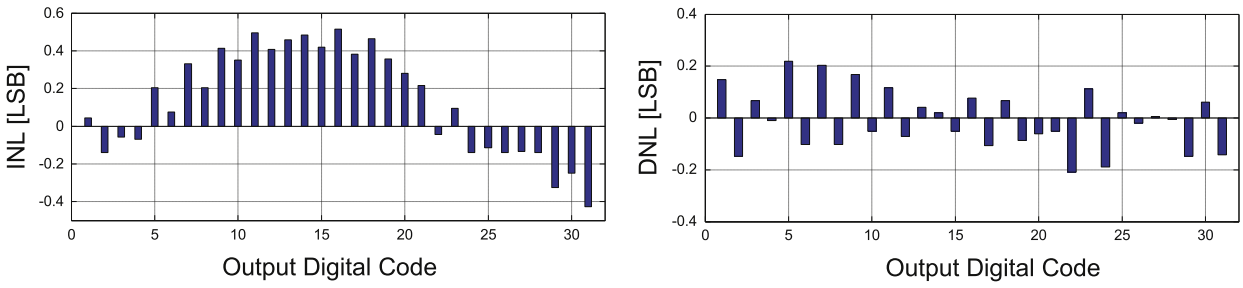

Fig. 11. Static test measurement results: INL and DNL.

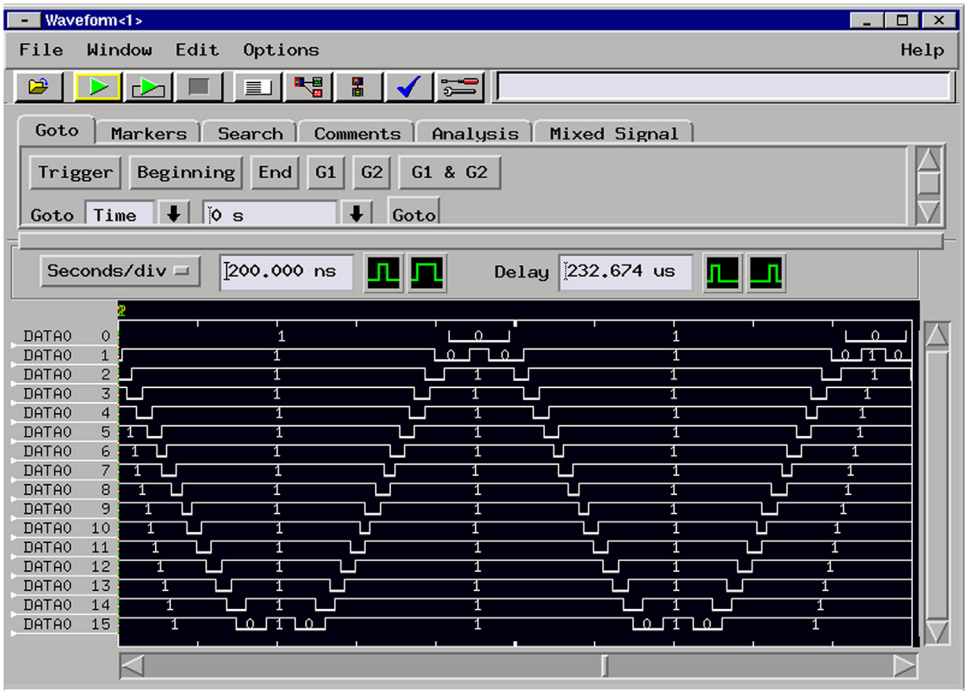

Fig. 13. Measured raw ADC digital output captured by the logic analyzer depicting the proposed decoding scheme (1 MHz input signal frequency).

Table 3
Comparison with GHz-range flash ADCs.

Publication	Process	Supply	ENOB	BW	Power	Efficiency (fJ/conv)
[14] Symp-VLSI 2008	90 nm Std CMOS	1 V	3–4.8	2 GHz	7.6 mW	150
[15] CICC 2008	180 nm SiGe BiCMOS	3–3.6 V	4.5	6.5 GHz	3.3 W	11,000
[16] Symp-VLSI 2009	65 nm Std CMOS	1.1 V	3.9	3.75 GHz	52 mW	490
[17] JSSC 2009	130 nm SiGe BiCMOS	1.2 V	4–5	20 GHz	4.8 W	11,200
[18] TCAS-II 2010	90 nm Std CMOS	1.2–2.5 V	3.22–3.75	2.5 GHz	86 mW	1320
[19] A-SSCC 2010	65 nm Std CMOS	1 V	4.7	1.5 GHz	36.2 mW	600
[20] JSSC 2011	65 nm Std CMOS	1.1 V	3.9	6 GHz	81 mW	350
[21] JSSC 2013	90 nm Std CMOS	1.2–1.5 V	4.89	2.05 GHz	76 mW	625
This work	180 nm Std CMOS	1.8 V	4.65	40 MHz	900 μW	445

Table 4
Comparison with MHz-range flash ADCs.

Publication	Process	Supply	ENOB	BW	Power	Efficiency (fJ/conv)
[22] TCAS-II 2008	90 nm Std CMOS	1 V	6.5–7	650 MHz	207 mW	1400
[23] CICC 2008	90 nm Std CMOS	0.6–1 V	4.08–4.45	30–300 MHz	1.3–6.7 mW	490–1060
[24] JSSC 2009	90 nm Std CMOS	1 V	4.7	878 MHz	2.2 mW	50
[25] TVLSI 2010	130 nm Std CMOS	1.2 V	4.54	600 MHz	120 mW	3070
[26] TCAS-I 2010	65 nm Std CMOS	1 V	4.4	700 MHz	1.97 mW	116
[27] A-SSCC 2010	90 nm Std CMOS	0.5 V	4.2	200 MHz	1.2 mW	160
[28] JSSC 2013	65 nm Std CMOS	1 V	4.8	630 MHz	595 μW	17
[29] JSSC 2002	130 nm Std CMOS	0.8 V	5.2	11 MHz	480 μW	600
[30] ESSCIRC 2003	180 nm Std CMOS	1.8 V	6	200 MHz	106 mW	4140
[31] JSSC 2007	65 nm Std CMOS	1.2 V	4.1	250 MHz	1.8 mW	440
[32] TCAS-I 2009	350 nm Std CMOS	3.3 V	5.7	387 MHz	1.1 W	28,200
[33] A-SSCC 2008	180 nm Std CMOS	0.9 V	5	9 MHz	631 μW	1095
[34]EDSSC 2013	180 nm Std CMOS	1.8 V	6.36	250 MHz	160 mW	4170
This work	180 nm Std CMOS	1.8 V	4.65	40 MHz	900 μW	445

the time-domain resolution increase in the advanced technology processes, this technique can potentially result in very high sampling rates and with high conversion efficiency. Moreover, the digital topology of the circuit enables a compact implementation which is very convenient for designing interleaved flash-ADCs with very high sampling rates.

Table 5
Comparison with other TDCs.

Publication	Process	Supply	Resolution	ENOB	BW	Power	Efficiency (fJ/conv)
[12] JSSC 2011	65 nm Std CMOS	1.33 V	9-bit	9.67	250 MHz	5.66 mW	450
[8] JSSC 2008	90 nm Std CMOS	1 V	9-bit	Not reported	33 MHz	3 mW	Not reported
[35] JSSC 2009	350 nm Std CMOS	2.7–3.5 V	26-bit	Not reported	50 MHz	33 mW	Not reported
[11] JSSC 2004	0.8 μm Std CMOS	3.3 V	11-bit	Not reported	100 kHz	10 mW	Not reported
[9] CICC 2014	45 nm Std CMOS	1 V	9-bit	8.94	100 MHz	24.2 mW	482
[13] ISIC 2011	180 nm Std CMOS	1.8 V	5-bit	4.13	250 MHz	8 mW	910
This work	180 nm Std CMOS	1.8 V	5-bit	4.65	40 MHz	900 μW	445

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