High Yield of GaAs Nanowire Arrays on Si Mediated by the Pinning and Contact Angle of Ga

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S Supporting Information

ABSTRACT: GaAs nanowire arrays on silicon offer great perspectives in the optoelectronics and solar cell industry. To fulfill this potential, gold-free growth in predetermined positions should be achieved. Ga-assisted growth of GaAs nanowires in the form of array has been shown to be challenging and difficult to reproduce. In this work, we provide some of the key elements for obtaining a high yield of GaAs nanowires on patterned Si in a reproducible way: contact angle and pinning of the Ga droplet inside the apertures achieved by the modification of the surface properties of the nanoscale areas exposed to growth. As an example, an amorphous silicon layer between the crystalline substrate and the oxide mask results in a contact angle around 90°, leading to a high yield of vertical nanowires. Another example for tuning the contact angle is anticipated, native oxide with controlled thickness. This work opens new perspectives for the rational and reproducible growth of GaAs nanowire arrays on silicon.
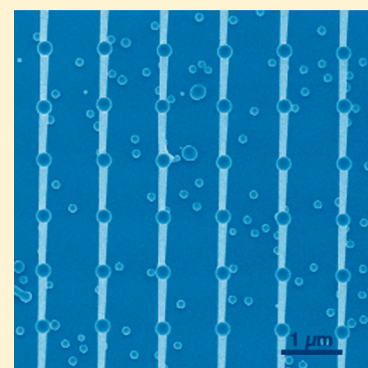
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S emiconductor nanowires (NWs) have been the subject of extensive investigations in recent years, motivated in part by the unique physical properties provided by their essentially one-dimensional geometry. These novel properties, as well as new material combinations that can only be achieved with NWs,[1−3] offer a large number of potentially useful applications in a broad range of electronic, optoelectronic, and energy harvesting devices.[4−10] A particularly useful property is that their small diameter allows their growth on lattice-mismatched substrates.[11−13] A natural consequence is that NWs enable the integration of highly functional III−V compounds with silicon-based technologies.[14−17] This represents a unique opportunity to combine the advantages of III−V materials such as direct band gap and high mobility with Si, which is extensively used in microelectronics industry.[18,19]

In the past, regular arrays of NWs have been achieved by patterning a substrate with gold nanoparticles;[20−23] such a configuration demonstrated the rational use of NWs, showing their potential integration in mass-production applications. These pioneering works rely on the use of the gold droplets for the nucleation and growth of the NWs through the vapor−liquid−solid process (VLS); however, gold is a nondesired impurity in silicon technology, so other methods have been investigated for the growth of NWs on silicon substrates.[24−26] Ga-assisted growth is a successful example showing how this precious metal can be avoided for the growth of III−V NWs on III−V and on Si substrates.[27] Following this method, nanoscale

gallium droplets collect arsenic from the gas phase. Subsequent supersaturation leads to the precipitation of GaAs underneath. The Ga droplet should be refilled continuously to ensure a sustainable growth. Applying this method, arrays of GaAs NWs have been obtained on patterned GaAs substrates,[28] whereas fabrication of GaAs NWs on a patterned Si surface has shown to be by far more challenging. One of the main challenges has been the reproducibility in obtaining high yield of vertical GaAs NWs. Key elements such as gallium predeposition, thickness and composition of the growth mask have shown to be important parameters for a successful growth.[29,30] Still, successful growths of GaAs NW arrays by the Ga-assisted method are rare in literature.[31−33]

In this work, we bring new elements of analysis for understanding how a high yield can be obtained for the growth of Ga-assisted GaAs arrays on silicon. We have found that the surface properties of the material exposed to growth is decisive for achieving highly controlled vertical GaAs NWs. We show in detail the case of amorphous silicon. Alloying of amorphous silicon with Ga in the predeposition step leads to a pinning of the droplet and adequate contact angle for vertical growth. Alternative layers such as native oxide are discussed at the end

of the manuscript. Progress in the deterministic GaAs NW growth at selected positions on a Si substrate is the first step toward the rational fabrication of advanced devices on the silicon platform.

SEM micrographs of successful GaAs NWs arrays grown on Si(111) by a gallium predeposition during the heating of the substrate are shown in Figure 1. Figure 1a−d show tilted views
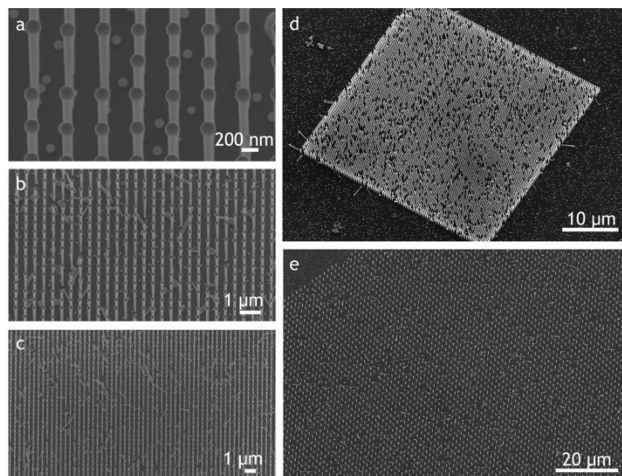

Figure 1. Scanning electron microscopy (SEM) images of GaAs nanowires grown on patterned Si(111) substrates at 630 °C, at a nominal Ga growth rate of 1 Å/s and under an As_4 partial pressure of 2 × 10^{-6} Torr. (a−c) are 20° tilted images and (d−e) are tilted views with additional in-plane rotation. The yield of vertical nanowires is 80%. The hole diameter size is 90 nm for all the images. The interhole distance is 400 nm in (a−d) and 1600 nm in (e).

of the NWs grown in patterns with a nominal hole diameter of 90 nm and an interhole distance of 400 nm at different magnification and with additional in plane rotation (d). Figure 1e shows the results for a larger interhole distance (1600 nm). The NWs are uniform in length and diameter. They present a slightly inverse tapering and a Ga droplet at their tip. The yield of vertical NWs—defined as number of openings nucleating vertical NWs divided by the total number of openings in the array—is 80%. The yield is independent from the interhole distance of the array. We notice that the 10% of the holes of the array do not lead to the nucleation of NWs because they seem to be closed. This could be due to an incomplete definition of the holes by the e-beam lithography. An optimization of the pattern definition could in principle lead to an improved yield of vertical wires. Only a few holes (5%) lead to the growth of tilted NWs. In the remnant, 5% of the holes we observe were parasitic and showed 2D growth. By subtracting the yield in hole fabrication, we obtain a yield in vertical nanowire growth of 89%. In the following, we demonstrate how this high yield can only be obtained in very special conditions of the nanoscale surfaces exposed to growth.

As found by other groups,[30,34] a gallium predeposition step has a strong influence on the yield of vertical NWs. We demonstrate how Ga predeposition is only useful in certain conditions by comparing growths in two different batches of Si wafers, one of them presenting amorphous silicon (a-Si) at the interface with the SiO_2 mask. Figure 2 (top) shows representative SEM images of the growth results obtained with and without the Ga predeposition, keeping all the other growth parameters unvaried. The two substrates originated
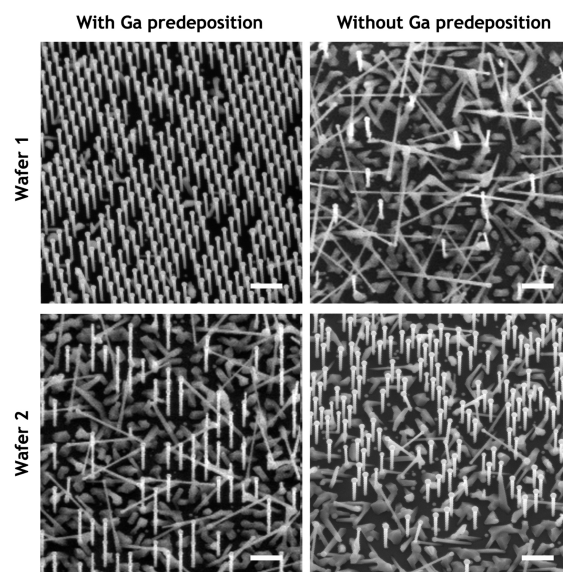

Figure 2. Tilted SEM micrographs of GaAs NWs grown in arrays defined on two different 4 in. wafers (Wafer 1 and Wafer 2) with and without the predeposition of Ga droplets. (Top) For the growth on Wafer 1, the yield of vertical wires strongly depends on the Ga predeposition. (Bottom) For the growth on Wafer 2, the yield of vertical nanowires is very low in both cases. For all the images, the interhole distance is 400 nm and the hole diameter size is 90 nm. The scale bar is 1 μm and the tilt angle is 20° for all the images.

from the same wafer, which we refer as "Wafer 1". As we can see in the picture, omitting the Ga predeposition step leads to an extremely low yield of vertical wires (6%) and a high density of nonvertical wires and parasitic growth. An identical set of growths, with and without the Ga predeposition, has been performed on a similar Si wafer of a different batch. We refer to these two samples as "Wafer 2". Figure 2 (bottom) shows the results of the growths. In this case, irrespective of the Ga predeposition, the yield of vertical wires is low and many tilted wires and parasitic growth are found on the substrates. The yield of vertical wires with Ga predeposition is 23%; omitting the Ga predeposition, the yield is 43%. We underline that these values of yield on substrates without the amorphous silicon layers are not reproducible. In this case, the yield oscillates between few and 45%. We show images from our best yield samples.

We turn now to explain the fundamental difference between Wafer 1 and 2, since a priori they have been subject to identical sample preparation and growth protocols. To this purpose, lamellas containing cross sections of the substrates were prepared by focus ion beam (FIB) and the local structure and composition mapping investigated by transmission electron microscopy related techniques. We start by analyzing the structure of the Si chip in a region outside the pattern. Figure 3 displays cross-sectional high angle annular dark field (HAADF) images of representative samples of Wafer 1 and Wafer 2 taken at the interfaces between Si and the thermal SiO_2, and the corresponding energy-dispersive X-ray spectroscopy (EDX) maps. The same analyses have been performed on four chips, two of Wafer 1 and two of Wafer 2. Two samples correspond to remaining wafer pieces which had not been loaded in the MBE reactor, that is, they have been analyzed just after the sample preparation; the other two have been analyzed at the end of the
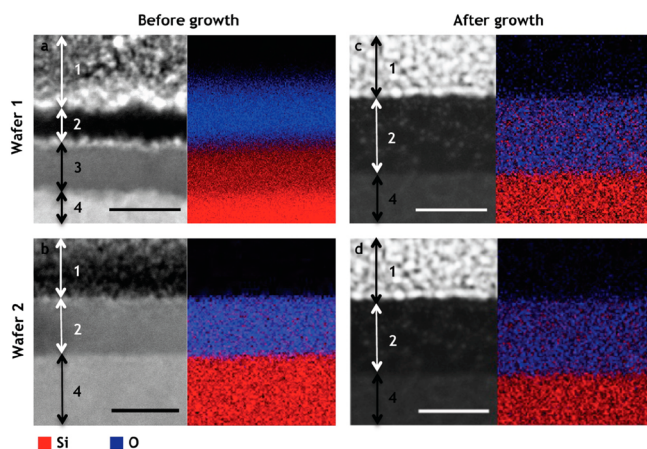
Figure 3. HAADF images of representative samples of Wafer 1 and Wafer 2, studied before and after growth, and corresponding EDX results, with the Si map in red and the O map in blue. The analysis is performed at the interface between the silicon substrate and the mask oxide. The numbers label the different layers analyzed: (1) protective layer for FIB preparation; (2) SiO_2; (3) a-Si layer; (4) c-Si. The sample from Wafer 1 shows an unexpected layer of a-Si that crystallizes after growth. The sample from Wafer 2 shows uniquely a thermal oxide layer grown directly on the crystalline silicon substrate. The scale bar is 20 nm.

Figure 4. (Top) HAADF image of a nanoscale hole where the SiO_2, the amorphous Si and the crystalline Si can be distinguished and the corresponding EDX map. (Center) HAADF and EDX analysis of the hole degassed in the MBE reactor. The amorphous silicon layer is crystallized. (Bottom) HAADF and EDX analysis performed after the growth. A GaAs NW nucleates in the hole and grows vertically and also radially once higher than the hole. The scale bar is 50 nm. The lower EDX signal from the amorphous silicon layer is due to a different thickness produced by the faster erosion of amorphous with respect to crystalline silicon during the FIB process.

growth process and correspond to the samples depicted in Figure 2.

We first consider the pieces not loaded in the MBE (Figure 3a−b). The sample from Wafer 1 shows an amorphous layer between the crystalline silicon (c-Si) and the SiO_2. This 13 nm thick layer consists of a-Si, as confirmed by the lack of oxygen in the EDX analysis. Conversely, the piece from Wafer 2 shows the thermal oxide layer directly on top of the c-Si, as one would expect from the sample preparation. The SiO_2 layer of the chip from Wafer 1 has been found to be rather nonuniform, with thickness ranging from 10 to 20 nm, unlike for Wafer 2 sample, although an identical dry oxidation has been performed on the wafers. The analysis of the chips after growth is shown in Figure 3c−d. In this case, for both samples only thermal oxide is found on the crystalline silicon. Because the crystallization of amorphous silicon starts at temperatures higher than 500 °C, we think that it has crystallized during the heating of the substrate inside the growth chamber.[35,36] Our Si provider suggested that the amorphous layer was generated by the mechanical treatments such as slicing and lapping and by an insufficiently long chemical mechanical polishing (CMP) step at the end of the substrate preparation. We believe indeed that the large thickness of the layer of a-Si layer prevented its full crystallization during the thermal oxidation.

We turn now the attention to a patterned region of the silicon chip: cross-sectional HAADF images of nanoscale holes from Wafer 1 with the corresponding EDX maps are shown in Figure 4. The analysis has been performed prior to growth (Figure 4 top), after the degassing step in the MBE chamber (Figure 4 center) and after the growth (Figure 4 bottom). For the analysis of the sample after the degassing step the Ga shutter was kept closed, as we were interested in understanding the evolution of the substrate in itself. We observe the presence of an a-Si layer below the SiO_2 prior to degassing or growth. The a-Si layer, which is also observed at the position of the holes, is completely crystallized after the degassing and growth steps. After crystallization, the silicon surface at the bottom of
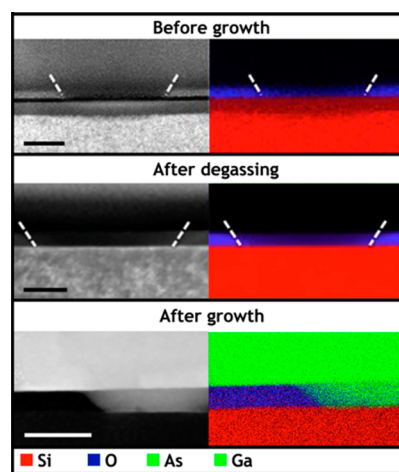
the hole appears completely flat, as shown in Figure 4 (bottom).

Thus, we conclude that the presence of a layer of a-Si seems to be a necessary but not sufficient condition to guarantee a high yield of vertical wires and that the addition of the Ga predeposition is also required. We remind here that, in our case, the Ga shutter is opened at the very beginning of the growth process and, thus, is during the degassing step. During this time, the temperature of the Ga cell is ramping up to achieve a nominal Ga growth rate of 1 Å/s, and the substrate temperature is ramped up from 200 °C up to 770 °C at a rate of 50 °C/s for the degassing step. Therefore, the a-Si layer is expected to crystallize in a relatively short time once the substrate approaches the degassing temperature.[36] The Ga predeposition, however, already starts at lower substrate temperatures, when the a-Si layer has not yet crystallized. The Ga droplets are pinned on the a-Si at the bottom of the holes before it crystallizes. The a-Si reacts preferentially with the Ga, forming a Ga−Si alloy. This changes the force balance at the interface and thereby the contact angle. We have included a drawing of this process as well as measurements showing the preferential reaction with the substrate in the case of a-Si in the Supporting Information. As a consequence, when a-Si layer is used, the Ga predeposition should be performed during the heating process of the substrate.

Knowing that the characteristics of the Ga droplets affect the yield of vertical NWs,[37,38] we have looked for a more universal reason for the high yield. We compared the contact angle of the Ga droplets on amorphous and crystalline silicon, using the same process used for the successful nanowire growth. SEM micrographs of the Ga droplets obtained on the two kinds of surfaces are shown in Figure 5. The Ga droplets deposited directly on c-Si are also significantly larger than the ones observed on amorphous silicon. Gallium droplets pin in an easier manner on the surface of a-Si, leading to a higher density. The Ga droplets deposited on what initially was a-Si exhibit a
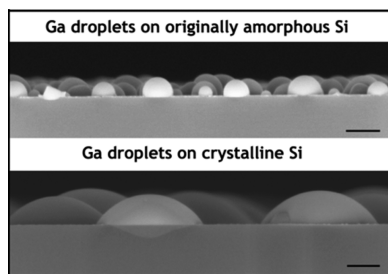
Figure 5. Cross-sectional SEM images of Ga droplets deposited on originally amorphous silicon (top) and on crystalline silicon (bottom). The droplets have different sizes and contact angles depending on the surface. The scale bar is 200 nm.

contact angle of $84 \pm 4°$; the ones deposited on c-Si have a contact angle of $52 \pm 3°$. It is well known that the contact angle affects the driving force in nanowire growth.[39] For example, contact angles much smaller than 90° render nucleation at the triple-phase line especially difficult.[40,41] Nucleation away from the triple-phase line favors nonvertical growth due to the so-called three-dimensional twining phenomenon.[37] An additional factor in patterned substrates is that the droplet should be smaller than the hole in order to avoid wetting on the oxide and raising of the triple-phase line away from the substrate. If the triple-phase line is located on the SiO_2, the loss of epitaxial relation with the substrate results in random orientation of the nanowires. Although this study has been performed on unpatterned substrates, we believe that it highlights important aspects of the initial stages of growth and how to obtain high yields of vertical wires.

We conclude that the size and the contact angle of the Ga droplets, resulting from their interaction with the substrate, play a fundamental role in the successful growth of vertical GaAs NW arrays by the VLS method. Our results suggest some possible modifications to the nanofabrication methods usually employed for arrays. In particular one should pay a particular attention to the wetting properties of the metal droplets at the open surfaces exposed to growth. Recent unpublished results show that an optimal contact angle close to 90° leads to high yield of vertical wires, which can be obtained by a careful control of the native oxide (see Supporting Information).[41] In that sense, we have used native oxide for engineering the contact angle of Ga droplets inside the nanoscale holes. Although the growth yield inside the holes is not yet close to 100%, most of the successful nanowires grow perpendicularly from the substrate (see Supporting Information). An advantage of this method is that the Ga droplet pins directly on the native oxide without the need for gallium predeposition. This initial data confirms the importance of engineering the contact angle of the metal used in VLS and could be used for other material systems. Finally, if amorphous silicon should be used at the interface between the substrate and the SiO_2 mask, it is necessary to use the optimal layer thickness around 15 nm, as the crystallization of the a-Si layer during the heating of the substrate for the growth becomes relevant (see Supporting Information). Alternatively, if the process should be compatible with thin amorphous silicon layers, the growth mask material should be reconsidered.

In conclusion, we have provided new elements for the achievement of a high yield of vertical GaAs NWs on a patterned Si substrate. The nature of the surface at the nanoscale holes opened in the mask is key. It determines the contact angle and position of the triple-phase line. We have obtained ideal conditions by using an oxidized Si substrate containing an amorphous layer at the interface with the crystalline substrate. Other treatments such as the creation of an appropriate native oxide layer may lead to a similar effect. The need of a gallium predeposition step depends on the nature of the substrate used. For example, it is not needed when engineered native oxide is used to pin the droplets with the required contact angle.

■ METHODS

Sample Preparation. Four inch $\langle 111 \rangle$ p-doped silicon wafers with a resistivity of $0.1-0.5\ \Omega$cm have been patterned to realize the growth of GaAs NWs in arrays. After patterning, the wafers were diced into $35 \times 35\ mm^2$ square chips sized for the MBE sample holder. The pattern consisted of a square arrangement of holes of sizes ranging between 90 and 150 nm; the interhole distance (or pitch) was varied between 200 and 2000 nm on the same substrate. The growth mask consisted of a 20 nm thick layer of thermal oxide obtained by dry oxidation in a Centrotherm furnace at 950 °C. The pattern was predefined in a ZEP resist with electron-beam lithography and then transferred on the oxide layer by a 12 s wet-chemical etching based on 7:1 buffered hydrofluoric acid solution (BHF). In order to ensure an oxide-free surface in the holes, the chips were shortly dipped in the same BHF solution prior to the introduction in the UHV chamber. The substrates were subsequently annealed at 500 °C for 2 h in UHV in order to ensure a pristine surface free of water and organic molecules. The substrate was then transferred to the growth chamber. There, they were degassed at 770 °C for 30 min to further remove any possible surface contaminants.

Growth. Ga-assisted GaAs NWs were synthesized at a nominal Ga growth rate of 1 Å/s, As_4 partial pressure of 2×10^{-6} Torr, at a substrate temperature of 630 °C, and with 7 rpm rotation. In some of the growths, Ga was predeposited by keeping the shutter open since the ramp up of the substrate temperature for the degassing step. The As_4 source was opened once the growth temperature had been reached. Both sources (As_4 and Ga) were switched off simultaneously at the end of the growth. The samples were then cooled down to 200 °C and removed from the reactor.

Wetting of Ga: Comparison between a-Si and c-Si. A thin amorphous silicon layer was deposited by means of plasma-enhanced chemical vapor deposition (PECVD) on a Si(111) wafer. This a-Si and the c-Si substrates were exposed to BHF wet etching to ensure their surfaces were free of oxide; both samples have been heated to 770 °C for the degassing step with the increasing Ga deposition during the ramp up, simulating the initial step of our growth process. The contact angle and size of the droplets have been measured by cross section scanning electron microscopy.

Transmission Electron Microscopy. To characterize the morphology of the samples we used scanning electron microscopy (SEM) and transmission electron microscopy (TEM). High-angle annular dark-field scanning transmission electron microscopy and EDX analysis were performed using a FEI Tecnai OSIRIS microscope operated at 200 kV using the Super-X (0.9 rad collection angle) detector and Bruker Esprit software. TEM cross sections were prepared by using a Focus Ion Beam (FIB).

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

It contains a more detailed description of the proposed model, along with measurements showing the reaction of the Ga with the a-Si and the effect of the contact angle on successful vertical nanowire growth on Si. This material is available free of charge via the Internet at http://pubs.acs.org.

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Author Contributions

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E.R.A., G.T., D.R, H.A.P., and F.M. contributed to the growth. E.R.A., J.V.P., G.T., and A.D.M. fabricated the samples and analyzed the results. J.A., M.d.l.M., and S.C.B. performed HAADF STEM and EDX analysis. E.R.A. made the figures and the artwork. E.R.A. and A.F.iM. wrote the manuscript in collaboration with all the authors. F.M. performed the contact angle measurements as a function of the nature of the native oxide of nonpatterned substrates. A.F.iM. supervised the project. All authors have given approval to the final version of the manuscript. We thank CMI and CIME for access to electron microscopy facilities and F. Bobard for the cross-section fabrication.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

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